## Antimonide NMOSFET with Source Side Injection Velocity of 2.7x10<sup>7</sup> cm/s for Low Power High Performance Logic Applications

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**Abstract:** Antimonide (Sb) quantum well (QW) MOSFETs demonstrated with integrated high-κ dielectric (1nmAl<sub>2</sub>O<sub>3</sub>-10nm HfO<sub>2</sub>). The long channel Sb NMOS exhibits effective electron mobility of 6,000 cm<sup>2</sup>/Vs at high field (2 x 10<sup>12</sup>/cm<sup>2</sup> of charge density (N<sub>s</sub>)), which is the highest reported value for any III-V MOSFET. The short channel Sb NMOSFET ( $L_G = 150$ nm) exhibits a cut-off frequency ( $f_T$ ) of 120GHz, f<sub>T</sub> - L<sub>G</sub> product of 18GHz.µm and source side injection velocity (v<sub>eff</sub>) of 2.7x10' cm/s, at drain bias (V<sub>DS</sub>) of 0.75V and gate overdrive of 0.6V. The measured  $f_T$  and  $f_T \times L_G$ are 2 x higher, and v<sub>eff</sub> is 4x higher than Si NMOS (1.0-1.2V  $V_{DD}$ ) at similar  $L_G$ , and are the highest for any III-V MOSFET. **Introduction:**InAs<sub>x</sub>Sb<sub>1-x</sub> quantum-well (QW) heterostructure with high electron mobility integrated with high hole mobility strained In<sub>x</sub>Ga<sub>1-x</sub>Sb QW, can potentially enable III-V CMOS and share the same metamorphic buffer on Silicon (Fig. 1a) [1]. In this paper, we report InAs<sub>0.8</sub>Sb<sub>0.2</sub> NMOSFETs with integrated high-k dielectric, which exhibit record high long channel electron mobility, short channel electron velocity and high-frequency small-signal performance, for the first time. The effects of interface trap density (Dit) which degrades the DC drive current and transconductance (g<sub>m</sub>) is studied in detail using pulsed I-V and radio frequency (RF) measurements.

**Device Fabrication and Characterization:** Fig. 1(b) shows the schematic of  $InAs_{0.8}Sb_{0.2}$  nMOSFET with  $1nmAl_2O_3/10nm$  HfO<sub>2</sub> high-κ gate dielectric. We obtain Hall mobility of 13,500 cm²/Vs at a carrier density of  $2.2x10^{12}$  /cm² for the as-grown device layers without dielectric. Fig. 1(c) shows the tilted view SEM of a device, fabricated using a process detailed in [2], with 150nm  $L_G$  and source-to-drain separation of 500nm.

<u>Development</u> of a Scaled Gate Stack for Antimonide MOSFETs: A high quality gate stack is needed for integration with InAs<sub>x</sub>Sb<sub>1-x</sub> QW, with low EOT and J<sub>OX</sub>, excellent interface properties and high carrier mobility in the channel. We use an ultra-thin (1nm) GaSb cap layer on top of the upper barrier for dielectric integration, to prevent oxidation of the In<sub>0.2</sub>Al<sub>0.8</sub>Sb barrier layer. Using ALD Al<sub>2</sub>O<sub>3</sub>/HfO<sub>2</sub> bilayer dielectric on n and p type GaSb, we demonstrate MOSCAPs with unpinned Fermi level across gap and scaled EOT (Fig. 2). The extracted D<sub>it</sub> (Fig. 2b) is low towards valence band of GaSb which results in good nMOS turn off, while the high D<sub>it</sub> from midgap to conduction band can affect drive current.

<u>DC Characterization:</u> Fig. 3(a-f) shows the transfer and output characteristics of Sb nMOSFETs with 5μm, 450nm and 150nm gate lengths. The long channel devices exhibit good  $I_{ON}$ - $I_{OFF}$  ratio and excellent saturation in the output characteristics. Contact resistance limits the drive current in the 150nm  $L_G$  device which has an  $I_{DSAT}$  of  $525\mu A/\mu m$  at  $V_{DS}$  of 1.0V. The sub-threshold characteristics and short channel effects degrade as  $L_G$  is scaled, due to the non-optimized barrier and oxide thickness and the thick quantum well structure (EOT=4.5nm). Long Channel Device Characterization: Fig. 4(a) shows the measured and simulated split C-V characteristics of  $L_G$ =20μm device. The stretch-out in the measured C-V compared to the simulated C-V is due to  $D_{it}$ . Fig. 4(b) shows the electron drift

mobility extracted from the output conductance and measured C-V characteristics. We report a record high effective electron mobility of 6,000 cm<sup>2</sup>/Vs at 2x10<sup>12</sup> /cm<sup>2</sup> of N<sub>s</sub>, which is 15x higher than Si NMOS inversion layer mobility and 3x higher than that of InGaAs NMOS[3]. The Sb NMOSFET electron mobility is 2.2x lower than the Hall mobility. This is further investigated in detail using pulsed IV (2µs pulsed width) and RF measurements. Figs. 4 (c-d) show the output and transfer characteristics of the 450nm L<sub>G</sub> device using DC and pulsed measurements. The pulsed  $I_D$ - $V_D$  data shows significant improvement (by 35% at 0.75V gate overdrive) in I<sub>ON</sub> and  $I_{ON}$ - $I_{OFF}$  ratio compared to the DC. Fig 4(e) shows extrinsic  $g_m$ comparing DC, pulsed IV and RF measurements. Peak extrinsic RF g<sub>m</sub> improves by 30% compared to DC G<sub>m</sub> for a gate overdrive of 0.6V. This improvement is due to reduced charge trapping in the dielectric at very high frequencies. This confirms that the reduction in FET mobility compared to Hall mobility is due to overestimation of charge from split C-V, and the actual electron mobility in Sb MOSFET should be at least 30-40% higher than the measured DC value of 6000 cm<sup>2</sup>/Vs. Short Channel Device Characterization: Fig. 5(a) shows the measured and modeled scattering parameters of the 150nm L<sub>G</sub> device from 100MHz to 50GHz and Fig. 5(b) shows the extracted circuit elements. Excellent agreement between the measured and simulated S-parameters confirms the extracted circuit element values. Fig. 5(c) shows the measured and modeled small signal current gain, |h21|, vs frequency for L<sub>G</sub>=150nm, 300nm and 450nm. The devices have cut-off frequencies of 120GHz, 55GHz and 27GHz, respectively. From the extracted parameters from small signal modeling, we evaluate the source side injection velocity (veff) of these devices as  $g_m/slope(C_{gs}\ vs\ L_G)$ . Figs. 5(d-e) benchmark the  $v_{eff}$ and f<sub>T</sub> of the Sb NMOS devices with state-of-the-art Si and III-V NMOS. The 150nm L<sub>G</sub> Sb NMOS exhibits a v<sub>eff</sub> of  $2.7 \times 10^7$  cm/s and  $f_{T-}L_G$  product of 18GHz.µm, which are the highest reported for III-V MOSFETs till date.

<u>Enhancement Mode Operation:</u> While above mentioned devices operate in depletion mode (normally ON) due to thick EOT, enhancement mode (normally OFF) operation is required for logic applications. We have recently demonstrated e-mode Sb nMOS devices with scaled barrier and quantum well [2], as shown in Fig. 6.

**Conclusions:** Long channel Sb NMOS devices are demonstrated with high field effective electron mobility of 6,000 cm²/Vs. Short channel Sb NMOS exhibit cut-off frequency ( $f_T$ ) of 120GHz,  $f_T$ -  $L_G$  product of 18 GHz.µm and source side injection velocity ( $v_{eff}$ ) of 2.7x10<sup>7</sup> cm/s, at  $V_{DS}$ = 0.75V and  $V_{GS}$  –  $V_T$  =0.6V. The measured  $f_T$ ,  $f_T$  x  $L_G$  are 2x higher, while  $v_{eff}$  is 4x higher than Si NMOS (1.0-1.2V  $V_{DD}$ ), and are the highest among III-V MOSFETs. The 150nm  $L_G$  device exhibits a drive current of 525 µA/µm at  $V_{DS}$  of 1.0V. **Acknowledgment:** Some of the authors acknowledge financial support from DARPA/SRC sponsored MARCO-MSD Center.

## References

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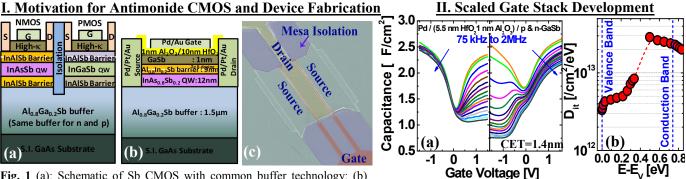


Fig. 1 (a): Schematic of Sb CMOS with common buffer technology; (b) Schematic of the Sb NMOS with 1nmAl<sub>2</sub>O<sub>3</sub>/10nm HfO<sub>2</sub> dielectric; (c) SEM image of the fabricated device with 150nm L<sub>G</sub> and 500nm source-to-drain

Fig. 2 (a): C-V of n and p type GaSb MOS capacitors with 1nmAl<sub>2</sub>O<sub>3</sub>-5.5nm HfO<sub>2</sub> dielectric; (b) Extracted D<sub>it</sub> vs energy

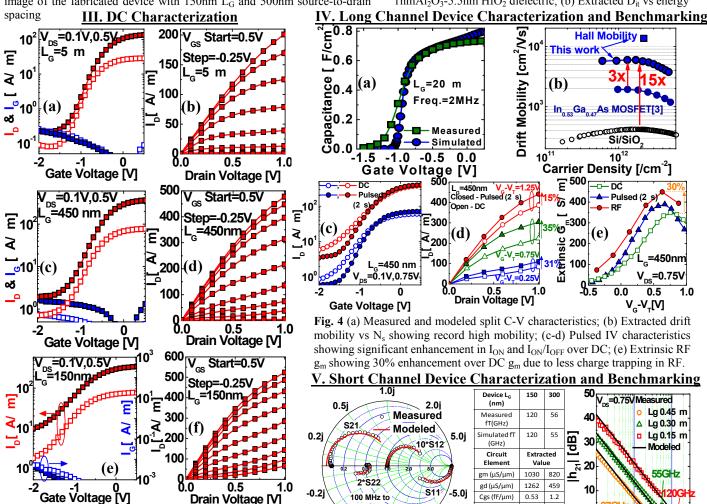


Fig. 3 (a-f): Transfer and output characteristics of Sb nMOSFETs with 150nm, 450nm and 5µm L<sub>G</sub>.

Drain Voltage [V]

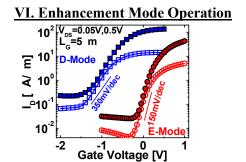


Fig. 6 Transfer characteristics of depletion and enhancement mode device. Scaling the QW and barrier, results in enhancement mode operation.

S11 -0.2j 100 MHz to Cgs (fF/µm) 0.53 1.2 50 GHz Cgd (fF/µm) 0.11 0.22 Rs ( $\Omega$ .  $\mu$ m) 594 1E10 1E11 -0.5j -2.0j Rd ( $\Omega$ .  $\mu$ m) 660 594 Frequency [Hz] -1.0j v<sub>eff</sub> [x 10<sup>7</sup>cm/s] 至00 (e) (d) Strained Si [2] SI NMOS ITRS (1.0-1.2V) Sb NMOS at V InGaAs NMOS Measured<sup>s</sup> ns=0.5V [4] Si NMOS [2] 0.01Projected for Rext/2 10 0.01 0.1 0.1 0.5 Gate Length [ m] Gate Length [ m]

Fig. 5 (a) Measured and modeled S-parameters of the 150nm  $L_G$  Sb NMOS at  $V_G$ - $V_T$ = 0.6V and  $V_{DS}=0.75V$ ; (b) Extracted circuit elements from the small signal model; (c) Measured and modeled  $|h_{21}|$  (d) Extracted source injection velocity; (e)  $f_T$  vs  $L_G$ . The measured  $f_T$ ,  $f_T x L_G$  and  $v_{eff}$  are the highest among III-V MOSFETs.