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Apparatus and Method for Controlling DC-AC Power Conversion

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Chapman et al.

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(54) **APPARATUS AND METHOD FOR CONTROLLING DC-AC POWER CONVERSION**

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(73) Assignee: **SunPower Corporation**, San Jose, CA (US)

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Related U.S. Application Data

(63) Continuation of application No. 13/936,744, filed on Jul. 8, 2013, now Pat. No. 9,225,256, which is a (Continued)

(51) **Int. Cl.**
H02M 5/458 (2006.01)
H02J 3/38 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H02M 5/458*** (2013.01); ***H02J 3/38*** (2013.01); ***H02M 1/12*** (2013.01); ***H02M 1/15*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H02M 5/458; H02M 7/48; H02M 7/47; H02M 7/493; H02M 1/15; H02M 3/285; H02J 3/38
(Continued)

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(Continued)

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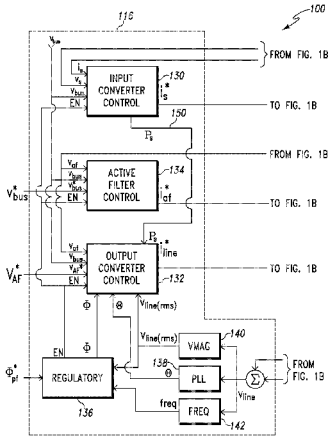
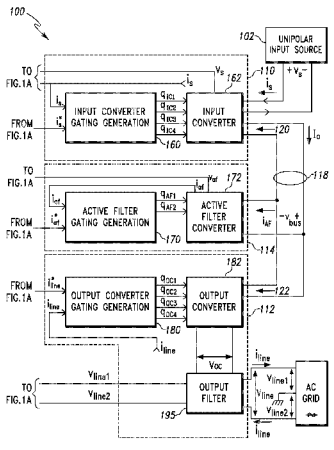
(74) *Attorney, Agent, or Firm* — Grasso PLLC

(57) **ABSTRACT**

An apparatus and method for controlling the delivery of power from a DC source to an AC grid includes an inverter configured to deliver power from the unipolar input source to the AC grid and an inverter controller. The inverter includes an input converter, an active filter, and an output converter. The inverter controller includes an input converter controller, an active filter controller and an output converter controller. The input converter controller is configured to control a current delivered by the input converter to a galvanically isolated unipolar bus of the inverter. The output converter is configured to control the output converter to deliver power to the AC grid. Additionally, the active filter controller is configured to control the active
(Continued)





filter to supply substantially all the power that is deliver by the output controller to the AC grid at a grid frequency.

20 Claims, 23 Drawing Sheets

Related U.S. Application Data

continuation of application No. 12/563,495, filed on Sep. 21, 2009, now Pat. No. 8,482,947.

(60) Provisional application No. 61/230,546, filed on Jul. 31, 2009.

(51) **Int. Cl.**

H02M 1/12	(2006.01)
H02M 1/15	(2006.01)
H02M 7/48	(2007.01)
H02M 1/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H02M 7/48*** (2013.01); *H02M 2001/007* (2013.01)

(58) **Field of Classification Search**

USPC 363/65, 71, 132

See application file for complete search history.

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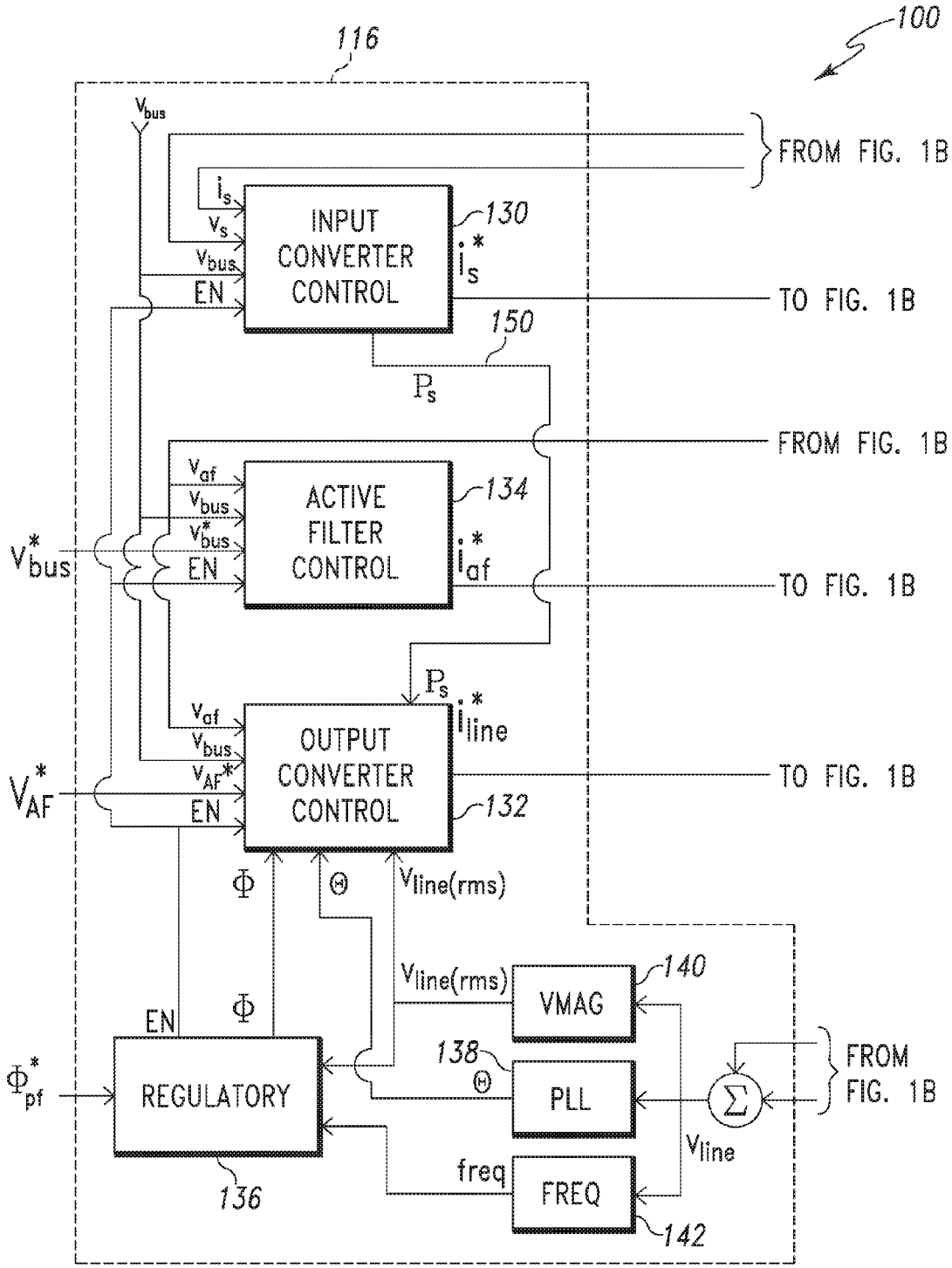
100
116
V_{bus}
FROM FIG. 1B
i_s
v_s
V_{bus}
EN
INPUT CONVERTER CONTROL
130
i_s^*
TO FIG. 1B
150
P_s
FROM FIG. 1B
V_{af}
V_{bus}
V_{bus}^*
EN
ACTIVE FILTER CONTROL
134
i_{af}^*
V_{bus}^*
TO FIG. 1B
P_s
V_{af}
V_{bus}
V_{AF}^*
EN
OUTPUT CONVERTER CONTROL
i_{line}^*
TO FIG. 1B
132
V_{AF}^*
Φ
Θ
$V_{line(rms)}$
$V_{line(rms)}$
VMAG
140
EN
Φ
138
Θ
PLL
FROM FIG. 1B
Φ_{pf}^*
REGULATORY
V_{line}
freq
FREQ
136
142

Fig. 1A

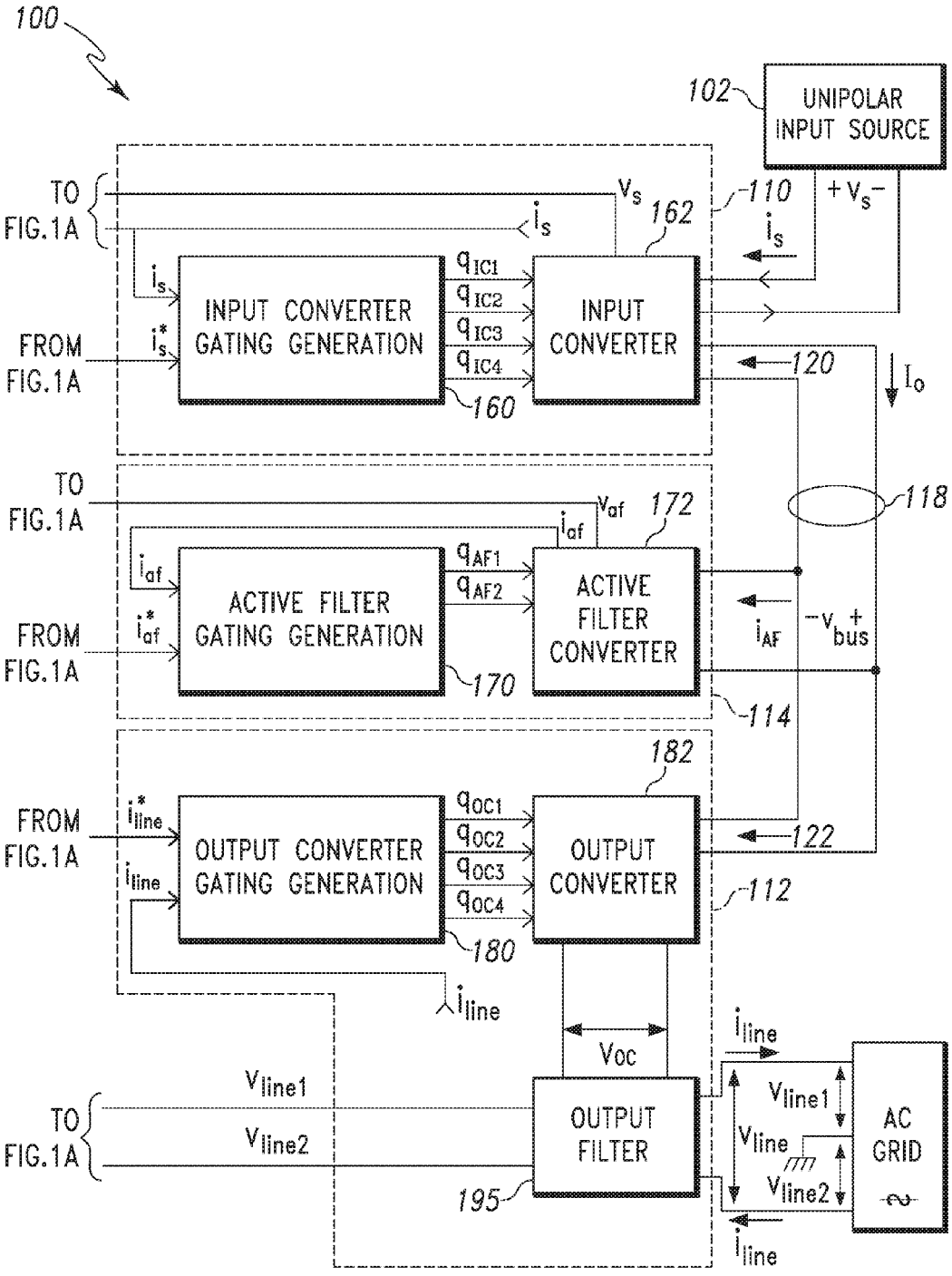
100
102
UNIPOLAR INPUT SOURCE
TO FIG.1A
FROM FIG.1A
INPUT CONVERTER GATING GENERATION
INPUT CONVERTER
ACTIVE FILTER GATING GENERATION
ACTIVE FILTER CONVERTER
OUTPUT CONVERTER GATING GENERATION
OUTPUT CONVERTER
OUTPUT FILTER
AC GRID
110
120
118
114
112
122
160
170
180
195
162
172
182

Fig. 1B

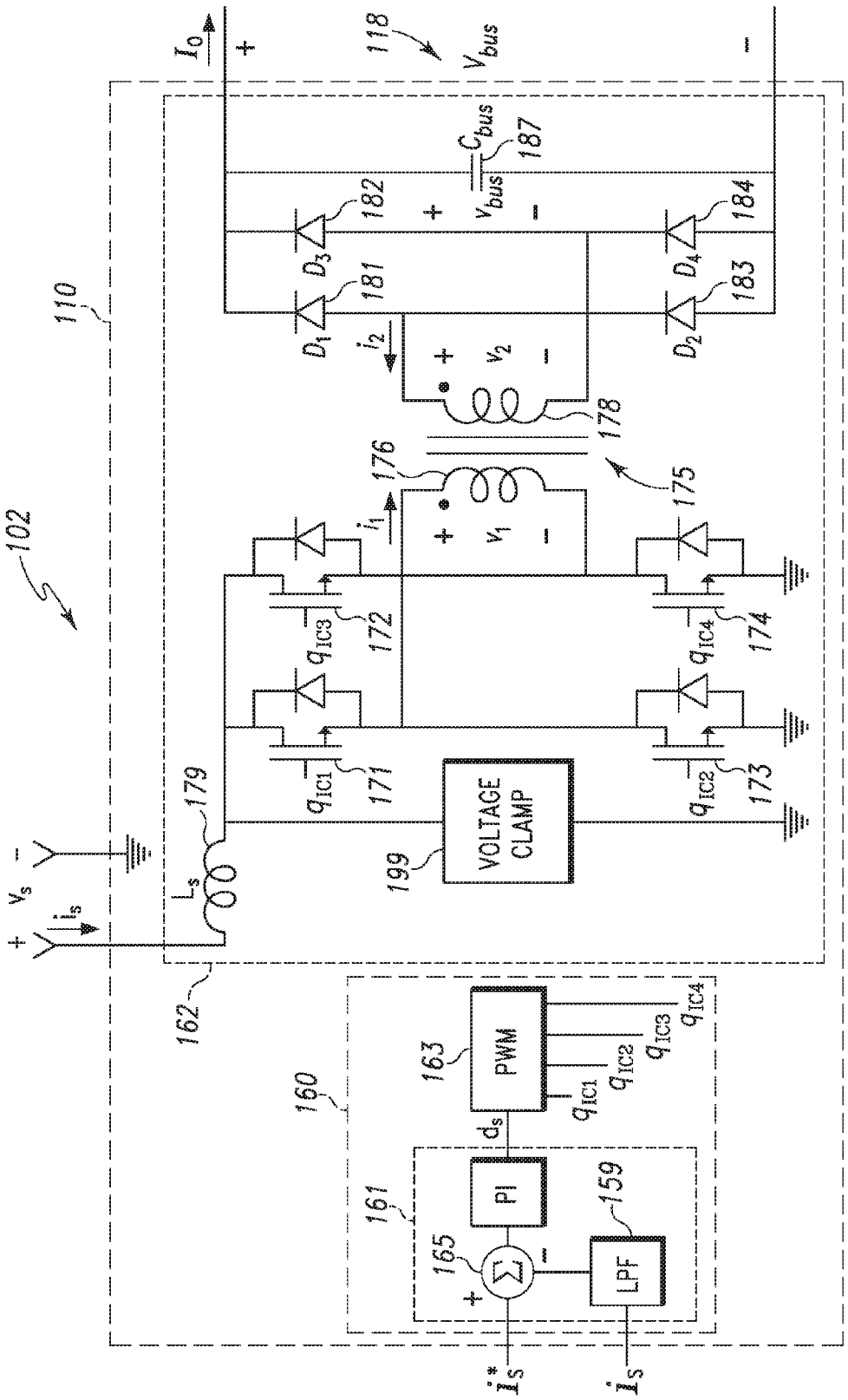
I_o
+
118
V_{bus}
−
C_{bus}
187
v_{bus}
182
184
D_3
D_4
181
183
D_1
D_2
i_2
v_2
178
176
175
i_1
v_1
102
110
q_{IC3}
172
q_{IC4}
174
q_{IC1}
171
q_{IC2}
173
179
L_s
v_s
i_s
199
VOLTAGE CLAMP
162
160
163
PWM
d_s
161
PI
159
LPF
165
i_s^*
i_s

Fig. 2

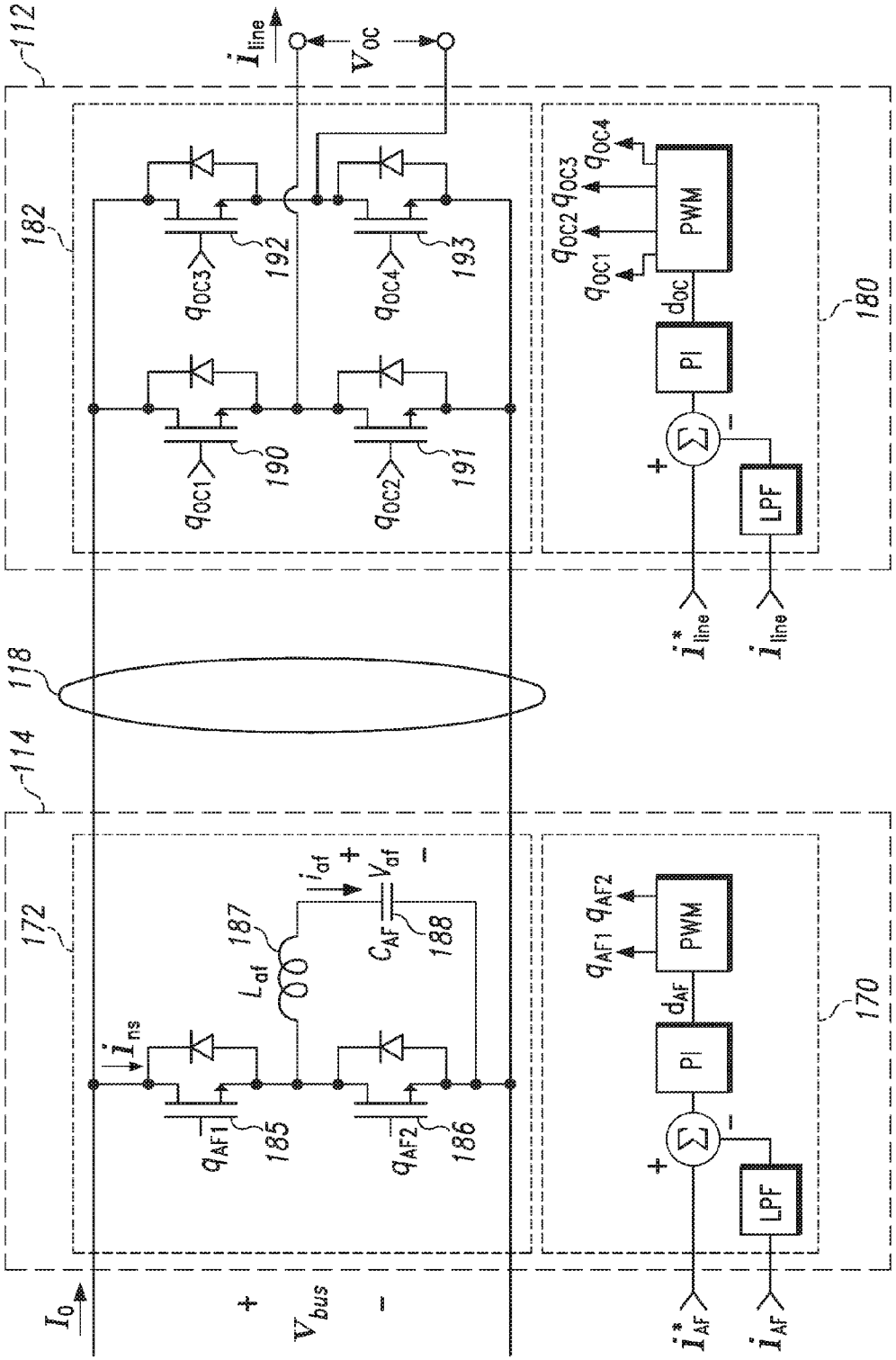
112
182
i_{line}
V_{oc}
q_{OC3}
192
q_{OC4}
193
q_{OC1}
190
q_{OC2}
191
q_{OC2} q_{OC3} q_{OC4}
PWM
q_{OC1}
d_{OC}
PI
180
LPF
i^*_{line}
i_{line}
118
114
172
187
L_{af}
i_{af}
V_{af}
C_{AF}
188
i_{ns}
q_{AF1}
185
q_{AF2}
186
q_{AF1} q_{AF2}
PWM
d_{AF}
PI
170
LPF
I_o
+
V_{bus}
-
i^*_{AF}
i_{AF}

Fig. 3

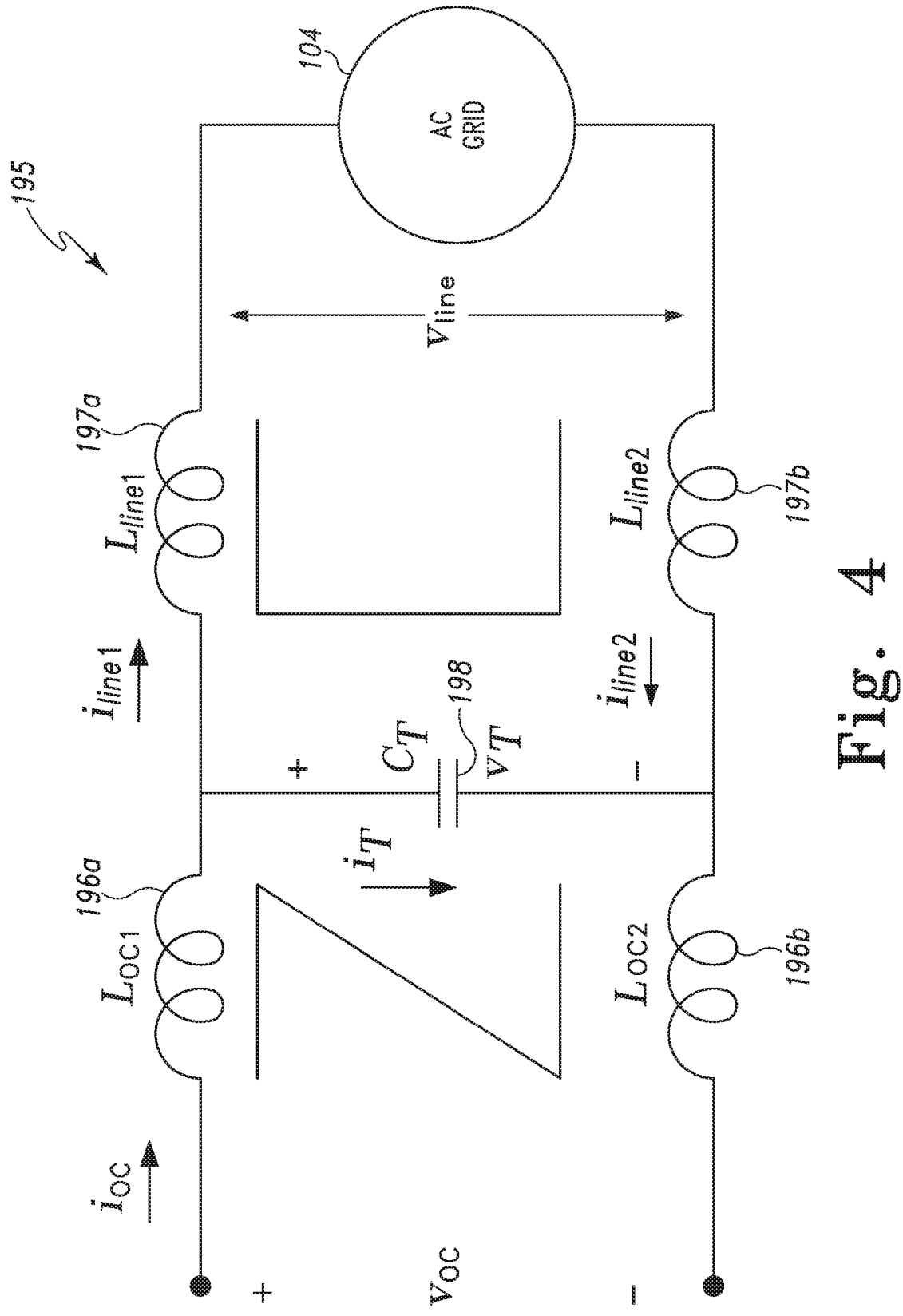
195
104
AC GRID
V_{line}
197a
L_{line1}
L_{line2}
197b
i_{line1}
i_{line2}
198
C_T
v_T
+
–
i_T
196a
L_{OC1}
L_{OC2}
196b
i_{OC}
+
v_{OC}
–

Fig. 4

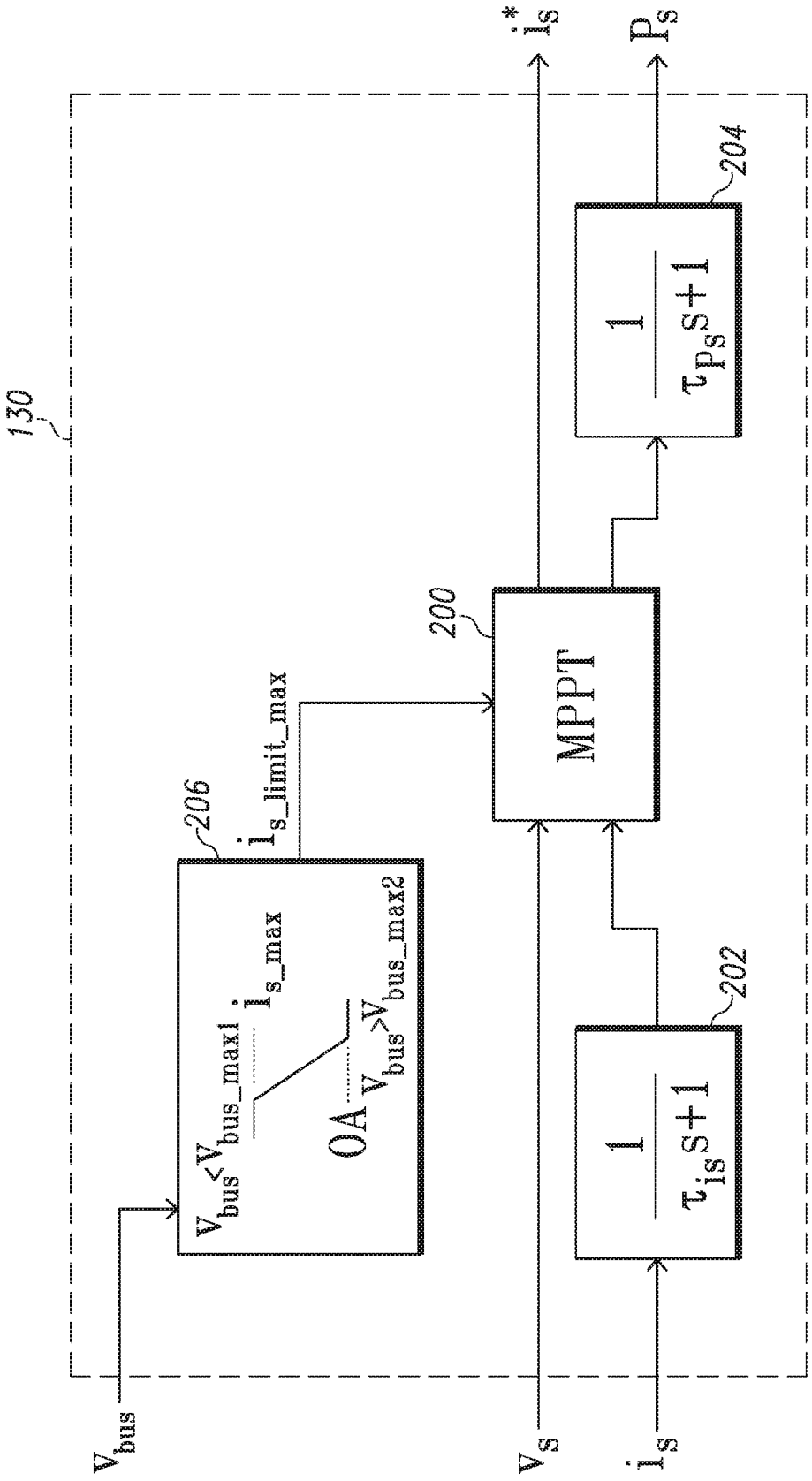
130
206
200
MPPT
202
204
$i_{s\_limit\_max}$
$V_{bus}<V_{bus\_max1}$
i_{s_max}
0A
$V_{bus}>V_{bus\_max2}$
$\frac{1}{\tau_{is}S+1}$
$\frac{1}{\tau_{Ps}S+1}$
i^*_s
P_s
V_{bus}
V_s
i_s

Fig. 5

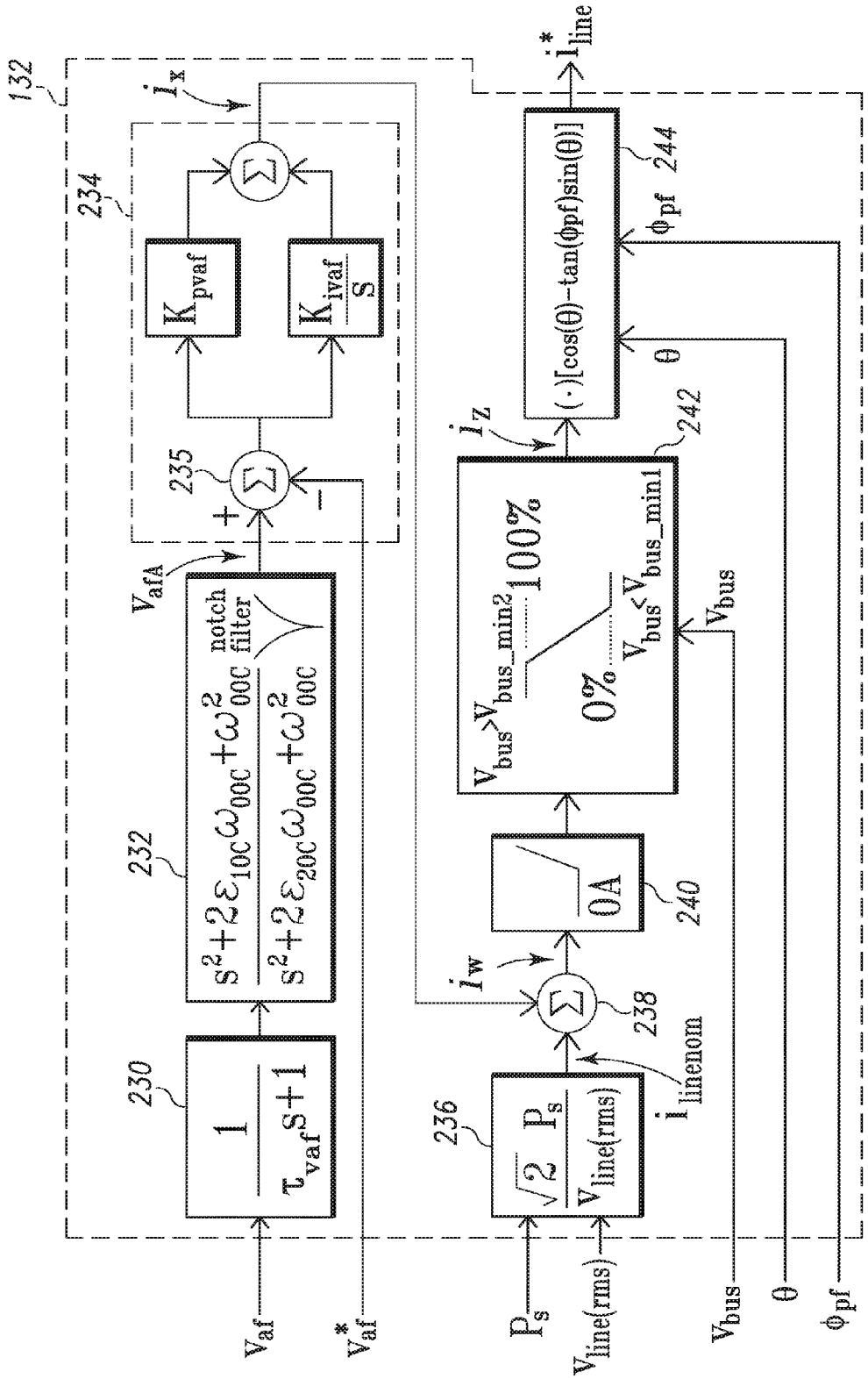
132
234
230
232
236
240
242
244
235
238
notch filter
$\frac{1}{\tau_{vaf}s+1}$
$\frac{s^2+2\varepsilon_{10c}\omega_{00c}+\omega_{00c}^2}{s^2+2\varepsilon_{20c}\omega_{00c}+\omega_{00c}^2}$
K_{pvaf}
K_{ivaf}/s
$\frac{\sqrt{2}\ P_s}{V_{line(rms)}}$
0A
$V_{bus}>V_{bus\_min2}$ 100%
0%
$V_{bus}<V_{bus\_min1}$
$(\cdot)[\cos(\theta)-\tan(\phi pf)\sin(\theta)]$
V_{afA}
i_x
i_w
i_z
$i_{linenom}$
i^*_{line}
V_{af}
V^*_{af}
P_s
$V_{line(rms)}$
V_{bus}
θ
ϕpf

Fig. 6

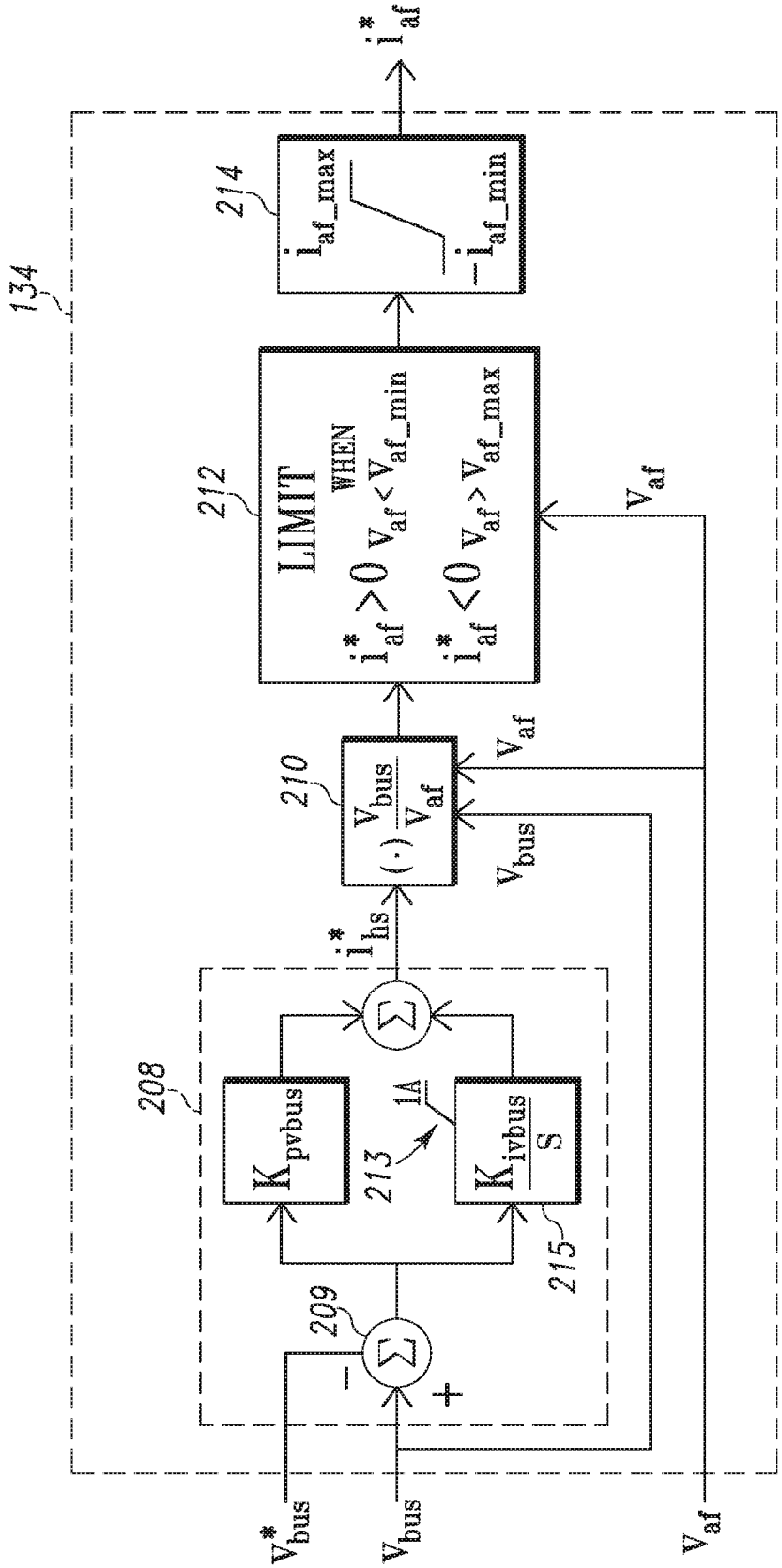
134
214
i_{af_max}
$-i_{af\_min}$
i^*_{af}
212
LIMIT
WHEN
$i^*_{af}>0$ $v_{af}<v_{af\_min}$
$i^*_{af}<0$ $v_{af}>v_{af\_max}$
v_{af}
210
$\frac{v_{bus}}{v_{af}}$
$(\cdot)$
v_{af}
v_{bus}
i^*_{hs}
208
K_{pvbus}
213
1A
$\frac{K_{ivbus}}{S}$
215
209
v^*_{bus}
v_{bus}
v_{af}

Fig. 7

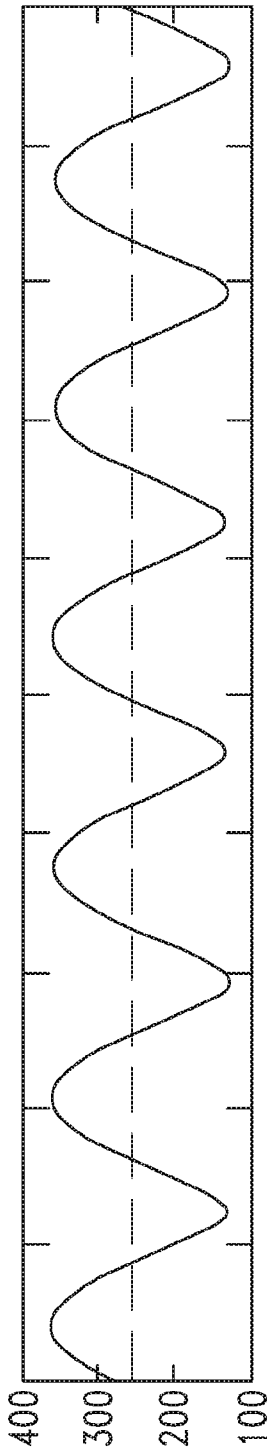

Fig. 8A

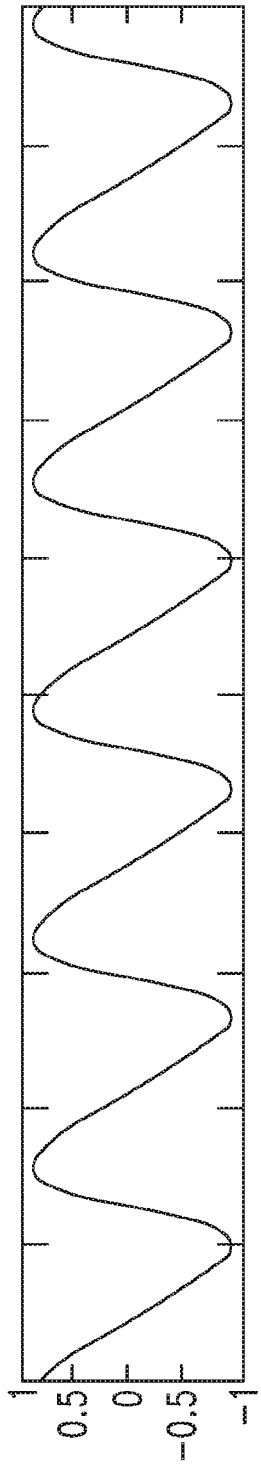

Fig. 8B

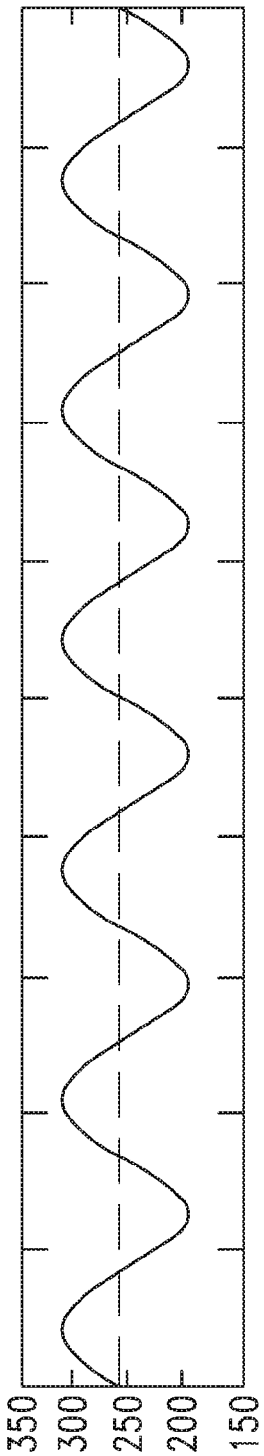

Fig. 9A

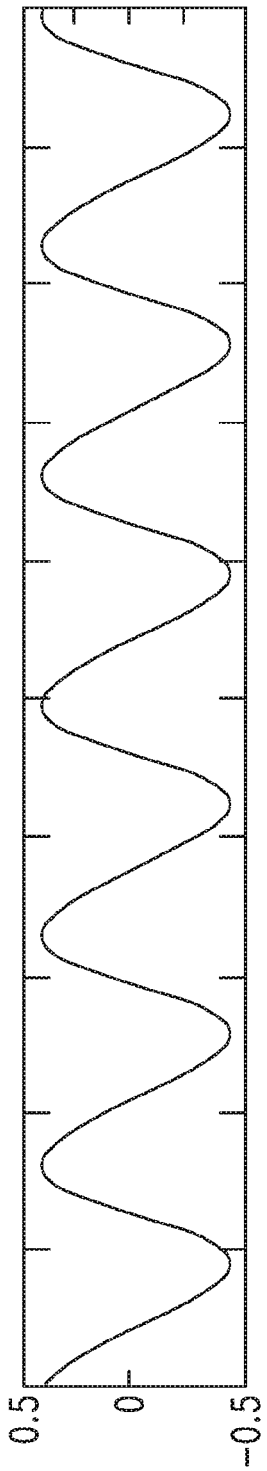

Fig. 9B

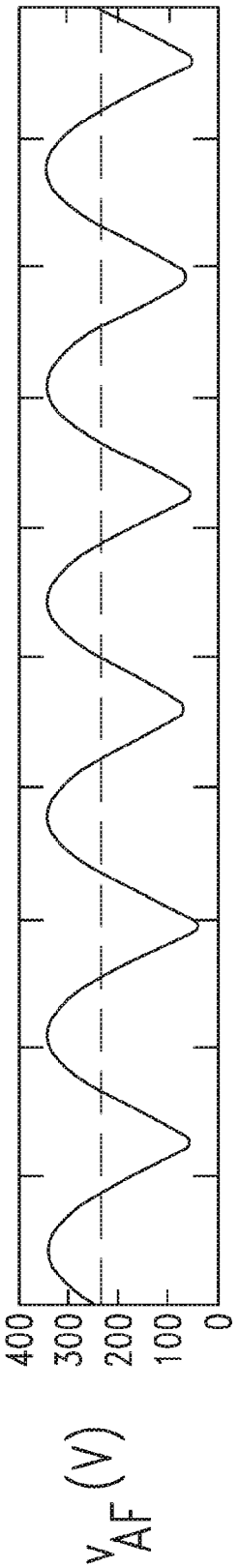

Fig. 10A

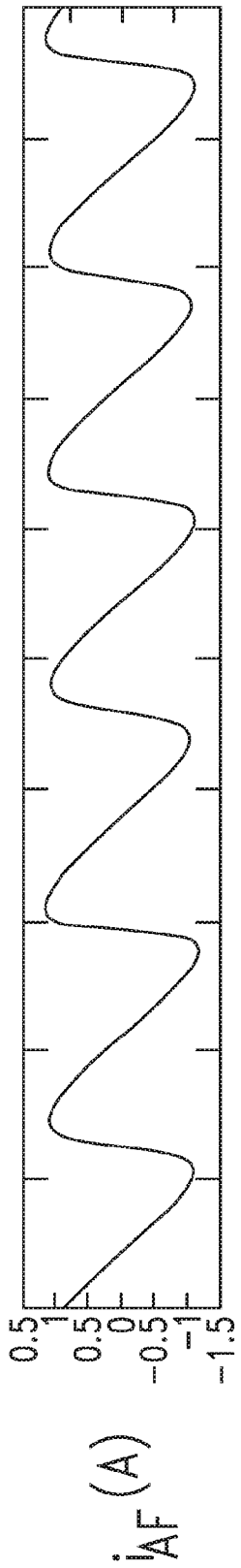

Fig. 10B

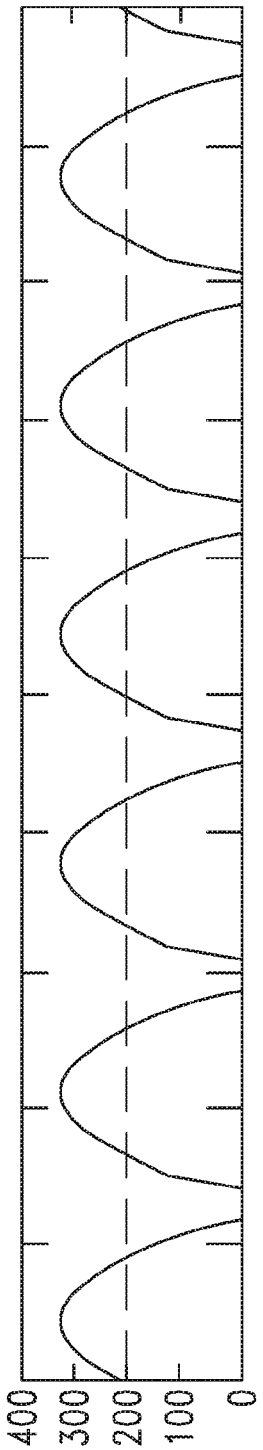

Fig. 11A

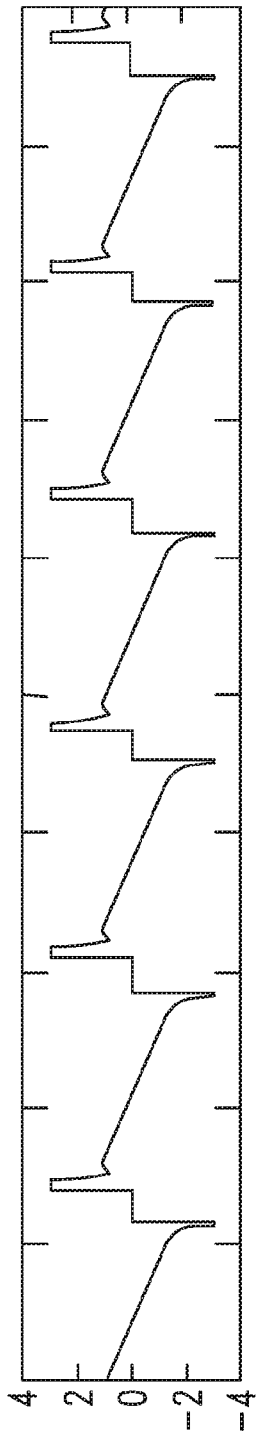

Fig. 11B

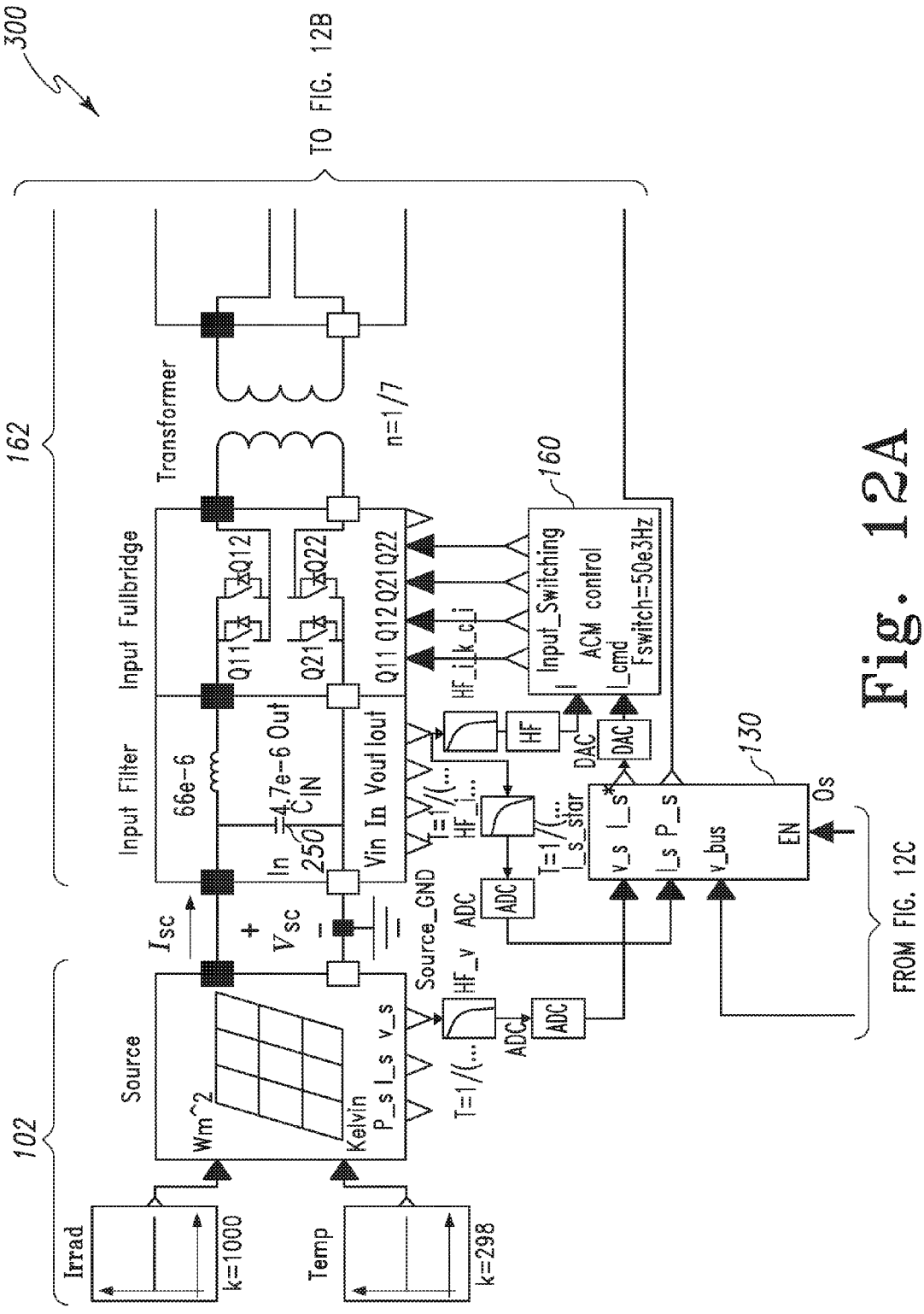
300
TO FIG. 12B
162
102
160
130
Irrad
k=1000
Temp
k=298
Source
Wm^2
Kelvin
P_s I_s v_s
Input Filter
66e-6
4.7e-6
C_IN
250
In
Out
Vin In Vout Iout
Input Fullbridge
Q11
Q12
Q21
Q22
Q11 Q12 Q21 Q22
Transformer
n=1/7
Isc
Vsc
Source_GND
HF_v
ADC
HF_i_k_c_i
HF
DAC
Input_Switching
ACM control
I_cmd
Fswitch=50e3Hz
v_s I_s* Is P_s v_bus EN Os
FROM FIG. 12C

Fig. 12A

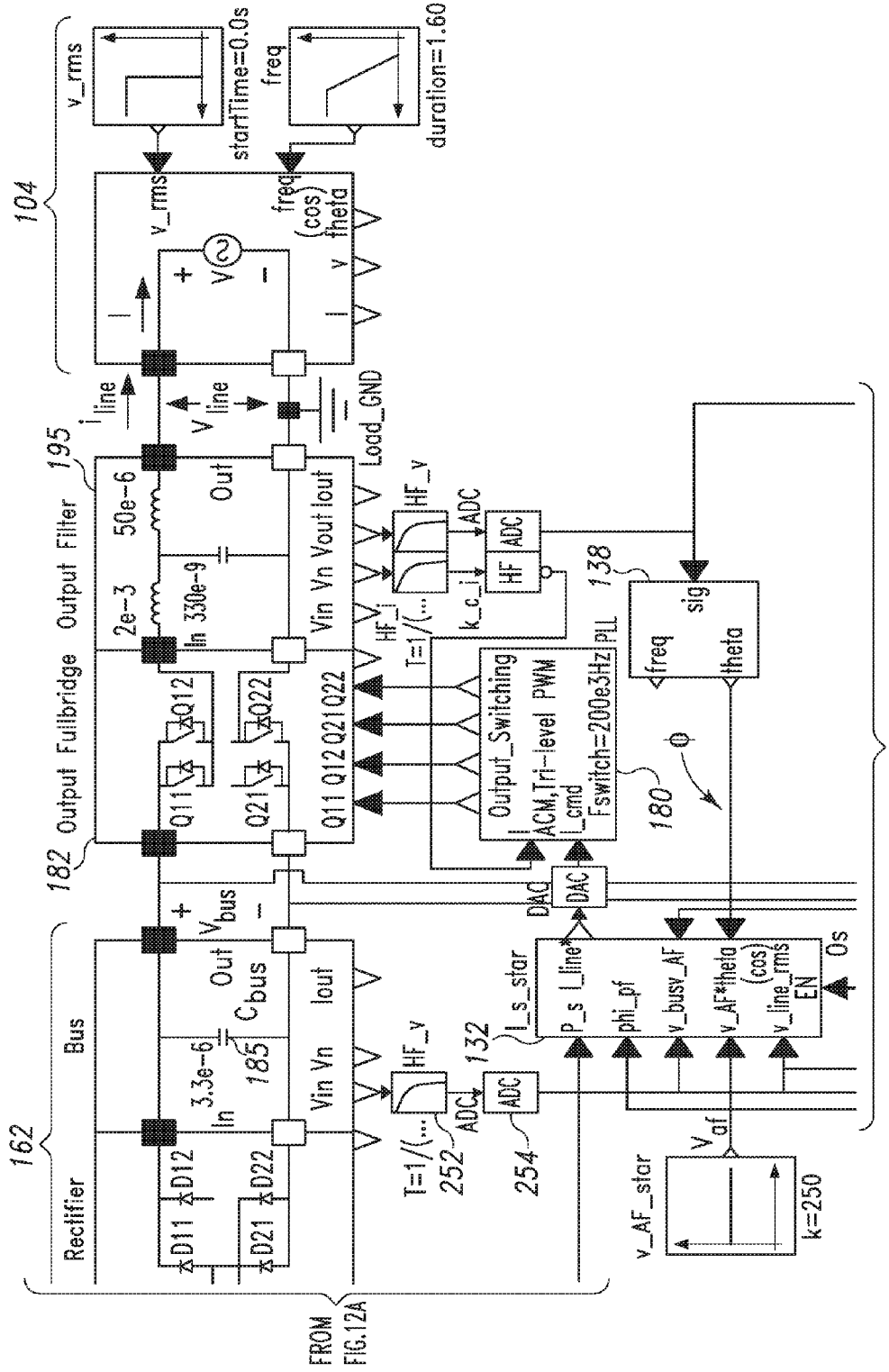
104
v_rms
startTime=0.0s
freq
duration=1.60
freq
(cos) theta
v
i
Load_GND
195
Output Filter
50e-6
2e-3
330e-9
Out
Vin Vn Vout Iout
HF_v
HF_i
ADC
HF ADC
k_c_i
138
sig
freq
theta
PLL
182
Output Fullbridge
Q11
Q12
Q21
Q22
Output_Switching
ACM,Tri-level PWM
I_cmd
Fswitch=200e3Hz
180
DAC
DAC
162
Rectifier
Bus
D11
D12
D21
D22
3.3e-6
185
Cbus
Out
Vin Vn
Iout
HF_v
T=1/(...
252
ADC
ADC
254
132
I_s_star
P_s I_line*
phi_pf
v_busv_AF
v_AF*theta
(cos)
v_line_rms
EN
Os
v_AF_star
Vaf
k=250
FROM FIG.12A
FROM FIG. 12D

Fig. 12B

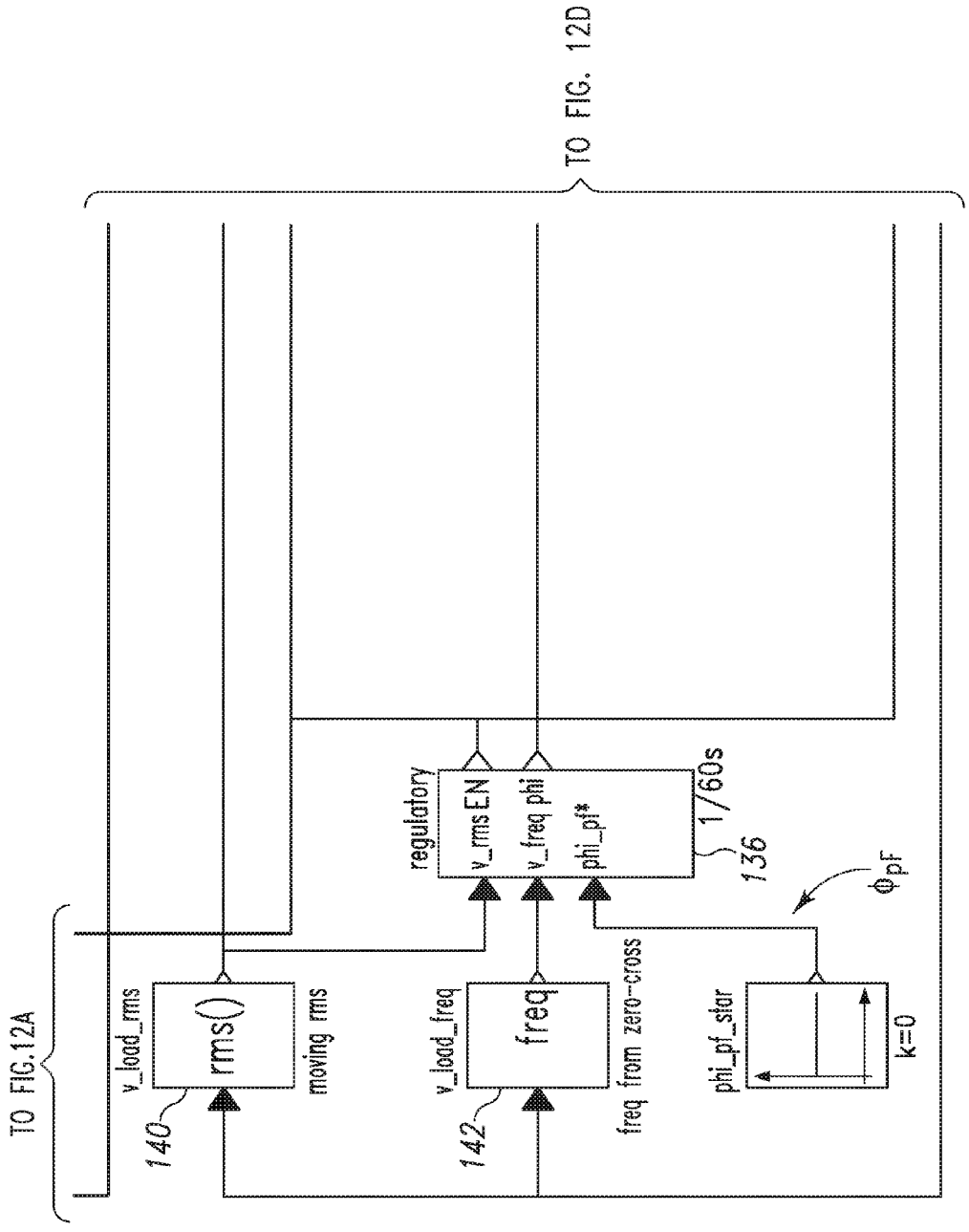
TO FIG. 12D
TO FIG.12A
v_load_rms
rms()
moving rms
140
v_load_freq
freq
freq from zero-cross
142
phi_pf_star
k=0
regulatory
v_rms EN
v_freq phi
phi_pf*
1/60s
136
ϕ_{pF}

Fig. 12C

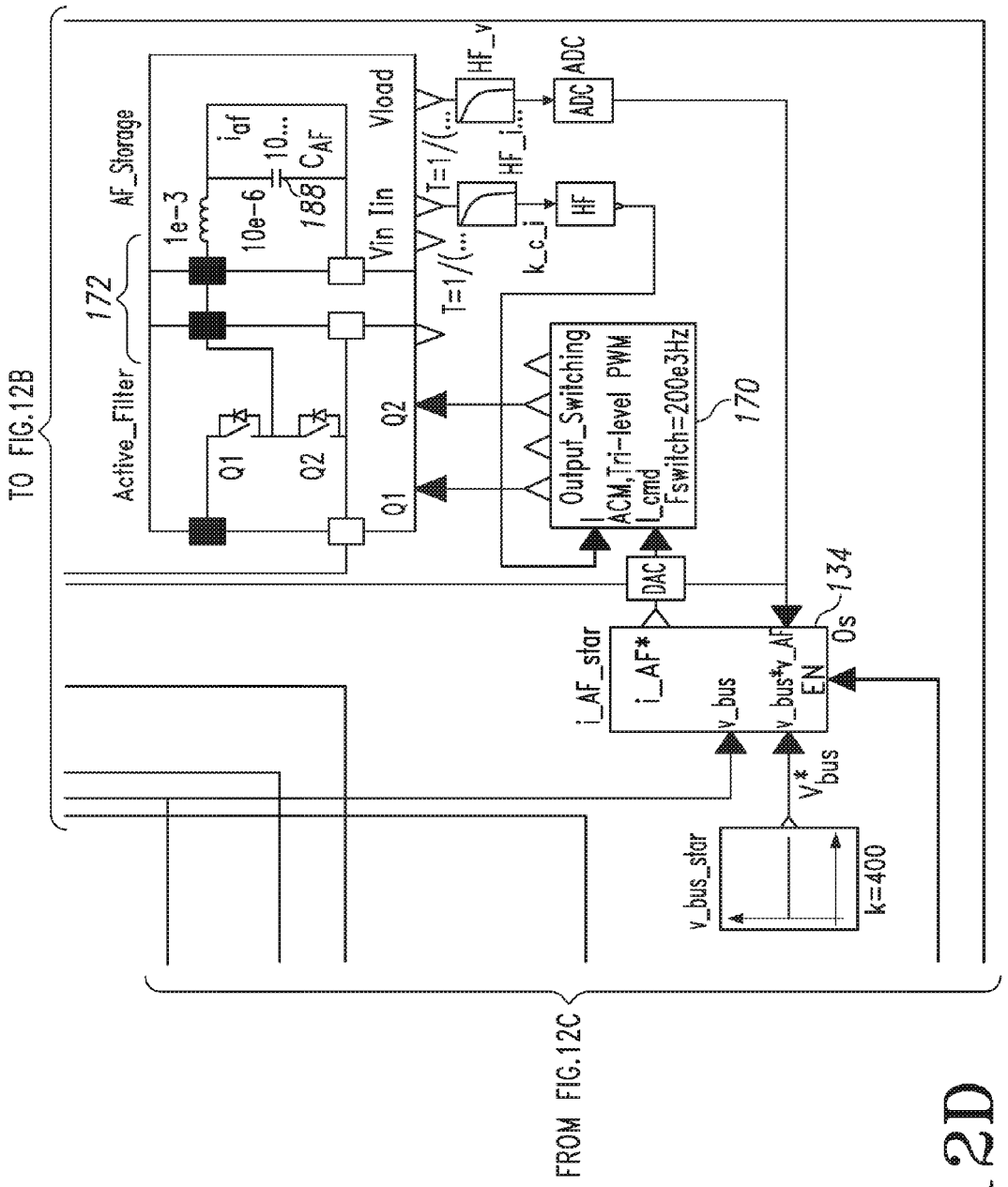
TO FIG.12B
AF_Storage
172
Active_Filter
1e-3
10e-6
iaf
10...
188
CAF
Vload
Vin Iin
Q1
Q2
Q2
Q1
T=1/(...
HF_v
HF_i...
ADC
ADC
k_c_i
HF
Output_Switching
ACM,Tri-level PWM
I_cmd
Fswitch=200e3Hz
170
DAC
i_AF_star
i_AF*
v_bus
v_bus*v_AF
EN
Os
134
V*bus
v_bus_star
k=400
FROM FIG.12C

Fig. 12D

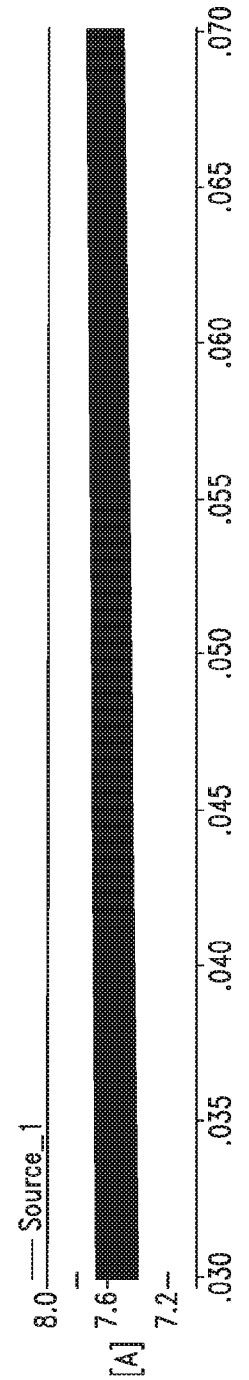

Fig.13A

Fig.13B

Fig.13C

Fig.13D

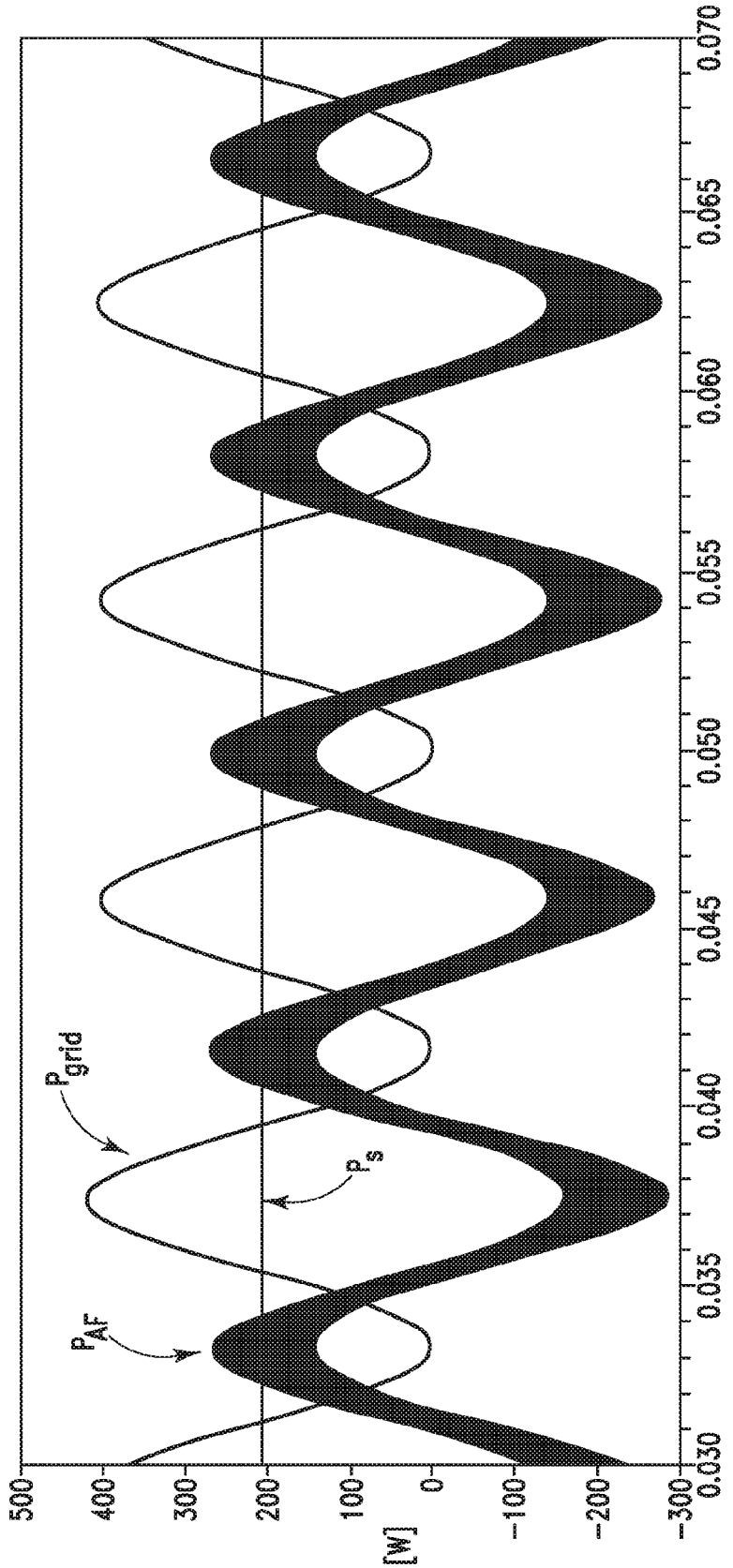
500
400
300
200
100
0
−100
−200
−300
[W]
0.030
0.035
0.040
0.045
0.050
0.055
0.060
0.065
0.070
P_{grid}
P_{AF}
P_s

Fig. 14

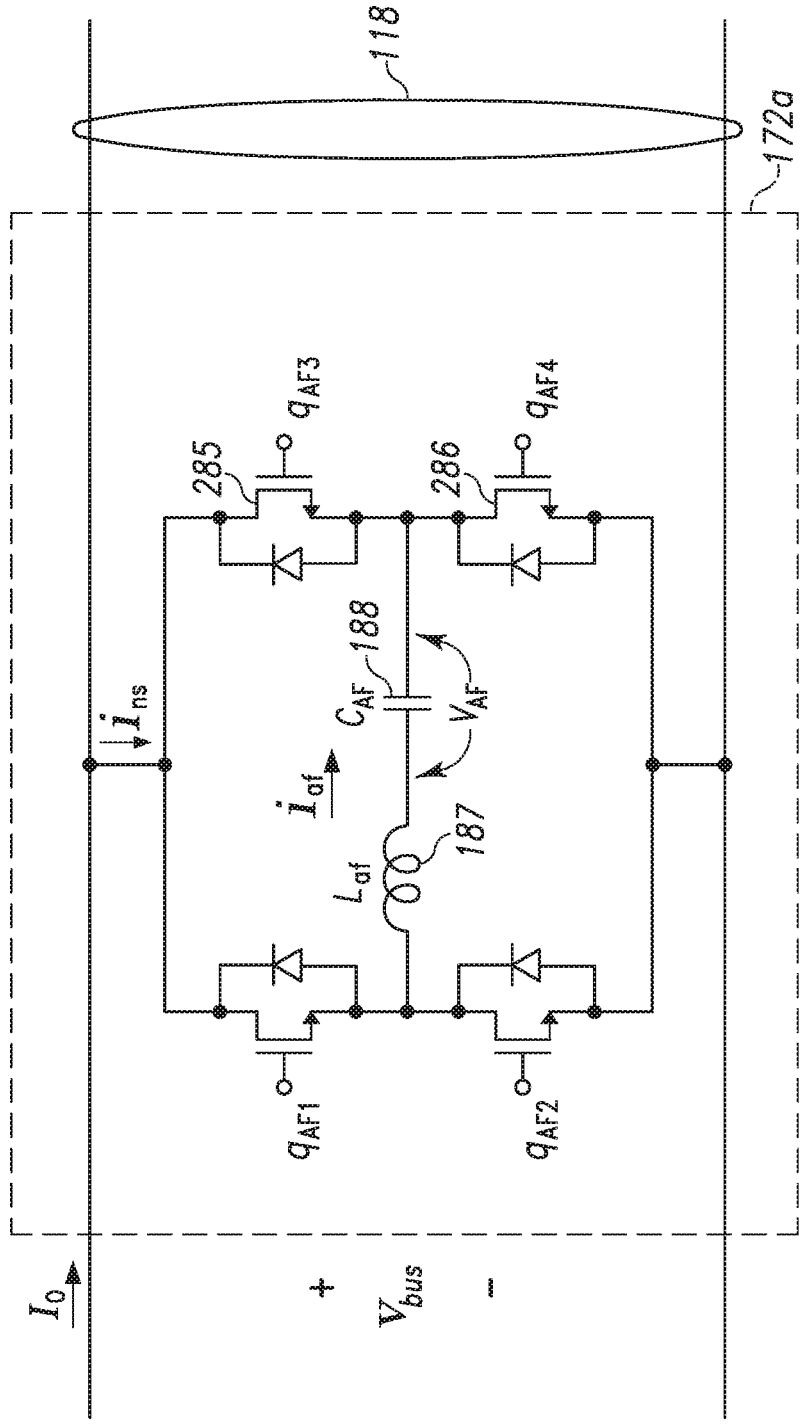
118
172a
285
286
q_{AF3}
q_{AF4}
188
C_{AF}
V_{AF}
i_{ns}
i_{af}
187
L_{af}
q_{AF1}
q_{AF2}
I_o
+
V_{bus}
-

Fig. 15

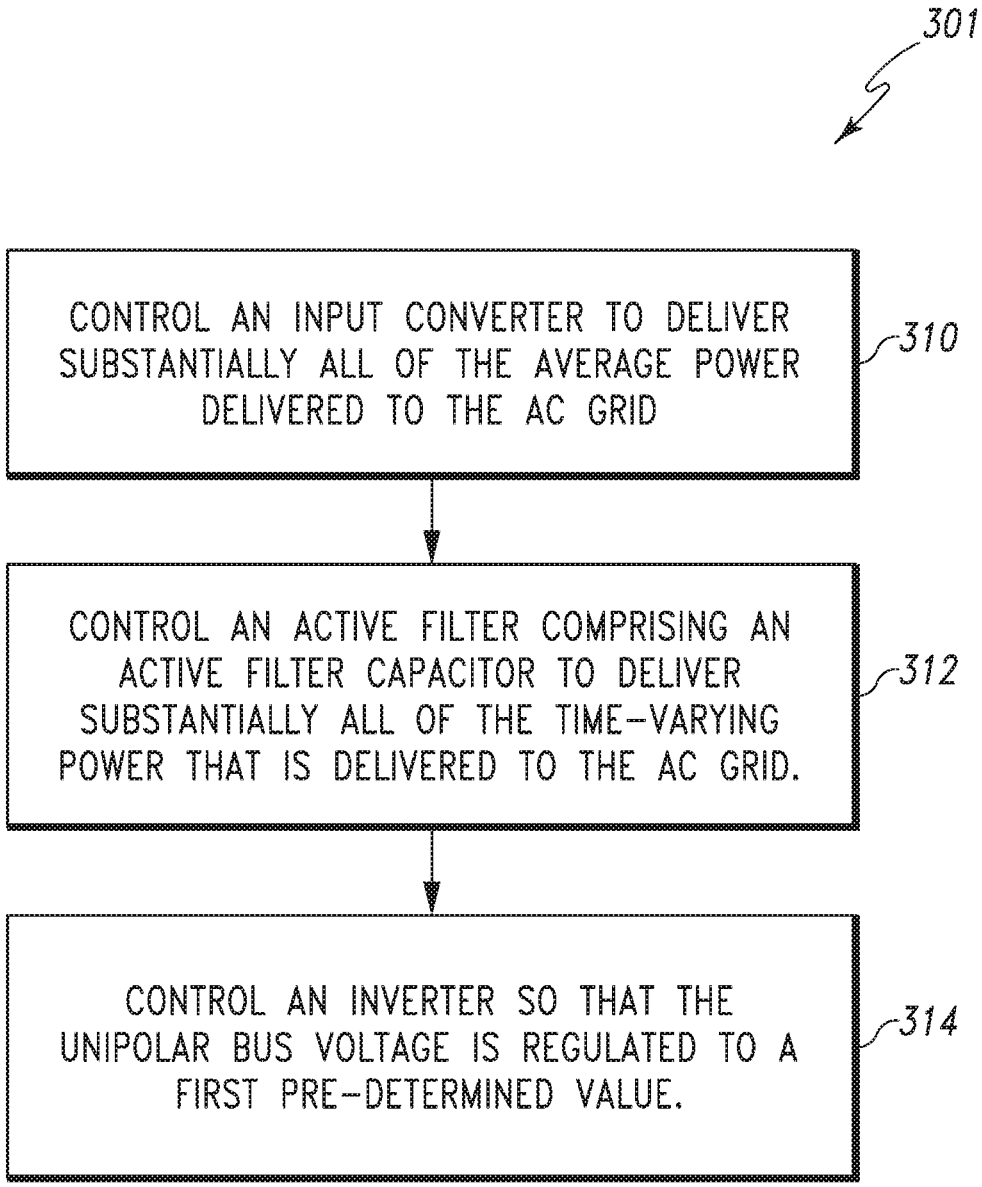
301
CONTROL AN INPUT CONVERTER TO DELIVER SUBSTANTIALLY ALL OF THE AVERAGE POWER DELIVERED TO THE AC GRID
310
CONTROL AN ACTIVE FILTER COMPRISING AN ACTIVE FILTER CAPACITOR TO DELIVER SUBSTANTIALLY ALL OF THE TIME-VARYING POWER THAT IS DELIVERED TO THE AC GRID.
312
CONTROL AN INVERTER SO THAT THE UNIPOLAR BUS VOLTAGE IS REGULATED TO A FIRST PRE-DETERMINED VALUE.
314

Fig. 16

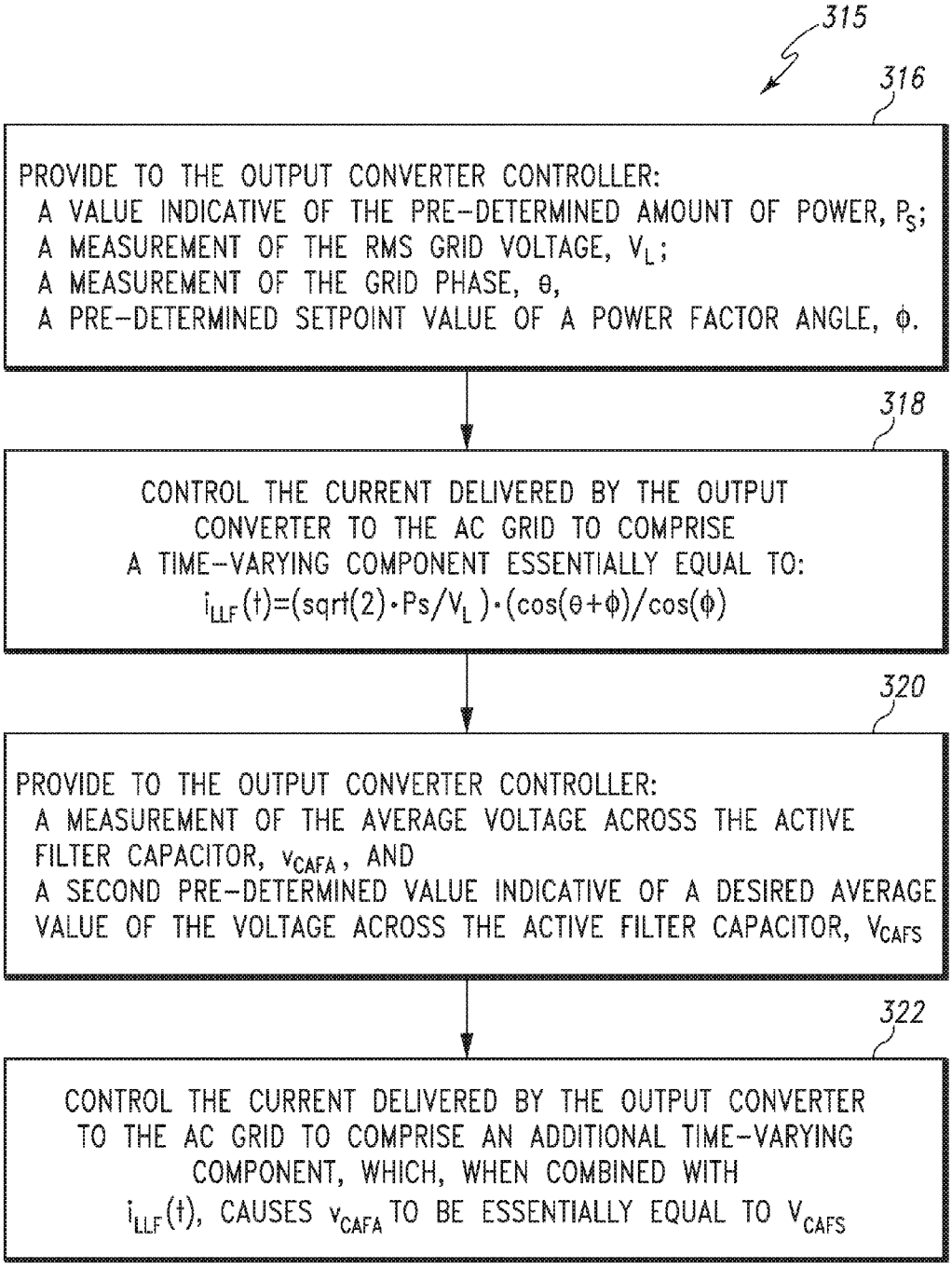
315
316
PROVIDE TO THE OUTPUT CONVERTER CONTROLLER:
A VALUE INDICATIVE OF THE PRE-DETERMINED AMOUNT OF POWER, P_S;
A MEASUREMENT OF THE RMS GRID VOLTAGE, V_L;
A MEASUREMENT OF THE GRID PHASE, θ,
A PRE-DETERMINED SETPOINT VALUE OF A POWER FACTOR ANGLE, ϕ.
318
CONTROL THE CURRENT DELIVERED BY THE OUTPUT CONVERTER TO THE AC GRID TO COMPRISE A TIME-VARYING COMPONENT ESSENTIALLY EQUAL TO:
$i_{LLF}(t)=(\text{sqrt}(2)\cdot Ps/V_L)\cdot(\cos(\theta+\phi)/\cos(\phi)$
320
PROVIDE TO THE OUTPUT CONVERTER CONTROLLER:
A MEASUREMENT OF THE AVERAGE VOLTAGE ACROSS THE ACTIVE FILTER CAPACITOR, v_{CAFA}, AND
A SECOND PRE-DETERMINED VALUE INDICATIVE OF A DESIRED AVERAGE VALUE OF THE VOLTAGE ACROSS THE ACTIVE FILTER CAPACITOR, V_{CAFS}
322
CONTROL THE CURRENT DELIVERED BY THE OUTPUT CONVERTER TO THE AC GRID TO COMPRISE AN ADDITIONAL TIME-VARYING COMPONENT, WHICH, WHEN COMBINED WITH $i_{LLF}(t)$, CAUSES v_{CAFA} TO BE ESSENTIALLY EQUAL TO V_{CAFS}

Fig. 17

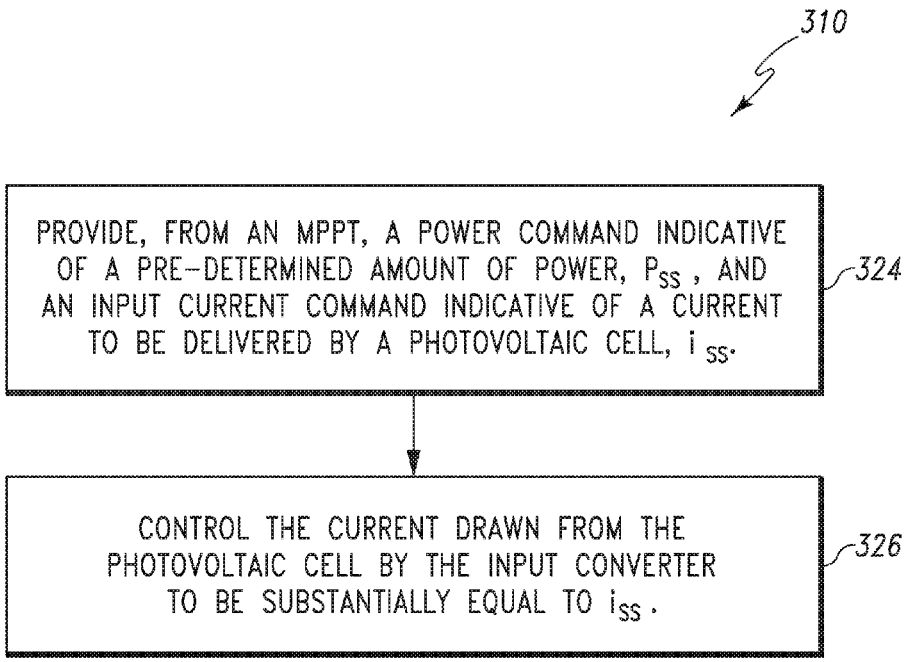
310
PROVIDE, FROM AN MPPT, A POWER COMMAND INDICATIVE OF A PRE-DETERMINED AMOUNT OF POWER, P_{SS}, AND AN INPUT CURRENT COMMAND INDICATIVE OF A CURRENT TO BE DELIVERED BY A PHOTOVOLTAIC CELL, i_{SS}.
324
CONTROL THE CURRENT DRAWN FROM THE PHOTOVOLTAIC CELL BY THE INPUT CONVERTER TO BE SUBSTANTIALLY EQUAL TO i_{SS}.
326

Fig. 18

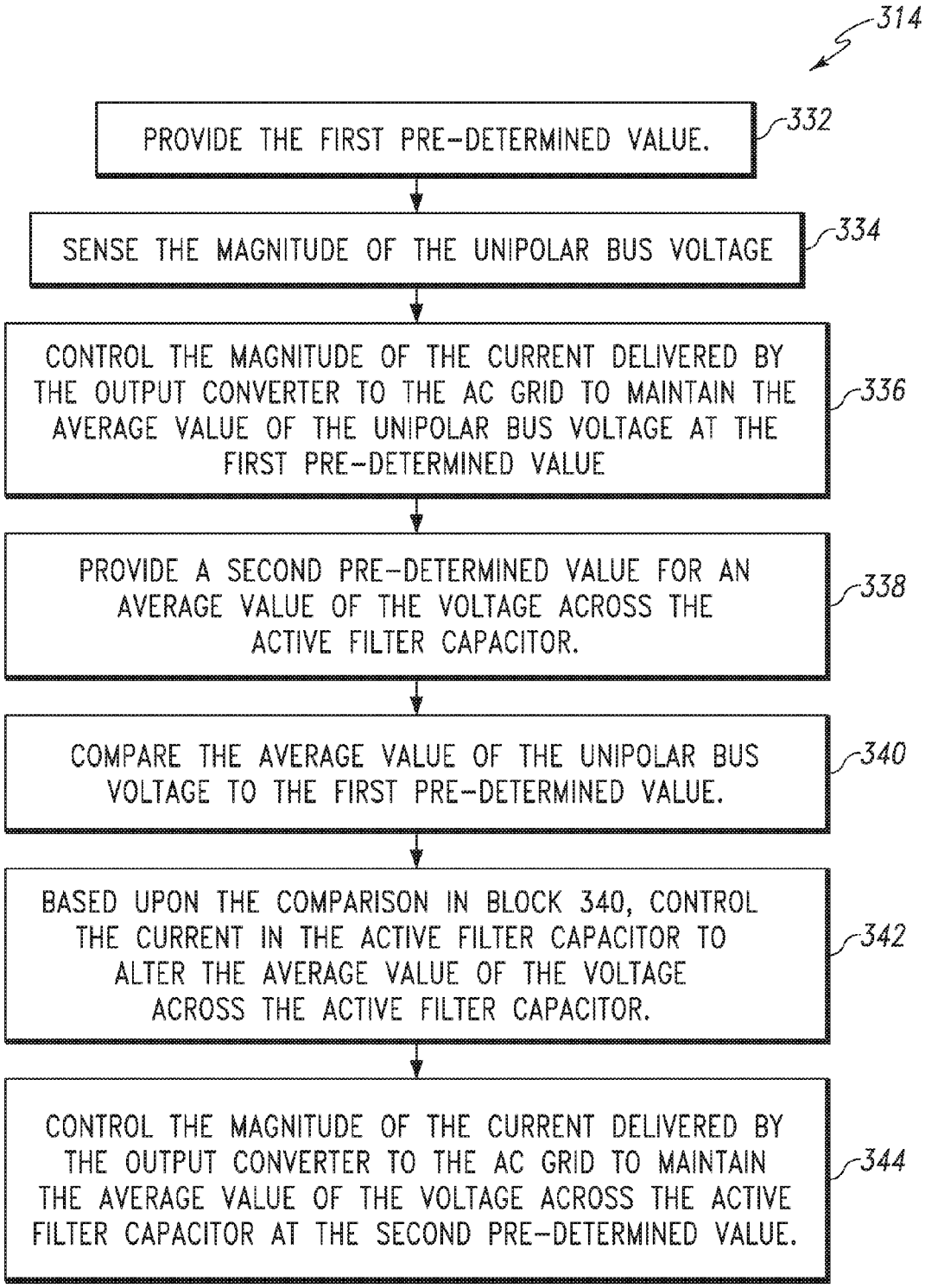
314
PROVIDE THE FIRST PRE-DETERMINED VALUE.
332
SENSE THE MAGNITUDE OF THE UNIPOLAR BUS VOLTAGE
334
CONTROL THE MAGNITUDE OF THE CURRENT DELIVERED BY THE OUTPUT CONVERTER TO THE AC GRID TO MAINTAIN THE AVERAGE VALUE OF THE UNIPOLAR BUS VOLTAGE AT THE FIRST PRE-DETERMINED VALUE
336
PROVIDE A SECOND PRE-DETERMINED VALUE FOR AN AVERAGE VALUE OF THE VOLTAGE ACROSS THE ACTIVE FILTER CAPACITOR.
338
COMPARE THE AVERAGE VALUE OF THE UNIPOLAR BUS VOLTAGE TO THE FIRST PRE-DETERMINED VALUE.
340
BASED UPON THE COMPARISON IN BLOCK 340, CONTROL THE CURRENT IN THE ACTIVE FILTER CAPACITOR TO ALTER THE AVERAGE VALUE OF THE VOLTAGE ACROSS THE ACTIVE FILTER CAPACITOR.
342
CONTROL THE MAGNITUDE OF THE CURRENT DELIVERED BY THE OUTPUT CONVERTER TO THE AC GRID TO MAINTAIN THE AVERAGE VALUE OF THE VOLTAGE ACROSS THE ACTIVE FILTER CAPACITOR AT THE SECOND PRE-DETERMINED VALUE.
344

Fig. 19

APPARATUS AND METHOD FOR CONTROLLING DC-AC POWER CONVERSION

CROSS-REFERENCE TO RELATED U.S. PATENT APPLICATION

This application is a continuation application U.S. application Ser. No. 13/936,744, entitled "Apparatus and Method for Controlling DC-AC Power Conversion," which was filed on Jul. 8, 2013 and which is a continuation application of U.S. application Ser. No. 12/563,495, now U.S. Pat. No. 8,482,947, entitled "Apparatus and Method for Controlling DC-AC Power Conversion," which was filed on Sep. 21, 2009 and which claims priority under 35 U.S.C. §119(e) to U.S. Provisional Patent Application Ser. No. 61/230,546 entitled "Apparatus for Converting Direct Current to Alternating Current," by Robert S. Balog, Jr. et al., which was filed on Jul. 31, 2009, the entirety of all of which is hereby incorporated by reference.

Cross-reference is made to U.S. Utility patent application Ser. No. 12/563,499 entitled "Apparatus for Converting Direct Current to Alternating Current" by Patrick P. Chapman et al., which was filed on Sep. 21, 2009, and to U.S. Utility patent application Ser. No. 11/871,015 entitled "Methods for Minimizing Double-Frequency Ripple Power in Single-Phase Power Conditioners" by Philip T. Krein. et al., which was filed on Oct. 11, 2007, the entirety of both of which is incorporated herein by reference.

TECHNICAL FIELD

The present disclosure relates, generally, to control of power converters that convert DC power to AC power and, more particularly, to control of DC-to-AC converters that deliver power from a photovoltaic source to an AC grid.

BACKGROUND

The amount of power that can be delivered by certain alternative energy sources, such as photovoltaic cells ("PV cells" or "solar cells"), may vary in magnitude over time owing to temporal variations in operating conditions. For example, the output of a typical PV cell will vary with variations in sunlight intensity, angle of incidence of sunlight, ambient temperature and other factors. One application of alternative energy sources is delivery of power to an alternating-current (AC) utility grid. In such applications, an inverter (i.e., a DC-AC power conditioner) is required in order to turn the DC power delivered by the alternative energy source into sinusoidal alternating-current (AC) power at the grid frequency. Certain inverters (e.g., those used by residential customers or small businesses) convert the DC power delivered by the alternative energy source into single-phase AC power and deliver a sinusoidal current to the AC grid at the grid frequency. One figure of merit for such an inverter is the utilization ratio, which is the percentage of available power that it can extract from an energy source. Ideally, an inverter will achieve a utilization ratio of 100%.

Some photovoltaic power systems comprise strings of solar cells that deliver relatively high DC voltages (e.g., nominal 450V). Because operating characteristics of cells in a large string will typically differ, and because individual cells may receive different amounts of sunlight, it is difficult or impossible to run large strings at the combined full power capacity of the individual cells. Strings also typically produce significant power (e.g., kilowatts), which requires a large inverter and high voltage wiring between the cells and the inverter. Additionally, failure of one inverter results in loss of power from the entire string.

Distributed photovoltaic power systems seek to overcome the problems of older, string-based, systems. In a distributed system, each one of a plurality of small, relatively low voltage (e.g. 25V), solar panels are provided with an inverter that feeds power to the AC grid. The benefits of such systems include improved utilization of total available solar cell power and a high level of redundancy: failure of a single inverter or panel may not result in a significant loss in delivered power.

Conversion efficiency in a distributed photovoltaic power system may be improved by placing the inverter in close proximity to its solar panel, thereby eliminating the need to bus a plurality of relatively high solar panel currents to remotely located inverters for processing. Putting the inverter next to its solar panel, however, exposes the inverter to relatively high operating temperatures and may make it more difficult to access for maintenance.

A basic electrical property of a single-phase AC power system is that the energy flow includes both an average power portion that delivers useful energy from the energy source to the load and a double-frequency portion that flows back and forth between the load and the source:

$$p(t)=Po+Po*\cos(2\omega t+\Phi) \quad (1)$$

In applications involving inverters, the double-frequency portion represents undesirable ripple power that, if reflected back into the DC power source, may compromise performance of the source. This is particularly true for photovoltaic cells.

Photovoltaic cells have a single operating point at which the values of the current and voltage of the cell result in a maximum power output. This "maximum power point" ("MPP") is a function of environmental variables, including light intensity and temperature. Inverters for photovoltaic systems typically comprise some form of maximum power point tracking ("MPPT") as a means of finding and tracking the maximum power point ("MPP") and adjusting the inverter to exploit the full power capacity of the cell at the MPP. Extracting maximum power from a photovoltaic cell requires that the cell operate continuously at its MPP; fluctuations in power demand, caused, for example, by double-frequency ripple power being reflected back into the cell, will compromise the ability of the inverter to deliver the cell's maximum power. One analysis has shown that that the amplitude of the ripple voltage across a photovoltaic module should be below 8.5% of the MPP voltage in order to reach a utilization ratio of 98%. Thus, it is preferable that inverters for photovoltaic energy systems draw only the average power portion of the energy flow from the photovoltaic cells at the inverter input. Such inverters should therefore comprise means to manage the double-frequency ripple power without reflecting it back into the source.

To manage double-frequency ripple power, energy needs to be stored and delivered at twice the AC frequency. One way to manage the double-frequency ripple power is to use passive filtering in the form of capacitance across a DC bus. This passive filtering arrangement requires a large capacitance value to filter the double-frequency power, since the energy exchange needs to be supported without imposing significant voltage ripple on the DC bus.

Another way to manage double-frequency ripple power is to use an active filter circuit that supplies the double-frequency ripple power by means of a capacitor internal to

the active filter. Whereas the passive filtering approach requires a relatively large filter capacitor, the internal capacitor in an active filter may be made relatively much smaller, since it is only required to store and deliver the double-frequency ripple power and is not required to support the DC bus voltage. Because the active filter "isolates" the internal capacitor from the DC bus, the voltage variation across the internal capacitor can be relatively large and the value of the capacitor may be made relatively small.

SUMMARY

According to one aspect, an apparatus for controlling the delivery of power from a unipolar input source to an alternating-current (AC) grid at a grid voltage and grid frequency may include an inverter and an inverter controller. The inverter may include an input converter, an active filter, and an output converter. The input converter may be configured to deliver power from the unipolar input source to a galvanically isolated unipolar bus. The active filter may be configured to supply energy to and absorb energy from the unipolar bus. Additionally, the output converter may be configured to deliver power from the unipolar bus to the AC grid.

The inverter controller may be configured to maintain a voltage of the unipolar bus at a pre-determined value. The inverter may include an input converter controller, an output converter controller, and an active filter controller. The input converter controller may be configured to control a current delivered by the input converter to the unipolar bus. The output converter controller may be configured to control the output converter to deliver power to the AC grid. Additionally, the active filter controller may be configured to control the active filter to supply time-varying power to the output converter.

In some embodiments, the active filter controller may be configured to control the active filter to supply substantially all of the time-varying power that is delivered to the output converter at the grid frequency and harmonics of the grid frequency. Additionally, the average power delivered to the grid by the output converter may be controlled by the output converter controller to be substantially equal to the power delivered by the unipolar source less the substantial total of the power losses in the inverter. In some embodiments, the power delivered to the grid may be controlled by the output controller to comprise an average power component and a time-varying power component. Additionally, the active filter controller may control the active filter to deliver substantially all of the time-varying component.

In some embodiments, the active filter is configured as a switching power converter embodied as an active filter capacitor. In such embodiments, the active filter controller may be configured to control the time-varying component by controlling all of the time-varying current that flows in the active filter capacitor. Additionally, the time-varying component may comprise a component at twice the grid frequency. Further, the output converter controller may be configured control the output converter to deliver power to the AC grid in the form of a substantially sinusoidal current at the grid frequency.

In some embodiments, the input converter controller may be embodied as a current-mode controller. Additionally, the output converter controller may be embodied as a current-mode controller. The active filter controller may also be embodied as a current-mode controller. In some embodiments, the galvanic isolation is provided by a transformer. The input converter may be embodied as a current-fed converter. In some embodiments, the input converter may be embodied as an isolated boost converter.

In some embodiments, the switching power converter may be embodied as a half-bridge switching circuit comprising a pair of controllable switches connected to the active filter capacitor. Alternatively, the switching power converter may be embodied as a full-bridge switching circuit comprising two pairs of controllable switches connected to the active filter capacitor. The active filter may be configured to control the switches so that the current in the active filter capacitor comprises a time-varying component comprising harmonics at multiples of the grid frequency. Additionally or alternatively, the active filter controller may control the switches so that the voltage across the active filter capacitor is substantially unipolar.

Additionally, in some embodiments, the active filter controller may be configured to receive a measurement of the unipolar bus voltage, V_{bus}, and a setpoint value indicative of the said pre-determined value for the unipolar bus voltage, V_{Sbus}, and may be configured to control the current flowing in the active filter capacitor, i_{CAF}, so that the magnitude of a ripple voltage across the unipolar bus, at the grid frequency and harmonics of the grid frequency, is reduced towards zero. In some embodiments, the active filter controller may include a feedback controller that delivers a feedback control output, i_{FB}, that is a function of the difference between V_{bus} and V_{Sbus}, and a scaling element that receives a measurement of the voltage across the active filter capacitor, v_{CAF}, and delivers a scaled control output equal to $i_{CAFI}=i_{FB}\cdot(V_{bus}/v_{CAF})$, wherein v_{CAFI} is indicative of a time-varying magnitude of the current that is controlled to flow in the active filter capacitor. Additionally, the active filter controller may include a voltage limiter configured to deliver to the active filter a setpoint, i_{SCAF}, for the current that flows in the active filter capacitor, in accordance with the following logic: i) if the voltage v_{CAF} is less than a pre-determined upper voltage limit and greater than a pre-determined lower voltage limit, i_{SCAF} is set equal to i_{CAFI}; ii) if the voltage v_{CAF} is less than the pre-determined lower voltage limit, i_{SCAF} is forced to be of a polarity that causes v_{CAF} to increase above the pre-determined lower voltage limit; and iii) if the voltage v_{CAF} is greater than the pre-determined upper voltage limit, i_{SCAF} is forced to be of a polarity that causes v_{CAF} to decrease below the pre-determined upper voltage limit.

In some embodiments, the unipolar input source may be embodied as a photovoltaic cell. Alternatively, the unipolar input source may be embodied as a fuel cell. In some embodiments, the pre-determined value of the unipolar bus voltage is a constant value. Alternatively, the pre-determined value of the unipolar bus voltage may be a function of one or more variables. In some embodiments, the pre-determined value of the unipolar bus voltage may be a function of the magnitude of the grid voltage.

Further, in some embodiments, the unipolar input source comprises a photovoltaic ("PV") cell and the input converter controller comprises a maximum-power-point-tracking ("MPPT") device configured to determine the maximum amount of power that may be withdrawn from the photovoltaic cell. In such embodiments, the MPPT device is configured to deliver a setpoint value, i_{SIC}, for the current that is drawn by the input converter from the PV cell. The input converter controller may be configured to receive a measurement of the voltage of the unipolar input source, V_I, and to calculate and deliver a power delivery setpoint $P_S=V_I\cdot i_{SIC}$. In some embodiments, the input converter controller is configured to control the current drawn by the input converter to be essentially equal to i_{SIC}. Additionally, in

some embodiments, the input converter controller is configured to receive a measurement of the unipolar bus voltage V_{bus} and to alter the value of i_{SIC} based upon the value of V_{bus}. In such embodiments, the input converter controller may be configured to progressively reduce i_{SIC} as the value of V_{bus} increases above a pre-determined limit.

The output converter may comprise, in some embodiments, a full-bridge switching circuit comprising two pairs of controllable switches configured to receive power from the unipolar bus and deliver power to the AC grid. Additionally, in some embodiments, the apparatus may further include an output filter connected between the output converter and the AC grid.

In some embodiments, the output converter controller may be configured to comprise a feedforward controller configured to receive: a measurement of the power delivered to the input converter by the unipolar input source, P_S, a measurement of the rms grid voltage, V_L, a measurement of a time-varying phase of the AC grid, θ, a pre-determined setpoint value of a power factor angle, Φ, and wherein the feedforward controller controls the output converter to deliver to the AC grid a time-varying component of current essentially equal to: $i_{LFF}(t)=(\mathrm{sqrt}(2)\cdot Ps/V_L)\cdot(\cos(\theta+\Phi)/\cos(\Phi)$. In such embodiments, (i) the active filter may be embodied as a switching power converter comprising an active filter capacitor and (ii) the active filter controller may be configured to control the current in the active filter capacitor such that the active filter supplies substantially all of the time-varying power delivered to the output converter at the grid frequency and harmonics of the grid frequency and in which the output converter controller comprises a feedback controller that receives: a measurement of the average voltage across the active filter capacitor, v_{CAFA}, and a pre-determined setpoint value indicative of a desired average value of the voltage across the active filter capacitor, V_{CAFS}, wherein the feedback controller controls the output converter to deliver to the AC grid an additional time-varying component of current, which, when combined with $i_{LFF}(t)$, causes v_{CAFA} to be essentially equal to V_{CAFS}.

In some embodiments, the output converter controller may be configured to receive a measurement of the unipolar bus voltage V_{bus} and to alter the magnitude of the current delivered to the AC grid based upon the value of V_{bus}. Additionally, the output converter controller may be configured to progressively reduce the magnitude of the current delivered to the AC grid as the value of V_{bus} decreases below a pre-determined limit. In some embodiments, the output converter controller may comprise a filter that receives a measurement of the voltage across the active filter capacitor and delivers the measurement of the average voltage across the active filter capacitor, v_{CAFA}. In some embodiments, the filter may comprise a notch filter configured to exhibit a sharp attenuation at a frequency equal to twice the grid frequency. Additionally, the filter may further a low-frequency rolloff filter having a pole at a frequency equal to one-tenth of the grid frequency.

According to another aspect, a method for controlling an inverter that is configured to deliver power from a unipolar input source to an alternating-current ("AC") grid at a grid voltage and grid phase may include delivering a pre-determined amount of power from the unipolar input source to a unipolar bus that is galvanically isolated from the unipolar input source using an input converter. The method may also include supplying energy to and absorbing energy from the unipolar bus using an active filter comprising an active filter capacitor and delivering power from the unipolar bus to the AC grid using an output converter. Additionally, the method may include controlling the operation of the inverter using an inverter controller. For example, controlling the operation of the inverter may include controlling the operation of the input converter to deliver substantially all the average power delivered to the AC grid, controlling the active filter to deliver substantially all the time-varying power that is delivered to the AC grid, and regulating the unipolar bus voltage to a first pre-determined value.

In some embodiments, delivering the predetermined amount of power may include delivering the predetermined amount of power from the unipolar input source to the unipolar bus using an input converter comprising a switching power converter. In such embodiments, controlling the operation of the input converter may include controlling the input converter using an input converter controller of the inverter controller to deliver the said substantially all the average power delivered to the AC grid. Additionally, in some embodiments, supplying energy to and absorbing energy from the unipolar bus may include supplying energy to and absorbing energy from the unipolar bus using an active filter comprising a switching power converter. In such embodiments, controlling the operation of the active filter may include controlling the active filter using an active filter controller of the inverter controller to deliver the substantially all of the time-varying power that is delivered to the AC grid. Additionally, in some embodiments, delivering power from the unipolar bus to the AC grid may include delivering power from the unipolar bus to the AC grid using an output converter comprising a switching power converter. In such embodiments, controlling the operation of the output converter comprises controlling the output converter using an output converter controller of the inverter controller to deliver power to the AC grid.

In some embodiments, controlling operation of the active filter may include controlling a time-varying current that flows in the active filter capacitor. In other embodiments, controlling operation of the active filter may include sensing the magnitude of the unipolar bus voltage and controlling the current in the active filter to reduce the ripple across the unipolar bus towards zero. Additionally, in some embodiments, controlling the output converter may include controlling the magnitude of the current delivered by the output converter to the AC grid so that the average power delivered to the grid by the output converter is substantially equal to the power delivered by the unipolar source less the substantial total of the power losses in the inverter. Further, in some embodiments, regulating the unipolar bus voltage may include sensing the magnitude of the unipolar bus voltage and controlling the magnitude of the current delivered by the output converter to the AC grid to maintain the average value of the unipolar bus voltage at the first pre-determined value.

The method may also include providing a second pre-determined value for an average value of the voltage across the active filter capacitor, comparing the average value of the unipolar bus voltage to the first pre-determined value, and, based upon the comparison, controlling the current in the active filter capacitor to alter the average value of the voltage across the active filter capacitor, and controlling the magnitude of the current delivered by the output converter to the AC grid to maintain the average value of the voltage across the active filter capacitor at the second pre-determined value. Additionally, in some embodiments, delivering a pre-determined amount of power from the unipolar input source may include delivering a pre-determined amount of power from a photovoltaic cell. In such embodiments, the method may further include determining the pre-determined amount of

power using a maximum-power-point-tracking ("MPPT") controller and generating a power command indicative of the pre-determined amount of power and an input current command indicative of the current to be delivered by the photovoltaic cell current.

The method may further include controlling the current drawn from the photovoltaic cell by the input converter to be substantially equal to the input current command Additionally, the method may include providing to the output converter controller: a value indicative of the pre-determined amount of power, P_S; a measurement of the rms grid voltage, V_L; a measurement of the grid phase, θ; and a pre-determined setpoint value of a power factor angle, Φ. In such embodiments, controlling the output converter comprises controlling the current delivered by the output converter to the AC grid to comprise a time-varying component essentially equal to: $i_{LFF}(t)=(\text{sqrt}(2)\cdot Ps/V_L)\cdot(\cos(\theta+\Phi)/\cos(\Phi))$. The method may also include providing to the output converter controller: a measurement of the average voltage across the active filter capacitor, v_{CAFA}, and a second pre-determined value indicative of a desired average value of the voltage across the active filter capacitor, V_{CAFS}. In such embodiments, controlling the output converter may include controlling the current delivered by the output converter to the AC grid to comprise an additional time-varying component, which, when combined with $i_{LFF}(t)$, causes v_{CAFA} to be essentially equal to V_{CAFS}.

According to yet a further aspect, a method for improving efficiency in an inverter, which is configured to deliver power from a unipolar input source to an alternating-current ("AC") grid at a grid voltage and grid phase and that operates in accordance with the method described above, may include connecting the active filter directly to the unipolar bus.

DESCRIPTION OF THE DRAWINGS

FIGS. **1**A and **1**B is a block diagram of one embodiment of an inverter according to the present disclosure;

FIG. **2** is a schematic of an embodiment of an input current regulator of the inverter of FIG. **1**;

FIG. **3** is a schematic of embodiments of an active filter and an output current regulator of the inverter of FIG. **1**;

FIG. **4** is a schematic of an embodiment of an output filter of the inverter of FIG. **1**;

FIG. **5** is a block diagram of an input current controller of the inverter of FIG. **1**;

FIG. **6** is a block diagram of an output current controller of the inverter of FIG. **1**;

FIG. **7** is a block diagram of an active filter controller of the inverter of FIG. **1**;

FIGS. **8**A, **8**B, **9**A, **9**B, **10**A, **10**B, **11**A, and **11**B illustrate simulated inverter waveforms of various circuits of the inverter of FIG. **1**;

FIGS. **12**A through **12**D is a schematic illustrating a simulation model of an inverter system according to the present disclosure;

FIGS. **13**A through **13**D and **14** illustrate, respectively, simulation waveforms and power flows for the inverter system of FIG. **12**;

FIG. **15** illustrates another embodiment of an active filter of the inverter of FIG. **1**;

FIG. **16** illustrates one embodiment of a method for controlling an inverter according to the present disclosure;

FIG. **17** illustrates one embodiment of a method for controlling an output converter according to the present disclosure;

FIG. **18** illustrates one embodiment of a method for controlling an input converter according to the present disclosure; and

FIG. **19** illustrated one embodiment of a method for regulating a unipolar bus voltage of an inverter according to the present disclosure.

DETAILED DESCRIPTION

While the concepts of the present disclosure are susceptible to various modifications and alternative forms, specific exemplary embodiments thereof have been shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that there is no intent to limit the concepts of the present disclosure to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

References in the specification to "one embodiment", "an embodiment", "an example embodiment", etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

Some embodiments of the disclosure, or portions thereof, may be implemented in hardware, firmware, software, or any combination thereof. Embodiments of the disclosure may also be implemented as instructions stored on a tangible, machine-readable medium, which may be read and executed by one or more processors. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computing device). For example, a machine-readable medium may include read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; and others.

Photovoltaic power systems that supply AC power comprise solar panels for delivering DC power and one or more inverters for converting the solar panel power into AC current for delivery to the AC grid. The DC power delivered by a solar panel is a function of environmental variables, such as, e.g., sunlight intensity, sunlight angle of incidence and temperature.

FIG. **1** shows a block diagram of an inverter **100** according to the present disclosure. The inverter is configured to control the delivery of power from a unipolar input source **102** (e.g., a DC source, a photovoltaic solar cell or module, a fuel cell) to an alternating-current ("AC") grid **104** and, in some embodiments, loads coupled to the AC grid **104**. An example of an AC grid is the utility power grid that supplies utility AC power to residential and industrial users; such a grid is characterized by its essentially sinusoidal bipolar voltage (e.g. voltage Vline, FIG. **1**) and a fixed grid frequency, f (e.g. $f=\omega/2\pi=50$ Hz or 60 Hz).

As shown in FIG. **1**, the inverter **100** comprises an input current regulator **110**, an output current regulator **112**, an active filter **114**, and an inverter controller **116**. A unipolar bus **118**, which is galvanically isolated from the unipolar input source, connects the output of the input converter **120** to the active filter **114** and to the input of the output converter

122. The inverter controller **116** comprises an input converter controller **130**, an output converter controller **132** and an active filter controller **134**. The inverter controller **116** may also comprise other elements, such as regulatory element **136** and PLL **138**, as described below.

Input current regulator **110** is embodied as a current-controlled switching converter that receives an input current command i_s* and controls the average current drawn from the input source **102**, i_s, to be substantially equal to the value indicated by the command value i_s*. With reference to FIG. **1**, input current regulator **110** comprises converter gating generation circuitry **160** and a switching input converter **162**. Converter gating generation circuitry **160** compares a measured value of the current i_s to the input current command i_s*, and, by means of switch control signals **1***c***1**-q**1***c***4**, adjusts the relative timing of switches in the input converter **162** in order to adjust the current i_s delivered by the converter to be substantially equal to the value indicated by i_s*.

An example of an input current regulator **110** is shown in FIG. **2**. In FIG. **2**, an isolated boost switching converter **162** receives power from the unipolar input source **102** at voltage V_s and current i_s. Gating generator circuitry **160** may comprise a proportional-integral ("PI") feedback controller **161** and a pulse-width modulation ("PWM") circuit **163**. A low pass filter ("LPF") **159** in the feedback controller may remove switching noise and other high frequency artifacts from a measured value of i_s which is compared to input current command i_s* at differencing junction **165**. Based upon the comparison, the feedback controller **161** adjusts its output signal, ds, which is delivers to PWM generator **163**. Based upon the received value of ds, the PWM generator **163** controls the relative timing of the switches **171-174** in the converter **162** to adjust the power delivered, and hence the current i_s drawn, by the converter **162**. By this process, the average current drawn by the converter **162** from the input source **102**, i_s, may be regulated to be substantially equal to the current command i_s*.

The converter **162**, comprising input inductor **179**, voltage clamp **199**, and transformer **175**, is one of several possible current-fed converter topologies. The voltage clamp **199** clamps the voltage applied to the bridge circuit formed by the switches **171-174**. The voltage clamp **199** may be embodied as a passive or active circuit. For example, in embodiments wherein the voltage clamp **199** is a passive circuit, a parallel diode and RC circuit may be used. The illustrative transformer **175**, comprising primary winding **176** and secondary winding **178**, provides galvanic isolation between the primary side converter circuitry (including input source **102**) and the secondary side circuitry (including unipolar bus **118**). The turn ratio of the transformer may also provide voltage and current transformation between the input source and the unipolar bus. The switches are turned on and off by the PWM circuitry **163** at a relatively high switching frequency (e.g., at a frequency that is substantially higher than the AC grid frequency). Power is transferred to the output of the inverter **100** (e.g. to unipolar output bus **118**) via isolation transformer **175** and rectifiers **181-184**. A filter capacitor **187** may be included to provide energy storage and filtering.

With reference to FIG. **1**, the output current regulator **112** is embodied as a current-controlled switching converter that receives an output current command i_{line}* and controls the magnitude of the AC current delivered to the AC grid, i_{line}, to be substantially equal to the value indicated by the command value i_{line}*. The output current regulator **112** illustratively comprises converter gating generation circuitry **180** and switching output converter **182**.

An example of an output current regulator **182** is shown in FIG. **3**. In FIG. **3**, the output converter **182** is embodied as a non-isolated full-bridge switching converter, comprising switches **190-193**, that are controlled by output converter gating generator **180** to deliver the current indicated by the command value i_{line}*. The full-bridge configuration enables the output converter to deliver a bipolar voltage, v_{oc}, and bipolar current i_{line}. Control, by gating generator **180**, of the current delivered by output regulator **112**, may be similar to that described above for the input converter shown in FIG. **2**. An output filter **195**, shown in FIGS. **1** and **4**, may be interposed between the output of the output converter **182** and the AC grid **104**, to filter the voltage v_{oc} as a means of reducing conducted interference and satisfying regulatory requirements. As shown in FIG. **4**, the filter **195** may comprise differential-mode inductors, L_{OC1} **196***a* and L_{OC2} **196***b*, a common-mode inductor L_{line1}-L_{line2} **197***a*, **197***b*, and line filter capacitor C_T **198**.

Active filter **114** is embodied as a current-controlled switching converter that supplies energy to or absorbs energy from the unipolar bus **118**, as explained below, in order to supply time-varying components of the power delivered by the output converter **182** to the AC grid **104**. Use of the active filter **114** is intended to reduce or eliminate the amount of time-varying power that must be provided by the input source **102**. Active filter **114** receives an active filter current command i_{af}* and controls the magnitude of the AC current in the active filter, i_{af}, to be essentially equal to the value indicated by the command value i_{af}*.

An example of an active filter **114** is shown in FIG. **3**. In FIG. **3**, the active filter converter **172** illustratively comprises a half-bridge switching converter, comprising switches **185**,**186**, that are controlled by active filter gating generator **170** to control the current flowing in the active filter capacitor, i_{af}, to be essentially equal to the value indicated by the command value i_{af}*. The switches control the charging and discharging of active filter capacitor C_{AF} **188**; an active filter inductor L_{af} is provided in series with C_{AF} to smooth the flow of current, i_{af}, in the capacitor. Control of the active filter converter **172** by gating generator **170** may be similar to that described above for the input converter shown in FIG. **2**.

By placing the active filter across the unipolar bus **118**, instead of across the unipolar input source (or elsewhere in the primary-side circuitry of input regulator **110**), the power processed by the active filter need not be processed by the input converter **162** and passed through the transformer **175**. This simplifies the design of the power transformer (e.g. a two-winding transfer may be used) and may increase the operating efficiency of the inverter because the losses that would otherwise occur in the input converter associated with processing of the active filter power are reduced or eliminated.

Use of active filtering, to provide the time-varying component of the output power, may reduce the required value of energy storage capacitance by a factor of twenty (20) or more, allowing cost-effective use of reliable capacitor technologies (e.g., film capacitors) in both the active filter (e.g., capacitor C_{AF} **188**, FIG. **3**) and in the output converter (e.g., filter capacitor C_{bus} **187**, FIG. **2**). Placement of the active filter across the unipolar bus may also allow operation of the active filter at a relatively high voltage (e.g., 400 Volts, as opposed to a few tens of volts on the solar-cell side of the isolation transformer), which may further improve the power density, and reduce the size, of the active filter capacitor.

A feature of the inverter **100** is that the unipolar bus voltage is regulated to a pre-determined value V_{bus}*. Regulating the unipolar bus voltage is intended to ensure that there is always enough voltage available to regulate the output current, i_{line}, thereby also ensuring continuous delivery of power without or with reduced high distortion. Regulation of V_{bus} may also improve inverter reliability by ensuring that V_{bus} remains within the range of the blocking capability of constituent power semiconductors. For example, in the case of MOSFETs, a 400-V bus voltage, V_{bus}, coupled with 650-V ratings on the semiconductors may result in a highly reliable design because the voltage operating margin of the MOSFETs is relatively high. Operating such MOSFETs at a higher bus voltage, or on a bus whose voltage is allowed to fluctuate to higher voltages, may significantly reduce inverter reliability.

In the remainder of the description that follows we assume that the unipolar input source **102** is a photovoltaic cell or module (collectively referred to herein as a "solar cell"); that the role of the inverter **100** is to regulate the power flow from the solar panel to the AC grid **104**; that the delivery of power to the AC grid **1011** by the output converter **122** is by controlled delivery of a substantially sinusoidal current i_{line} into the AC grid at the grid frequency; and that the converter topology is that illustrated in FIGS. **1** through **4**. However, such assumptions are for the clarity of the description only. It should be appreciated that in other embodiments, other topologies and control methodologies may be used.

Referring to FIG. **1**, the inverter controller **116** provides supervisory control of the input current regulator **110**, the output current regulator **112** and the active filter **114**. That is, the inverter controller delivers current commands to the regulators. The input current regulator receives the current command i_s* from the input converter controller **130**; the output current regulator receives the current command i_{line}* from the output converter controller **132**; and the active filter receives the current command i_{af}* from the active filter controller **134**. In addition, each of the regulators receive measured signals (i.e., signals indicative of the measured values of voltages, currents, or power levels): the input current regulator receives the measured signal i_s, indicative of the value of the current, i_s, drawn by the input converter **162**; the output current regulator receives the measured signal i_{line}, indicative of the value of the actual current, i_{line}, delivered to the AC grid **104** by the output converter **182** (via output filter **195**); and the active filter **114** receives the measured signal i_{af}, indicative of the value of the current, i_{af}, flowing in the active filter capacitor **188**. Use of the same symbols for both actual and measured signals is for ease of discussion. The measured signals may be scaled, level-shifted, filtered, or isolated by known means as needed and it may also be assumed that power signals may be calculated from voltage and current signals in their respective blocks. Furthermore, the fundamental and/or RMS value of the line voltage, v_{line}, as well as its phase angle, θ, may be determined by known means (e.g., as indicated by in FIG. **1** by VMAG block **140** and phase-locked loop (PLL) block **138**).

As previously described, the gating generators **160**, **170**, **180** within each regulator block compare measured current to commanded current and generate the switch timing and gating logic for their respective switching power converters **162**, **172**, **182**. Although specific embodiments of the input converter, output converter and active filter have been described and illustrated (FIGS. **2** and **3**), it is understood that the regulators may be implemented in a number of ways and controlled using conventional methods, such as average current mode control, hysteresis current control, or any current-regulated voltage-source inverter control. A system-level requirement for these regulators may be that they respond to current commands with an effective bandwidth much greater than the line frequency and its lower harmonics. This will generally be true for switching frequencies at or above 10 kHz and reasonable bandwidth limits on the current regulators.

In addition to measured values, certain pre-determined command values are delivered to the inverter controller **116**, as shown in FIG. **1**. One command value is the commanded unipolar bus voltage, V_{bus}*, which indicates a pre-determined value of V_{bus} that is sufficiently high to power the output regulator and active filter. The pre-determined value of V_{bus} may be a constant value (e.g., 400 VDC) or it may be a value that is a function of one or more other variables (e.g., V_{bus} may be a function of AC grid voltage—if the grid voltage is relatively low, e.g., 200 VAC instead of 240 VAC, the value of V_{bus} may be reduced, e.g., to 360 VDC instead of 400 VDC, which may reduce losses in the converter). Another pre-determined command value is the voltage, V_{AF}*, which is the desired average value of the voltage on active filter capacitor C_{AF} **188**. The average value of this voltage is regulated so that the capacitor voltage doesn't "walk" toward one rail (because the active filter is intended to be lossless, there is no load to dispose of a DC offset current that might cause C_{AF} to charge or discharge undesirably). Another pre-determined command value is the power factor angle, Φ_{pf}. The power factor angle commands the phase shift of the line current with respect to the line voltage. One reason to vary the phase shift away from zero may be to supply reactive power to the grid for purposes of providing ancillary services; another reason may be to implement "anti-islanding" protection, a consideration in contemporary inverters—varying Φ_{pf} may enable the controller to sense certain resonant conditions that might otherwise not be detected by other island detection algorithms

Referring to FIG. **1**, one embodiment of an inverter control strategy features simultaneous control of input current i_s, output current i_{line}, active filter current i_{ac}, and unipolar bus **118** voltage, v_{bus}. As discussed above, the input regulator **110** is controlled by the input converter controller **130** to deliver an essentially constant amount of power, Po, to the unipolar bus. A measurement of this power is communicated to the output converter controller **132** which controls the output regulator **112** to deliver a corresponding amount of average power to the AC grid **104** at the grid frequency, $f=\omega/(2\cdot\pi)$. Assuming ideal sinusoidal waveforms for both the grid voltage, V_{line}, and the current, i_{line}, the power delivered to the grid by the output converter, p(t), comprises both an average power component, equal to Po (assuming no losses), and a time-varying component at twice the grid frequency:

$$p(t)=Po+Po*\cos(2\omega t) \tag{2}$$

It is understood that Equation 2 is for the ideal case of perfectly sinusoidal grid voltage and current. In practice, AC grid voltages are generally not perfectly sinusoidal and therefore both the grid voltage and the time-varying power p(t) may contain higher order harmonics of the grid frequency. As the output converter **182** delivers this time-varying power to the AC grid, the active filter controller **134** controls the active filter **114** to supply energy to and absorb energy from the unipolar bus so that essentially all of the time-varying component of p(t) is supplied by the active filter **172**, thereby enabling the solar cell to operate at an essentially constant power point, Po. Use of the active filter

to supply the time-varying power may also reduce the voltage ripple on the unipolar bus **118**. Another feature of the controller **116** is that it regulates the unipolar bus voltage, V_{bus}, to an essentially constant value.

A block diagram of one embodiment of an input current controller **130** for use in an inverter according to the present disclosure is shown in FIG. **5**. A low pass filter **202** (e.g., single pole rolloff at 1 KHz) removes switching noise from a measured value of the solar cell current, i_s, which, along with a measured value of the solar cell voltage, v_s, is delivered to an MPPT controller **200**. The MPPT controller (which may operate in accordance with any one of a number of known MPPT algorithms (see, e.g., U.S. Patent Publication No. 2008/018338, entitled "Ripple Correlation Control Based on Limited Sampling" by Jonathan W. Kimball et al.) establishes the maximum power point, Ps, for the solar cell and calculates and delivers both the corresponding input current command $i_s^*=Ps/v_s$ and the value of $Ps=v_s \cdot i_s^*$. The current command i_s^* is passed to the input current regulator **110** and sets the value of current which input converter **162** is controlled to draw from the solar cell **102**. The value of Ps is passed through a low pass filter **204** (e.g., single pole rolloff at 1 KHz) and delivered to the output converter controller **132** for use in setting a command value for the current, i_{line}, as explained below. The input current controller **130** may also comprise a current limiting circuit **206** that may, depending on the value of the unipolar bus voltage, V_{bus}, set an upper limit, $i_{s\_limit\_max}$, on the value of i_s^*. As shown in FIG. **5**, if V_{bus} is below a pre-determined value, V_{bus_max1} (e.g., 450V), the current command is limited only by the solar cell's maximum allowable operating current i_{s_max}. As V_{bus} rises above V_{bus_max1}, however, the value of i_s^* is progressively reduced until, at a bus voltage at or above V_{bus_max2} (e.g. 500V) it is reduced to zero. By this means, power delivered by the input converter is throttled back if the unipolar bus voltage rises above a defined limit, which might occur, for example, in the event of a rapid change in load or a grid fault.

A block diagram of one embodiment of an output converter controller **132** for use in an inverter according to the present disclosure is shown in FIG. **6**. The output converter controller **132** controls the magnitude and phase of the sinusoidal AC current, i_{line}, that is delivered to the AC grid and also controls the average value of the voltage across the active filter capacitor (C_{AF}, FIG. **3**). The controller **132** receives measured values of the active filter capacitor voltage v_{af}, the unipolar bus voltage v_{bus}, the AC grid line voltage $V_{line(rms)}$ (from line voltage calculator block VMAG, FIG. **1**), and the phase of the AC grid, θ (from PLL **138**, FIG. **1**). Controller **132** also receives commanded values for the average value of the active filter capacitor voltage, V_{af}^*, the power factor angle Φ_{pf}, and the value of solar cell power, Ps, received from input current controller **130** (FIG. **5**). In an ideal system, $\theta=\omega t=2\pi ft$ is considered to be a constant; in real systems, ω varies with time and the PLL must track this variation so that the phase of the current delivered to the AC grid is accurately synchronized to the phase of the grid voltage. Thus, the PLL **138** generates θ by tracking the actual phase of the line voltage (e.g., θ is the mathematical integral of the grid angular frequency ω)).

Filter blocks **230** and **232** extract the average value of the time-varying active filter capacitor voltage v_{af}. Filter block **230** is a low-pass filter (e.g. single pole rolloff at 6 Hz); filter block **232** is a notch filter with a sharp notch at twice the grid frequency. The two filter blocks **230**, **232** remove substantially all of the time-varying components of v_{af} and deliver a measured average value of the filter capacitor voltage, v_{afA}, to the input of PI feedback controller **234** (e.g., $K_{pvaf}=0.00375$ A/V; $K_{ivaf}=0.1$ A/V·s), where it is compared to the commanded value of the average value of the active filter capacitor voltage, V_{af}^*, by summing junction **235**. Differences between the commanded average value and the measured average value of v_{af} are reflected as variations in the signal output of the feedback controller, i_x, which is delivered as an input to summing junction **238**. The other input of summing junction **238** is a calculated nominal value for the line current, $i_{linenom}=\text{sqrt}(2)\cdot Ps/V_{line(rms)}$, delivered by calculator block **236**. $i_{linenom}$ represents the ideal value of line current, at zero power factor, that would result in the output power being equal to the input power. Summing junction **238** adds i_x to $i_{linenom}$ to produce control signal i_w.

Ignoring, for the moment, the positive signal limiter **240** and the bus voltage limiter block **242**, the signal i_w is received at the input of sinusoidal signal generator **244** as the signal i_z. The sinusoidal signal generator **244** generates the sinusoidal, time-varying output current command i_{line}^*:

$$i_{line}^*=i_z\cdot(\cos(\theta)-\tan(\Phi_{pf})\cdot\sin(\theta))=i_z\cdot\cos(\theta+\Phi_{pf})/\cos(\Phi_{pf}) \quad (3)$$

$$i_{line}^*=i_{linenom}\cdot\cos(\theta+\Phi_{pf})/\cos(\Phi_{pf})+i_x\cdot\cos(\theta+\Phi_{pf})/\cos(\Phi_{pf})=\text{iff}(t)+\text{ifb}(t) \quad (4)$$

i_{line}^* consists of two components, a feedforward component, $\text{iff}(t)=i_{linenom}\cdot\cos(\theta+\Phi_{pf})/\cos(\Phi_{pf})$, representing the ideal time-varying line current that would result in delivery of Ps watts to the AC grid at the power factor angle Φ_{pf}, and a feedback component, $\text{ifb}(t)=i_x\cdot\cos(\theta+\Phi_{pf})/\cos(\Phi_{pf})$, that is adjusted by feedback controller **234** to ensure that the output power and input power are balanced, as explained below.

In operation, the power delivered to the AC grid should be equal to the power delivered by the solar cell, less the total of circuit and other losses, else the unipolar bus voltage may go out of control. If too little power is delivered to the grid, the bus voltage will rise; if too much is delivered, the bus voltage will fall. Because the calculated nominal value of line current, $i_{linenom}$, is subject to measurement and calculation errors and cannot accurately account for the range of possible variations in circuit losses and other factors that affect power delivery, i_{line} cannot be controlled by feedforward control alone.

During steady-state operation, a variation in the unipolar bus voltage, V_{bus}, resulting, e.g., from variations in power delivered by the output converter, will result in a variation in the average value of the filter capacitor voltage. For example, if the power delivered by the output stage is low relative to the power delivered by the input converter, both the unipolar bus voltage and the average value of the voltage across the active filter capacitor will tend to increase. This increase will cause the output of feedback controller **234**, i_x, to increase, thereby increasing the magnitudes of ifb(t) and i_{line}^* (Equation 4) and increasing the power delivered to the AC grid. By this feedback process, the power delivered to the AC grid will be adjusted so that power flow from input to output is properly balanced and so that the average value of the voltage across the active filter capacitor is controlled to be at its commanded value, V_{af}^*.

Referring again to FIG. **6**, bus voltage limiter block **242** provides attenuation in the magnitude of i_{line}^* if the unipolar bus voltage, V_{bus}, drops below a pre-defined minimum value V_{bus_min2} (e.g., 350 V). If the bus voltage is at or above V_{bus_min2} there is no attenuation; for bus voltages between V_{bus_min2} and V_{bus_min1} (e.g., 300 V) the magnitude of i_{line}^* is progressively attenuated until, at voltages at or below V_{bus_min1}, i_{line}^* is reduced to zero. By this means, power

delivered by the output converter is throttled back if the bus voltage falls below a defined limit, which might occur, for example, in the event of a sudden decrease in input power or a grid fault. Positive signal limiter **240** ensures that the command signal into sinusoidal signal generator **244** can never be negative.

A block diagram of one embodiment of an active filter controller **134** for use in an inverter according to the present disclosure is shown in FIG. **7**. The active filter controller **134** receives measured values of the unipolar bus voltage V_{bus} and the time-varying active filter capacitor voltage v_{af} and also receives the commanded value for the unipolar bus voltage V_{bus}*. The active filter controller controls the current in the active filter capacitor, i_{af}, as a means of controlling the voltage ripple on the unipolar bus and also, in concert with the output voltage controller **132**, controls the DC magnitude of the unipolar bus voltage.

Summing junction **209** in PI feedback controller **208** (e.g., K_{pvbus}=0.04125 A/V; K_{ivbus}=259 A/V·s) compares a measured value of V_{bus} to the commanded value, V_{bus}*, and produces a first error signal, i_{hs}*, which is scaled, by scaling block **210**, by a factor V_{bus}/v_{af}. The scaling factor is derived from the requirement that the power delivered by the capacitor be essentially equal to the power delivered to the unipolar bus:

$$V_{bus} \cdot i_{hs} = v_{af} i_{af} \tag{5}$$

where i_{hs} (FIG. **3**) is the current flowing into the active filter from the unipolar bus and i_{af} is the current in the active filter capacitor **188**. Therefore $i_{af}=(V_{bus}/v_{af})\cdot h_{is}$. Ignoring, for the moment, limiter blocks **212** and **214**, the output of scaling block **210** will be delivered to the active filter as the current command signal i_{af}*.

Because the PI controller **208** receives a DC setpoint, it controls i_{af}* so that AC variations on the unipolar bus (e.g., ripple at the grid frequency and harmonics of the grid frequency) are driven towards zero. Because reflection of ripple power back into the solar cell would cause voltage ripple on the unipolar bus, controlling the active filter to cancel or reduce bus ripple requires that the active filter deliver substantially all of the time-varying power required by the output converter.

The active filter controller **132** also regulates the average value of the bus voltage V_{bus}. If, for example, the average value of V_{bus} rises above the commanded value, V_{bus}*, the PI controller will increase i_{af}, thereby also increasing the average voltage across the active filter capacitor, v_{af}. As discussed previously, the output current controller (**132**, FIG. **6**) will respond to an increase in the average value of v_{af} by increasing the line current, i_{line}, which will, in turn, cause a compensating reduction in V_{bus}.

Limit block **212** prevents the capacitor voltage from exceeding maximum and minimum voltage limits. If the voltage v_{af} increases above an upper limit V_{af_max} (e.g. 450 V) the limiter will force i_{af}* to be negative, supplying energy to the unipolar bus and reducing v_{af}, until v_{af} drops back below the upper limit; if the voltage v_{af} decreases below a lower limit V_{af_min} (e.g., 50V) the limiter will force i_{af}* to always be positive, withdrawing energy from the unipolar bus and increasing v_{af}, until v_{af} comes back above the lower limit. Limiter block sets maximum and minimum limits (e.g. +3 A, −3 A) on the commanded active filter current to reduce the possibility of excessive filter capacitor current causing the capacitor voltage v_{af} to exceed the maximum and minimum operating voltage limits of the filter (e.g., V_{bus} and zero). Also shown in FIG. **7**, a windup limit **213** (e.g. 1 A) is imposed on the maximum value that can be output by the integrator in the PI controller **208**.

Maintaining the active filter capacitor voltage, v_{af}, at an appropriate average value, v_{AF}, improves operation of the inverter. Ignoring switching artifacts, the active filter capacitor voltage v_{af} comprises a DC component, v_{AF}, and an AC component having a peak-to-peak variation that increases with increasing inverter output power. Because the active filter (**172**, FIG. **3**) comprises a half-bridge converter, the controllable operating range of the active filter capacitor voltage lies between zero volts and V_{bus}. Thus, both the capacitor value, C_{AF}, and the average voltage, v_{AF}, may be selected to be consistent with delivering full inverter output power while maintaining the peak-to-peak variation of v_{af} within the controllable voltage operating range.

FIGS. **8** through **11** show simulated waveforms illustrating the effects of average capacitor voltage on inverter performance FIGS. **8-11** illustrate wave forms of a converter comprising the conversion circuits shown in FIGS. **2** through **7**. In the FIGS. **8-11**, the active filter capacitor value is C_{AF}=10 μF and the average value of the unipolar bus voltage V_{bus}*=400 V. The simulations were performed using an averaging model for the converter, so switching waveforms and noise are not present.

FIGS. **8**A, **9**A, **10**A and **11**A show the voltage across the active filter capacitor, v_{af}; FIGS. **8**B, **9**B, **10**B and **11**B show the active filter capacitor current i_{af}. FIGS. **8**A and **8**B show waveforms for an inverter operating with an average filter capacitor voltage V_{AF}=260V and at full rated power, Ps=210 Watts; FIGS. **9**A and **9**B show waveforms for an inverter operating with an average filter capacitor voltage V_{AF}=260V and with Ps=105 Watts; FIGS. **10**A and **10**B show waveforms for an inverter operating with an average filter capacitor voltage V_{AF}=225V and with Ps=210 Watts; and FIGS. **11**A and **11**B show waveforms for an inverter operating with an average filter capacitor voltage V_{AF}=200V and with Ps=210 Watts.

FIGS. **8** and **9** show waveforms for an inverter in which the average value of the active filter capacitor voltage (260V) has been selected to be approximately at the midpoint in energy between the maximum capacitor operating voltage (approximately 350V, FIG. **8**A) and the minimum capacitor operating voltage (approximately 150V, FIG. **8**A). The waveforms are smooth and well-behaved, both at full power (FIG. **8**) and at half power (FIG. **9**). FIG. **9** shows that the peak-to-peak variations in both the active filter voltage and current decrease with decreasing inverter output power.

FIG. **10** shows waveforms for an inverter in which the average value of the active filter capacitor voltage (225V) is lower than that in the converter of FIGS. **8** and **9**. The active filter voltage (FIG. **10**A) is approaching a rectified sine wave and is on the verge of clipping, approaching within approximately 50V of both its lower and upper operating voltage limits; the active filter capacitor current (FIG. **10**B) is exhibiting rapid rates of change, owing to the rapid change in slope around the minimum voltage peak of the voltage waveform. Sharp discontinuities of this kind may result in reduced control performance, causing both an increase in the power reflected back into the solar cell and an increase in distortion in the current delivered to the AC grid.

In FIG. **11**, the average value of the active filter capacitor voltage (200V) has been further reduced. The active filter capacitor voltage (FIG. **8**A) is clipping and severe distortion is seen in the capacitor current (FIG. **8**B). Operation in clipped mode will result in an increase in the power reflected back into the solar cell and an increase in distortion in the current delivered to the AC grid **104**.

Providing sufficient active filter capacitor operating voltage margins (i.e., the difference between minimum and maximum capacitor operating voltages at full operating power and their respective operating limits (0V and V_{bus}, respectively)), as illustrated in FIGS. **8** through **11**, may prevent clipping and reduce the maximum rate-of-change of the voltage across the active filter capacitor. The positive effects of increased voltage margins may include smoother waveforms and better control performance, as also illustrated in FIGS. **8** through **11**. Increased voltage margins are, however, traded off against capacitor size and cost, since increased margins imply reduced energy storage. As a practical matter, however, sufficient voltage margins may ensure long-term reliability, because both the peak-to-peak variation, and the average value, of the voltage across the active filter capacitor are subject to variations arising from tolerances in the value of the active filter capacitor and other circuit components and voltages, and to variations owing to aging and thermal and other environmental and operating factors. As such, operating voltage margins sufficient to ensure predictable operating performance and low distortion over the full range of operating conditions and the full expected life of the inverter may be used.

In other embodiments, the active filter may, as shown in FIG. **15**, be configured as a full-bridge switching converter **172***a*. A benefit of using a full-bridge configuration is the bipolar voltage across the active filter capacitor, which may have a more consistently sinusoidal waveform than the voltage in the half-bridge embodiment; a drawback is the increased cost associated with the additional switches **285**, **286** and the more complex controller required to drive the additional switches (not shown in FIG. **15**).

FIG. **12** shows a simulation model of an inverter **300** according to the present disclosure. The unipolar input source **102** is a simulated solar cell. Isolated boost input converter **162**, of the type shown in FIG. **2** (with the addition of a 4.7 μF input filter capacitor C_{IN} **250**, FIG. **12**), is controlled by input converter gating generator **160** and input current controller **130**, also of the types previously described. Input converter **162** operates at a switching frequency of 50 kHz and comprises a 3.3 μF filter capacitor C_{bus} **187**. Referring to FIGS. **2**, **5** and **12**, input gating generator **160** comprises a single-pole LPF with a time constant of 3.18 microseconds, a PI controller with K_p=0.3 and K_i=10,000, and limits on ds set for 0% and 98%; parameters for the input current controller **130** are those described previously with respect to FIG. **5**. Full-bridge output converter **162**, of the kind shown in FIG. **3**, and output filter **195**, supply AC current i_{ine} at voltage V_{line}=240 volts RMS to the AC grid **104** at a grid frequency of 60 Hz. Output converter **162** is controlled by output converter gating generator **180** and output current controller **132**, also of the types previously described, and operates at a switching frequency of 50 kHz. Referring to FIGS. **3**, **6** and **12**, output gating generator **180** comprises a single-pole LPF with a time constant of 6.63 microseconds, a PI controller with K_P=0.6 and K_i=25,000, and limits on ds set for 0% and 98%; parameters for the output current controller **132** are those described previously with respect to FIG. **6** and ϵ_{1OC}=0.005, ϵ_{2OC}=0.25 and ω_{0OC}=760.26. Half-bridge active filter **172**, of the kind shown in FIG. **3**, comprises 10 μF active filter capacitor C_{AF}, operates at a switching frequency of 200 kHz and is controlled by active filter gating generator **170** and active filter current controller **134**, of the types previously described. Referring to FIGS. **3**, **7** and **12**, active filter gating generator **170** comprises a single-pole LPF with a time constant of 6.63 microseconds, a PI controller with K_P=0.6 and K_i=25,000, and limits on ds set for 0% and 98%; parameters for the active filter controller **134** are those described previously with respect to FIG. **7**. PLL **139** provides phase information, θ, synchronized to the phase of the AC grid **104**. The simulation model comprises commanded power factor angle Φ_{pf}=0; commanded average active filter capacitor voltage V_{AF}*=250V; and commanded unipolar bus voltage V_{bus}=400 V. Blocks labeled "HF" in FIG. **12** represent hardware filters for filtering switching noise and other relatively high-frequency artifacts from measured signals; blocks marked ADC represent analog-to-digital converters; blocks marked DAC represent digital-to-analog converters. ADC blocks convert analog signal levels to digital format for use by logical controller blocks; DAC blocks take calculated values of variables in digital format from logical controller blocks and convert them to analog values. ADC blocks and DAC blocks are 8-bit or higher in digital resolution. It is understood that in some embodiments supervisory controllers **130**, **132**, **134**, and other control blocks, may be implemented in logic, such as by use of a digital signal processor ("DSP"), and that filters and PI controllers may be implemented in processor code using, e.g., the Tustin transformation and/or other known conversion methods.

Operating waveforms and power flows for the inverter of FIG. **12** are shown in Figures and **14** for a solar cell **102** irradiance level of 1000 W/m^2 and with the solar cell delivering 210 Watts at a MPP corresponding to I_{SC}=I_{MPP}=7.9 A and V_{SC}=V_{MPP}=26.6V. The waveforms in FIG. **13** are for a converter that is converging on, but that has not quite reached, steady-state operation (i.e. FIG. **13**A shows the current I_{SC} delivered by the solar cell (the peak-to-peak ripple is switching noise at 50 kHz); FIG. **13**B shows the unipolar bus voltage, V_{bus}; FIG. **13**C shows the active filter capacitor voltage, v_{af}; and FIG. **13**D shows the sinusoidal current i_{line} delivered to the AC grid **104**. Waveforms are smooth; the input current exhibits no visible double-frequency ripple; the active filter capacitor voltage is free of sharp discontinuities and the output current is low in distortion. The peak ripple on the unipolar bus is approximately +/−1.3% of the DC value of 400v.

FIG. **14** shows power delivered from the input converter, Ps; power supplied and absorbed by the active filter, P_{AF}; and power delivered to the AC grid, P_{grid}. The input power, Ps, exhibits no visible double-frequency power ripple and both the active filter power, P_{AF}, and the grid power, P_{grid}, are smoothly varying and essentially sinusoidal at twice the grid frequency.

FIG. **16** shows a flow diagram illustrating a method **301** of controlling an inverter of the kind that delivers power from a unipolar input source to an AC grid, and that comprises an input converter for delivering a pre-determined amount of power from the unipolar input source to a unipolar bus that is galvanically isolated from the unipolar input source; an active filter comprising an active filter capacitor for supplying energy to and absorbing energy from the unipolar bus; an output converter for delivering power from the unipolar bus to the AC grid; and an inverter controller to control the operation of the input converter, the active filter and the output converter. As previously discussed, the input converter, the active filter and the output converter may, respectively, comprise a switching power converter, and the inverter controller may comprise an input converter controller for controlling the current delivered by the input converter, an active filter controller for controlling the time-varying power delivered by the active filter and an

output converter controller for controlling the power delivered by the output converter to the AC grid.

As shown in FIG. **16**, the method **301** may comprise the following elements: as shown in block **310**, the input converter may be controlled to deliver substantially all of the average power delivered to the AC grid; as shown in block **312**, the active filter, comprising an active filter capacitor, may be controlled to deliver substantially all of the time-varying power that is delivered to the AC grid; and, as shown in block **314**, the inverter may be controlled so that the unipolar bus voltage is regulated to a first pre-determined value.

The method of FIG. **16** may also comprise a method for controlling an output converter **315** as illustrated in FIG. **17**. The method **315** may comprise, as shown in blocks **316** and **318** in FIG. **17**, providing to the output converter controller a value indicative of the pre-determined amount of power, P_S; a measurement of the rms grid voltage, V_L; a measurement of the grid phase, θ; and a pre-determined setpoint value of a power factor angle, Φ; and controlling the current delivered by the output converter to the AC grid to comprise a time-varying component essentially equal to $i_{LFF}(t)=(\text{sqrt}(2)\cdot Ps/V_L)\cdot(\cos(\theta+\Phi)/\cos(\Phi)$. As shown in blocks **320** and **322** in FIG. **17**, the method of controlling the output converter **315** may also comprise providing to the output converter controller a measurement of the average voltage across the active filter capacitor, v_{CAFA}, and a second pre-determined value indicative of a desired average value of the voltage across the active filter capacitor, V_{CAFS}, and controlling the current delivered by the output converter to the AC grid to comprise an additional time-varying component, which, when combined with $i_{LFF}(t)$, causes v_{CAFA} to be essentially equal to V_{CAFS}.

In an inverter in which the unipolar input source comprises a photovoltaic cell and the input converter controller comprises a maximum-power-point-tracking ("MPPT") controller for determining the pre-determined amount of power, the step of controlling the input converter (block **310**, FIG. **16**) may, as illustrated in block **324** of FIG. **18**, comprise providing, from the MPPT, a power command indicative of a pre-determined amount of power, P_{SS}, and an input current command indicative of the current, i_{SS}, to be delivered by the photovoltaic cell current, i_{SS}. The method may further comprise, as illustrated in block **326** of FIG. **18**, controlling the current drawn from the photovoltaic cell by the input converter to be substantially equal to i_{SS}.

As shown in blocks **332**, **334** and **336** in FIG. **19**, a method for regulating the unipolar bus voltage (block **314**, FIG. **16**) may comprise providing the first pre-determined value; sensing the magnitude of the unipolar bus voltage; and controlling the magnitude of the current delivered by the output converter to the AC grid to maintain the average value of the unipolar bus voltage at the first pre-determined value. The method may further comprise, as shown in blocks **338**, **340** **342** and **344**, providing a second pre-determined value for an average value of the voltage across the active filter capacitor; comparing the average value of the unipolar bus voltage to the first pre-determined value; based upon the comparison, controlling the current in the active filter capacitor to alter the average value of the voltage across the active filter capacitor; and controlling the magnitude of the current delivered by the output converter to the AC grid to maintain the average value of the voltage across the active filter capacitor at the second pre-determined value.

The inverter, controllers, and methods described herein may be implemented as discrete circuits or in the form of software code and/or logical instructions that are processed by a microprocessor, digital processor, DSP or other means, or any combination thereof. The logical processes may run concurrently or sequentially with respect to each other or with respect to other processes, such as measurement processes and related calculations. Controllers may be implemented in mixed-signal circuitry; in circuitry comprising mixed-signal circuitry comprising a digital processor core; or in circuitry comprising a combination of mixed-signal circuitry and a separate digital signal processor. They may be implemented as an integrated circuit or a hybrid device. There may also be additional logical processes that may not be shown, such as, e.g., safety and protection mechanisms; timing and frequency generation mechanisms; and hardware and processes related to regulatory requirements. Pre-determined values, such as, e.g., the commanded values V_{bus}* and V_{AF}, may be stored in read-only or re-programmable non-volatile memory or other storage media. Communication means may also be incorporated into the inverter as a means of downloading commanded values or other operating information to the inverter and/or for uploading inverter operating information to user equipment.

Certain embodiments of the present disclosure have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the disclosure. For example, any of a wide variety of known non-resonant and resonant switching power converter topologies may be used in place of the specific converter embodiments described herein. The unipolar input source may be a fuel cell or another kind of DC source. The inverter controller may comprise elements for regulatory and safety monitoring and control (e.g., circuits or processes for disabling the inverter in the event of AC grid fault or input source fault; anti-islanding protection). Switches in power converters (e.g., switches **171-174**, FIG. **2**) are shown to be MOSFETs and to comprise diodes across their terminals. It is understood that other types of switches may be used (e.g., bipolar transistors, IGBTs) and that diodes may be intrinsic to the semiconductor switch or may be discrete devices. Switches may also be provided with passive or active snubbers to prevent losses and/or to limit voltage or current stresses.

There is a plurality of advantages of the present disclosure arising from the various features of the apparatuses, circuits, and methods described herein. It will be noted that alternative embodiments of the apparatuses, circuits, and methods of the present disclosure may not include all of the features described yet still benefit from at least some of the advantages of such features. Those of ordinary skill in the art may readily devise their own implementations of the apparatuses, circuits, and methods that incorporate one or more of the features of the present disclosure and fall within the spirit and scope of the present invention as defined by the appended claim.

The invention claimed is:

1. An apparatus for controlling the delivery of power from a unipolar input source to an alternating-current (AC) grid at a grid voltage and a grid frequency, the apparatus comprising:

an inverter comprising:

an active filter configured to supply energy to and absorb energy from a unipolar bus, wherein the unipolar bus is configured such that power is to be delivered from the unipolar input source to the unipolar bus by an input converter and from the unipolar bus to the AC grid by an output converter; and

an inverter controller configured to (i) control a power delivered by the input converter to the unipolar bus, (ii) control the output converter to deliver power to the AC grid, and (iii) maintain a voltage of the unipolar bus at a pre-determined value, the inverter controller comprising:

an active filter controller configured to control the active filter to supply time-varying power to the output converter.

2. The apparatus of claim **1**, wherein the inverter controller comprises:

an input converter controller to control a power delivered by the input converter to the unipolar bus; and

an output converter controller to control the output converter to deliver power to the AC grid.

3. The apparatus of claim **1**, wherein the unipolar bus is a galvanically isolated unipolar bus.

4. The apparatus of claim **1**, wherein the active filter controller is configured to control the active filter to supply substantially all of the time-varying power that is delivered to the output converter at the grid frequency and harmonics of the grid frequency.

5. The apparatus of claim **1**, wherein the power delivered to the AC grid includes an average power component and a time-varying power component at twice the grid frequency.

6. The apparatus of claim **1**, wherein the power delivered to the AC grid includes an average power component and a time-varying power component; and

wherein the active filter controller is configured to control the active filter to deliver substantially all of the time-varying power.

7. The apparatus of claim **1**, wherein the power delivered to the AC grid includes an average power component and a time-varying power component;

wherein the active filter is configured as a switching power converter comprising an active filter capacitor; and

wherein the active filter controller is configured to control the time-varying power component by controlling all time-varying current that flows in the active filter capacitor.

8. The apparatus of claim **7**, wherein the active filter controller is configured to control switches of the switching power converter such that the current in the active filter capacitor has a time-varying component with harmonics at multiples of the grid frequency.

9. The apparatus of claim **7**, wherein the active filter controller is configured to control switches of the switching power converter such that the voltage across the active filter capacitor is substantially unipolar.

10. The apparatus of claim **7**, wherein the active filter controller is configured to receive a measurement of the unipolar bus voltage, V_{bus}, and a setpoint value indicative of the said pre-determined value for the unipolar bus voltage, V_{Sbus}, and to control the current flowing in the active filter capacitor, i_{CAF}, based on V_{bus} and V_{Sbus} so that the magnitude of a ripple voltage across the unipolar bus, at the grid frequency and harmonics of the grid frequency, is reduced towards zero.

11. An apparatus for controlling the delivery of power from a unipolar input source to an alternating-current (AC) grid at a grid voltage and grid frequency, the apparatus comprising:

an inverter comprising:

an input converter configured to deliver power from the unipolar input source to a unipolar bus;

an active filter configured to supply energy to and absorb energy from the unipolar bus; and

an output converter configured to deliver power from the unipolar bus to the AC grid, and

an inverter controller configured to maintain a voltage of the unipolar bus at a pre-determined value, the inverter controller comprising:

an input converter controller to control a power delivered by the input converter to the unipolar bus;

an output converter controller to control the output converter to deliver power to the AC grid; and

an active filter controller to control the active filter to supply time-varying power to the output converter.

12. The apparatus of claim **11**, wherein the active filter controller controls the active filter to supply substantially all of the time-varying power that is delivered to the output converter at the grid frequency and harmonics of the grid frequency.

13. The apparatus of claim **11**, wherein the average power delivered to the grid by the output converter is controlled by the output converter controller to be substantially equal to the power delivered by the unipolar source less the substantial total of the power losses in the inverter.

14. A method for controlling an inverter that is configured to deliver power from a unipolar input source to an alternating-current ("AC") grid at a grid voltage and grid phase, comprising:

delivering, by an input converter, a pre-determined amount of power from the unipolar input source to a unipolar bus;

supplying, by an active filter, energy to and absorbing energy from the unipolar bus;

delivering, by an output converter, power from the unipolar bus to the AC grid; and

controlling, by an inverter controller, the operation of the inverter by (i) controlling the input converter to deliver a first portion of the average power delivered to the AC grid, (ii) controlling the active filter to deliver a second portion of the time-varying power that is delivered to the AC grid, and (iii) regulating the unipolar bus voltage to a first pre-determined value.

15. The method of claim **14**, wherein controlling the input converter comprises controlling the operation of the input converter to deliver substantially all of the average power delivered to the AC grid.

16. The method of claim **14**, wherein controlling the active filter comprises controlling the active filter to deliver substantially all of the time-varying power that is delivered to the AC grid.

17. The method of claim **14**, wherein supplying energy to and absorbing energy from the unipolar bus comprises supplying energy to and absorbing energy from the unipolar bus by an active filter that includes an active filter capacitor.

18. The method of claim **14**, wherein delivering the pre-determined amount of power comprises delivering a pre-determined amount of power from the unipolar input source to a unipolar bus that is galvanically isolated from the unipolar input source.

19. The method of claim **14**, wherein controlling the active filter comprises:

sensing the magnitude of the unipolar bus voltage, and

controlling the current in the active filter to reduce the ripple across the unipolar bus towards zero.

20. The method of claim **14**, wherein regulating the unipolar bus voltage comprises:

sensing the magnitude of the unipolar bus voltage, and

controlling the magnitude of the current delivered by the output converter to the AC grid to maintain the average value of the unipolar bus voltage at the first predetermined value.

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