



APPLICATION HANDBOOK  
FOR  
A STANDARDIZED CONTROL MODULE (SCM)  
FOR  
DC TO DC CONVERTERS  
VOLUME I  
FINAL REPORT  
BY

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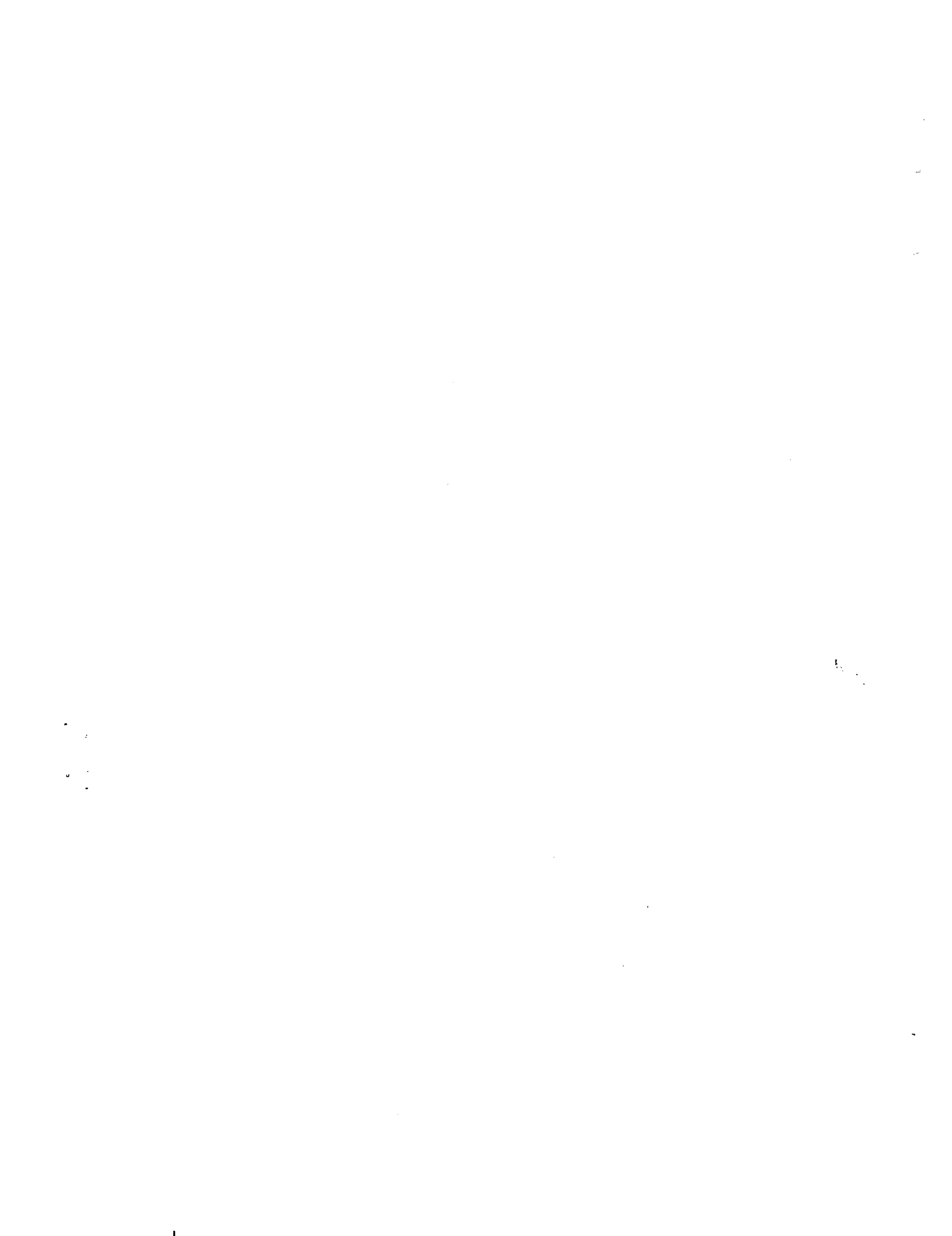
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16. Abstract The Standardized Control Module (SCM) has been developed for application in the Buck, Boost and Buck/Boost DC-DC Converters. The SCM uses multiple feedback loops to provide improved input line and output load regulation, stable feedback control system, good dynamic transient response and adaptive compenstion of the control loop for changes in open loop gain and output filter time constraints. This project, "Application Handbook for a Standardized Control Module (SCM) for DC-DC Converters" develops the necessary modeling and analysis tools to aid the design engineer in the application of the SCM to DC-DC Converters. A discussion is presented on the SCM Functional Block Diagram and the different analysis techniques. The Average Time Domain Analysis technique is chosen as the basic analytical tool. The Power Stage Transfer Functions are developed for the Buck, Boost and Buck/Boost Converters. The Analog Signal and Digital Signal Processor Transfer Functions are developed for the three DC-DC Converter types using the constant on-time, constant off-time and constant frequency control laws. A discussion is presented on the adaptive control concept of the SCM. An analysis is presented on the following DC-DC Converter characteristics: <ul style="list-style-type: none"> <li>● Stability.</li> <li>● Audio-Susceptibility.</li> <li>● Output Impedance and Load Transient.</li> <li>● Input Filter Interaction.</li> <li>● Discontinuous Current Operation.</li> </ul> The Design Handbook (Volume II) is based on the technical results presented in the Final Technical Report (Volume I), and establishes design guidelines and procedures to meet regulator performance specifications using the Standardized Control Module (SCM).					
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## FORWARD

The modeling and analysis tasks were performed by Dr. Fred Lee at TRW Defense and Space Systems Group and later at Virginia Polytechnic Institute and State University under subcontract GB2313CHBM, by Dr. Yuan Yu at TRW Defense and Space Systems Group, and by M. F. Mahmoud at Virginia Polytechnic Institute while working toward his Master Degree in Electrical Engineering.

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## NOTATIONS

The symbols for currents and voltages at the terminals of devices have subscripts. The uppercase and lowercase symbols and subscripts are used to distinguish between instantaneous values, quiescent values, and small signal low-frequency averaged values.

For example:  $v_I$  : input voltage, instantaneous value

$$v_I \approx V_I + \hat{v}_i$$

$V_I$  : input voltage, dc average value

$\hat{v}_i$  : input voltage, small signal low-frequency average term

$v_O$  : output voltage, instantaneous value

$$v_O \approx V_O + \hat{v}_o$$

$V_O$  : output voltage, dc average term

$\hat{v}_o$  : output voltage, small-signal low-frequency average term.

$T_P$  : Period of a switching cycle

$T_{ON}$  : **Switch on time**

$T_{F1}$  : **Switch off time in continuous inductor mmf operation**

$T_{F2}$  : **A portion of the switching off time when the inductor mmf has vanished**

$d$  :  $\frac{T_{ON}}{T}$  duty cycle ratio  $d \approx D + \hat{d}$

$D$  : **Steady state duty cycle ratio**

$\hat{d}$  : **Small signal duty cycle variation**

$d'$  :  $\frac{T_{OFF}}{T_P}$   $d' \approx D' - \hat{d}$

$D'$  : **Steady state value for  $d'$**

$v_C$  : Output filter capacitor voltage

$i_L$  : Inductor current of the buck and boost converter

$\phi$  : Magnetic flux of the energy-storage inductor of the two-winding buck/boost converter

$\underline{x} = [i_L, v_C]^T$  state variables for buck and boost converter

$\underline{x} = [\phi, v_C]^T$  state variables for the buck/boost converter

$v_{DC}$  : dc loop sensing voltage  $v_{DC} = v_O$

$v_{AC}$  : ac loop sensing voltage

#### Power Stage

L : energy storage inductor

$R_\ell$  : winding resistance of L

$R_p, R_s$  : winding resistance of the primary winding and secondary winding, respectively of the two-winding buck/boost converter

C : output filter capacitor

$R_C$  : output filter capacitor ESR

$N_L$  : number of turns of L

$N_p, N_s$  : number of turns for the primary and secondary windings of two winding buck/boost converter

$$\begin{aligned} R_e &= R_\ell && \text{buck} \\ &= R_\ell / (D')^2 && \text{boost} \\ &= R_s / (D')^2 && \text{buck/boost} \end{aligned}$$

$$\begin{aligned}
L_e &= L && \text{buck} \\
&= L/(D')^2 && \text{boost} \\
&= L_S(D')^2 && \text{buck/boost} \\
R_{Ce} &= R_C && \text{buck} \\
&= R_C/D' && \text{boost and buck/boost} \\
R_{eq} &= R_e + R_{Ce} - R_C \\
\omega_o &= 1/\sqrt{L_e C} \\
\zeta &= \frac{1}{2\omega_o} \left[ \frac{1}{CR_L} + \frac{R_e + R_{Ce}}{L_e} \right] \\
\tau_{Z1} &= R_C C
\end{aligned}$$

### Control Circuit

- $R_1, R_2$  : control loop resistor divider
- $R_3$  : dc loop resistor
- $R_4$  : ac loop resistor
- $R_5$  : compensation loop resistor
- $C_1$  : operational amplifier integrator capacitor
- $C_2$  : compensation loop capacitor
- $N_3$  : number of turns of the ac sensing winding
- $n$  : ac loop sensing winding turns ratio .  $n = N_3/N_S$  for buck/boost converter.
- $R_x = R_1 // R_2$
- $g = R_2/(R_1 + R_2)$



$$R_y = (R_3 + R_x)/g$$

$$m = R_4/(n R_y)$$

$$\alpha = R_4/(n R_y) \quad \text{buck}$$

$$= R_4/(D' n R_y) \quad \text{boost and buck/boost}$$

$$A_1 = 1 \quad \text{buck}$$

$$= 1 - \frac{R_{eq}}{R_L} + \frac{2\zeta\omega_o L_e}{R_L} - \left(\frac{L_e \omega_o}{R_L}\right)^2 \quad \text{boost}$$

$$= 1 - \frac{DR_{eq}}{R_L} + \frac{2\zeta\omega_o DL_e}{R_L} - D\left(\frac{L_e \omega_o}{R_L}\right)^2 \quad \text{buck/boost}$$

$$A_2 = 0 \quad \text{buck}$$

$$= 1/(R_L C) \quad \text{boost}$$

$$= D/(R_L C) \quad \text{buck/boost}$$

$$\tau_{Z2} = (R_5 + R_y)C_2$$

$$\tau_{P1} = R_5 C_2$$

$$\alpha' = \frac{\alpha}{A_1 - A_2 \tau_{Z2} \alpha}$$

$$\tau_{Z2}' = \tau_{Z2} \quad \text{buck}$$

$$= \left(\tau_{Z2} + \frac{L_e}{\alpha R_L}\right) \left(1 - \frac{R_{eq}}{R_L}\right) + (1-\alpha) \frac{L_e}{\alpha R_L} \quad \text{boost}$$

$$= \left(\tau_{Z2} + \frac{L_e}{\alpha R_L}\right) \left(1 - \frac{DR_{eq}}{R_L}\right) + (1-\alpha) \frac{DL_e}{\alpha R_L} \quad \text{buck/boost}$$

Pulse Modulator:

$$F_M = \frac{2R_4 C_1}{n M} \quad \text{duty cycle modulator gain}$$

M is defined in Table 7-1

Others:

$$K_1 = \frac{2 V_I}{M} \text{ buck, } K_1 = \frac{2V_I}{D'M} \text{ boost, } K_1 = \frac{N_S}{N_P} \frac{2V_I}{DM} \text{ buck/boost}$$

$$K_2 = D \text{ buck}$$

$$= \frac{D}{D'} \left(1 + \frac{2V_I L e}{R_L M}\right) \text{ boost}$$

$$= \frac{N_S}{N_P} \frac{D}{D'} \left(1 + \frac{2V_I L e}{R_L M}\right) D \text{ buck/boost}$$

$$\mu = 1/D \text{ buck}$$

$$= D' \text{ boost}$$

$$= (N_P D') / (N_S D) \text{ buck/boost}$$

System model:

A. Power stage transfer functions  $F_I, F_D, F_p, Z_p, F_1, F_2, F_3$  and  $F_4$ :

$F_p(s)$  : equivalent output filter transfer function

$F_I(s)$  : input voltage gain, ( $F_I F_p$  represents the open loop input-to-output-voltage transfer function)

$F_D(s)$  : duty cycle gain, ( $F_D F_p$  represents the duty-cycle-to-output-voltage gain)

$Z_p(s)$  : the output impedance of the open-loop converter power stage ( $Z_p \hat{i}_o$  represents the open-loop output voltage variation due to the load current disturbance  $\hat{i}_o$ )

$F_1(s)$  and  $F_2(s)$  together provides the small-signal low-frequency ac inductor (or magnetic flux) current due to disturbances from the output voltage  $\hat{V}_o$  and duty cycle  $\hat{d}$ .

$F_3(s)$  : Impedance function employed to convert the inductor current or magnetic flux into an ac loop error voltage  $V_{ac}(s)$  across the sensing winding.

$F_4(s)$  : Transfer function characterizing the amount of disturbance of the inductor current due to load disturbance.

B. Analog signal processor (ASP) transfer functions:  $F_{DC}$  and  $F_{AC}$ :

$F_{DC}(s)$  : the transfer function of the combined dc loop and RC compensation loop.

$F_{AC}(s)$  : the transfer function of the ac loop

C. Duty cycle pulse modulator transfer function  $F_M$

$F_M$  : the describing function of the duty cycle pulse modulator

Analytical expression for F's are defined in Table 8-1.



## CHAPTER I

### INTRODUCTION

Due to the finite flux capacity of the inductive elements, a dc-dc converter must be oscillatory in nature. The oscillation is achieved by cyclically operating the power switch of the converter in conduction and non-conduction state. Consequently, the converter control system must be able to accept an analog signal obtained from the sensing circuit and the reference, and to convert it into discrete time intervals in controlling the conduction and non-conduction of the power switch.

The electrical performance of a dc-dc converter depends primarily on the quality of its control system. The performance characteristics of interest to a converter designer include stability as well as the converter-output response to step and sinusoidal disturbances, both from the line and the load. The incentive for performance improvement prompted the initial development of a multiple-loop control concept at NASA in the late sixties [1]. Since then, the control concept has undergone several major program efforts, which culminates in the development of a Standardized Control Module (SCM) for dc-dc converter under Contracts NAS3-14392 [2] and NAS3-18918 [3].

Features of the SCM include the following:

#### (1) Adaptive Stability

In the SCM, a conventional dc control loop, sensing the capacitor state variable in the form of output-capacitor voltage, is augmented by an additional ac loop sensing the inductor state. The total sensing of states associated with the LC output filter provides the converter with excellent static and dynamic stabilities in that stable operation immune to output-filter parameter changes can be maintained. Such a characteristic can be significant as most converters do employ second-order filters, and poor phase margins invariably exist if proper control-loop compensations are not provided. Conventional

frequency-response shaping can become grossly ineffective due to variations of power/control component parameters resulting from tolerances, environments, aging, operating condition, and more importantly, external reactive loadings (e.g. capacitor banks). The reactive-loading configurations are often poorly defined or not defined at all during the converter development. A risk thus exists in that the original compensation immaculately conceived for an assumed resistive load may turn out to be grossly ineffective when the converter and the complex loads are ultimately introduced at a rather inconveniently late stage of the program. In contrast, the multiple-loop control used in the SCM will accommodate whatever changes in power/control parameters including reactive loadings, and adaptively maintain the converter-load system stability.

## (2) Power Component Stress Limiting

The reliability of a dc-dc converter depends on the ability of its control system to limit power-component stresses during steady-state and dynamic operations such as step line/load changes, sudden output faults, and converter starting. Without this stress control, the reliability data based on collective component statistical failure rates becomes meaningless, and no elaborate quality assurance can increase the level of confidence. The SCM achieves the reliability enhancement, through standard circuit implementations, to limit electrical stresses in all converter power components on an instantaneous basis, thus ensuring orderly and predictable steady-state as well as transitional operations between steady states.

## (3) Implementation of Various Control Laws

Various control laws can be used to govern the power switch conduction (on) and non-conduction (off). While it is true that quite often only the achievement of a control objective is important and that the means employed to accomplish the objective is irrelevant, the use of a given duty cycle control law for dc to dc converter is mandatory for many specific applications. For example, requirements on electromagnetic compatibility may dictate a control based on a constant switching frequency,

whereas in series resonant type of applications a sinusoidal current in the power switch for one half of a resonant cycle inherently demands a control law based on a constant power-switch conduction time. In this regard, the SCM is capable of implementing a maximum number of control laws through minimum circuit changes.

#### (4) Unification of Design Approach.

Performance characteristics of dc-dc switching regulators are largely dictated by the particular power stage configuration and control scheme chosen. Often in the design practice, when a power stage configuration is chosen and parts designed, the subsequent attention is focused on selecting the most suitable control method and frequency stabilization (compensation) network in order to optimize the overall system performance. The lack of universal control method and a uniform design strategy often necessitates the undertaking of time-consuming paper and bench design iterations which frequently result in incompatible and intricate performance characteristics. The SCM control provides a unified design procedure which enables the designer to select the control circuit parameters so that, for an arbitrarily given power stage, the prescribed performance characteristics concerning stability, audiosusceptibility and transient response can be met concurrently.

These merits have been thoroughly demonstrated through performances exhibited by power processors controlled by the SCM. In conjunction with NASA's increasing demand for development and manufacturing cost reduction through design and fabrication standardization, these features have provided NASA with the necessary impetus to enhance the widespread applicability of the SCM. Such an enhancement will invariably lead to reduced cost and improved performance for future NASA and military-related power processing programs.

The necessary conditions for a given control system to flourish must contain the following ingredients: (1) a basic system concept capable of providing unique and outstanding control characteristics, (2) various equipment using the control system and demonstrating superior performances, and (3) the availability of analytically-based control system design guidelines from which the converter performance can be predicted.

Previous SCM-related programs have been, to a large extent, oriented toward the first two conditions. The effort was essential in establishing the multiple-loop SCM as a high-performance control concept that is applicable to a variety of power converters, thus paving the way for its acceptance and further development. With such a demonstration now properly fulfilled, attention is naturally focused on the third aspect concerning the design/analysis of the SCM. It is therefore the objective of the current contract to perform the SCM control-system analysis and to generate control-system design guidelines. These guidelines are expected to enable an engineer to design readily the SCM control-circuit parameters and to confidently predict that the converter performances based on such a design will satisfy the specified requirements. It is immediately apparent that such an endeavor transcends the effort normally involved in a task whose singular objective is to provide only the control-system analysis. Rather, the ultimate goal here is to provide the control design as a function of control requirements - a design that is so intrinsically based on comprehensive analytical results that the confidence in such a SCM design to meet all given requirements indeed can be upheld without further analysis by a prospective SCM user.

To achieve this goal, extensive analytical effort is a prerequisite. Based on the analytical results, useful design information can then be formulated into a SCM application handbook for the user. The following key activities are therefore comprised:

- (1) Analytically characterize the converter functional blocks that include (a) three most commonly-used power stages (buck, boost, and buck-boost), (b) the pulse modulation stage effecting various control laws, and (c) the multiple-loop SCM error processor linking the power stage and the pulse modulation.
- (2) Analyze converter performance characteristics based on models obtained for the aforementioned functional blocks. Since it is a common practice to perform the initial design of a non-linear system in terms of linear operations, each aforementioned functional block is linearized, and all linear blocks are then used jointly for evaluating system performances.



- (3) Extract both qualitative and quantitative relationships between SCM design parameters and required performance characteristics, formulate SCM design parameters and required performance characteristics, and formulate SCM design guidelines to meet a given set of performance requirements.

## CHAPTER 2

### STANDARDIZED CONTROL MODULE (SCM) FUNCTIONAL BLOCKS

Functionally speaking, a dc-dc regulated converter can be divided into two parts: a power circuit and a control circuit. By definition, the power circuit handles the energy transfer from the source to the load. Three most commonly used power circuits are the buck, the boost, and the buck-boost. A familiarity of these circuits on the part of the readers is assumed.

The control circuit manages the rate of the source-load energy transfer as a function of the load demands. During nominal steady-state and transient operations, the control objectives are associated with (A) the tracking of a certain controlled quantity in accordance with a given reference, and (B) the compliance to converter specifications such as the system response to step or sinusoidal line and load disturbances, and to external command signals. During transient operations, the control objective becomes electrical-stress limiting for all elements associated with the converter to provide effective protection against catastrophic/degradation types of failures. A control circuit thus serves the multiple functions of regulation, command, and protection.

This chapter presents a generalized SCM-controlled converter, through which the three aforementioned control functions can be described for the SCM. It should be emphasized at this juncture that the purpose of this report is not to conduct a detailed description of SCM; such a description has already been given in NASA CR-135072, published under a previous contract [3]. Instead, the SCM analysis and design are features of the current work. Therefore, the inclusion of the SCM description here is merely intended to enable this report to be somewhat self-contained for the benefit of those who have yet to read reference [3]. For details of the SCM implementation, reference [3] is strongly recommended.

A SCM-controlled dc-dc converter is shown in Figure 2.1. The power circuit, occupying the upper half of the block diagram, processes the transfer of energy from a raw input  $V_i$  to a regulated output  $V_o$ . Three basic power stages are shown here as buck, boost, and buck-boost. The control circuit regulates the rate of energy transfer. It receives an analog signal from the power-stage output, and delivers a discrete-time interval signal  $d$  to achieve

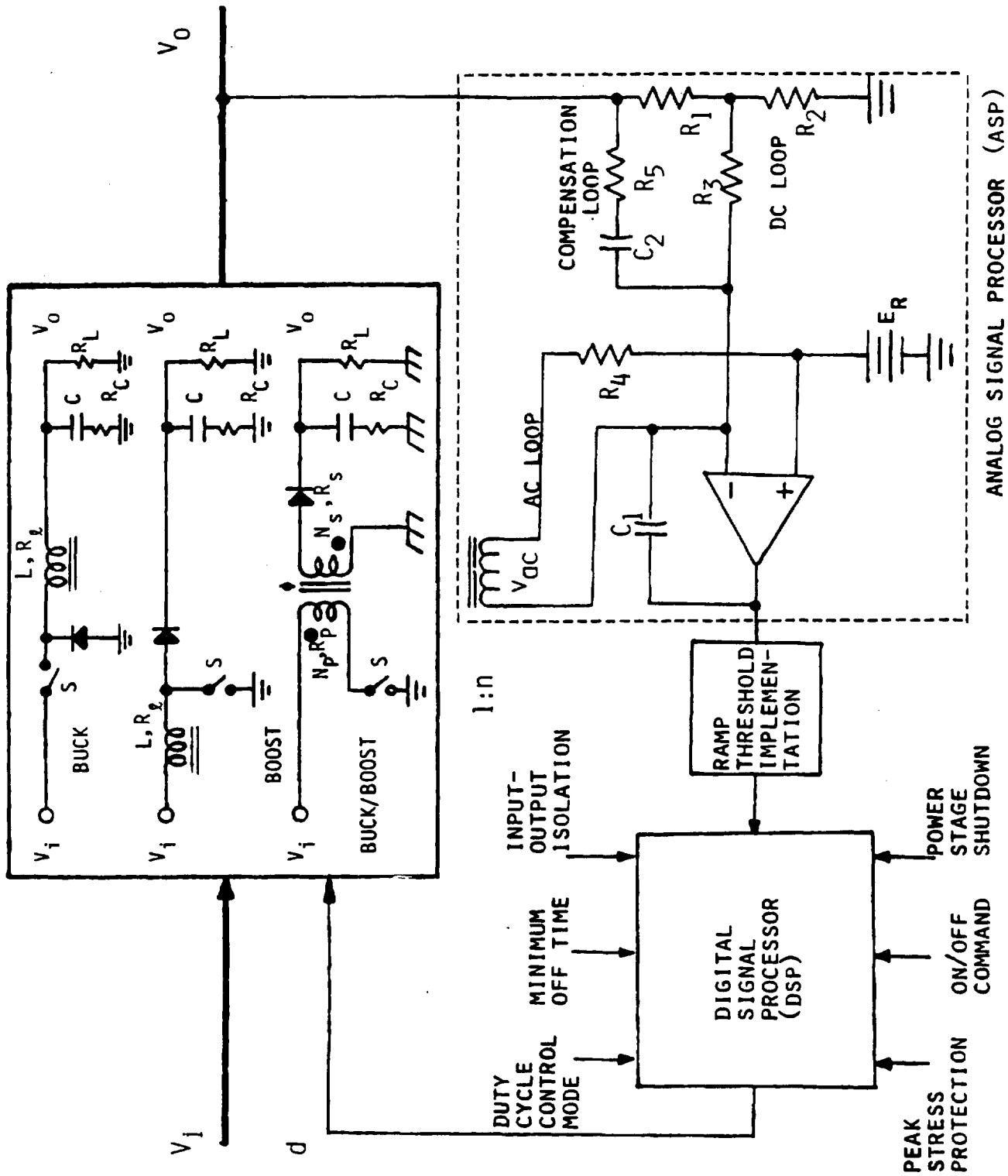


FIG. 2.1 SCM CONTROLLED SWITCHING REGULATORS

the required on-off control of the power switch within each power stage. The discrete-time voltage or current pulses generated in the power stage are averaged by an LC filter having a much longer time constant than the discrete-time pulse intervals. The averaged output therefore contains negligible switching-frequency components, and can be regarded as an analog signal containing only lower-frequency information.

The SCM, occupying the lower half of the block diagram, performs the control function within the converter. It contains an Analog Signal Processor (ASP) and a Digital Signal Processor (DSP). Implementations of both ASP and DSP are standardized; they combine to provide the required analog signal to discrete-time interval conversion. The key feature of the SCM is the utilization of an inherent ac switching-frequency signal within the power stage. This utilization is in addition to the conventional dc sensing of output  $V_o$ . The sensed ac signal and the dc error are processed by the ASP. As a result, an adaptive stability is obtained which is independent of the filter parameter changes. The SCM control function is completed by the DSP, which processes the control-signal output from the ASP in conjunction with a prescribed control law, and operates the on-off of the power switch via a duty-cycle signal  $d$ .

As stated previously, the control-circuit functions also include command and protection. The command function generally requires the converter to respond to an external signal capable of overriding control signal  $d$  in determining the on-off of the power switch. The protection function includes power-component peak-stress limiting and the converter shutdown in the event of a sensed abnormality such as overvoltage, undervoltage, or overcurrent beyond a predetermined, tolerable level and duration. These functions are performed within SCM by the DSP. Detailed ASP and DSP implementations have been presented in reference [3].

The three basic functional blocks of an SCM-controlled converter are shown in the block diagram of Figure 2.2. Analysis of these three blocks will be presented in Chapters 4, 5 and 6, following a general discussion of the basic analytic approach presented in Chapter 3.

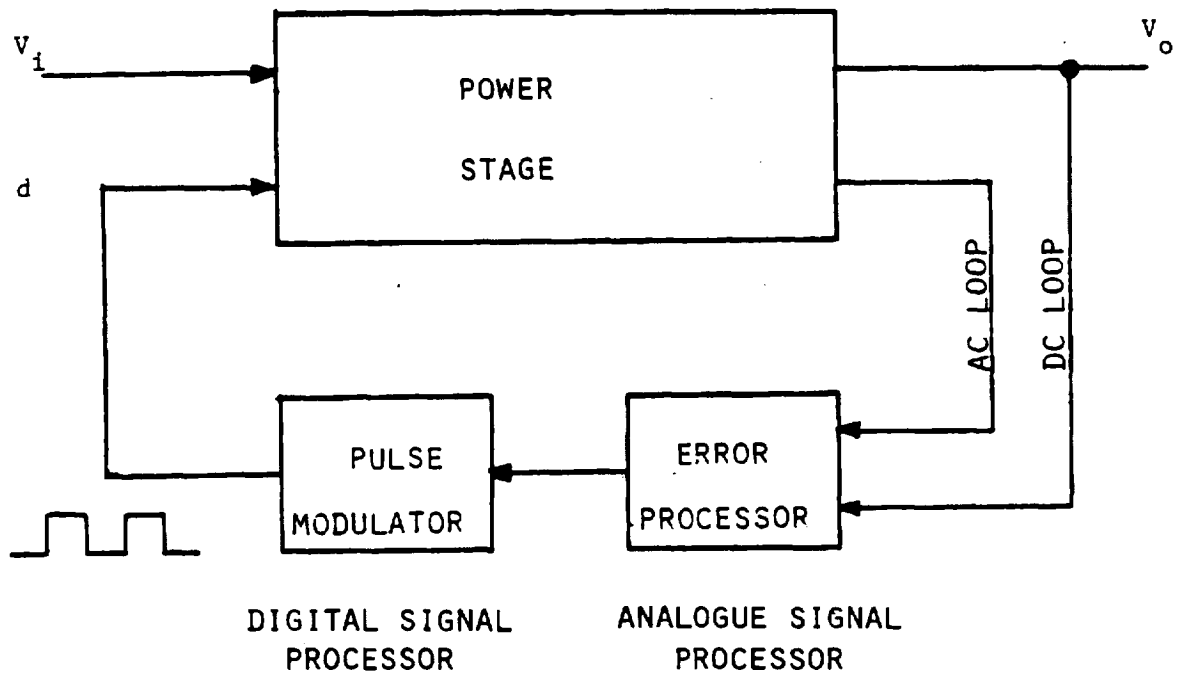


FIG. 2.2. SWITCHING REGULATOR BLOCK DIAGRAM

## CHAPTER 3

### SELECTION OF ANALYTICAL APPROACH

A dc-dc switching-regulated converter is an inherent nonlinear device containing multiple nonlinearities. The first major nonlinearity exists in the power stage, and is due to the operation of the power switch. Different circuit topologies correspond to the respective on and off time intervals in the switching cycle. The second major nonlinearity exists in the Digital Signal Processor (DSP). Harmonic frequencies, which are multiples of the input disturbance frequency, are contained in the DSP output. Because of such system nonlinearities, difficulties are encountered in reaching performance assessments of various system performances such as stability, attenuation of sinusoidal/step line disturbances, and response to sinusoidal/step load disturbances.

In the present chapter, these nonlinearities are elaborated, and various analytical approaches capable of treating these nonlinearities are discussed. In light of the stated objective of this program, which is the preparation of analytically-based and performance-oriented design guidelines, a specific approach is then selected as the basic analytical tool for the entire program.

#### 3.1 Power Stage Nonlinearity

Each of the power stages shown in Figure 2.1 can be divided as a function of the inductor MMF status in the output filter. In Figure 3.1(A), often referred to as "continuous-conduction" or Mode 1 of operation, the MMF ascends during on time  $T_{on}$  when the power switch is ON and the diode is OFF, and descends during  $T_{F1}$  when the diode is ON. Notice that the MMF never vanishes in the output inductor. In Figure 3.1(B), often referred to as "discontinuous-conduction" or Mode 2 of operation, the MMF ascends from zero MMF at the beginning of  $T_{on}$ , and descends during  $T_{F1}$ . An additional off time  $T_{F2}$  exists when both the power switch and the diode are OFF, during which the inductor MMF remains zero, and the load current is supplied entirely by the output-filter capacitor.

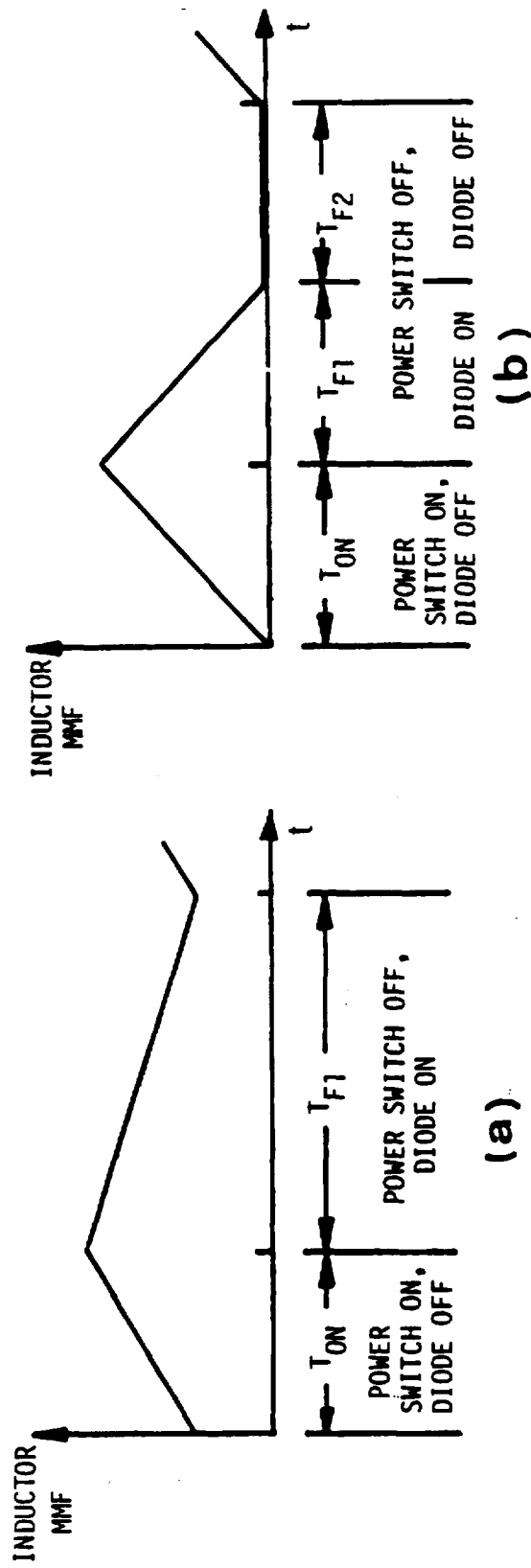


FIG. 3.1 INDUCTOR CURRENT WAVEFORMS (A) CONTINUOUS MMF OPERATION  
 (B) DISCONTINUOUS CURRENT OPERATION

Taking the continuous-conduction buck-boost converter for illustration, the circuit topologies corresponding to  $T_{on}$  and  $T_{F1}$  are shown in Figure 3.2. Even though the power stage is linear for each time interval, the combination of the two different linear circuits for the purpose of analyzing a complete switching cycle of operation composed of both  $T_{on}$  and  $T_{F1}$  becomes a nonlinear analysis problem. The difficulty here is how to integrate these different topologies and collectively evaluate their responses to various line/load disturbances having a much longer time period than individual  $T_{on}$  or  $T_{F1}$ .

The power stage nonlinearity caused by the input filter is also demonstrated in Figure 3.2. Being an integral part of the power stage during  $T_{on}$  in Figure 3.2(B), it withdraws its presence in Figure 3.2(C), thus severely increasing the nonlinearity of the power-stage, and causing major complications in the derivation of a linear power stage model for analysis and design purposes.

### 3.2 Digital Signal Processor Nonlinearity

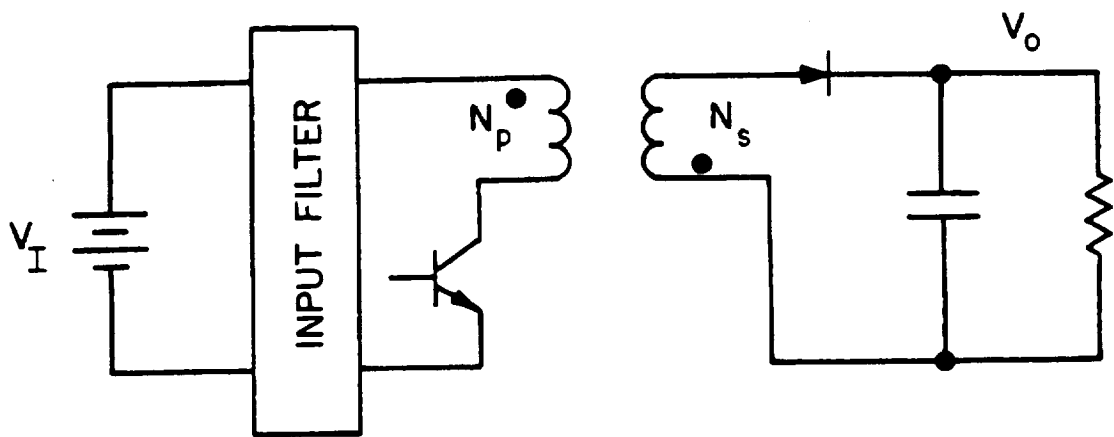
To characterize how a disturbance is propagated in the analog-signal-to-discrete-time conversion, one is interested in how the duty cycle  $d(t)$  of the power switch is being affected by a small disturbance in the processed error at the Analog Signal Processor (ASP) output. Obviously, if one seeks a complete analytical portrait of the propagation, such a disturbance, the analysis, using Fourier techniques, would have to include all harmonics of the disturbance frequency as well as the beat frequencies of the disturbance frequency and the regulator switching frequency. Thus a single-frequency input results in an multiple-frequency output, an inherent characteristic of nonlinear circuit operation.

### 3.3 Various Nonlinear Analysis Techniques

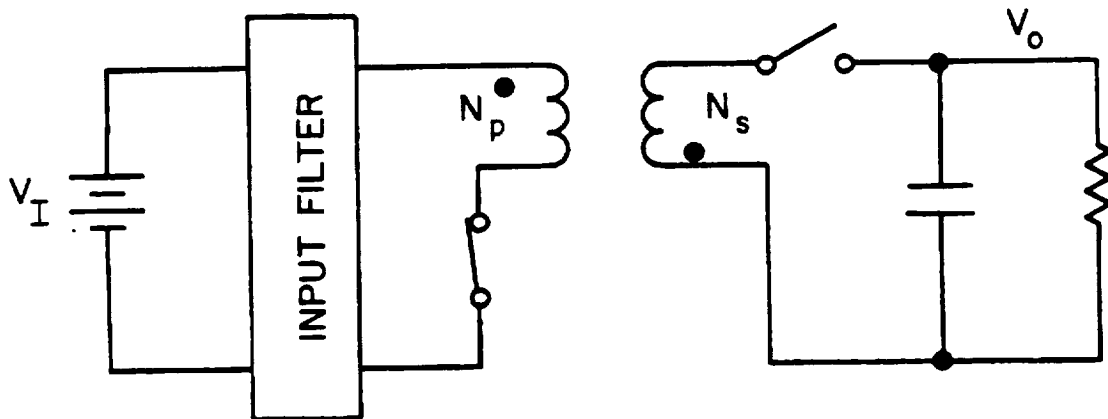
A common starting point for switching-regulator analysis is the identification of a state vector  $X$  and an input vector  $U$ . The  $(n \times 1)$  vector  $X$  contains all the system state variables, while the  $(n \times 1)$  vector  $U$  is associated with the regulator input voltage, the reference, etc. For continuous conduction the system representation is:

$$\begin{aligned} \dot{X} &= F1X + G1U && \text{during } T_{on} \\ \dot{X} &= F2X + G2U && \text{during } T_{F1} \end{aligned}$$

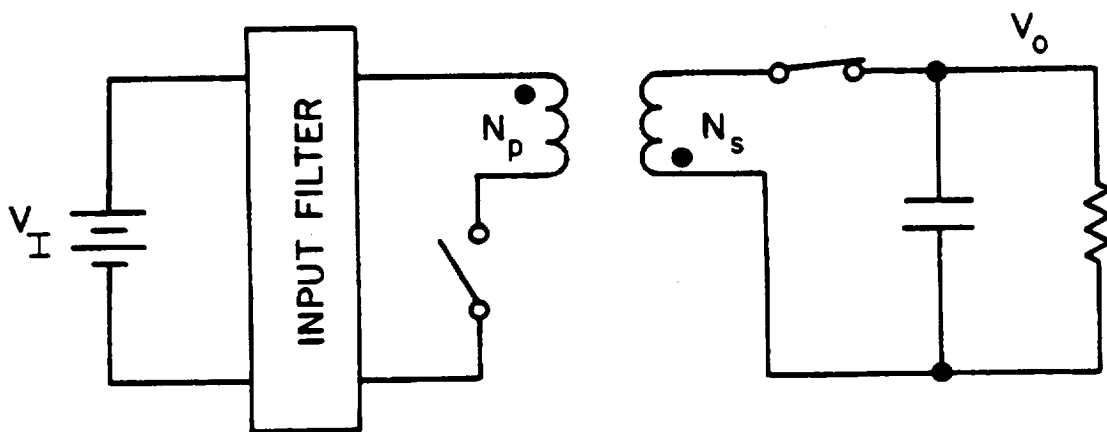




(A) Buck/Boost Converter.



(B) Buck/Boost Topology During  $T_{on}$ .



(C) Buck/Boost Topology During  $T_{F1}$ .

FIG. 3.2 BUCK/BOOST CONVERTER TOPOLOGY CHANGES DURING EACH SWITCHING INTERVAL.

The (nxn) matrices F1 and F2 and the (nxn) matrices G1 and G2 are constant matrices composed of various circuit and input parameters. In the case of discontinuous conduction, an additional equation

$$\dot{\underline{x}} = F3\underline{x} + G3U \quad \text{during } T_{F2}$$

is added to complete the system representation.

Starting from this common representation, various analysis techniques differ only by the means through which linearization of the nonlinear system is achieved. These techniques have been described in detail in the literature [4,5].

In the Discrete Time Domain Analysis, [6,7], the system equilibrium state is numerically evaluated and linearization about the equilibrium is achieved by analytically/numerically performing the partial differentiation of  $\partial f/\partial x$ , where function "f" relates X at time instant  $t_{k+1}$  to X at an early time instant  $t_k$  in the equilibrium state. By so doing, the linearization applies to a complete switching regulator as a single entity without separating it into functional blocks and attacking each block piece by piece. For most practical switching-regulator applications, a digital computer is indispensable in carrying out the detailed numerical analysis.

In the Discrete Time Domain Simulation, [8], no linearization is needed as the disturbance in the nonlinear system is allowed simply to propagate through the state-transition matrices corresponding to one switched interval until a specific threshold condition for that interval is reached, upon which the disturbance enters into the next switched interval recurringly. The process actually simulates the nonlinear-circuit response, thus depending entirely on digital or analog computers.

In the Average Time Domain Analysis [9,10], an averaged state-space representation for a complete switching period T is formulated by simply summing the

state-space representation of the individual switched interval  $T_i$  properly weighed by the corresponding time ratio  $T_i/T$ . Linearization is accomplished through straightforward perturbation of the averaged representation. A small-signal power-stage transfer function is thus obtained in the frequency domain. The transfer function of the ASP is readily derived using linear circuit analysis, as the ASP is strictly a linear device in small-signal operations. The nonlinear DSP is treated by the describing-function technique, [11,12]. The power stage, the ASP, and the DSP are treated as as three separate functional blocks, and the transfer function for each is derived to facilitate a complete regulator system analysis.

In the Discrete Time Impulse Response Analysis, [13, 14], each topology in Figure 3.2 is described by state-space equations. Through mathematical manipulation of the state transition matrices for each specific time interval, and matching up boundary conditions, a discrete time domain representation can be derived that characterizes the system exactly. This discrete system is subsequently linearized and approximated by a continuous impulse response if one is willing to neglect switching details and study the long range trends. The frequency domain transfer function can be derived simply by performing the Laplace transformation of the linear impulse response.

The discrete time domain modeling technique provides a uniform approach which covers both continuous and discontinuous inductor. The model derived from the discrete time domain technique is exact up to half of the switching frequency, unlike the average model which is only a low frequency approximation. The technique, however, becomes rather cumbersome, sometimes impossible, to obtain a closed-form solution as the order of the system increases beyond the second order. Consequently, the existence of an input filter will complicate the analysis considerably so that only numerical results rather than close-form solutions can be obtained.

### 3.4 Selection of the Average Time Domain Analysis for the SCM.

Although the discrete time domain analysis and/or simulation offer a higher degree of accuracy in describing the behavior of the control system, they are, basically, numerical approaches. Consequently, it is difficult to gain from the discrete-time approach any closed-form insight and to visualize control-performance-oriented design procedures. Although the discrete impulse response model of the power stage offers high accuracy and closed-form representation, the method is sophisticated and obtaining a closed-form solution becomes rather cumbersome when the order of the system increases beyond the second order. The method is therefore somewhat impractical for generation of design guidelines. Since the objective of this program is the preparation of analytically-based and performance-oriented design guidelines, the average time domain analysis approach is seen as a more suitable engineering tool to fulfill the stated objective. In conjunction with the fact that the skill of comprehending and performing the frequency domain analysis resides in most engineers while the same cannot be said for the time domain analysis, the average time domain (continuous frequency domain) analysis is selected as the basic analytical tool for this program.

In essence, the averaging technique provides a means of deriving an equivalent linear circuit model, with all the RLC elements modified by the appropriate duty cycle. The discrete nature of the system is therefore lost in the averaging process. The approach is plausible due to the fact that a low-pass filter generally exists at a converter output for ripple attenuation. As a result, the small-signal behaviors of practical concern are usually confined to a frequency range considerably lower than the switching frequency. The circuit configurations to be analyzed are presented in Chapter 4. The analysis will start in Chapter 5, with power stage transfer-function derivations.

## CHAPTER 4

### SCM-CONTROLLED DC-DC SWITCHING REGULATED CONVERTERS

Three most commonly used power-stage configurations, the buck, the boost, and the buck-boost, are shown in Figure 2.1. Each can be controlled by an identical SCM shown in the lower half of Figure 2.1.

Each of the three power stages converts an input voltage  $V_i$  to an output voltage  $V_o$ . When power switch  $S$  conducts during on time  $T_{on}$ , energy is stored in inductor  $L$ , which has a series winding resistance  $R_e$ . The conducting switch  $S$  causes diode  $D$  to be back biased, and load current in  $R_L$  is contributed by output capacitor  $C$ , partially for the buck converter and entirely for the boost and buck-boost converters. Capacitor  $C$  has an equivalent series resistance  $R_c$ . When on time  $T_{on}$  is completed, off time  $T_{F1}$  is initiated, and continuity of current in  $L$  is maintained by a current through  $D$ , which supplies load  $R_L$  and replenishes the charge in  $C$ . Neglecting all dissipative voltage drops associated with  $L$  and  $C$ , equal flux excursions in  $L$  during  $T_{on}$  and  $T_{F1}$  for "continuous-conduction" operations dictate that

$$V_o = V_i / (1 + T_{F1}/T_{on}) \quad \text{buck} \quad (4-1)$$

$$V_o = V_i (1 + T_{on}/T_{F1}) \quad \text{boost} \quad (4-2)$$

$$V_o = V_i (T_{on}/T_{F1}) (N_s/N_p) \quad \text{buck-boost} \quad (4-3)$$

Thus, by controlling the time ratio  $T_{on}/T_{F1}$ , a constant  $V_o$  can be maintained for a varying  $V_i$  for as long as

$$\begin{array}{ll} V_o < V_i & \text{buck} \\ V_o > V_i & \text{boost} \\ V_o \geq V_i & \text{buck-boost} \end{array}$$

As stated in Chapter 2, the SCM is composed of an ASP and a DSP. The central element of the ASP is an integrator-amplifier with a feedback

capacitor C1, as shown in Figure 2.1. It processes the following three signals:

- The dc output voltage  $v_o$  through a voltage divider R1-R2 and the dc loop resistance R3.
- The ac voltage  $v_{ac}$  across a winding on filter inductor L, through the ac loop resistance R4.
- The rate of change of  $v_o$ , i.e.,  $dv_o/dt$ , through capacitor C2 and resistance R5.

Let  $g = R_2/(R_1 + R_2)$  be the divider ratio of the dc loop, the voltage  $gv_o$  is then compared with reference  $E_R$ . The difference  $v_{dc} = gv_o - E_R$  becomes the dc error input to the integrator amplifier. The dc output level  $V_T$  of the integrator amplifier is determined by  $v_{dc}$ . Concurrently, an ac voltage,  $v_{ac}$ , is differentially fed to the amplifier. Both  $v_{dc}$  and  $v_{ac}$  are integrated; the triangular integrator output is superimposed on the amplified dc error to intersect a fixed threshold level  $E_T$ , which actuates the DSP to control the duty cycle of power switch S. To improve the transient response, capacitor C2 and resistor R5 are added to sense  $dv_o/dt$ . Any transient change in  $v_o$  will cause a current in C2-R5, which is processed by the integrator amplifier to cause a corresponding change in the duty cycle in the direction of restoring  $v_o$  to its nominal state.

The leading edge of the digital pulse output from the threshold detector is used to actuate the DSP. The DSP is composed of IC oscillators, time delays, and memories [3]. Depending on how the DSP is mechanized, the duty-cycle control can be achieved through a variety of combinations of  $T_{on}$  and  $T_{F1}$ , which include: (1) constant ( $T_{on} + T_{F1}$ ), variable  $T_{on}$  and  $T_{F1}$ , (2) constant  $T_{F1}$ , variable  $T_{on}$ , (3) Constant  $V_i T_{on}$  (or constant  $T_{on}$ ), variable  $T_{F1}$ . Any of these DSP mechanizations is capable of providing a regulated  $V_o$  per equations (4-1) to (4-3) for the respective power stages.

The following features should become apparent from the foregoing description.

- Since there always exists, within any switching regulator configuration, an inherent ac waveform suitable for ac-loop processing within the ASP, the SCM implementation shown in Figure 2.1 can be readily applied to achieve the desired analog-to-discrete-

time conversion for all types of switching regulators.

- All possible duty-cycle control laws are within the ready implementation of the DSP.

The circuit shown in Figure 2.1 thus exhibits a commonality in accommodating various power circuits as well as control laws. It therefore serves as the basic configuration for all analytical effort to be pursued in this program. The analysis starts in Chapter 5, with the derivation of transfer functions for all three power stages.

## CHAPTER 5

### POWER STAGE TRANSFER FUNCTIONS AND BLOCK DIAGRAMS

Having adopted the average time domain analysis, the power-stage functional block is now analyzed for each of the three power stages shown in Figure 2.1. The analysis will be carried out in the "continuous-conduction" operation, as this is the prevalent operating mode for most dc-dc converters. The discontinuous-conduction operation will occur at light load, but it is seldom used as the intended design at full load since it leads to a higher semiconductor peak current and a poorer form factor for all the power-component currents. Consequently, the SCM design guidelines will be formulated for the continuous-conduction operation only. The effect of the discontinuous-conduction operation on the control system will be treated in Chapter 15. However, no design guidelines have been contemplated.

The continuous-conduction power stage receives two small-signal inputs: the input voltage  $v_I$  and the duty cycle  $d$ . To derive the power-stage transfer function, one must formulate output  $v_O$  in relation to these two quantities. The formulation can be achieved in the following sequences:

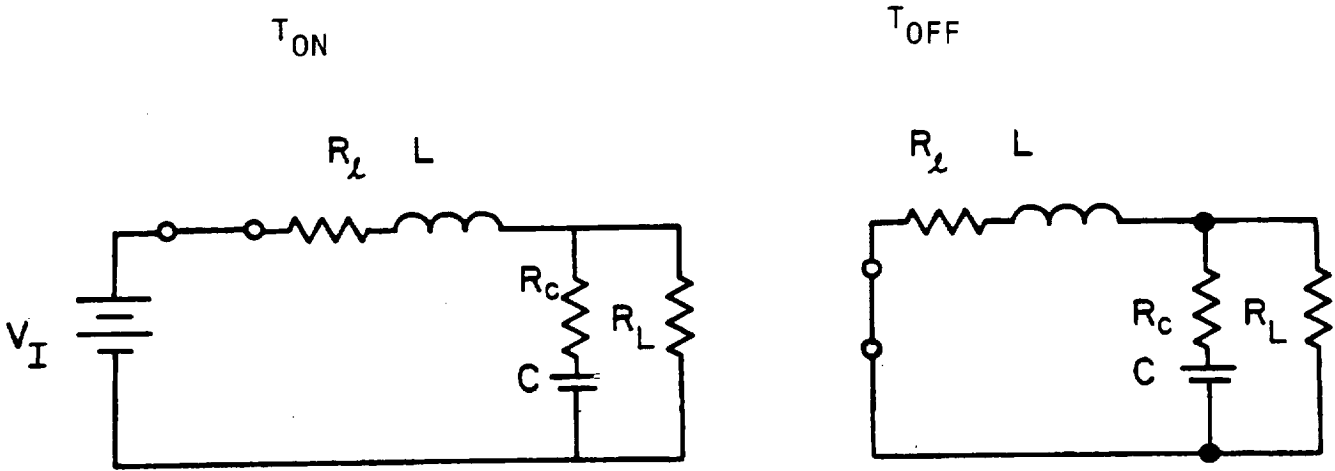
- (1) Matrix formulation for power stages during  $T_{on}$  and  $T_{F1}$ .
- (2) State-space averaging and perturbation.
- (3) Linearization and System Behaviors.
- (4) Transfer function and block diagram derivations.

To enhance commonality, the three different power stages in Figure 2.1 will be treated concurrently.

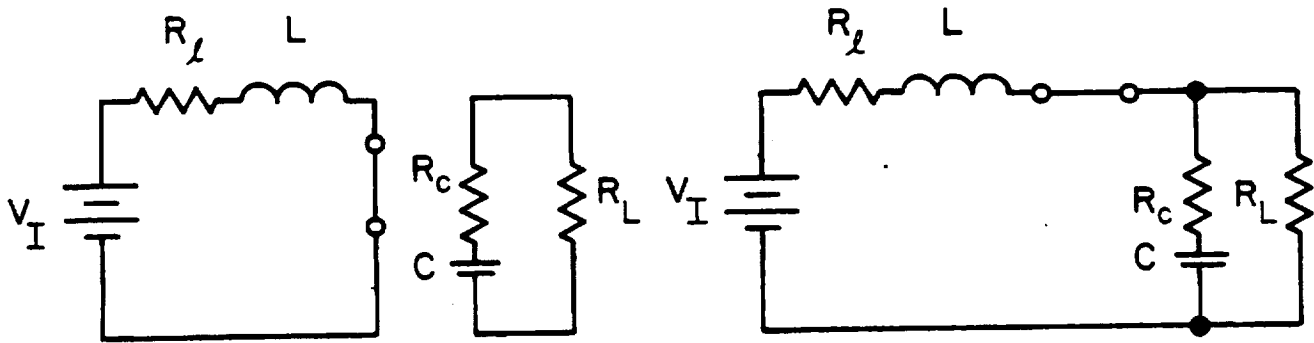
#### 5.1 Matrix Formulation For Power Stages During On Time and Off Time.

During  $T_{on}$  and  $T_{F1}$ , three power stages shown in Figure 2.1 can be represented in Figures 5.1(A) to (C), respectively. State variables are chosen as follows:

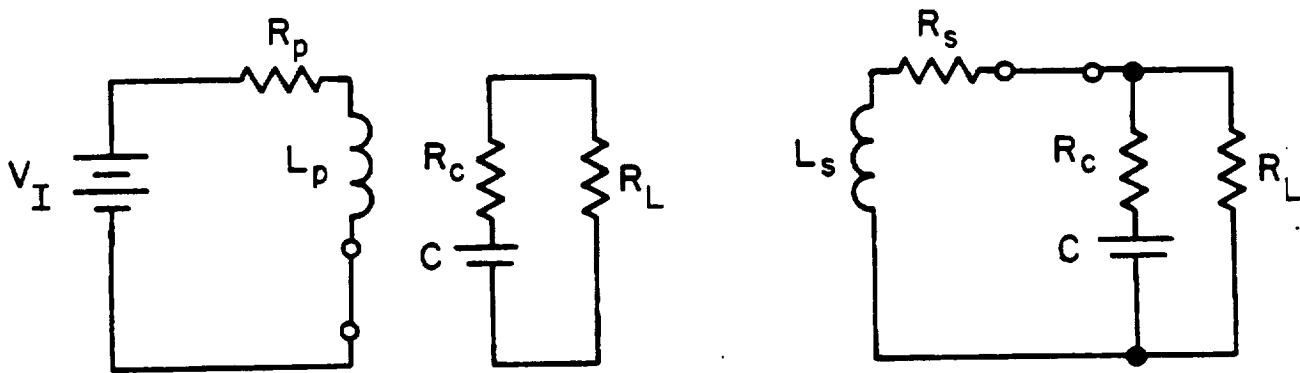




(A) BUCK



(B) BOOST



(C) BUCK/BOOST

FIG. 5.1 CONVERTER TOPOLOGY VARIATIONS DURING  $T_{ON}$  AND  $T_{OFF}$

$$\text{Buck} \quad \underline{x}^T = [i_L, v_C] \quad (5-1)$$

$$\text{Boost} \quad \underline{x}^T = [i_L, v_C] \quad (5-2)$$

$$\text{Buck-boost} \quad \underline{x}^T = [\phi, v_C] \quad (5-3)$$

Where  $i_L$  is the inductor current, and  $v_C$  is the capacitor voltage in Figure 5.1. Flux  $\phi$  is chosen as the state variable for the buck-boost converter in place of the inductor current, as the flux is continuous with time whereas the current is not in this converter. The complete behavior of each power stage can be described by the following two sets of equations:

For  $T_{on}$  Interval:

$$\dot{\underline{x}} = A_1 \underline{x} + b_1 v_I \quad (5-4)$$

$$v_O = C_1^T \underline{x}$$

For  $T_{F1}$  Interval:

$$\dot{\underline{x}} = A_2 \underline{x} + b_2 v_I$$

$$v_O = C_2^T \underline{x} \quad (5-5)$$

Here,  $A_1$ ,  $b_1$ ,  $C_1^T$ ,  $A_2$ ,  $b_2$ , and  $C_2^T$  are constant matrices composed of circuit parameters. It is proved that if the assumption  $R_L \gg R_C + R_2$  is made, the following matrices are obtained:

For buck power stage:

$$A_1 = \begin{bmatrix} -\frac{1}{L} (R_\ell + R_C) & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR_L} \end{bmatrix}, \quad A_2 = \begin{bmatrix} -\frac{1}{L} (R_\ell + R_C) & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR_L} \end{bmatrix} \quad (5-6)$$

$$b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \quad b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$c_1^T = \begin{bmatrix} R_C & 1 \end{bmatrix}, \quad c_2^T = \begin{bmatrix} R_C & 1 \end{bmatrix}$$

For boost power stage:

$$A_1 = \begin{bmatrix} -\frac{R_2}{L} & 0 \\ 0 & -\frac{1}{CR_L} \end{bmatrix}, \quad A_2 = \begin{bmatrix} -\frac{R_\ell + R_C}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR_L} \end{bmatrix} \quad (5-7)$$

$$b_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \quad b_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$c_1^T = \begin{bmatrix} 0 & 1 \end{bmatrix}, \quad c_2^T = \begin{bmatrix} R_C & 1 \end{bmatrix}$$

For buck-boost stage:

$$A_1 = \begin{bmatrix} -\frac{R_p}{L_p} & 0 \\ 0 & \frac{-1}{CR_L} \end{bmatrix}, \quad A_2 = \begin{bmatrix} -\frac{R_s + R_C}{L_s} & -\frac{1}{N_s} \\ \frac{N_s}{L_s C} & -\frac{1}{CR_L} \end{bmatrix} \quad (5-8)$$

$$b_1 = \begin{bmatrix} \frac{1}{N_p} \\ 0 \end{bmatrix}, \quad b_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$c_1^T = \begin{bmatrix} 0 & 1 \end{bmatrix}, \quad c_2^T = \begin{bmatrix} \frac{N_s R_C}{L_s} & 1 \end{bmatrix}$$

## 5.2 State-Space Averaging and Perturbation

Averaging over a single period ( $dT + d'T$ ) where  $d = T_{\text{on}}/T$ ,  $T = T_{\text{on}} + T_{\text{F1}}$ , and  $d' = 1 - d$ , equations (5-4) and (5-5) are combined to give:

$$\begin{aligned}\dot{\underline{x}} &= [dA_1 + d'A_2] \underline{x} + [db_1 + d'b_2] v_I \\ v_0 &= [dC_1^T + d'C_2^T] \underline{x}\end{aligned}\tag{5-9}$$

Or,

$$\begin{aligned}\dot{\underline{x}} &= A\underline{x} + b v_I \\ v_0 &= C^T \underline{x}\end{aligned}\tag{5-10}$$

Substituting eqs. (5-6), (5-7), and (5-8) into (5-9) and (5-10), one can obtain:

For buck power stage:

$$A = [dA_1 + d'A_2] = \begin{bmatrix} -\frac{R_L + R_C}{L} & -\frac{1}{L} \\ \frac{1}{c} & -\frac{1}{CR_L} \end{bmatrix}$$

$$b = [db_1 + d'b_2] = \begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix}$$

(5-11)

$$c^T = [dC_1^T + d'C_2^T] = [R_C \quad 1]$$

For boost power stage:

$$A = \begin{bmatrix} -\frac{R_L + d'R_C}{L} & -\frac{d'}{L} \\ \frac{d'}{c} & -\frac{1}{CR_L} \end{bmatrix}$$

$$b = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

(5-12)

$$c^T = [d'R_C \quad 1]$$

For buck-boost power stage:

$$\begin{aligned}
 A &= \begin{bmatrix} -\frac{R_s + d'R_c}{L_s} & -\frac{d'}{N_s} \\ \frac{d'N_s}{L_s C} & -\frac{1}{R_L C} \end{bmatrix} \quad \text{assuming } \frac{R_p}{L_p} = \frac{R_s}{L_s} \\
 b &= \begin{bmatrix} \frac{d}{N_p} \\ 0 \end{bmatrix} \\
 c^T &= \begin{bmatrix} \frac{d'N_s R_c}{L_s} & 1 \end{bmatrix}
 \end{aligned} \tag{5-13}$$

In the derivation of (5-13), a simplifying assumption  $R_p/L_p = R_s/L_s$  has been made.

The state-space averaging has combined the different circuit topologies corresponding to  $T_{on}$  and  $T_{F1}$  into equivalent time-varying systems which are presented in equations (5-11) to (5-13). Each of these systems can be linearized using perturbation techniques, by introducing the line variation  $\hat{v}_i$  and the duty-cycle variation  $\hat{d}$  in the following forms:

$$\begin{aligned}
 v_i &= V_I + \hat{v}_i \\
 d &= D + \hat{d} \\
 d' &= D' - \hat{d}
 \end{aligned} \tag{5-14}$$

where  $V_I$  is the dc line input voltage,  $D$  is the steady-state duty cycle corresponding to  $V_I$  for a given  $V_O$ , and  $D'$  is equal to  $(1-D)$ . Such perturbations cause the state vector  $\underline{x}$  and output voltage  $v_O$  to be similarly perturbed:

$$\underline{x} = \underline{x} + \hat{\underline{x}} \quad (5-15)$$

$$v_0 = V_0 + \hat{v}_0 \quad (5-16)$$

Substituting (5-14) and (5-15) into the first part of (5-10), and knowing  $\dot{\underline{x}} = 0$ , one obtains:

$$\hat{\underline{x}} = (A \underline{x} + b V_I) + (A \hat{\underline{x}} + b \hat{v}_i) + [(A_1 - A_2) \underline{x} + (b_1 - b_2)V_I] \hat{d}$$

(steady-state) (line variation) (duty-cycle variation)

$$+ [(A_1 - A_2) \hat{\underline{x}} + (b_1 - b_2) \hat{v}_i] \hat{d}$$

(nonlinear term) (5-17)

Substituting (5-15) and (5-16) into (5-10), one obtains

$$\hat{v}_0 = c^T \hat{\underline{x}} + [c_1^T - c_2^T] \underline{x} \hat{d} + [c_1^T - c_2^T] \hat{\underline{x}} \hat{d} \quad (5-18)$$

(line) (duty-cycle) (nonlinear)

It can be seen from (5-17) and (5-18) that the perturbed state-space description and output voltage are nonlinear due to the presence of the products of time-dependent quantities  $\hat{\underline{x}}$  and  $\hat{d}$  as well as  $\hat{v}_i$  and  $\hat{d}$ .

### 5.3 Linearization and System Behaviors

Assuming that under small-signal perturbation the departure of each state from its corresponding steady-state value is small in relation to the steady-state value itself, namely:

$$\frac{\hat{v}_i}{V_I} \ll 1, \quad \frac{\hat{d}}{D} \ll 1, \quad \frac{\hat{x}_1}{x_1} \ll 1, \quad \frac{\hat{x}_2}{x_2} \ll 1$$

where  $\underline{x} = (x_1, x_2)$  and  $\hat{\underline{x}} = (\hat{x}_1, \hat{x}_2)$ .

Then, the second-order nonlinear term in eqs. (5-17) and (5-18) becomes negligible, and a linear system emerges. Separating steady-state (dc) and

small-signal (ac) portions of the linearized system, the following results are obtained:

Steady-state:

$$\begin{aligned}\underline{x} &= -A^{-1} b v_I \\ v_O &= C^T \underline{x} = -C^T A^{-1} b v_I\end{aligned}\tag{5-19}$$

Small-signal:

$$\begin{aligned}\dot{\hat{x}} &= A\hat{x} + b\hat{v}_i + [(A_1 - A_2) \underline{x} + (b_1 - b_2) v_I] \hat{d} \\ \hat{v}_O &= C^T \hat{x} + (C_1^T - C_2^T) \underline{x} \hat{d}\end{aligned}\tag{5-20}$$

Equations (5-19) and (5-20) are foundations for defining the following system behaviors:

(1) Input to Output Disturbance Attenuation, with  $\hat{d} = 0$

From (5-20) with  $\hat{d} = 0$ ,

$$\begin{aligned}\dot{\hat{x}} &= A\hat{x} + b\hat{v}_i \\ \hat{v}_O &= C^T \hat{x} \\ \frac{\hat{x}(s)}{\hat{v}_i(s)} &= (sI - A)^{-1} b\end{aligned}\tag{5-21}$$

$$\frac{\hat{v}_O(s)}{\hat{v}_i(s)} = C^T (sI - A)^{-1} b\tag{5-22}$$



## 2. Duty cycle to Output Disturbance Attenuation, with $\hat{v}_i = 0$

From (5-20) with  $\hat{v}_i = 0$ ,

$$\dot{\underline{\hat{x}}} = A \underline{\hat{x}} + [(A_1 - A_2) \underline{x} + (b_1 - b_2) V_I] \hat{d}$$

$$\underline{\hat{v}}_o = C^T \underline{\hat{x}} + (C_1^T - C_2^T) \underline{x} \hat{d}$$

$$\frac{\underline{\hat{x}}(s)}{\underline{\hat{d}}(s)} = (sI - A)^{-1} [(A_1 - A_2) \underline{x} + (b_1 - b_2) V_I] \quad (5-23)$$

$$\frac{\underline{\hat{v}}_o(s)}{\underline{\hat{d}}(s)} = C^T (sI - A)^{-1} [(A_1 - A_2) \underline{x} + (b_1 - b_2) V_I] + (C_1^T - C_2^T) \underline{x} \quad (5-24)$$

Here, I is the unity matrix. Equations (5-21) through (5-24) are general, and can be used for deriving transfer functions in terms of circuit parameters for each power stage.

### 5.4 Transfer Function Derivations

The Transfer Functions to be derived include the following:

- Steady state dc input-to-output voltage,  $V_o/V_I$
- Voltage ratio  $\hat{v}_o/\hat{v}_i$
- Output voltage to duty cycle ratio  $\hat{v}_o/\hat{d}$

#### 5.4.1 Derivation of dc Steady-state Ratio of Output to Input Voltage

From eq. (5-19),

$$\frac{V_o}{V_I} = -C^T A^{-1} b \quad (5-25)$$

Substituting (5-11), (5-12) and (5-13) to (5-25), and assuming that the load  $R_L$  is much greater than any of the winding resistance or the ESR, one obtains:

For buck power stage:

$$\frac{V_0}{V_I} = -[R_C \ 1] \begin{bmatrix} R_\ell + R_C & -\frac{1}{L} \\ -\frac{1}{L} & -\frac{1}{CR_L} \end{bmatrix}^{-1} \begin{bmatrix} D \\ L \\ 0 \end{bmatrix} \approx D \quad (5-26)$$

For boost power stage:

$$\frac{V_0}{V_I} = -[dR_C \ 1] \begin{bmatrix} R_\ell + D'R_C & -\frac{D'}{L} \\ \frac{D'}{c} & -\frac{1}{CR_L} \end{bmatrix}^{-1} \begin{bmatrix} 1 \\ L \\ 0 \end{bmatrix} \approx \frac{1}{D'} \quad (5-27)$$

For buck-boost power stage

$$\frac{V_0}{V_I} = \begin{bmatrix} \frac{N_s R_C D'}{L_s} & 1 \end{bmatrix} \begin{bmatrix} R_s + D'R_C & -\frac{D'}{N_s} \\ \frac{D'N_s}{L_s C} & -\frac{1}{R_L C} \end{bmatrix}^{-1} \begin{bmatrix} D \\ N_p \\ 0 \end{bmatrix} = \frac{N_s}{N_p} \frac{D}{D'} \quad (5-28)$$

#### 5.4.2. Derivation of Small-Signal Ratio of Output to Input Voltage

Let ratio  $\hat{v}_o(s)/\hat{v}_i(s)$  be designated as  $F_{oi}(s)$ , then from eq. (5-22),

$$F_{oi}(s) = \frac{\hat{v}_o(s)}{\hat{v}_i(s)} = C^T (sI - A)^{-1} b \quad (5-29)$$

By substituting (5-11), (5-12), and (5-13) to (5-29), and assuming that load  $R_L$  is much greater than any winding resistance or the capacitor ESR, one has:

For buck power stage:

$$F_{oi}(s) = \begin{bmatrix} R_c & 1 \end{bmatrix} \begin{bmatrix} s + \frac{R_l + R_c}{L} & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{1}{CR_L} \end{bmatrix}^{-1} \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix}$$

$$= \frac{D}{L_e C} \frac{1 + SR_c C}{s^2 + s\left(\frac{1}{CR_L} + \frac{R_e + R_{ce}}{L_e}\right) + \frac{1}{L_e C}} \quad (5-30)$$

The quantities  $L_e$ ,  $R_e$ , and  $R_{ce}$  are defined later.

For boost power stage:

$$F_{oi}(s) = \begin{bmatrix} D'R_c & 1 \end{bmatrix} \begin{bmatrix} s + \frac{R_l + D'R_c}{L} & \frac{D'}{L} \\ -\frac{D'}{C} & s + \frac{1}{CR_L} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

$$= \left(\frac{1}{D'}\right) \frac{1}{L_e C} \frac{1 + SR_c C}{s^2 + s\left(\frac{1}{CR_L} + \frac{R_e + R_{ce}}{L_e}\right) + \frac{1}{L_e C}} \quad (5-31)$$

In deriving (5-31), the assumption  $1 \gg (R_e + R_{ce})/R_L$  is made.

For buck-boost power stage:

$$F_{oi}(s) = \begin{bmatrix} \frac{N_s R_C D'}{L_s} & 1 \end{bmatrix} \begin{bmatrix} s + \frac{R_s + D'R_C}{L_s} & \frac{D'}{N_s} \\ -\frac{D'N_s}{L_s C} & s + \frac{1}{R_L C} \end{bmatrix}^{-1} \begin{bmatrix} \frac{D}{N_p} \\ 0 \end{bmatrix}$$

$$= \left( \frac{D}{D'} \frac{N_s}{N_p} \right) \frac{1}{L_e C} \frac{1 + SCR_C}{s^2 + s \left( \frac{1}{CR_L} + \frac{R_e + R_{ce}}{L_e} \right) + \frac{1}{L_e C}} \quad (5-32)$$

In deriving (5-32), the same assumption used in deriving (5-31) is made. Notice that except for  $D$ ,  $1/D'$ , and  $(D/D')(N_s/N_p)$  in the right-hand side of (5-30), (5-31), and (5-32), the remainder of the equations are identical.

This common term is:

$$F_p(s) = \frac{1}{L_e C} \frac{1 + SR_C}{s^2 + s \left( \frac{1}{CR_L} + \frac{R_e + R_{ce}}{L_e} \right) + \frac{1}{L_e C}} \quad (5-33)$$

The quantities  $R_e$ ,  $L_e$ , and  $R_{ce}$  are defined by the equations:

$$\begin{aligned} R_e &= R_l \\ L_e &= L \\ R_{ce} &= R_c \end{aligned} \quad \text{for buck power stage} \quad (5-34)$$

$$\begin{aligned} R_e &= R_l / (D')^2 \\ L_e &= L / (D')^2 \\ R_{ce} &= R_c / D' \end{aligned} \quad \text{for boost power stage} \quad (5-35)$$

$$\begin{aligned}
 R_e &= R_s / (D')^2 && \text{for buck-boost power stage} \\
 L_e &= L_s / (D')^2 && (5-36) \\
 R_{ce} &= R_c / D'
 \end{aligned}$$

Having defined  $F_p(s)$  completely, eqs. (5-30), (5-31), and (5-32) can be simplified to read:

$$F_{oi}(s) = \frac{\hat{v}_o(s)}{\hat{v}_i(s)} = F_I(s) F_p(s) \quad (5-37)$$

where  $F_I(s) = \begin{cases} D & \text{for buck power stage (5-38)} \end{cases}$

$\begin{cases} 1/D' & \text{for boost power stage (5-39)} \end{cases}$

$\begin{cases} \frac{D}{D'} \frac{N_s}{N_p} & \text{for buck-boost power stage (5-40)} \end{cases}$

### 5.4.3 Derivation of Small-Signal Ratio of Output Voltage to Duty Cycle

Let ratio  $\hat{v}_o(s)/\hat{d}(s)$  be designated as  $F_{od}(s)$ , then from eq. (5-24),

$$F_{od}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = c^T (sI-A)^{-1} \left[ (A_1-A_2) \underline{x} + (b_1-b_2) v_I \right] + (c_1^T - c_2^T) \underline{x} \quad (5-42)$$

Attention is now focused on expressing  $\underline{x}$  and  $v_I$  as functions of  $v_o$ . The relation of  $v_I$  to  $v_o$  has been derived in eqs. (5-26) to (5-28) for all three power stages. The relation of  $\underline{x}$  to  $v_o$  is given in (5-19) which states:

$$\underline{x} = -A^{-1} b v_I$$

$$v_o = c^T \underline{x} = -c^T A^{-1} b v_I$$

Substituting eqs. (5-11) to (5-13) and eqs. (5-26) to (5-28) into the above equation, and assuming that  $R_L \gg R_L + R_C$ , one has:

$$\underline{x} = \begin{bmatrix} \frac{1}{R_L} \\ 1 \end{bmatrix} v_o \quad \text{for buck power stage} \quad (5-43)$$

$$\underline{x} = \begin{bmatrix} \frac{1}{D^2 R_L} \\ 1 \end{bmatrix} v_o \quad \text{for boost power stage} \quad (5-44)$$

$$\underline{x} = \begin{bmatrix} D'L_e \\ N_s R_L \\ 1 \end{bmatrix} V_0 \quad \text{for buck-boost power stage} \quad (5-45)$$

Substituting into (5-42) the matrices for  $\underline{x}$  given in (5-43), (5-44), and (5-45) and the values of  $V_1$  as derived in eqs. (5-26) to (5-28), and using the matrices of  $C^T$ ,  $sI-A$ ,  $A_1$ ,  $A_2$ ,  $b_1$ ,  $b_2$ ,  $C_1^T$ , and  $C_2^T$ , known previously, one can obtain:

$$F_{od}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = F_D(s) F_p(s) \quad (5-46)$$

where

$$F_D(s) = \begin{cases} \frac{v_0}{D} & \text{for buck power stage} & (5-47) \\ \frac{v_0}{D'} \left(1 - s \frac{L_e + R_{eq}}{R_L}\right) & \text{for boost power stage} & (5-48) \\ \approx \frac{v_0}{D'} \left(1 - s \frac{L_e}{R_L}\right) & & \\ \frac{v_0}{DD'} \left(1 + sD \frac{L_e + R_{eq}}{R_L}\right) & \text{for buck-boost power stage} & (5-49) \\ \approx \frac{v_0}{DD'} \left(1 - s \frac{DL_e}{R_L}\right) & & \end{cases}$$

The existence of a "positive-zero" term in the form of  $(1-sK)$  is evident from (5-48) and (5-49) for boost and buck-boost power stages [10, 11]. In deriving (5-48) and (5-49), the inequality  $R_L \gg R_{eq}$  has been assumed. The term  $R_{eq}$  is defined in equation (5-53).

Having derived the power stage dual-input describing functions,  $F_{O1}(s)$  of eq. (5-37) and  $F_{Od}(s)$  of (5-46), the power-stage block diagram is readily conceived as that of Figure 5.2. Here,  $F_I(s)$  is given in eqs. (5-38), (5-39), and (5-40), for the buck, boost, and buck-boost power stage, respectively. Likewise, the corresponding  $F_D(s)$  can be found in eqs. (5-47), (5-48), and (5-49). Circuit parameters shown in  $F_p(s)$  are illustrated in Figure 2.1 and further defined in eqs. (5-34), (5-35), and (5-36).

It is often desirable to visualize  $F_p(s)$  in the form of an equivalent circuit. The following definitions are made:

$$\omega_o^2 = \frac{1}{L_e C} \quad (5-50)$$

$$2\tau = \frac{1}{\omega_o} \left( \frac{1}{CR_L} + \frac{R_e + R_{ce}}{L_e} \right) \quad (5-51a)$$

Expanding (5-51a) and using (5-50) we have:

$$\begin{aligned} 2\tau &= \frac{1}{\omega_o} \left( \frac{L_e}{(L_e C)R_L} + \frac{C(R_e + R_{ce})}{L_e C} \right) \\ &= \frac{1}{\omega_o} \left( \frac{\omega_o^2 L_e}{R_L} + \omega_o^2 C(R_e + R_{ce}) \right) \\ &= \frac{\omega_o L_e}{R_L} + \omega_o C(R_e + R_{ce}) \end{aligned}$$

The term in parenthesis can be modified to read

$$(R_e + R_{ce}) = (R_e + R_{ce} - R_c + R_c) = (R_{eq} + R_c)$$

where  $R_{eq} = R_e + R_{ce} - R_c$ . Thus:

$$2\tau = \frac{\omega_o L_e}{R_L} + \omega_o C(R_{eq} + R_c) \quad (5-51b)$$



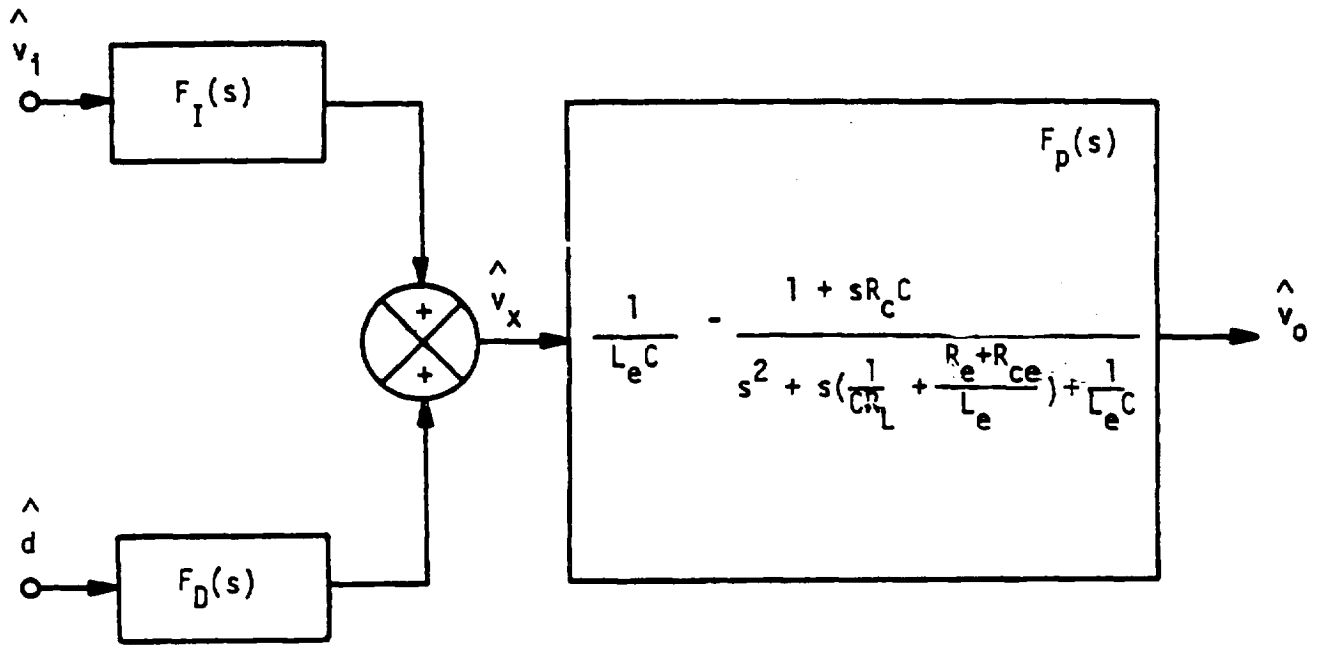


FIG. 5.2 TRANSFER FUNCTION BLOCK DIAGRAM

Using (5-50) and (5-51a) in (5-33), the expression for  $F_p(s)$ ,

$$F_p(s) = \frac{1 + sR_c C}{\frac{2}{\left(\frac{s}{\omega_o}\right)^2 + 2\zeta\left(\frac{s}{\omega_o}\right) + 1}} \quad (5-52)$$

The damping terms in  $2\zeta$ , namely  $\frac{L_e}{R_L}$  and  $C(R_{eq} + R_c)$ , can be seen in the equivalent circuit representation for  $F_p(s)$  in figure 5.3, where, using expressions for  $R_{ce}$  from (5-34), (5-35), and (5-36) in  $R_{eq}$ , we have:

$$R_{eq} = \begin{cases} R_e & \text{for buck} \\ R_e + R_c \frac{D}{D'} & \text{for boost and buck/boost} \end{cases} \quad (5-53)$$

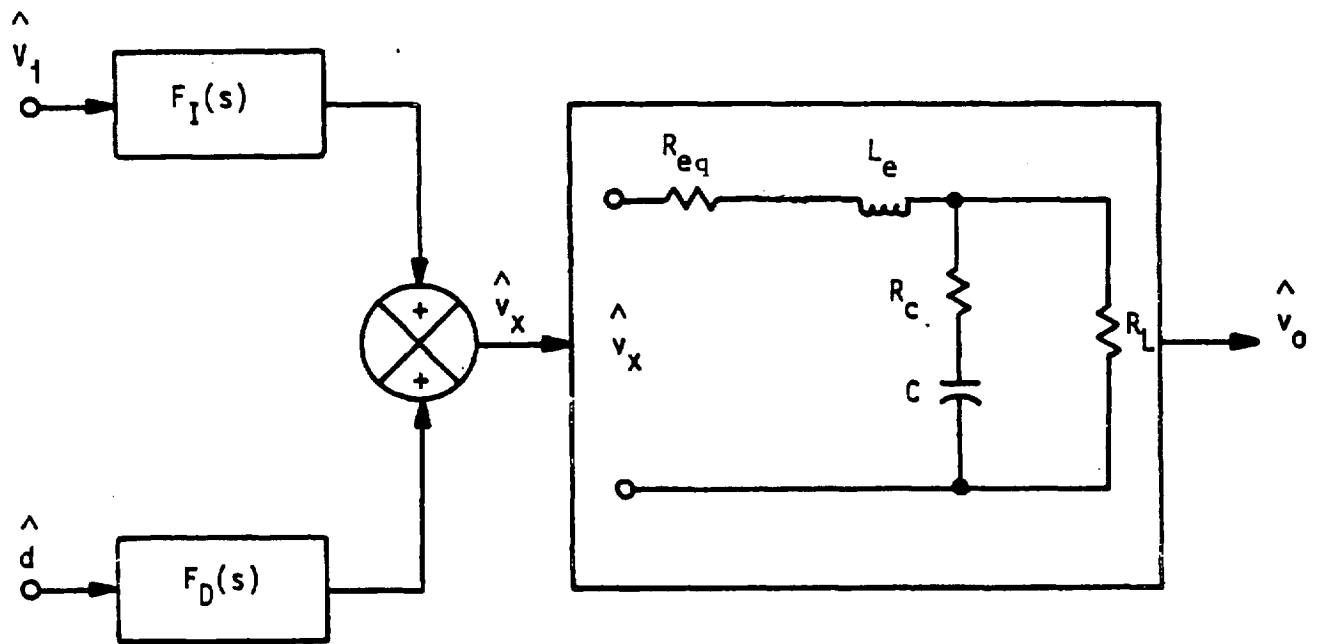


FIG. 5.3 EQUIVALENT CIRCUIT BLOCK DIAGRAM

## CHAPTER 6

### ANALOG SIGNAL PROCESSOR TRANSFER FUNCTIONS AND BLOCK DIAGRAMS

The Analog Signal Processor (ASP) isolated from Figure 2.1, is illustrated in Figure 6.1. The ASP processes multiple input control signals derived from the power stage, and delivers its analog output to the Digital Signal Processor to effect the required analog-signal-to-discrete-time conversion. From a small-signal viewpoint, the ASP is essentially a linear network, with a common configuration for all three power stages. Three signals processed by the ASP are converter output-voltage  $v_0$ , rate of change  $dv_0/dt$ , and voltage  $v_{AC}$  across the sensed winding associated with the power inductor.

The loop sensing  $v_0$  is the same as any conventional dc loop. The sensed  $v_0$  is processed by an amplifier with reference  $E_R$  to generate an amplified dc error, which then contributes to the control of the dc level of output voltage  $V_0$ . The loop sensing  $dv_0/dt$  serves to shape the frequency response in such a way as to improve the regulator system dynamic response. The loop sensing  $v_{AC}$  across the inductor fulfills two functions. The first function is to couple the large-signal switching voltage across the inductor to the integrating amplifier. The large voltage signal is integrated to form a triangular output. The triangular output is superimposed on the amplified dc error to form the integrator output voltage  $V_T$ . The triangular ramp in  $V_T$ , working in unison with a fixed threshold level in the DSP and a control law prescribed by the DSP to be discussed later, effects the required duty cycle control. The second function of sensing the inductor-voltage is to derive the lower-frequency small-signal disturbance across the inductor, thus providing additional loop compensation. This particular compensation is responsible for many favorable performances exhibited by SCM-controlled switching regulators. The adaptive stability, a fundamental feature of the SCM, is made possible by this compensation.

This chapter discusses the small-signal behavior of the ASP. The only objective is to obtain the transfer function and the block-diagram representation of the ASP. No attempt is made here to reveal the virtues of the ASP such as its adaptive nature. The ASP features will become clear in

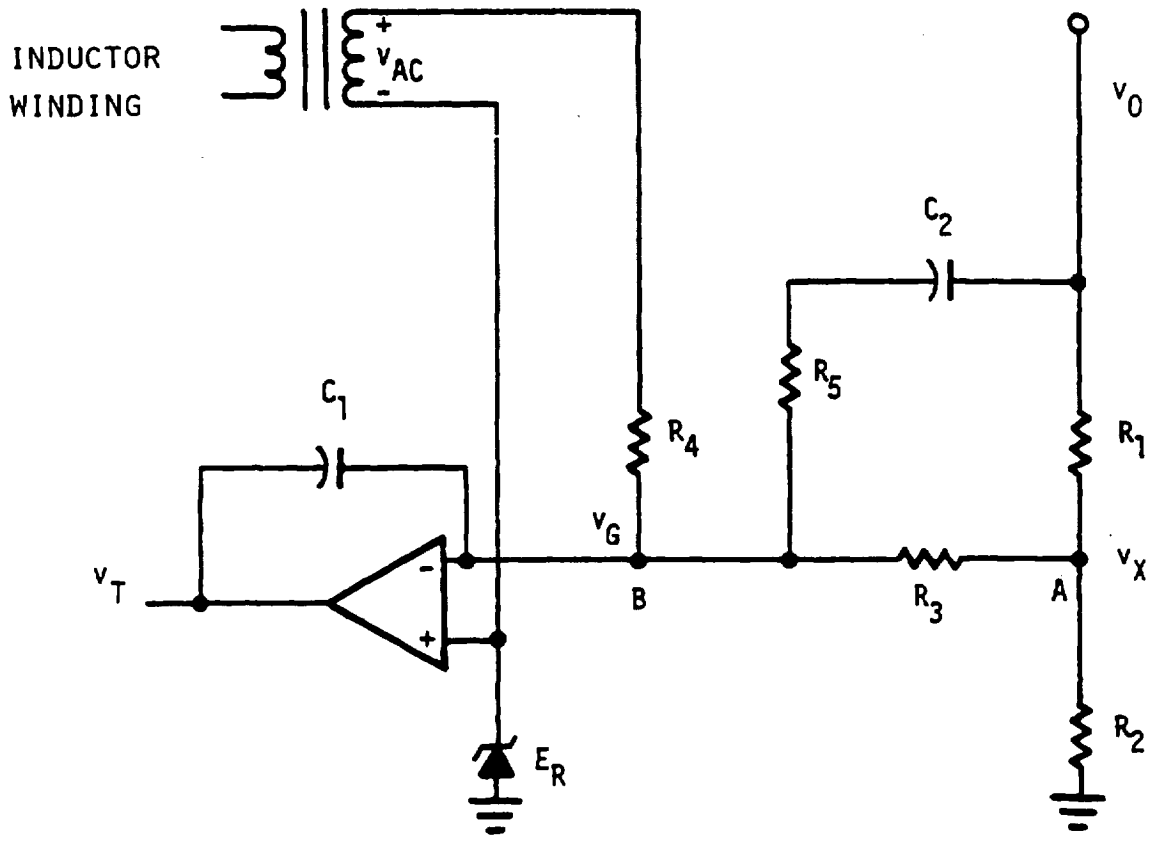


FIG. 6.1 ANALOG SIGNAL PROCESSOR SCHEMATIC

later chapters concerning SCM-controlled regulator performances.

### 6.1 ASP Transfer Function In Terms of $\hat{V}_o$ and $\hat{V}_{ac}$

In performing the small-signal analysis of the network shown in Figure 6.1, reference  $E_R$  is replaced by a short circuit. Applying Kirchhoff's law at node A,

$$\frac{\hat{V}_x}{R_2} + \frac{\hat{V}_x - \hat{V}_o}{R_1} + \frac{\hat{V}_x - \hat{V}_g}{R_3} = 0 \quad (6-1)$$

where  $\hat{V}_x$  is the voltage across  $R_2$  as shown, and  $\hat{V}_g$  is the differential voltage across the amplifier input. At node B, the following equation applies:

$$\frac{\hat{V}_g - \hat{V}_x}{R_3} + \frac{\hat{V}_g - \hat{V}_o}{R_5 + \frac{1}{sC_2}} + \frac{\hat{V}_g - \hat{V}_t}{\frac{1}{sC_1}} + \frac{\hat{V}_g - \hat{V}_{ac}}{R_4} = 0 \quad (6-2)$$

The open-loop response of the amplifier is  $A(s)$ , i.e.,

$$\hat{V}_t = -A(s) \hat{V}_g \quad (6-3)$$

Eliminating  $\hat{V}_x$  and  $\hat{V}_g$  in eqs. (6-1) to (6-3), one has

$$\hat{V}_t = \frac{\left(\frac{g}{R_x + R_3} + \frac{1}{Z_c}\right) \hat{V}_o + \frac{1}{R_4} \hat{V}_{ac}}{\frac{1}{A(s)} \left(\frac{1}{R_x + R_3} + \frac{1}{R_4} + \frac{1}{Z_c} + sC_1\right) + sC_1} \quad (6-4)$$

where

$$R_x = \frac{R_1 R_2}{R_1 + R_2} \quad (6-5)$$

$$Z_c = R_5 + \frac{1}{sC_2} \quad (6-6)$$

$$g = \frac{R_2}{R_1 + R_2} \quad (6-7)$$

Equation (6-4) can be reduced to:

$$\hat{V}_t(s) = -F_{DC}(s) \hat{V}_o(s) - F_{AC}(s) \hat{V}_{ac}(s) \quad (6-8)$$

where

$$F_{DC} = \frac{\frac{g}{R_x + R_3} + \frac{1}{Z_c}}{\frac{1}{A(s)} \left( \frac{1}{R_x + R_3} + \frac{1}{R_4} + \frac{1}{Z_c} + sC_1 \right) + sC_1} \quad (6-9)$$

$$F_{AC} = \frac{\frac{1}{R_4}}{\frac{1}{A(s)} \left( \frac{1}{R_x + R_3} + \frac{1}{R_4} + \frac{1}{Z_c} + sC_1 \right) + sC_1} \quad (6-10)$$

The foregoing analysis holds for all three power stages, as the term  $v_{ac}$  represents ac signal across the inductor, without regarding an inductor for any specific power stage.

## 6.2 Derivation of $\hat{v}_{ac}$ as a Function of $\hat{V}_o$ and $d$

The fact that  $v_{AC}$  is derived from the inductor of a given power stage suggests that the small-signal contents of  $v_{AC}$  will be different for different power stages. Using the equation

$$\hat{v}_{ac}(t) = N_3 \frac{d\hat{\phi}}{dt} \quad (6-11)$$

as a common starting point where  $N_3$  is the sensing turns and  $d\hat{\phi}/dt$  is the rate of change of induction-flux, the task at hand is to express  $\hat{v}_{ac}(s)$  as functions of other known control signals for each power stage. Since the power stage has been linearized through state-space averaging, equation (6-11) can be expressed as:

$$\hat{v}_{ac}(s) = N_3 s \hat{\phi}(s) \quad (6-12)$$

where,

$$\begin{aligned} \hat{\phi}(s) &= \frac{L \hat{i}_L(s)}{N} && \text{for buck} \\ &= \frac{L \hat{i}_L(s)}{N} && \text{for boost} \\ &= \hat{\phi}(s) && \text{for buck/boost} \end{aligned} \quad (6-13)$$



In (6-13), flux  $\hat{\phi}(s)$  is related to inductor current  $\hat{i}_L(s)$  through inductance  $L$  and main-winding turns  $N$ .

It is recalled that  $i_L$  for buck and boost power stages and  $\phi$  for buck-boost power stage were chosen as state variables in Chapter 5. The state-variable vector  $\hat{x}$  is related to input voltage  $\hat{v}_i$  and duty cycle  $\hat{d}$  by the equations:

$$\frac{\hat{\phi}(s)}{\hat{v}_i(s)} = (SI-A)^{-1}b \quad (\text{where } \hat{d} = 0) \quad (\text{Repeat of 5-21})$$

$$\frac{\hat{x}(s)}{\hat{d}(s)} = (SI-A)^{-1} [(A_1 - A_2)\underline{x} + (b_1 - b_2)V_I] \quad (\text{where } \hat{v}_i = 0) \quad (\text{Repeat of 5-23}).$$

Substituting into these equations the known matrices  $A$ ,  $b$ ,  $A_1$ ,  $A_2$ ,  $b_1$ , and  $b_2$ , one has:

For buck power stage:

$$\frac{\hat{x}(s)}{\hat{v}_i(s)} = \frac{\frac{D}{LeC}}{\Delta} \begin{bmatrix} sC + \frac{1}{R_L} \\ 1 \end{bmatrix} \quad (6-14)$$

$$\frac{\hat{x}(s)}{\hat{d}(s)} = \frac{\frac{1}{LeC} \frac{V_0}{D}}{\Delta} \begin{bmatrix} sC + \frac{1}{R_L} \\ 1 \end{bmatrix} \quad (6-15)$$

For boost power stage:

$$\frac{\hat{x}(s)}{\hat{v}_i(s)} = \frac{\frac{1}{(D')^2} \frac{1}{L_e C}}{\Delta} \left[ sC + \frac{1}{R_L} \right] \quad (6-16)$$

$$\frac{\hat{x}(s)}{\hat{d}(s)} = \frac{V_o \frac{1}{L_e C} \frac{1}{D'^2}}{\Delta} \left[ sC + \frac{2}{R_L} \right] \left[ D - \frac{D'}{R_L} (sL_e + R_{eq} + R_c) \right] \quad (6-17)$$

For buck-boost power stage:

$$\frac{\hat{x}(s)}{\hat{v}_i(s)} = \frac{\frac{D}{N_p}}{\Delta} \left[ \begin{array}{c} s + \frac{1}{R_L C} \\ \frac{N_s}{D' L_e C} \end{array} \right] \quad (6-18)$$

$$\frac{\hat{x}(s)}{\hat{d}(s)} = \frac{V_o}{\Delta} \left[ \begin{array}{c} \frac{1}{DN_s} \left( s + \frac{1}{R_L C} \right) + \frac{1}{R_L N_s C} \\ \frac{1}{DD' L_e C} - \left( s + \frac{R_{eq} + R_c}{L_e} \right) \left( \frac{1}{D' R_L C} \right) \end{array} \right] \quad (6-19)$$

where  $\Delta$  in equations (6-14 through (6-19) is given by the expression:

$$\Delta = s^2 + s \left( \frac{1}{CR_L} + \frac{R_{eq} + R_c}{L_e} \right) + \frac{1}{L_e C} \quad (6-20)$$

From state variables defined in eqs. (5-1), (5-2), and (5-3), one obtains readily the following:

For buck power stage:

$$\frac{\hat{i}_L(s)}{\hat{v}_i(s)} = \frac{1}{\Delta} \frac{1}{L_e C} \frac{D}{R_L} (1 + sCR_L)$$

(6-21)

$$\frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{1}{\Delta} \frac{1}{L_e C} \frac{V_0}{DR_L} (1 + sCR_L)$$

(6-22)

For boost power stage:

$$\frac{\hat{i}_L(s)}{\hat{v}_i(s)} = \frac{1}{\Delta} \frac{1}{L_e C} \frac{1}{(D')^2 R_L} (1 + sCR_L)$$

(6-23)

$$\frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{1}{\Delta} \frac{1}{L_e C} \frac{V_0}{(D')^2 R_L} (2 + sCR_L)$$

(6-24)

For buck-boost power stage:

$$\frac{\hat{\phi}(s)}{\hat{v}_i(s)} = \frac{1}{\Delta} \frac{D}{N_p} \left( s + \frac{1}{R_L C} \right) \quad (6-25)$$

$$\frac{\hat{\phi}(s)}{\hat{d}(s)} = \frac{1}{\Delta} \frac{V_0}{DN_s} \left( s + \frac{1+D}{R_L C} \right) \quad (6-26)$$

From eqs. (6-21) to (6-26), the composite expressions of  $\hat{i}_L$  and  $\hat{\phi}$  become the following:

For buck power stage:

$$\begin{aligned}\hat{i}_L(s) &= \frac{1}{\Delta} \frac{1}{L_e C} \frac{D}{R_L} (1 + sCR_L) \hat{v}_i(s) \\ &+ \frac{1}{\Delta} \frac{1}{L_e C} \frac{V_o}{DR_L} (1 + sCR_L) \hat{d}(s)\end{aligned}\tag{6-27}$$

For boost power stage:

$$\begin{aligned}\hat{i}_L(s) &= \frac{1}{\Delta} \frac{1}{L_e C} \frac{1}{(D')^2 R_L} (1 + sCR_L) \hat{v}_i(s) \\ &+ \frac{1}{\Delta} \frac{1}{L_e C} \frac{V_o}{(D')^2 R_L} (2 + sCR_L) \hat{d}(s)\end{aligned}\tag{6-28}$$

For buck-boost power stage:

$$\begin{aligned}\hat{\phi}(s) &= \frac{D}{N_P} \frac{\left(s + \frac{1}{R_L C}\right)}{\Delta} \hat{v}_i(s) \\ &+ \frac{V_o}{DN_s} \frac{\left(s + \frac{1+D}{R_L C}\right)}{\Delta} \hat{d}(s)\end{aligned}\tag{6-29}$$

The term  $v_i(s)$  on the right-hand side of equations (6-27) through (6-29) may now be replaced by expressions involving  $\hat{v}_o(s)$  and  $\hat{d}(s)$  for each of the three power stages. Equations (5-37) and (5-46) are combined to yield the composite expression

$$\hat{v}_o(s) = F_I(s) F_p(s) \hat{v}_i(s) + F_D(s) F_p(s) \hat{d}(s)$$

which may be solved for  $v_i(s)$  to yield

$$\hat{v}_i(s) = \frac{\hat{v}_o(s)}{F_I(s) F_p(s)} - \frac{F_D(s) \hat{d}(s)}{F_I(s)} \quad (6-30)$$

Equation (6-30) is general, and holds for all three power stages. Substituting equation (6-30) successively into equations (6-27), (6-28), and (6-29), and using the expressions for  $F_I(s)$ ,  $F_p(s)$ , and  $F_D(s)$  found in chapter 5, equations relating the terms  $\hat{i}_l(s)$  and  $\hat{\phi}(s)$  to  $\hat{v}_o(s)$  and  $\hat{d}(s)$  for each of the three power stages may be obtained. These equations are:

For buck power stage:

$$\hat{i}_l(s) = \frac{1}{R_L} \frac{1 + sCR_L}{1 + sCR_C} \hat{v}_o(s) \quad (6-31)$$

For boost power stage:

$$\hat{i}_l(s) = \frac{1 + sCR_L}{D' R_L (1 + sCR_C)} \hat{v}_o(s) + \frac{V_0}{(D')^2 R_L} \hat{d}(s) \quad (6-32)$$

For buck-boost power stage:

$$\hat{\phi}(s) = \frac{L_s}{N_s} \frac{1 + sCR_L}{D'R_L(1 + sCR_C)} \hat{v}_o(s) + \frac{L_s}{N_s} \frac{V_o}{(D')^2 R_L} \hat{d}(s) \quad (6-33)$$

Substituting (6-31), (6-32), and (6-33) into (6-12) and (6-13),

$$\hat{v}_{ac}(s) = F_3(s) \left[ F_1(s) \hat{d}(s) + F_2(s) \hat{v}_o(s) \right] \quad (6-34)$$

where:

For buck power stage:

$$F_1(s) = 0$$

$$F_2(s) = \frac{1}{R_L} \frac{1 + sCR_L}{1 + sCR_C}$$

$$F_3(s) = snL$$

$$n = \frac{N_3}{N}$$

(6-35)

For boost power stage:

$$F_1(s) = \frac{V_o}{(D')^2 R_L}$$

$$F_2(s) = \frac{1 + sCR_L}{D'R_L(1 + sCR_C)}$$

$$F_3(s) = snL$$

$$n = \frac{N_3}{N}$$

(6-36)

For buck-boost stage:

$$F_1(s) = \frac{V_0}{(D')^2 R_L}$$

$$F_2(s) = \frac{1 + sCR_L}{D'R_L (1 + sCR_C)}$$

$$F_3(s) = snL_s$$

$$n = \frac{N_3}{N_s}$$

(6-37)

### 6.3 ASP Transfer Function and Block Diagram

Equations (6-8) and (6-34) completely define the transfer function of the ASP. An equivalent block diagram is readily shown to be that of Figure 6.2, where  $F_{DC}$ ,  $F_{AC}$ ,  $F_1$ ,  $F_2$ , and  $F_3$  are given in eqs. (6-9), (6-10), (6-35), (6-36), and (6-37), respectively. Functions  $F_{DC}$  and  $F_{AC}$  are identical for three different power stages, whereas  $F_1$ ,  $F_2$ , and  $F_3$  are somewhat different for each power stage.



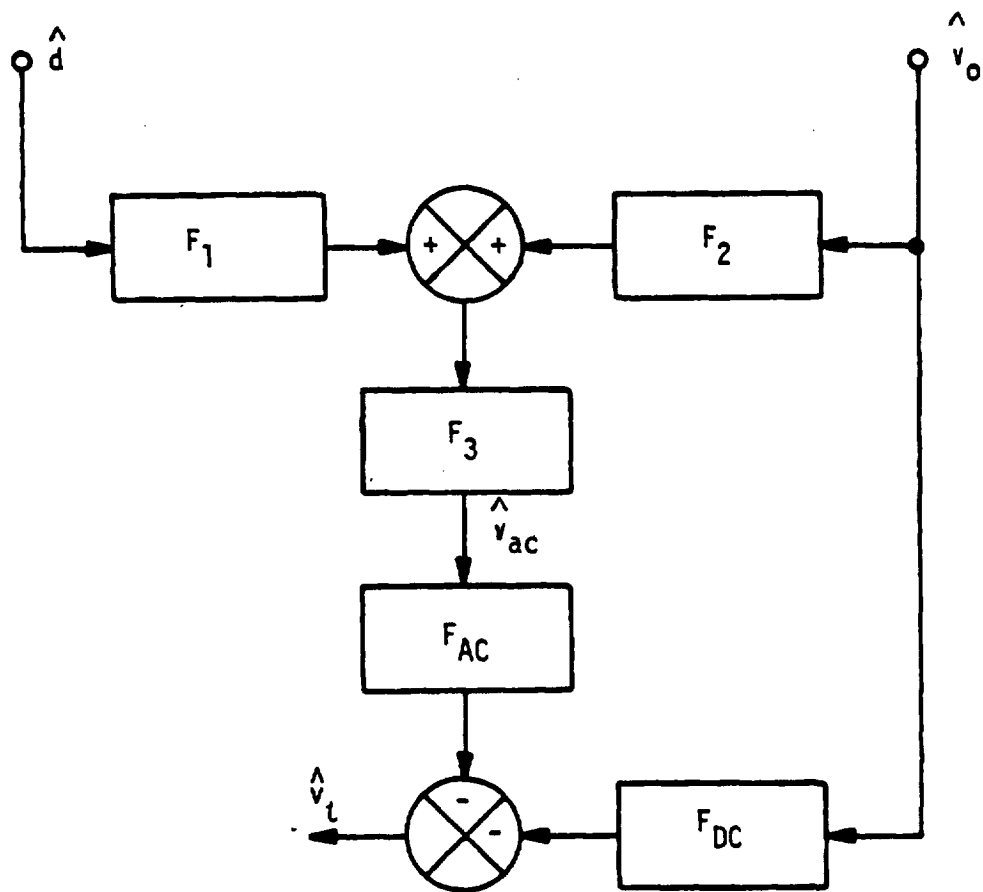


FIG. 6.2 SMALL SIGNAL MODEL FOR THE ASP.

## CHAPTER 7

### DIGITAL SIGNAL PROCESSOR DESCRIBING FUNCTION AND BLOCK DIAGRAM

The Digital Signal Processor (DSP) converts the output voltage  $v_T$  of the ASP into discrete-time pulses to control the on-off of the power switch. Voltage  $v_T$ , which contains the amplified dc error and the triangular ramp, is made to intersect a fixed threshold level. A digital signal is issued at the DSP output when the intersection occurs. This signal initiates a switching event for the power switch. The duration of the switching event and its repetition rate are prescribed by a control law implemented in the DSP.

The present chapter is devoted to the derivation of the DSP describing functions for a variety of control laws. The control laws can be implemented with either one of the following:

- Constant on time regardless of converter input voltage  $v_I$ .
- Constant on time for a given converter input voltage  $v_I$ , with  $v_I T_{on}$  being kept constant.
- Constant off time.
- Constant on time plus off time, i.e., constant frequency.

For reasons discussed in detail in Reference [3], the last two control laws are preferred by the SCM due to their more effective peak-stress limiting and source EMI control. Being the more commonly used approach, the constant-frequency DSP will serve as an illustrative example for the describing-function derivation. Derived results for other control laws will also be summarized.

#### 7.1 Definition of Pulse Modulator Stage

In a typical two-loop control system, as illustrated in Fig. 7.1 for the buck regulator, a dc loop is employed to sense the output voltage of the converter to achieve a proper dc regulation, and an ac loop is used to sense the switching waveform across the output filter inductor to provide a triangular ramp  $v_T$  at the integrator amplifier output. This ramp, when working in unison with the externally generated threshold level, produces the necessary mechanism to effect the regulator duty-cycle control. Using the constant frequency duty cycle control shown as an example in Fig. 7.2, the clock initiates the on-time and the intersection of the integrator out-

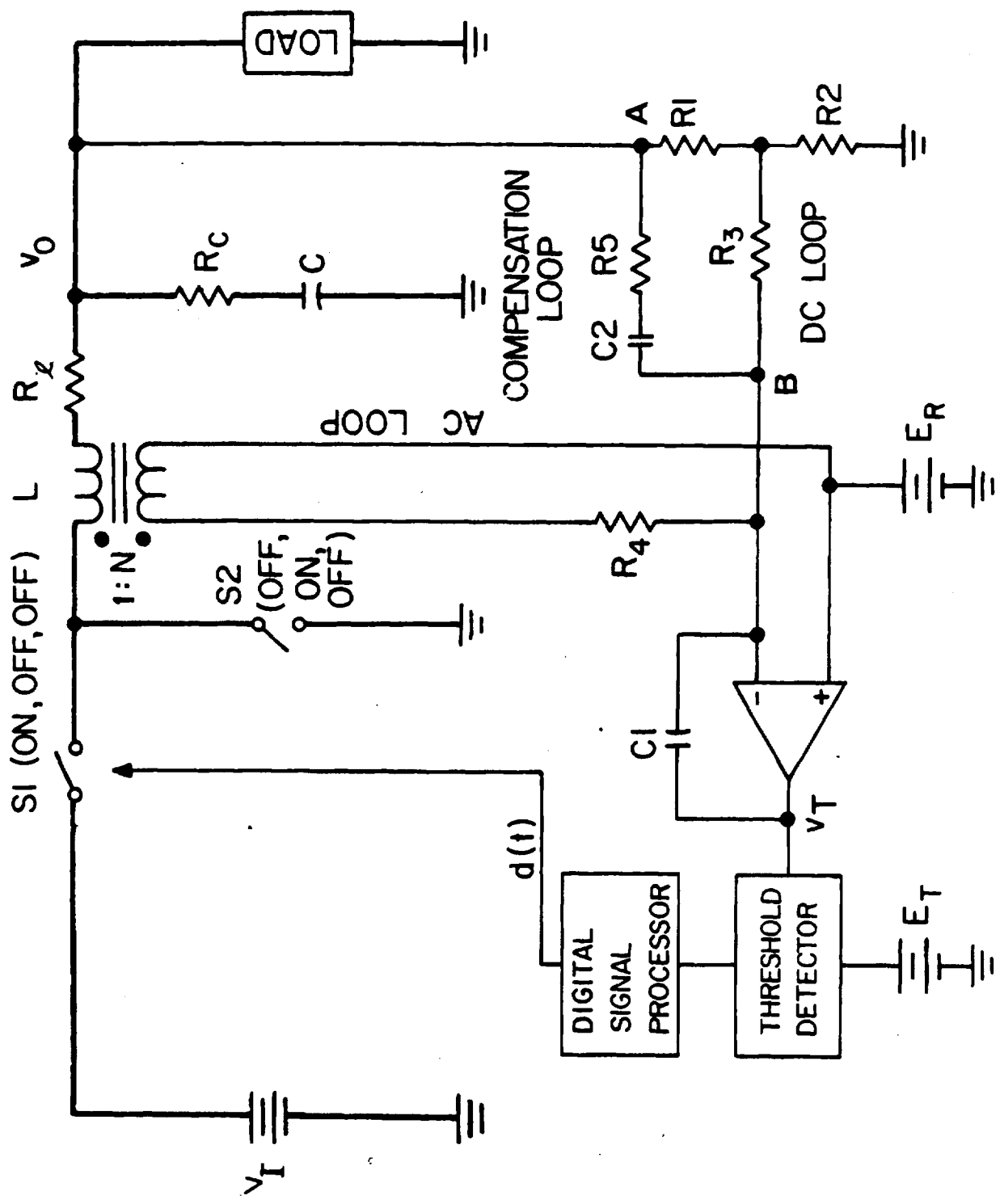


FIG. 7.1 SCHEMATIC OF A BUCK REGULATOR EMPLOYING THE SCM

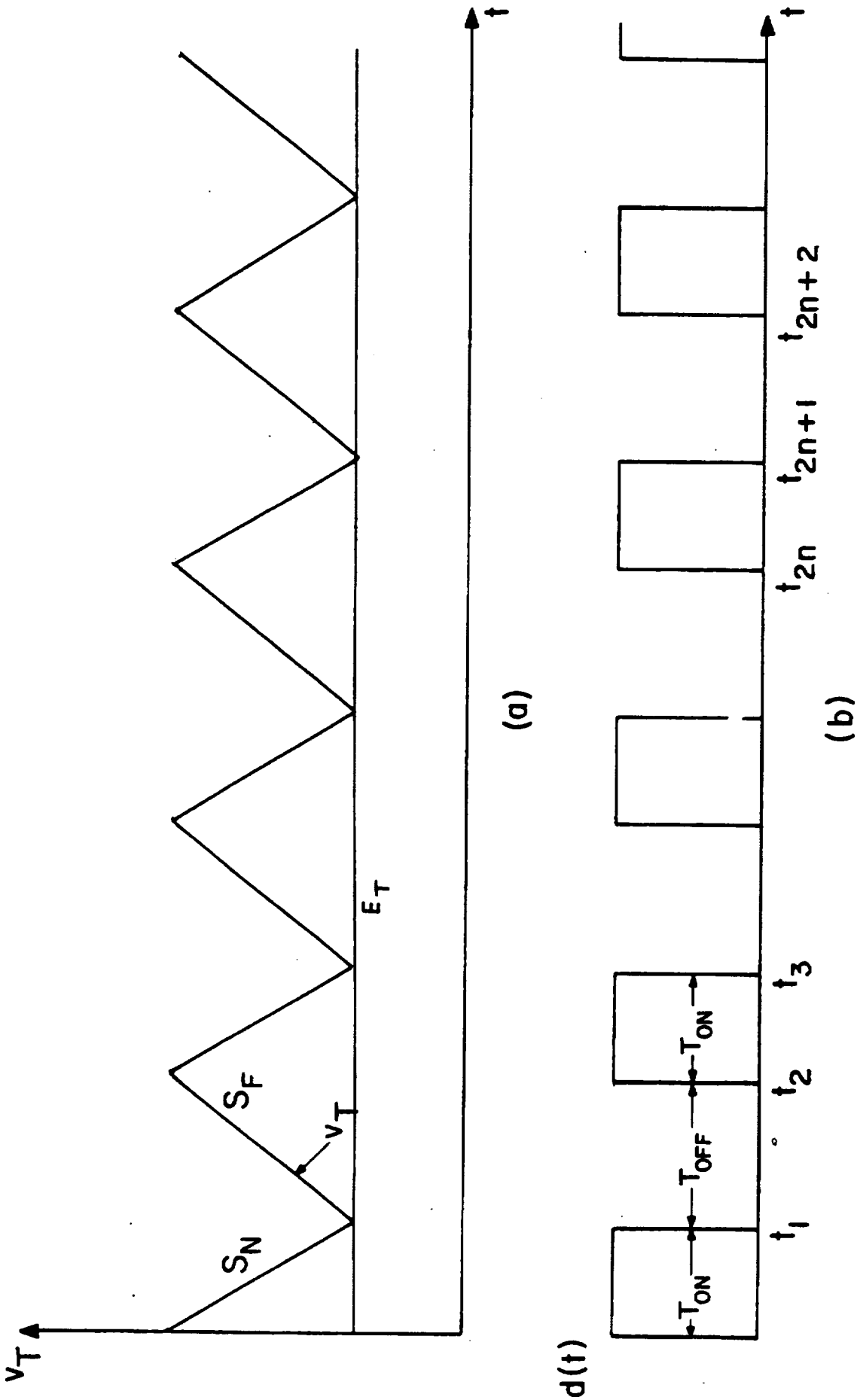


FIG. 7.2 IMPLEMENTATION OF CONSTANT FREQUENCY DUTY CYCLE CONTROL (DISTURBANCE FREE)

put voltage  $v_T$  with the threshold voltage  $E_T$  marks the termination of the  $T_{ON}$  interval. During the on-time interval, the slope of the ramp voltage  $v_T$  decays almost linearly with a slope  $S_N$  approximately by the following equation

$$S_N = \frac{-n(v_I - v_0)}{R_4 C_1}$$

where  $v_I - v_0$  is the voltage drop across the energy storage inductor and series resistor  $R_L$ ,  $n$  is the turns ratio of the ac sensing winding, and  $R_4 C_1$  is the time constant of the ac loop. The length of the subsequent off time is determined by the next clock signal of the predetermined interval ( $T_{ON} + T_{OFF}$ ). The slope  $S_F$  of  $v_T$  during  $T_{OFF}$  is approximated by

$$S_F = \frac{nv_0}{R_4 C_1}$$

Following this pattern, the duty cycle signal  $d(t)$  is illustrated in Fig. 7-2. If the converter is subjected to a small-signal low frequency disturbance, the voltage waveform  $v_T$ , shown as the solid curve in Fig. 7.3, will be modulated. As a result, the duty cycle signal  $d(t)$  also contains a low-frequency-modulation component. It is shown in Fig. 7.3 that the integrator output voltage contains the following information: a low amplitude error signal (disturbance) propagated through both the dc feedback loop and the ac feedback loop, and a high-amplitude switching waveform generated by the operational amplifier integrator. The latter which provides a necessary ramp function for analog-to-digital conversion is considered as an integral part of the duty cycle pulse modulator. The low-amplitude error signal and the high amplitude ramp switching waveform are integrated into a composite waveform  $v_T$  by the operational amplifier summing junction. In order to characterize the pulse modulator by a describing function, it is necessary to separate the composite waveform of  $v_T$  into two components as illustrated in Fig. 7.4, one representing the low frequency error signal as the input to the intended pulse modulator model, and the other representing the switching frequency triangular ramp which is a necessary element in the pulse modulator to implement the analog-to-digital conversion. It should be noted in Fig 7.4 that

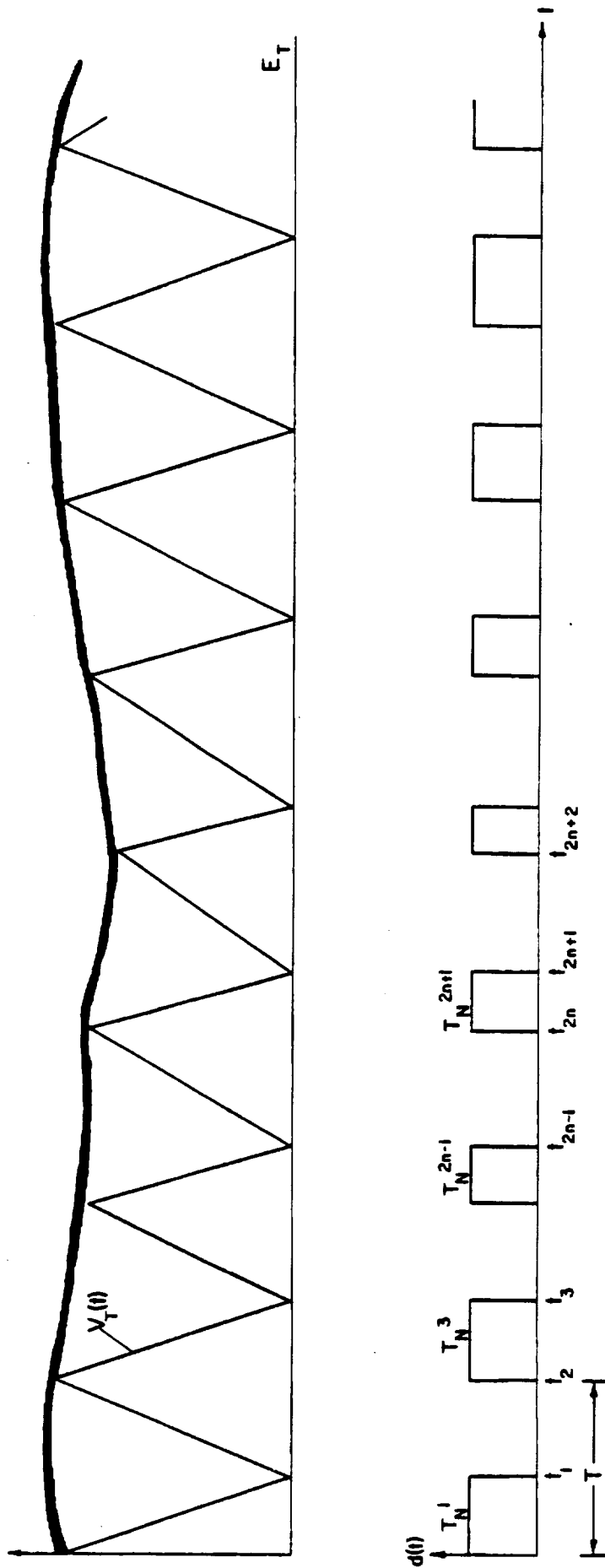


FIG. 7.3 WAVEFORMS OF FIG. 7.2 WHEN CONVERTER IS SUBJECTED TO DISTURBANCE.

MODELING APPROACH

AC ERROR SIGNAL

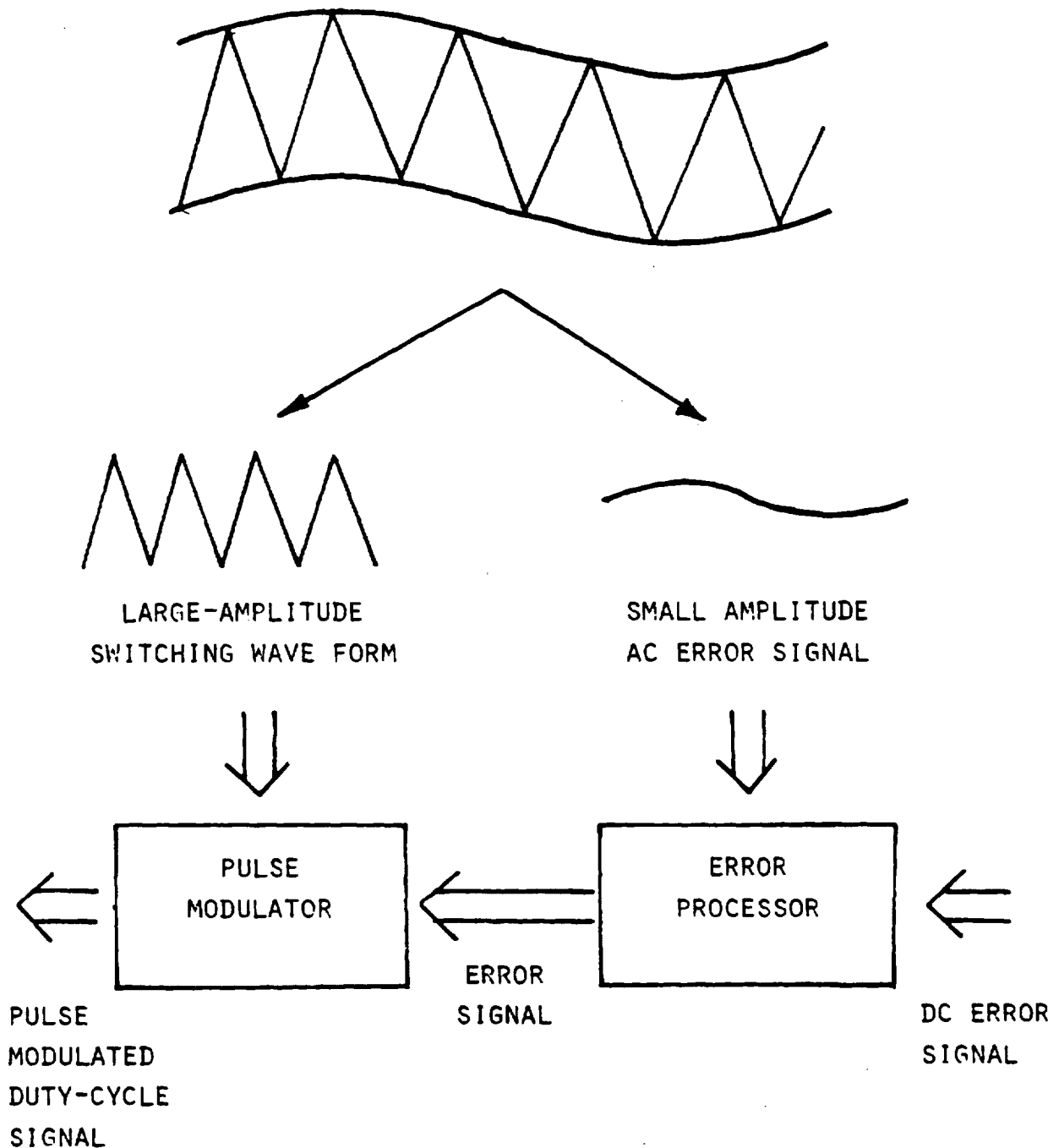


FIG. 7.4 SEPARATION OF THE ANALOG SIGNAL FROM THE AC LOOP- SMALL-AMPLITUDE LOW FREQUENCY ERROR SIGNAL AND LARGE-AMPLITUDE SWITCHING RAMP WAVEFORM.

not only are switching intervals,  $T_{ON}$  and  $T_{OFF}$ , modulated by a low frequency disturbance, so are the respective slopes,  $S_N$  and  $S_F$ .

To characterize the small-signal behavior of the DSP, a low-frequency disturbance  $v_X$ , shown in Figure 7-5, is injected between the amplifier output and the threshold-detector input, where:

$$v_X(t) = A \sin \omega t \quad (7-1)$$

As a result of the disturbance,  $v_X(t)$ , waveforms of  $v_T(t)$ ,  $v_Y(t)$ , and  $d(t)$  can be constructed in Figure 7-6, where

$$v_T(t) = v_X(t) + v_Y(t) \quad (7-2)$$

The duty-cycle signal  $d(t)$  at the DSP output, which contains a series of pulses of equal amplitude but sinusoidally-varying pulse widths, will have a low-frequency content corresponding to the input disturbance frequency. Fourier-series expansions of  $d(t)$  and  $v_T(t)$  become:

$$\left. \begin{aligned} d(t) &= D + a_1 \sin \omega t + b_1 \cos \omega t + \dots \\ v_T(t) &= V_T + c_1 \sin \omega t + d_1 \cos \omega t + \dots \end{aligned} \right\} \quad (7-3)$$

The describing function  $F_M$  of the DSP is defined as:

$$F_M \triangleq \frac{\hat{d}}{\hat{v}_t} = \frac{(a_1^2 + b_1^2)^{1/2}}{(c_1^2 + d_1^2)^{1/2}} \exp \left[ -j \left( \tan^{-1} \frac{b_1}{a_1} - \tan^{-1} \frac{d_1}{c_1} \right) \right] \quad (7-4)$$

In the following presentations, the describing function  $F_M$  is derived for a constant-frequency DSP. Analytical results and an operating subtlety involving certain instability phenomenon beyond a stable duty-cycle range will be discussed. An effective remedy to extend the stable operation to a wider duty-cycle range is then analyzed. Finally, results of describing function derivations for other control laws are summarized; the aforementioned duty-cycle-related instability is found to be unique to the constant-frequency control law.



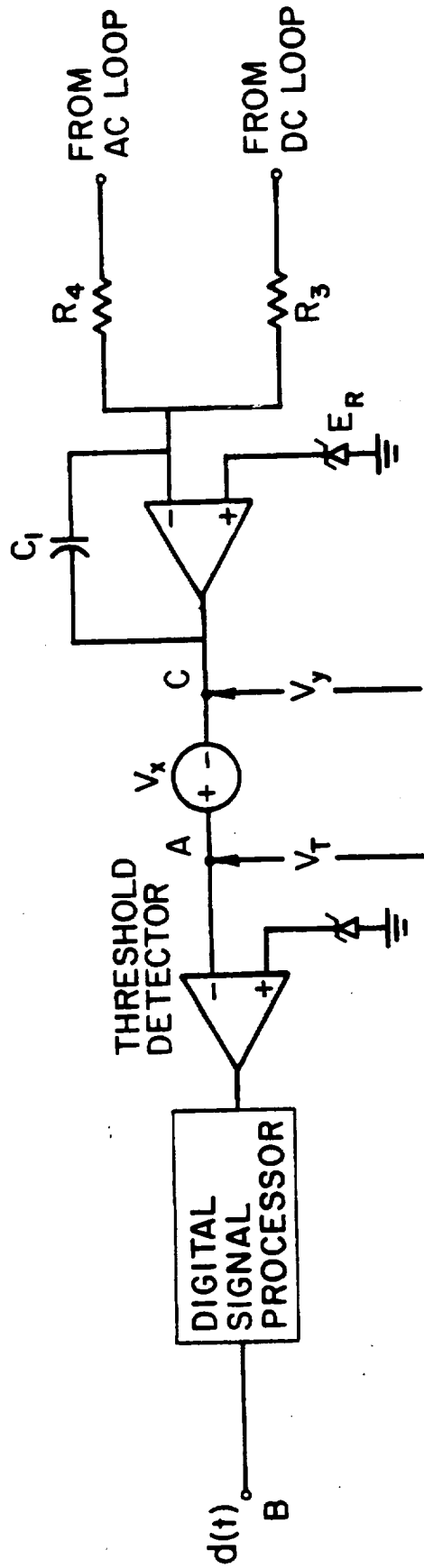


FIG. 7.5 INJECTION OF THE DISTURBANCE SIGNAL  $V_x$  BETWEEN THE OUTPUT OF THE ERROR AMPLIFIER AND THE INPUT OF THE PULSE MODULATOR

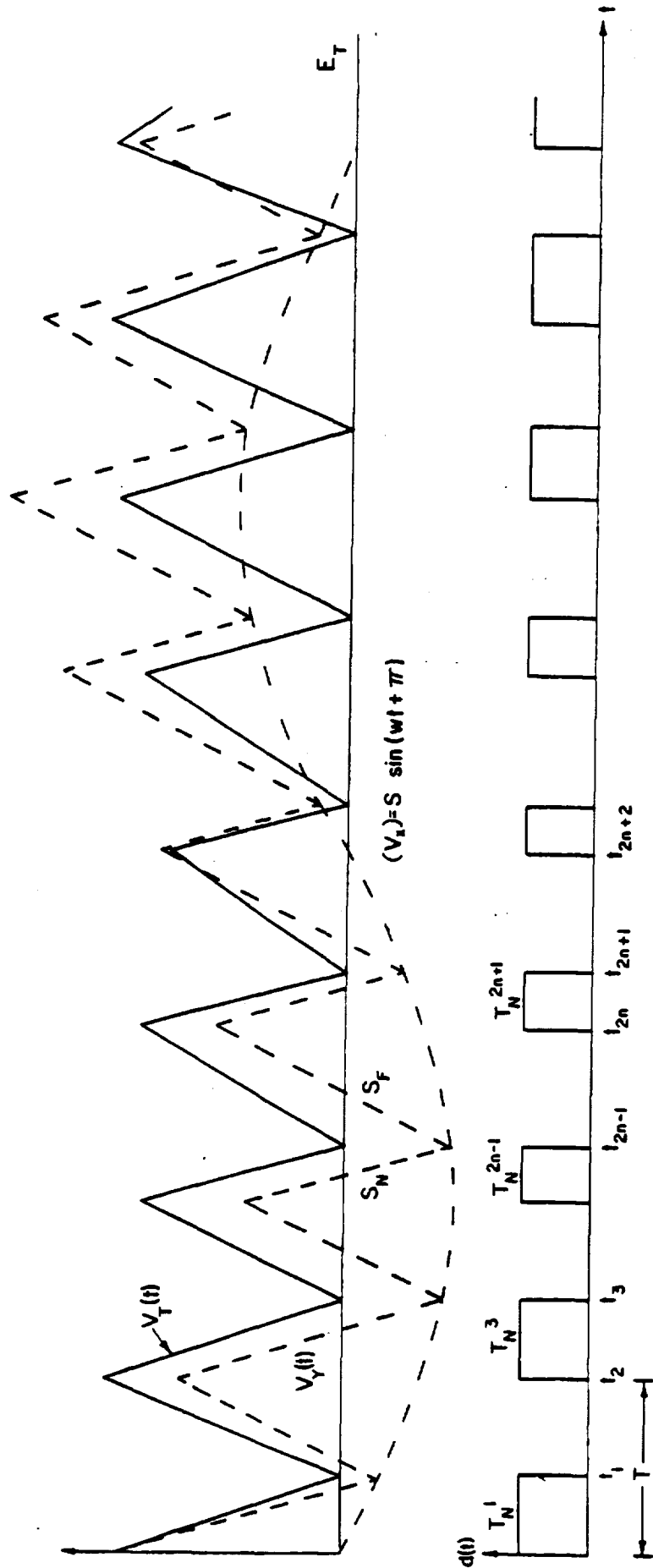


FIG. 7.6 WAVEFORMS OF FIG. 7.5.

Before venturing into analytical details, it is worthwhile to provide a few significant clarifications:

- (1) To simplify the derivations, it is assumed that the low-frequency disturbance and the switching frequency are commensurate, i.e. a disturbance cycle encompasses an integral number of switching cycles, with the initiation of a switching cycle coinciding with the beginning of a disturbance cycle. For conditions other than the aforementioned, the mathematical derivations become intractable, yet the results are expected to be the same [11].
- (2) The describing function  $F_M$ , as defined in eq. (7-5) and derived herein, is applicable to all three different power stages.
- (3) Experimental verifications of the analytical results are quite good for the gain portion of eq. (7-5) throughout the frequency range of interest, but are somewhat dismal for the phase portion at higher disturbance frequencies, (e.g. above 30% of the switching frequency). To the author's best knowledge, no other techniques have been reported to yield highly-accurate phase information regarding the dc-dc converter analog-to-discrete-time conversion process. Realizing that more research effort is needed in this specific area, the derived phase of the DSP describing-function will not be relied on exclusively in generating the SCM design guidelines. Rather, the phase information based on actual test-circuit measurement will be used to supplement the formulation of design guidelines in Volume II of the Report.

## 7.2 Constant-Frequency DSP Describing-Function Analysis

Assuming the low-frequency small-signal disturbance  $v_x(t)$  does not materially affect the slope of voltage  $v_y(t)$  at the integrator-amplifier output during either the on-time or the off-time interval, then for a given set of input and output voltages the triangular ramp, therefore, descends during  $T_{ON}$  with a constant slope  $S_F$ . Figure 7.6 can then be constructed in accordance with eqs. (7-1) and (7-2). The on-time of each cycle is initiated by a constant-frequency clock with period  $T$ , and theoretically is terminated at the instant when the descending  $v_T(t) = v_y(t) + v_x(t)$  intersects a threshold level  $E_T$ .

The sinusoidal disturbance thus modulates the duty-cycle signal  $d(t)$  as shown. The analytical task at hand is to extract from  $d(t)$  the fundamental component corresponding to the frequency of disturbance  $v_x(t)$ , i.e., to evaluate  $a_1$  and  $b_1$  of eq. (7-3) for  $d(t)$  and  $c_1$  and  $d_2$  of eq. (7-4) for  $v_T(t)$  of Figure 7.3 so that  $F_M$  of eq. (7-5) can be determined.

### 7.2.1 Derivation of Coefficients $a_1$ and $b_1$

The coefficient  $b_1$  of eq. (7-3) can be derived as:

$$\begin{aligned}
 b_1 &= \frac{\omega}{\pi} \left( \int_0^{t_1} \cos \omega t \, dt + \int_{t_2}^{t_3} \cos \omega t \, dt + \dots \right) \\
 &= \frac{1}{\pi} \sum_{n=1}^{\infty} B_{2n+1}
 \end{aligned} \tag{7-5}$$

Where

$$\begin{aligned}
 B_{2n+1} &\triangleq \omega \int_{t_{2n}}^{t_{2n+1}} \cos \omega t \, dt \\
 &= 2 \cos \omega \left( t_{2n} + \frac{T_N^{2n+1}}{2} \right) \sin \omega \left( \frac{T_N^{2n+1}}{2} \right)
 \end{aligned} \tag{7-6}$$

where  $T_N^1, T_N^3, \dots, T_N^{2n+1}$  are on time intervals shown in Figure 7.6.

An assumption is made here that the time interval between  $t_{2n-1}$  and  $t_{2n+1}$  is  $T_p$ , the period of a switching cycle. This assumption is valid considering that the small-signal disturbance frequency is much lower than the switching frequency. Thus:

$$T_F^{2n-1} \approx T_F^{2n+1}$$

It can be shown from Figure 7.6 that

$$A \sin \omega t_{2n+1} - A \sin \omega t_{2n-1} + S_F(t_{2n} - t_{2n-1}) - S_N(t_{2n+1} - t_{2n}) = 0 \tag{7-7}$$

where A is the amplitude of the sinusoidal modulation signal. Equation (7-7) may be rewritten to read:

$$2 A \sin \omega \left( \frac{T_N^{2n+1} + T_F^{2n-1}}{2} \right) \cos \omega \left( t_{2n} + \frac{T_N^{2n+1} - T_F^{2n-1}}{2} \right) + S_F(T_F^{2n-1}) - S_N(T_N^{2n+1}) = 0 \quad (7-7a)$$

By invoking the aforementioned assumption of a time interval  $T_p$  between  $t_{2n-1}$  and  $t_{2n+1}$ , equation (7-7a) becomes

$$2A \sin \omega \frac{T_p}{2} \cos \omega \left( t_{2n} + \frac{T_N^{2n+1} - T_F^{2n-1}}{2} \right) + S_F(T_p - T_N^{2n+1}) - S_N T_N^{2n+1} = 0 \quad (7-8)$$

Making the approximation:

$$\cos \omega \left( t_{2n} + \frac{T_N^{2n+1} - T_F^{2n-1}}{2} \right) \approx \cos \omega \left( t_{2n} + \frac{T_N - T_F}{2} \right), \text{ where}$$

$T_N$  and  $T_F$  are the steady-state values, one can solve for  $T_N^{2n+1}$  using (7-8).

$$T_N^{2n+1} = \frac{1}{S_N + S_F} \left[ S_F T_p + 2 A \sin \frac{\omega T_p}{2} \cos \omega \left( t_{2n} + \frac{T_N - T_F}{2} \right) \right] \quad (7-9)$$

Substituting eq. (7-9) into eq. (7-6), and realizing  $\sin \theta \approx \theta$  when  $\theta$  is small, the term  $B_{2n+1}$  becomes:

$$B_{2n+1} \approx \frac{\omega}{S_N + S_F} \left[ S_F T_p + 2A \sin \frac{\omega T_p}{2} \cos \omega \left( t_{2n} + \frac{T_N - T_F}{2} \right) \right] \cdot \cos \omega \left( t_{2n} + \frac{T_N}{2} \right) \cdot \frac{\Delta T}{\Delta T} \quad (7-10)$$

where  $\Delta T = T_p$  the period of one switching cycle.

Substituting (7-10) into (7-5),

$$b_1 = \frac{1}{\pi} \sum_{n=1} \frac{1}{S_N + S_F} \omega \cos \omega \left( t_{2n} + \frac{T_N}{2} \right) \left[ S_F T_p + 2A \sin \frac{\omega T_p}{2} \cos \omega \left( t_{2n} + \frac{T_N - T_F}{2} \right) \right] \frac{\Delta T}{\Delta T} \quad (7-11)$$

If  $\Delta T \ll \frac{2\pi}{\omega}$ , one can approximate (7-11) by setting  $\frac{\Delta T}{\Delta T} \approx \frac{dt}{T_p}$  and writing:

$$b_1 \approx \frac{1}{\pi(S_N+S_F)} \frac{1}{T_P} \int_0^{2\pi} \omega \cos \omega(t_{2n} + \frac{T_N}{2}) [S_F T + 2A \sin \frac{\omega T_P}{2} \cos \omega(t_{2n} - \frac{T_P}{2} + T_N)] dt. \quad (7-12)$$

where the summation of (7-11) is replaced by the integration of (7-12).

Upon integration, (7-12) reduces to the following expression:

$$b_1 = \frac{2A}{(S_N+S_F)T_P} \sin \frac{\omega T_P}{2} \cos(\frac{\omega T_P}{2} \frac{S_N}{S_N+S_F}) \quad (7-13)$$

Making use of the fact that  $\omega T_P$  is very small,

$$\begin{aligned} \sin \frac{\omega T_P}{2} &\approx \frac{\omega T_P}{2} \\ \cos \frac{S_N \omega T_P}{2(S_N+S_F)} &\approx 1 \end{aligned} \quad (7-14)$$

equation (7-13) becomes

$$b_1 \approx \frac{\omega A}{S_N+S_F} \quad (7-15)$$

Following the same detailed procedure in deriving  $b_1$ , one can prove that

$$a_1 \approx 0 \quad (7-16)$$

### 7.2.2 Derivation of $c_1$ and $d_1$

From Figure 7.6, one has  $v_T$  at  $t=t_{2n}$  as:

$$\begin{aligned} v_T(t_{2n}) &= S_N(t_{2n+1} - t_{2n}) - A \sin \omega t_{2n+1} + A \sin \omega t_{2n} + E_T \\ &= S_N T_N^{2n+1} - 2A \sin \frac{\omega T_N^{2n+1}}{2} \cos \omega(t_{2n} + \frac{T_N^{2n+1}}{2}) + E_T \end{aligned} \quad (7-17)$$

Making use of the fact that  $\omega T_N^{2n+1}/2$  is negligibly small, eq. (7-17) can be simplified into:

$$v_T(t_{2n}) \cong S_N T_N^{2n+1} - A\omega T_N^{2n+1} \cos \omega(t_{2n} + \frac{T_N}{2}) + E_T \quad (7-18)$$

Substituting (7-9) into (7-18) and discarding all terms containing  $\cos^2 \omega t$ ,  $(\sin \omega t_{2n})(\cos \omega t_{2n})$ , and  $\omega^2 \sin \omega t_{2n}$ , the low frequency fundamental component of  $v_T(t_{2n})$  will emerge as:

$$v_T(\omega) \approx \frac{S_N - S_F}{S_N + S_F} A\omega T_p \cos \omega t_{2n} \quad (7-19)$$

Considering that  $v_T$  here represents the peak amplitude of a triangular waveform, its average value becomes:

$$\hat{v}_T = \frac{S_N - S_F}{2(S_N + S_F)} A\omega T_p \cos \omega t_{2n} \quad (7-20)$$

Therefore  $C_1 = 0$  and  $d_1 = (S_N - S_F)/2(S_N + S_F)$  (7-20a)

Finally, substituting (7-15), (7-16), and (7-20) into (7-4),

$$\left| F_M \right| = \frac{2}{T_p(S_N - S_F)}$$

It is iterated here that  $T_p$  is the switching period,  $S_N$  is the absolute value of the slope of the unperturbed integrator ramp during the on time, and  $S_F$  is that during the off time.

### 7.3 Duty-Cycle Instability for Constant-Frequency Control Law

The denominator of equation (7-21) is seen to have a term  $(S_N - S_F)$ . In a disturbance-free environment, a steady-state integrator output requires that:

$$S_N T_{ON} = S_F T_{F1}$$

i.e., the descending voltage during the on time must be exactly matched by the ascending voltage during the off time within the same switching cycle, lest the integrator eventually lose its linear operation. Consequently, when  $T_{ON}$  and  $T_{F1}$  are equal at a duty-cycle operation for  $d=0.5$ ,  $S_N$  will be identical to  $S_F$ . Consequently,

$$F_M > 0 \quad \text{for } S_N > S_F \quad \text{or } T_{ON} < T_{F1}$$

$$F_M < 0 \quad \text{for } S_N < S_F \quad \text{or } T_{ON} > T_{F1}$$

A negative  $F_M$  means a negative gain for the DSP. In conjunction with an inherently-negative gain presented by the previously-described ASP, a negative  $F_M$  results in a positive-feedback condition, causing system instability. Consequently, unless a remedy is provided, the SCM operating under a constant-frequency control law will cause the regulated system to be unstable. The following observations are noted regarding the instability phenomenon:

- (1) The general analysis predicting the instability is not based on any particular power stage; it is applicable to all three power stages previously described.
- (2) A physical understanding was given in Reference [3] regarding the instability, which is now completely analyzed. From the description therein, it is clear that the duty cycle instability will exist in any regulator which utilizes a voltage or current state sensed within the regulator power stage as the ramp function to control the analog-signal-to-discrete-time-cycle conversion. It is by no means limited to the SCM.
- (3) For triangular ramp, the instability is intimately related to a 0.5 duty cycle. For other types of ramps such as a sinusoidal or cosinusoidal ramp, the duty cycle representing the threshold of stability will be a different value.
- (4) From eq. (7-21), as  $S_N$  approaches  $S_F$ , gain  $F_M$  tends to increase rapidly. This effect has actually been measured and confirmed through laboratory testing.
- (5) The conclusion that  $T_{ON} > T_{F1}$  (or,  $d > 0.5$ ) leads to instability in a constant-frequency operation is true when the constant-frequency clock initiates on time  $T_{ON}$ , and the regulator-control terminates  $T_{ON}$ . This mechanization is illustrated in Figure 7.3. If an implementation is made such that the clock initiates  $T_{F1}$ , and the regulator-control terminates  $T_{F1}$ , then the condition of instability is reversed, i.e., (or,  $d < 0.5$ ).
- (6) This instability can be eliminated through circuit means, to be discussed and analyzed next.



#### 7.4 Extending Stable Duty-Cycle Operation Range

From eq. (7-21), it is clear that a stable operation can be extended beyond the 0.5 duty-cycle by increasing  $S_N$  for a given  $S_F$  in Figure 7-3. Figure 7-7 illustrates the effect of such an implementation, where an additional ramp with slope  $S_E$  is added during the on time. The attendant analysis is presented as the following.

##### 7.4.1 Derivation of Coefficient $b_1$

Expressing  $d(t) = D + a_1 \sin \omega t + b_1 \cos \omega t$ , coefficient  $b_1$  can be evaluated exactly the same as the previous case without an externally added ramp:

$$b_1 = \frac{1}{\pi} \sum_{n=1} B_{2n+1} \quad (7-22)$$

where

$$\begin{aligned} B_{2n+1} &\triangleq \omega \int_{t_{2n}}^{t_{2n+1}} \cos \omega t \, dt \\ &= 2 \cos \omega \left( t_{2n} + \frac{T_N^{2n+1}}{2} \right) \sin \omega \frac{T_N^{2n+1}}{2} \end{aligned} \quad (7-23)$$

Similar to the derivation of (7-9), it can be shown that:

$$T_N^{2n+1} = \frac{1}{S_N + S_F} \left[ S_F T_P + 2A \sin \frac{\omega T_P}{2} \cos \omega \left( t_{2n} + \frac{T_N - T_F}{2} \right) \right] \quad (7-24)$$

Since (7-24) is exactly the same as (7-9), the Fourier analysis of  $d(t)$  with an external ramp is the same as that of the previous case with an external ramp. The results are shown in the following

$$\begin{aligned} b_1 &\approx \frac{A\omega}{S_N + S_F} \\ a_1 &\approx 0 \end{aligned} \quad (7-25)$$

##### 7.4.2 Derivation of $c_1$ and $d_1$ for $V_T$

Similar to eq. (7-17), the following equation can be derived from Figure 7.7:

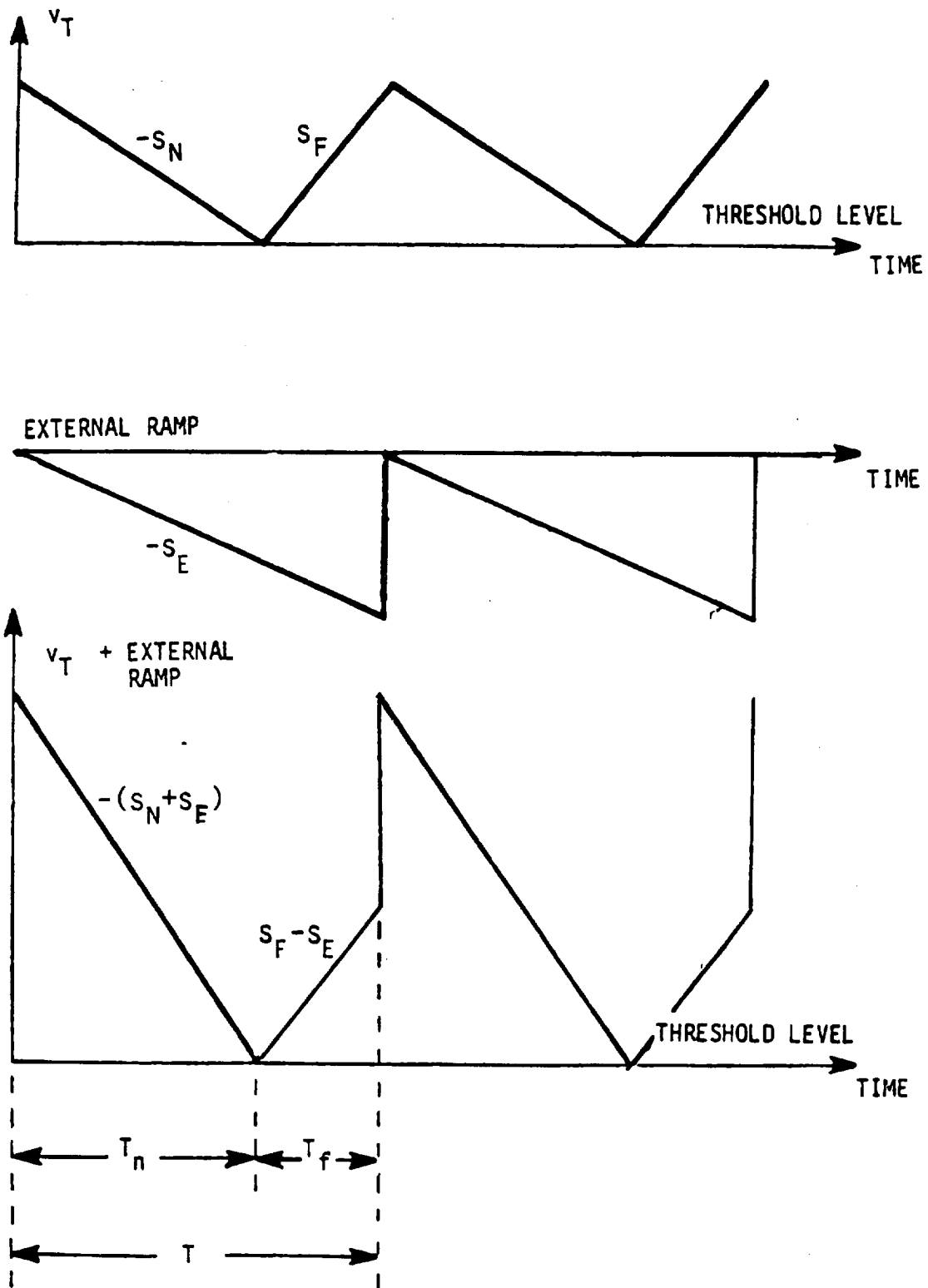


FIG. 7.7 EXTENDING CONSTANT FREQUENCY STABLE DUTY CYCLE LIMIT THROUGH EXTERNAL RAMP ADDITION.

$$\begin{aligned}
v_T(t_{2n}) &= E_T + (t_{2n+1} - t_{2n})(S_N + S_E) + A \sin \omega t_{2n} - A \sin \omega t_{2n+1} \\
&= E_T + (S_N + S_E)T_N^{2n+1} \sin \frac{\omega T_N^{2n+1}}{2} \cos \omega \left( t_{2n} + \frac{T_N^{2n+1}}{2} \right) \quad (7-26)
\end{aligned}$$

Combining (7-24) and (7-26), and letting  $\sin(\omega T_N^{2n+1}/2) \cong \omega T_N^{2n+1}/2$ .

$$\begin{aligned}
v_T &= E_T + \frac{S_N + S_E}{S_N + S_F} \left\{ S_F T_P + 2A \sin \frac{\omega T_P}{2} \cos \omega \left( t_{2n+1} + \frac{T_P}{2} \right) \right\} \\
&\quad - \frac{A\omega}{S_N + S_F} \left[ S_F T_P + 2A \sin \frac{\omega T_P}{2} \cos \omega \left( t_{2n+1} + \frac{T_P}{2} \right) \right] \cos \omega \left( t_{2n} + \frac{T_N^{2n+1}}{2} \right) \quad (7-27)
\end{aligned}$$

Extracting only the fundamental-frequency component from (7-27),

$$\begin{aligned}
v_T(\omega) &= A\omega T_P \frac{S_N + S_E}{S_N + S_F} \cos \omega \left( t_{2n-1} + \frac{T_P}{2} \right) \\
&\quad - A\omega T_P \frac{S_F}{S_N + S_F} \cos \omega \left( t_{2n} + \frac{T_N^{2n+1}}{2} \right) \\
&= \frac{A\omega T_P}{S_N + S_F} \left\{ (S_N + S_E) \cos \omega \left( t_{2n} - T_N^{2n+1} + \frac{T_P}{2} \right) \right. \\
&\quad \left. - S_F \cos \omega \left( t_{2n} + \frac{T_N^{2n+1}}{2} \right) \right\} \quad (7-28)
\end{aligned}$$

Employing the approximation of equation (7-14) and neglecting higher order terms, one obtains

$$v_T(\omega) \approx \frac{A\omega T_P}{S_N + S_F} (S_N + S_E - S_F) \cos \omega t_{2n}. \quad (7-29)$$

From Figure 7.7, the waveform  $v_T$  is clearly not triangular as was Figure 7.6. The average value of  $v_T(\omega)$  is no longer simply  $v_T(\omega)/2$ , but can be derived as:

$$\begin{aligned}
\langle V_T \rangle = & \frac{1}{T_P} \left\{ \frac{A\omega T_P}{S_N + S_F} (S_N + S_E - S_F) \left( \frac{T_N^{2n+1}}{2} \right) \cos \omega t_{2n-2} \right. \\
& \left. + \left[ \frac{A\omega T_P}{S_N + S_F} (S_N + S_E - S_F) \cos \omega t_{2n} - S_E T_P \right] \frac{T_P - T_N^{2n+1}}{2} \right\} \quad (7-30)
\end{aligned}$$

By simplifying (7-30) and retaining only the fundamental-frequency terms,

$$\hat{V}_T \approx \frac{A\omega T_P}{2} \frac{2S_E + S_N - S_F}{S_N + S_F} \cos \omega t_{2n} \quad (7-31)$$

From (7-25) and (7-31), the DSP gain for this case becomes:

$$|F_M| = \frac{\hat{d}}{\hat{V}_T} = \frac{2}{T_P} \frac{1}{2S_E + S_N - S_F} \quad (7-32)$$

It becomes apparent from (7-32) that gain  $F_M$  remains positive at 0.5 duty cycle when  $S_N = S_F$ , due to the presence of the additional  $2S_E$  term in relation to eq. (7-21). Stable operation is thus extended beyond the 0.5 duty cycle, and can be maintained for any higher duty cycle for as long as the following relation holds:

$$S_E > \frac{S_F - S_N}{2} \quad (7-33)$$

Taking a duty cycle of 0.9 for example, which is high for a practical application,

$$T_{ON} = 0.9 T_P$$

$$T_{F1} = 0.1 T_P$$

With  $S_N T_{ON}$  and  $S_F T_{F1}$  constrained to be identical for a steady state operation,

$$S_F = 9 S_N$$

In accordance with (7-33), an external ramp with slope  $S_E > 4S_N$  is there-

fore needed to maintain stable operations. If the required operating duty-cycle range is reduced, the slope  $S_E$  can be reduced likewise.

### 7.5 Describing Functions for Other Control Laws

In the previous sections of this chapter, the most-commonly used control law has been used in all discussions pertaining to the DSP transfer functions in terms of describing functions. As stated earlier, there are other control laws, among which constant on time and constant off time are the more significant ones. Their describing functions in conjunction with the SCM applications can be derived in a similar manner [2]. Without elaborating the analytical details, the derived results are presented as the following:

For Constant on-time ( $T_{ON}$ ) control:

$$F_M = \frac{1}{S_N + S_F} \frac{2}{T_{ON}} \exp(-j\omega T_{ON}) \quad (7-34)$$

For Constant volt-second ( $v_I T_{ON}$ ) control:

$$F_M = \frac{1}{S_N + S_F} \frac{2v_I}{v_I T_{ON}} \exp(-j\omega T_{ON}) \quad (7-35)$$

where

For Constant off-time ( $T_{OFF}$ ) control:

$$F_M = \frac{1}{S_N + S_F} \frac{2}{T_{OFF}} \exp(-j\omega T_{OFF}) \quad (7-36)$$

Examining the gain portion of each describing function shows that  $F_M$  is always positive. It is thus concluded that there is no duty-cycle related instability when control laws other than the constant-frequency are used.

It is pointed out again that the gain information derived for  $F_M$  in eqs. (7-34), (7-35), and (7-36) have all been test verified. However, good agreements to the same extent have not been obtained for the phase information. Measured DSP phase delays at high disturbance frequencies is quite significant. Figure 7.8 and 7.9 shows the measured pulse modulator gain and phase for constant  $v_I T_{ON}$  and constant frequency control.

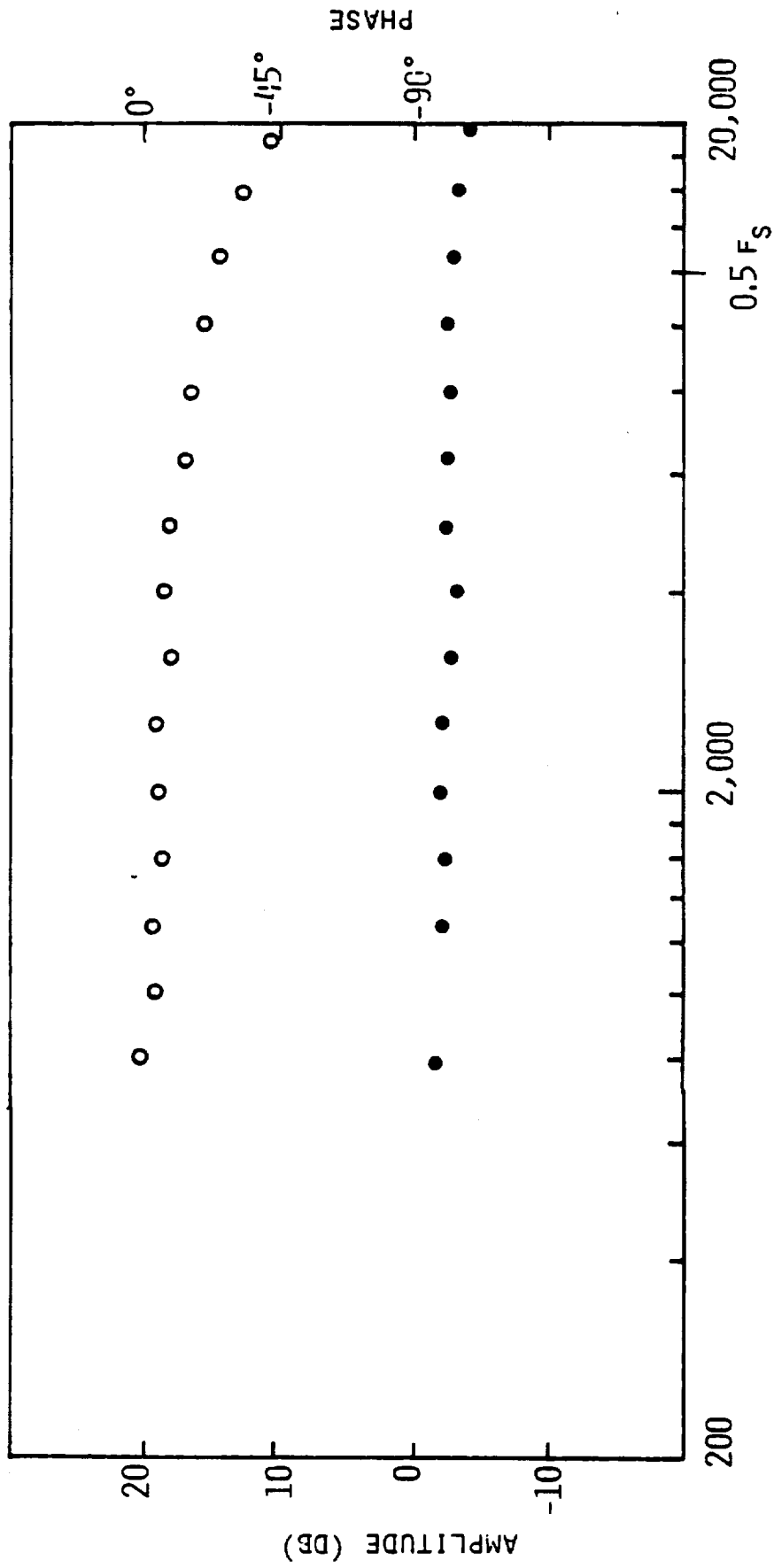


FIG. 7.3 MEASUREMENTS OF PULSE MODULATOR GAIN AND PHASE FOR CONSTANT  $V_{I\text{ON}}$  CONTROL.

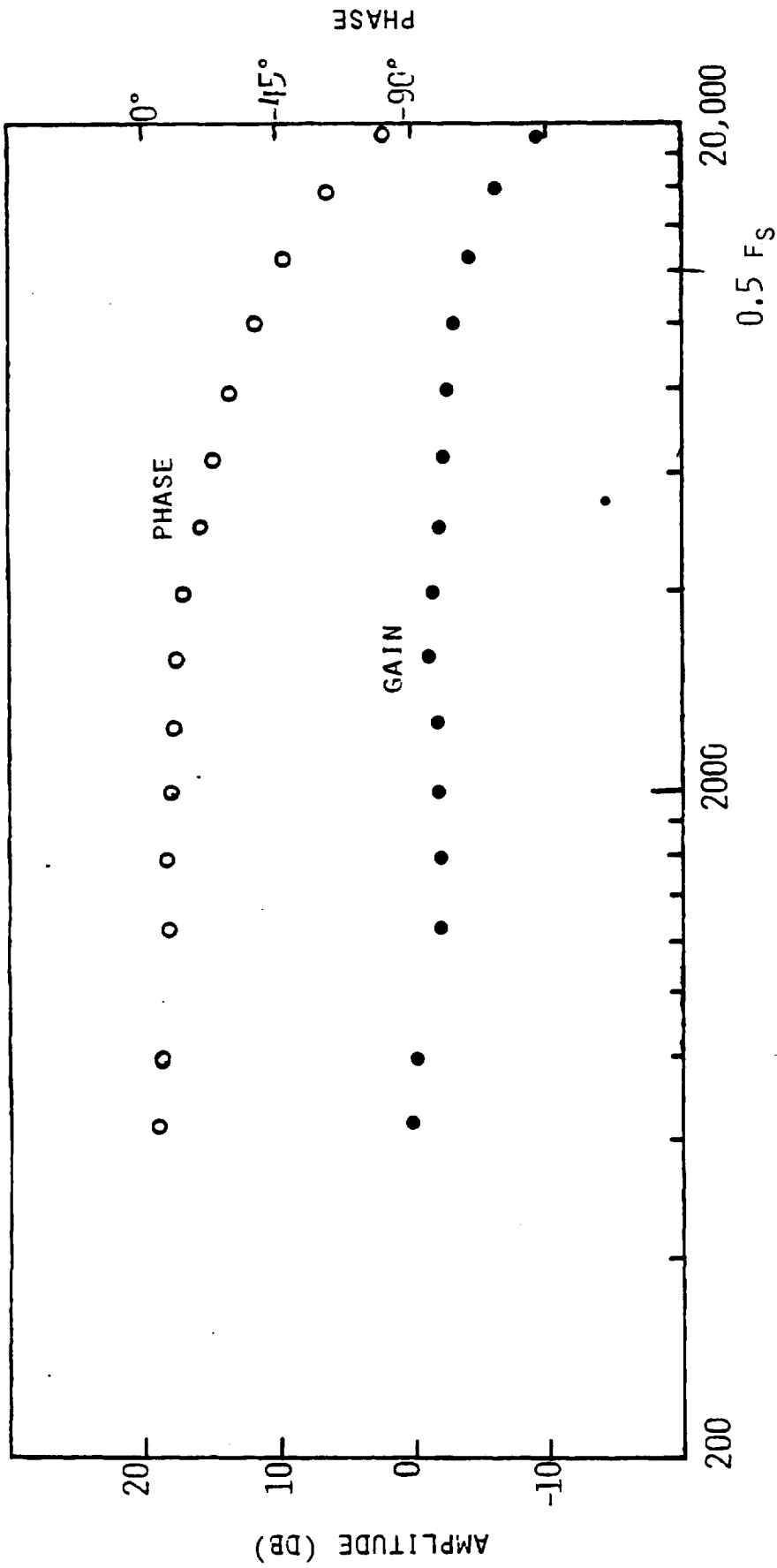


FIG. 7.9 MEASUREMENT OF PULSE MODULATOR GAIN AND PHASE FOR CONSTANT FREQUENCY CONTROL WITH AN EXTERNAL RAMP.

respectively. The measurement is made by inserting a sinusoidal modulation signal at the output of the operational amplifier integrator. The fundamental components of both the input signal  $V_T$  to the pulse modulator and the output signal (base drive signal) of the pulse modulator are extracted to provide the gain and phase of the pulse modulator. It is shown in Figure 7.8 and 7.9 that the phase delay at half of the switching frequency is as much as  $25^\circ$  to  $45^\circ$ . When the modulation frequency is low with respect to the switching frequency, the amount of phase delay is almost negligible. The discrepancies between the analytical model and the actual measurements have to be taken into account in both analysis and design to avoid unexpected instability of the switching regulators. A major reason for this discrepancy can be undoubtedly attributed to the various assumptions and approximations made in the mathematical derivations of these results. Judging from the scarcity of literature dealing with the describing function of a switching-regulator analog-to-discrete-time conversion, there appears to be a need for a continued effort pursuing a more refined analytical technique.

#### 7.6 DSP Block-Diagram Representations for Three Power Stages

The block diagram for the DSP is simply a single block with transfer function  $F_M$ . The equations relating the control modes to their respective  $F_M$  values are:

For constant-frequency control without external ramp: eq. (7-21)

For constant-frequency control with external ramp: eq. (7-32)

For constant-on-time control: eq. (7-34)

For constant volt-second control: eq. (7-35)

For constant off-time control: eq. (7-36)

These equations were expressed in terms of  $S_N$ ,  $S_F$ , and the respective time intervals, which apply equally well to all three power stages. However,  $S_N$  and  $S_F$  for each power stage are different from the others. Consequently, for each control law, a specific power stage will have its unique set of  $S_N$  and  $S_F$ .

Let  $n$  be the ratio of ac sensing turns to the main power inductor turns, as shown in Figure 2.1.



$$\begin{aligned}
n &= N_{AC}/N && \text{for buck power stage} \\
n &= N_{AC}/N && \text{for boost power stage} \\
n &= N_{AC}/N_S && \text{for buck-boost power stage}
\end{aligned} \tag{7-37}$$

Then,

$$\begin{aligned}
S_N &= n(V_I - V_O)/R_4 C_1 && \text{for buck power stage} \\
&= nV_I/R_4 C_1 && \text{for boost power stage} \\
&= n(N_S/N_P)V_I/R_4 C_1 && \text{for buck-boost power stage}
\end{aligned} \tag{7-38}$$

$$\begin{aligned}
S_F &= nV_O/R_4 C_1 && \text{for buck power stage} \\
&= n(V_O - V_I)/R_4 C_1 && \text{for boost power stage} \\
&= nV_O/R_4 C_1 && \text{for buck-boost power stage}
\end{aligned} \tag{7-39}$$

Using these expressions in the various equations derived for  $F_M$ , and letting the additional ramp  $S_E$  (for constant-frequency control law only) be:

$$S_E = K S_N \tag{7-40}$$

the DSP gain expression for each power stage operating under a given control law can be found from the derived results summarized in Table 7-I. In Table 7-I, the pulse modulator gain is represented by the general expression

$$F_M = \frac{2R_4 C_1}{nM} \tag{7-41}$$

This expression is obtained by substituting equations (7-37) to (7-40) into equations (7-32), (7-34), (7-35) and (7-36) neglecting the phase delay term.

TABLE 7-1

$$\text{PULSE MODULATOR GAIN } F_M = \frac{2R_4C_1}{N} \frac{1}{M}$$

(CONTINUOUS CURRENT OPERATION)

M	CONSTANT $T_{ON}$	CONSTANT $T_{OFF}$	CONSTANT $T_p$ W/O RAMP	CONSTANT $T_p$ WITH RAMP
BUCK	$V_I T_{ON}$	$V_I T_{OFF}$	$V_I (1-2D) T_p$	$V_I (1-2D) T_p + 2S_{EP} \frac{R_4C_1}{N}$
BOOST	$V_0 T_{ON}$	$V_0 T_{OFF}$	$V_I (2-\frac{1}{D}) T_p$	$V_I (2-\frac{1}{D}) T_p + 2S_{EP} \frac{R_4C_1}{N}$
BUCK/ BOOST	$(\frac{N_S}{N_P} V_I + V_0) T_{ON}$	$(\frac{N_S}{N_P} V_I + V_0) T_{OFF}$	$\frac{N_S}{N_P} V_I (1 - \frac{D}{D'}) T_p$	$\frac{N_S}{N_P} V_I (1 - \frac{D}{D'}) T_p + 2S_{EP} \frac{R_4C_1}{N}$

## CHAPTER 8

### COMPLETE SMALL-SIGNAL BLOCK DIAGRAM OF SCM-CONTROLLED SWITCHING REGULATORS

Chapters 5, 6, and 7 have provided the low-frequency small-signal characterizations of the three SCM-controlled switching regulator functional blocks: the Power Stage, the Analog Signal Processor (ASP), and the Digital Signal Processor (DSP). Based on the power-stage block diagram of Figure 5.3, the ASP block diagram of Figure 6.2, and the single block  $F_M$  derived for the DSP, a complete system block diagram applicable to all three power stages operating under any duty-cycle control law can be shown as Figure 8.1.

While both input and duty-cycle effects on the system output are represented in Figure 8.1, it is nevertheless noted that no output-current perturbation has been included. Since this information will be needed in assessing the output-impedance characteristic of each SCM-controlled regulator, it is highly desirable to expand the generality of this block diagram by incorporating in it the output-current-perturbation effect.

An output-current perturbation  $i_o$  applied to a SCM-controlled system results in the following:

- It will cause an open-loop regulator to have a voltage disturbance  $i_o Z_p$  where  $Z_p$  is the open-loop output impedance of the converter. This voltage is then attenuated by the closed-loop regulator.
- A portion of  $i_o$  will cause disturbance of the output-inductor current  $i_A$  which in turn will contribute to the  $v_{ac}$  sensed by the ac loop of the SCM, as  $v_{ac}$  is equal to  $snLi_A$ . For two-winding Buck/Boost converter,  $i_A$  represents the equivalent inductor current defined in Chapter 12.

With the output-current perturbation effects thus identified, Figure 8.1 can be modified into Figure 8.2 to include these effects. The block diagram of Figure 8.2 will serve as the basis for all small-signal performance analyses to be performed in the following chapters. Except for blocks  $Z_p$  and  $F_A$ , each block has been analytically identified. Strictly for convenience of references, the transfer functions for all blocks shown in Figure 8.2 are summarized in Table 8-1 for each power stage. The newly added  $Z_p$  and  $F_A$ , will be derived in Chapter 12 when the output impedance is studied.

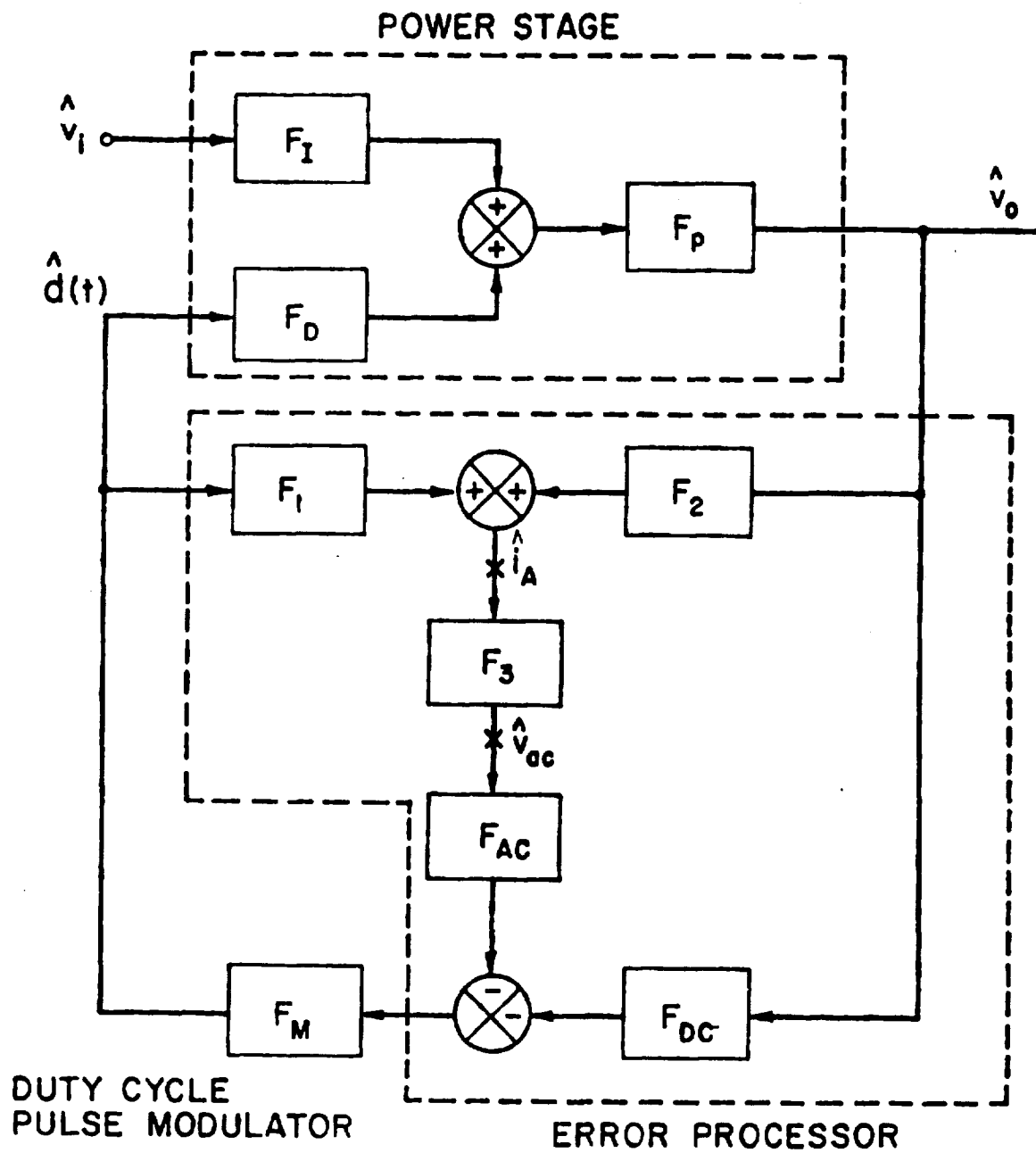


FIG. 8.1 SMALL SIGNAL BLOCK DIAGRAM OF SCM-CONTROLLED SWITCHING REGULATORS.



Table 8-I Summary of Transfer Functions for All Functional Blocks.

Power Stage Block	Buck	Boost	Buck-Boost
F <sub>I</sub>	D	$\frac{1}{D'}$	$\frac{D}{D'} \frac{N_s}{N_p}$
F <sub>D</sub>	$\frac{V_0}{D}$	$\frac{V_0}{D'} (1-s \frac{L_e}{R_L})$	$\frac{V_0}{DD'} (1 - \frac{sDL_e}{R_L})$
F <sub>1</sub>	0	$\frac{V_0}{(D')^2 R_L}$	$\frac{V_0}{(D')^2 R_L}$
F <sub>2</sub>	$\frac{1+sCR_L}{R_L(1+sCR_C)}$	$\frac{1}{D'} \frac{1+sCR_L}{1+sCR_C}$	$\frac{1}{D'R_L} \frac{1+sCR_L}{1+sCR_C}$
F <sub>3</sub>	snL	snL	snL <sub>s</sub>
F <sub>4</sub>	1	$\frac{1}{D'}$	$\frac{1}{D'}$
F <sub>p</sub>		$\frac{1+sCR_C}{\Delta}$	$\Delta = s^2 + s(\frac{1}{CR_L} + \frac{R_{eq}+R_C}{L_e}) + \frac{1}{L_e C}$
Z <sub>p</sub>		$F_p \cdot (R_{eq} + sL_e)$	
F <sub>AC</sub>		$\frac{1}{sC_1 R_4}$	
F <sub>DC</sub>		$\frac{1}{sC_1} (\frac{g}{R_3+R_X} + \frac{1}{Z_C})$	$R_X = R_1 // R_2, g = \frac{R_X}{R_1}, Z_C = R_5 + \frac{1}{sC_2}$
F <sub>M</sub>		$2R_4 C_1 / (nm)$	see Table 7-I for M

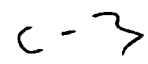


Figure 8.2 is a unified blockdiagram representation for the three converter types. This block diagram will be employed to examine the control loop dependent performance of the converter including stability, output impedance and audiosusceptibility of the converter.

Stability. The loop stability is investigated via converter open-loop transfer function assuming the disturbance from both the line and the output are zero, i.e.  $\hat{v}_i = 0$ .  $\hat{i}_o = 0$ . By opening the loop at the pulse modulator input, the open loop transfer function can be expressed as

$$G_T(s) = F_M(s)F_D(s)F_p(s)F_{DC}(s) + F_M(s)F_3(s)F_{AC}(s)[F_1(s) + F_2(s)F_p(s)F_D(s)] \quad (8-1)$$

Audiosusceptibility. The audiosusceptibility of a converter is evaluated by the closed-loop input-to-output transfer function. It is employed to measure the rejection rate of a sinusoidal disturbance propagated from the converter input to the output. Assuming  $\hat{i}_o = 0$ , the closed-loop input to output transfer function  $G_A(s)$  is expressed as

$$G_A(s) = \frac{\hat{v}_o(s)}{\hat{v}_i(s)} = \frac{F_I(s)F_p(s)[1 + F_1(s)F_3(s)F_{AC}(s)F_M(s)]}{1 + G_T(s)} \quad (8-2)$$

Output Impedance. The converter performance due to sinusoidal disturbance at the output current can be investigated using the output impedance characteristic. The output impedance is measured as the ratio of  $\hat{v}_o(s)/\hat{i}_o(s)$ , where  $\hat{i}_o(s)$  is the sinusoidal disturbance at the converter output. The output impedance is employed to measure dc or dynamic performance of a switching regulator subjected to sinusoidal load variations.

Letting  $\hat{v}_i = 0$ , one can express the output impedance as

$$\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = Z_o(s) = \frac{Z_p(s)(1+F_M(s)F_1(s)F_3(s)F_{Ac}(s))+F_D(s)F_p(s)F_3(s)F_4(s)F_{Ac}(s)F_M(s)}{1+G_T(s)} \quad (8-3)$$

These control-loop dependent characteristics of switching regulators will be examined in detail in the following chapters.



## CHAPTER 9

### ADAPTIVE CONTROL - BASIC CONCEPT AND IMPLEMENTATION

#### 9-1 Adaptive Control - Basic Concept

The control loops when properly designed can provide the complex zero to cancel completely the complex pole presented by the low-pass filter of the converter power stage [12]. Employing a buck converter as an illustrative example, it will be shown mathematically that the control loop has the ability to sense filter parameter changes and automatically provide pole-zero cancellation. To examine such an adaptive nature of the control loops, one can investigate the regulator open-loop transfer function. Since the regulator control contains multiple feedback paths, the loop should be open at a place common to all the feedback paths. It is for this reason the loop is opened at the output terminal of the op-amp integrator as shown in Fig. 9.1. The open-loop transfer function  $G_T(s)$  for the buck converter can be expressed as

$$G_T(s) = F_M(s)F_D(s)F_p(s)(F_2(s)F_3(s)F_{AC}(s) + F_{DC}(s)) \quad (9-1)$$

where the term involving  $F_1$  has been omitted since, for the buck converter,  $F_1=0$ .

Substituting the circuit expression for F's in Table 8.1 of the previous chapter into Equation (9-1),

$$G_T(s) = \frac{F_M F_D}{C_1} \frac{\frac{nLs}{R_4} + \frac{R_L(R_C Cs + 1)}{(R_L + R_C)C + 1} \frac{1}{R_y}}{R_x + sL + \frac{R_L(R_C Cs + 1)}{(R_L + R_C)Cs + 1}} \quad (9-2)$$

where  $R_y = \frac{R_x + R_3}{g}$

Let  $\alpha = \frac{R_4}{nR_y}$

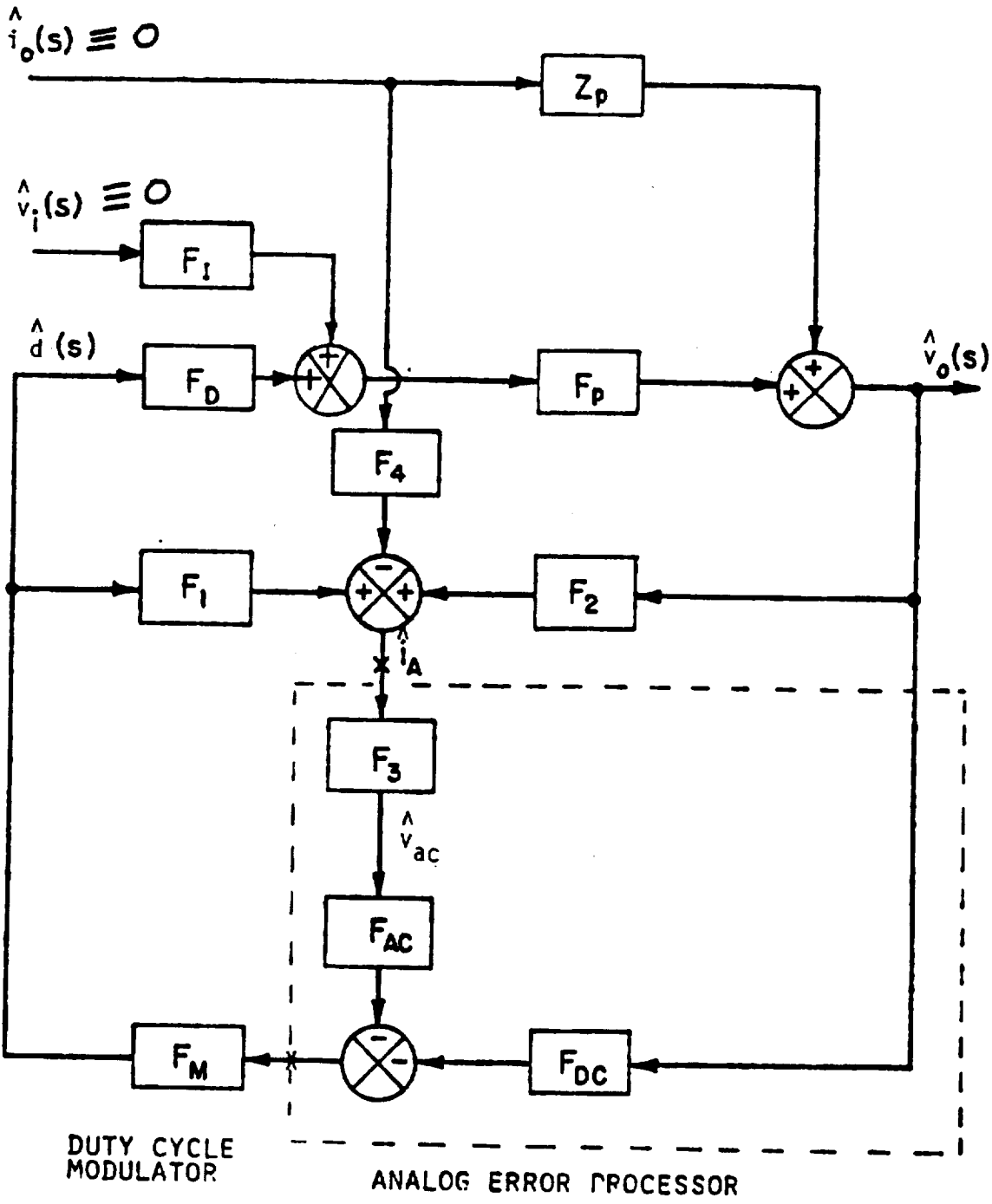


FIG. 9.1 OPEN LOOP GAIN.

Equation (9-2) can be simplified as follows:

$$G_T(s) = \frac{F_M F_D}{C_1 R_y} \frac{\frac{1}{\alpha} (R_L + R_C) LCs^2 + \left(\frac{L}{\alpha} + R_L R_C C\right) s + R_L}{(R_L + R_C) LCs^2 + [L + R_L R_C C + R_\ell (R_L + R_C) C] s + R_L + R_\ell} \quad (9-3)$$

if  $\alpha = 1$

$$G_T(s) = \frac{F_M F_D}{s C_1 R_y} \frac{(R_L + R_C) LCs^2 + (L + R_L R_C C) s + R_L}{(R_L + R_C) LCs^2 + [L + R_L R_C C + R_\ell (R_L + R_C) C] s + R_L + R_\ell} \quad (9-4)$$

The above equation can be further simplified by assuming  $R_L \gg R_\ell$  and  $R_L \gg R_C$

$$G_T(s) = \frac{F_M F_D}{s C_1 R_y} \frac{LCs^2 + \left(\frac{L}{R_L} + R_C C\right) s + 1}{LCs^2 + \left[\frac{L}{R_L} + R_C C + R_\ell C\right] s + 1} \quad (9-5)$$

Examining (9-5) it is obvious that the complex pole in the denominator is provided by the low-pass filter in the power stage and the complex zero is provided by the two feedback loops. The control parameters, namely the dc loop resistance  $R_y$ , the ac loop resistance  $R_4$ , and the turn-ratio  $n$  of the ac loop sensing transformer, can be designed such that  $\alpha = 1$ . When this condition is met, the numerator and denominator of (9-5) are almost identical except for a slightly lower damping constant in the numerator. To get a qualitative understanding of the open-loop transfer characteristic, one can assume that  $R_\ell C \ll \frac{L}{R_L} + R_C C$ . The effect of  $R_\ell C$  term will be discussed later. Under this assumption (9-5) can be simplified as shown in the following equation:

$$G_T(s) = \frac{F_M F_D}{s C_1 R_y} \quad (9-6)$$

It is interesting to note that the two loop implementation can indeed provide a pole-zero cancellation so that the open-loop transfer function is independent of the output filter parameters. The open-loop transfer function expressed in (9-6) is only of first order. It produces a phase lag at most of  $90^\circ$  (assuming the transport lag and phase delay due to the pulse modulator are negligible). It is obvious that the stability problem is minimized. The adaptive nature of the control loops is clearly demonstrated in (9-5). When the output filter parameters are subjected to changes due perhaps to component tolerance, aging, or temperature variations, the complex zeros imitate the change of the complex poles and thus preserve the pole-zero cancellation. It is also of interest to note that when a load of capacitive nature is applied to a single-loop control system it often causes degradation of converter performance and sometimes even causes a stable system to become an unstable one. (To illustrate the effect of a capacitive load, one can visualize that when such a load is applied to a converter the filter characteristic of the converter is varied. As a result, a previously well compensated control loop tailored to a particular filter configuration and parameter values may become inadequate to handle the filter change due to the added capacitive load.) However, employing the two-loop control, the pole-zero cancellation of  $G_T(s)$  still holds true even when such a capacitive load is applied.

The open-loop transfer function can be expressed in terms of known circuit parameters of the buck converter by substituting

$$F_D = V_I$$

and

$$F_M = \frac{2R_4 C_1}{n} \frac{1}{M} \tag{9-7}$$

where  $M$  is determined by the particular duty cycle control method given in Table 7.1. For example,  $M = (V_I - 2V_O)T_P$  for constant frequency duty cycle control.

$$G_T(s) = \frac{R_4}{nR_y} \frac{2C_1 V_I}{M} \frac{1}{sC_1}$$

$$= \frac{2V_I}{M} \frac{1}{s} \quad (9-8)$$

The open-loop transfer function has a slope of -6 db/octave and a gain determined by  $2V_I/M$ . For constant frequency control, such gain is determined by the input voltage, output voltage, and the frequency of operation. The higher the switching frequency, the higher the gain. However, if the switching frequency is fixed, the loop transfer characteristic is also fixed, independent of control circuit parameters.

The effect of the  $R_\ell C$  term in the denominator of (9-5) is examined as follows:

$$\text{Let } Z(s) = LCs^2 + \left(\frac{L}{R_L} + R_C C\right)s + 1$$

$$\text{and } P(s) = LCs^2 + \left(\frac{L}{R_L} + R_C C + R_\ell C\right)s + 1$$

Substituting  $s = j\omega$  into the above two equations, one obtains

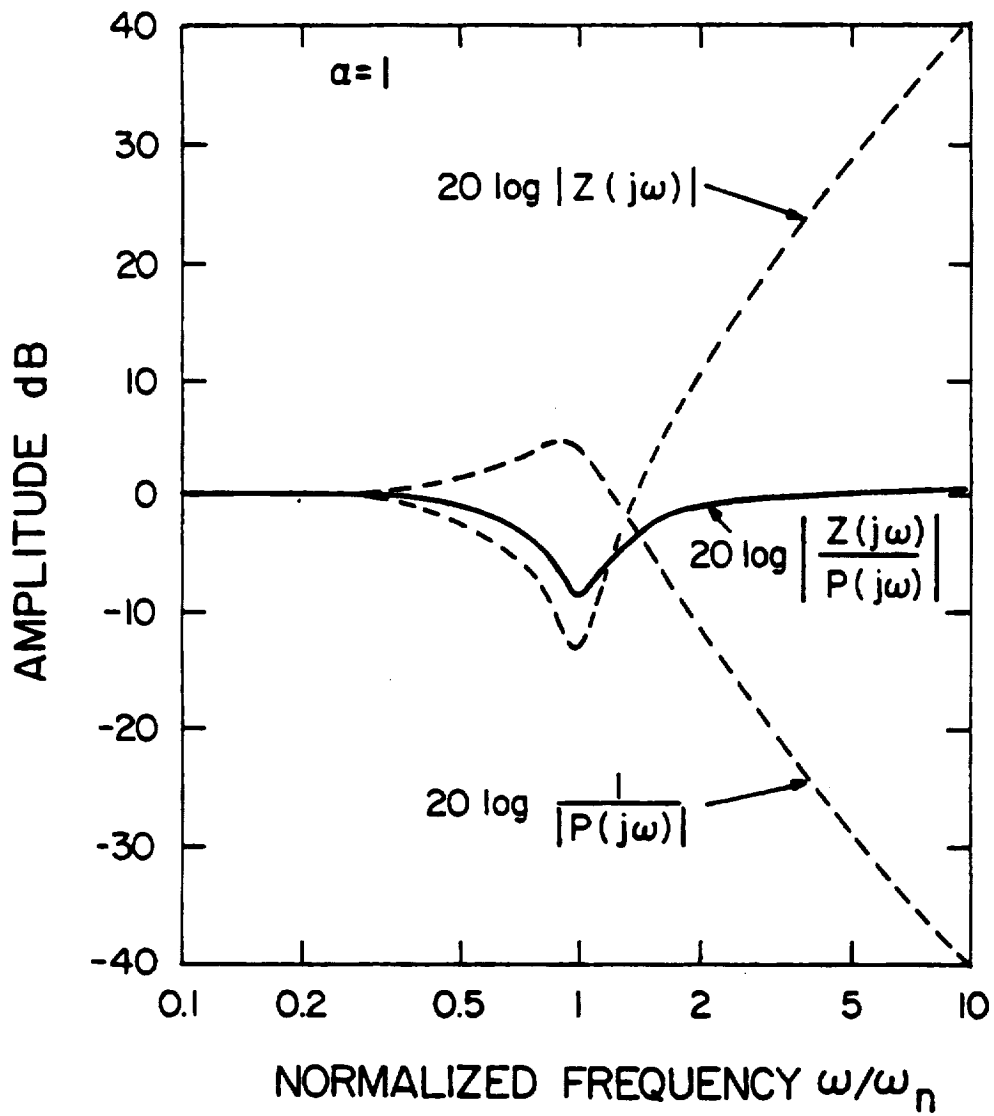
$$Z(j\omega) = 1 + j2\zeta_1 \omega/\omega_n - \omega^2/\omega_n^2 \quad (9-9)$$

$$P(j\omega) = 1 + j2\zeta_2 \omega/\omega_n - \omega^2/\omega_n^2 \quad (9-10)$$

$$\text{where } \omega_n = \frac{1}{\sqrt{LC}}, \quad \zeta_1 = \frac{\omega_n}{2} \left(\frac{L}{R_L} + R_C C\right) \quad (9-11)$$

$$\text{and } \zeta_2 = \frac{\omega_n}{2} \left(\frac{L}{R_L} + R_C C + R_\ell C\right)$$

Figure (9-2)(a) and (b) show the gain and phase of  $Z(j\omega)/P(j\omega)$  as well as



(a)

FIG. 9.2 BODE DIAGRAM OF  $P(j\omega)$  AND  $Z(j\omega)$  (a) GAIN

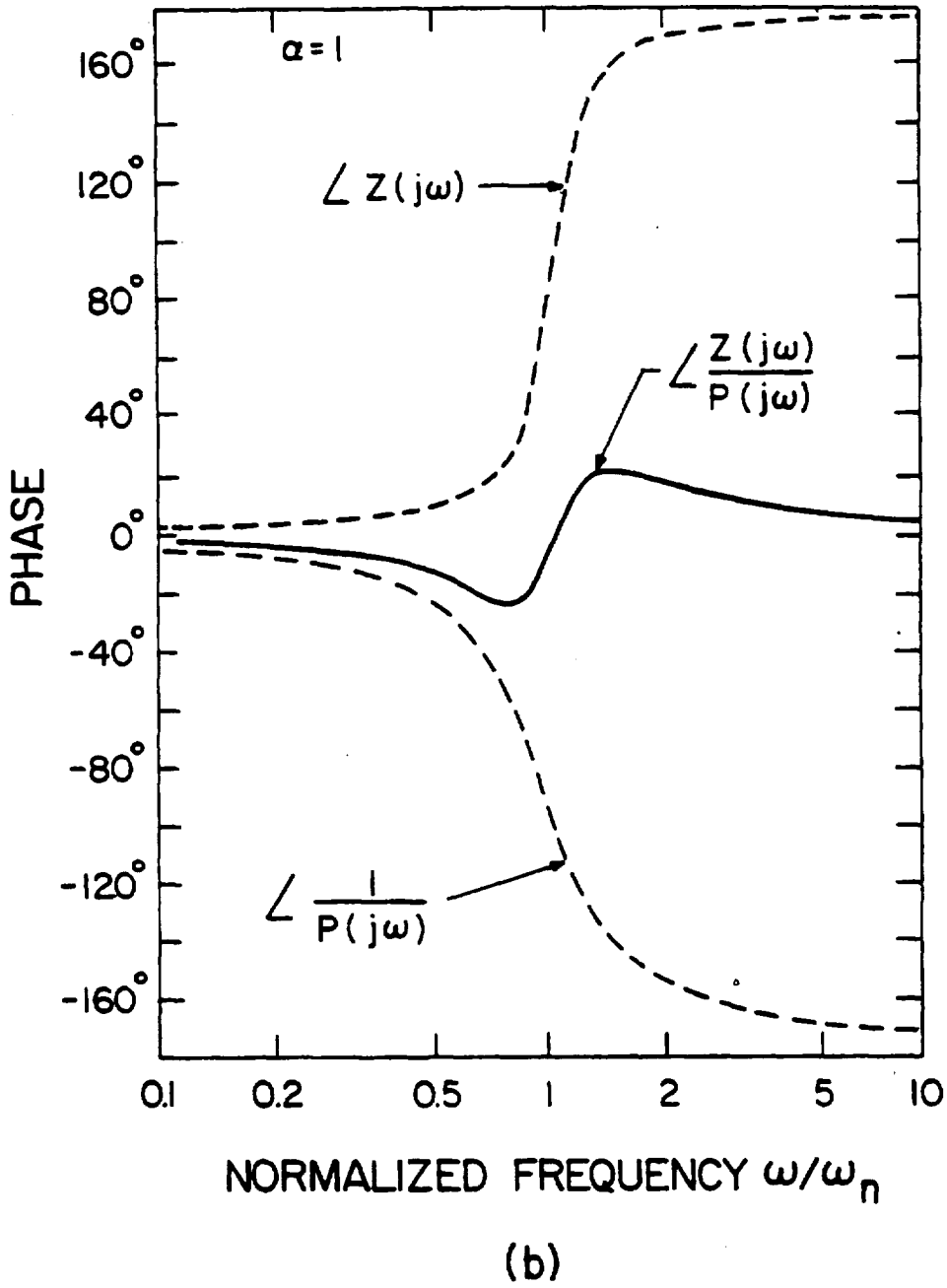


FIG. 9.2 BODE DIAGRAM OF  $P(j\omega)$  AND  $Z(j\omega)$  (b) PHASE

each individual term  $Z(j\omega)$  and  $1/P(j\omega)$ . It is interesting to note that the second-order pole  $P(j\omega)$  associated with LC filter of the power stage is almost cancelled entirely by the complex zeros provided by the feedback control loops. The effect of different damping ratios  $\zeta_1$  and  $\zeta_2$  is to cause disturbances of gain and phase of  $Z(j\omega)/P(j\omega)$  only near the resonant frequency. In this example,  $\zeta_1 = 0.1$  and  $\zeta_2 = 0.3$ .

A test circuit is built to verify the analysis. The following circuit parameter values are employed:  $R_L = 10$  ohms,  $R_x = R_C = 0.2$  ohm,  $C = 300$   $\mu$ F,  $L = 230$   $\mu$ H,  $V_I = 50$  volts,  $V_0 = 20$  volts,  $\alpha = 1$ . A constant  $T_{ON}$  duty cycle control is employed with  $T_{ON} = 17.6$   $\mu$ sec. For constant  $T_{ON}$  control the expression for  $M$  as defined in Table 7.1 is equal to  $V_I T_{ON} = 0.88 \times 10^{-3}$  V-sec. The switching frequency is 22 KHz. The open loop gain and phase measurements are conducted by injecting a sinusoidal voltage source  $v_x$  in series with the integrator output signal as illustrated in Fig. 9-3. The open loop gain and phase at any specific modulation frequency are measured by comparing the signals  $\hat{v}_y$  and  $\hat{v}_t$  which are respectively the modulation components of the voltage  $v_Y$  and  $v_T$  as shown in Figure 9-3.

$$\text{open loop gain} = \frac{\text{amplitude of } \hat{v}_y(\omega)}{\text{amplitude } \hat{v}_t(\omega)} \quad (9-12)$$

$$\text{open loop phase} = \angle \hat{v}_y(\omega) - \angle \hat{v}_t(\omega)$$

The open loop gain and phase margin are plotted in Fig. 9-4. Good agreements are shown between measurements and analytical predictions. Excessive measured phase delay in the high frequency range is due to the phase delay of the duty cycle modulator which is neglected in the analysis. The crossover frequency is about 11 KHz with a phase margin of 70°. Figure 9-5 shows the Bode plot of the open loop characteristic when  $\alpha = 0.355$ . Larger variation of gain and phase characteristics at the filter resonant frequency are shown. However, the crossover frequency and phase margin



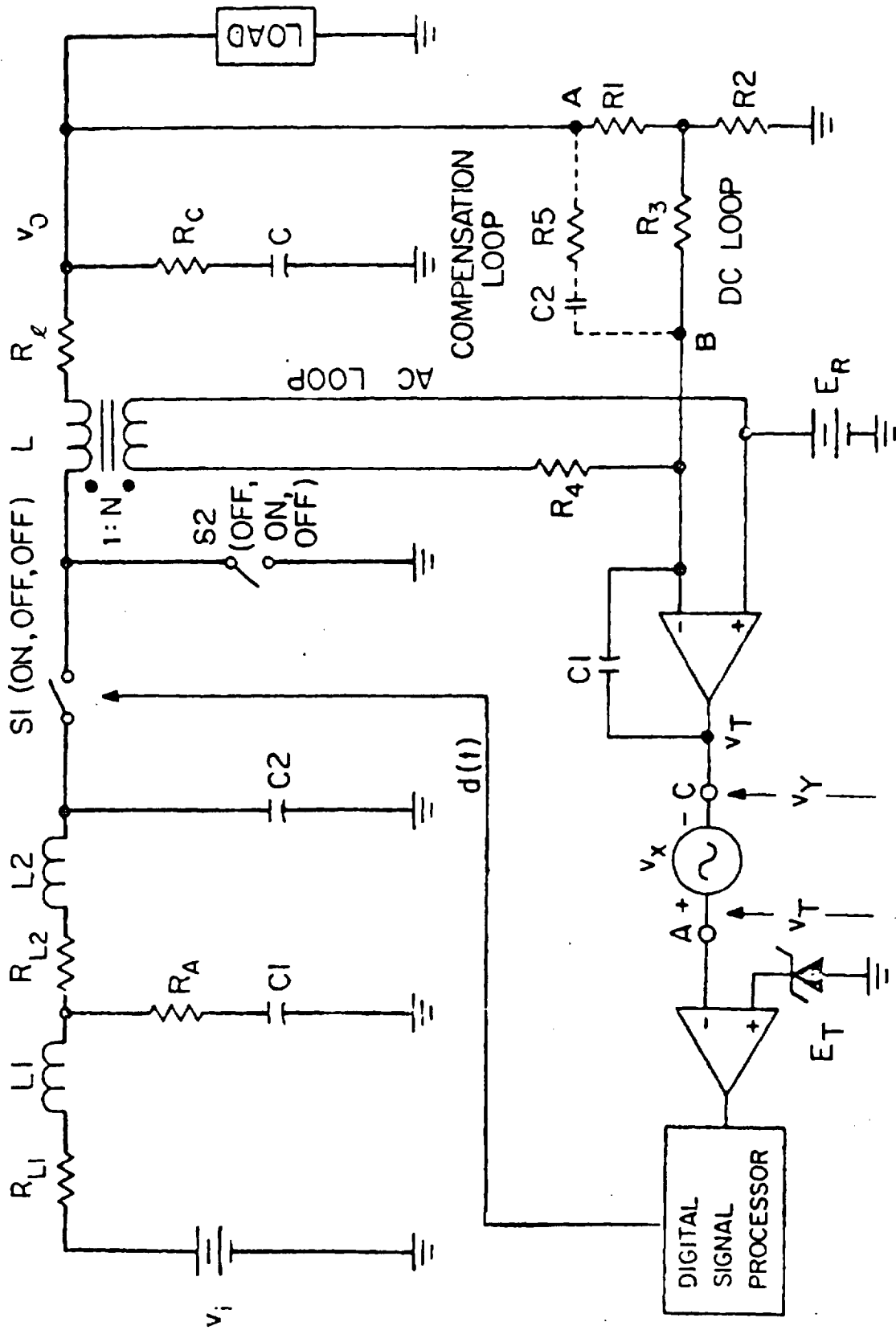


FIG. 9.3 OPEN LOOP GAIN AND PHASE MEASUREMENT

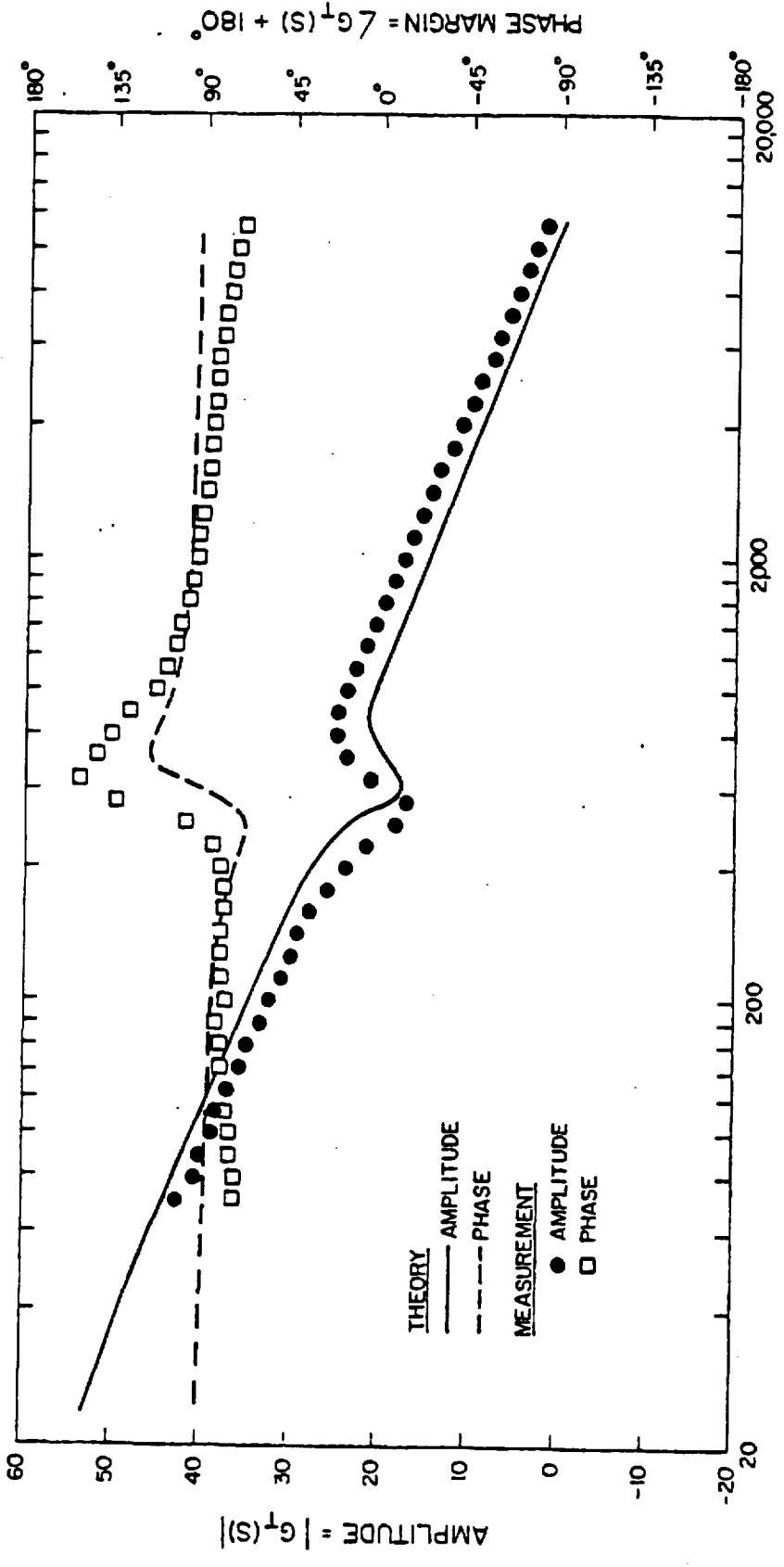


FIG. 9.4 OPEN LOOP GAIN AND PHASE OF A SCM-CONTROLLED BUCK REGULATOR ( $\alpha=1$ )

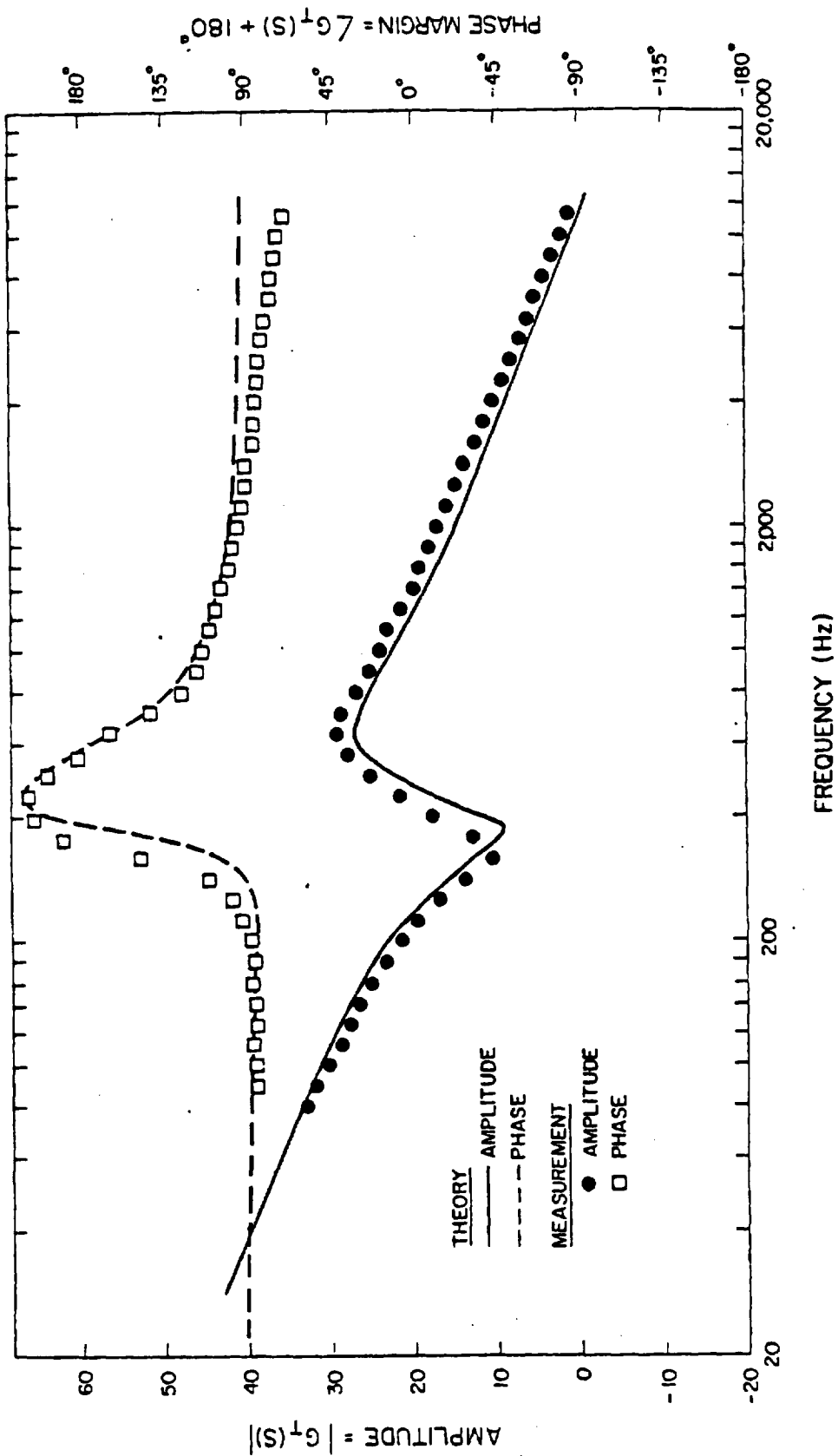


FIG. 9.5 OPEN LOOP GAIN AND PHASE OF A SCM-CONTROLLER BUCK REGULATOR ( $\alpha=0.355$ )

remain almost the same values as the previous case when  $\alpha = 1$ .

## 9.2 Other Small Signal Performance Characteristics

Small signal performance characteristics of a switching regulator can be summarized into the following three categories:

- 1) Stability: concerned with sinusoidal disturbance in the control loop.
- 2) Audio susceptibility: concerned with sinusoidal disturbance at the input line.
- 3) Output impedance: concerned with sinusoidal disturbance at the converter output.

While the loop stability has been discussed rather extensively in the previous sections, audiosusceptibility and output impedance will be discussed in the sections that follow.

### 9.2.1 Audiosusceptibility

The audiosusceptibility is defined as the closed loop input-to-output transfer function  $G_A(s)$ . It is employed to measure the attenuation of a sinusoidal disturbance from the input line to the regulator output. It can be proved using the block diagram representation in Fig. 8.2 that for the buck converter

$$G_A(s) = \frac{F_I(s)F_p(s)}{1 + G_T(s)} \quad (9-13)$$

where  $G_T(s)$  is the open loop transfer function defined in equation (8.1) and  $F_I(s)$  and  $F_p(s)$  are given in Table 8.1.

Figure 9.6 presents the closed loop input-to-output transfer function of two different conditions. The solid curve corresponds to  $\alpha = 1$  and the dashed curve for  $\alpha = 0.355$ . The excessive peaking which occurs at the output filter resonant frequency is caused by the second-order complex zeros of  $G_T(s)$ .

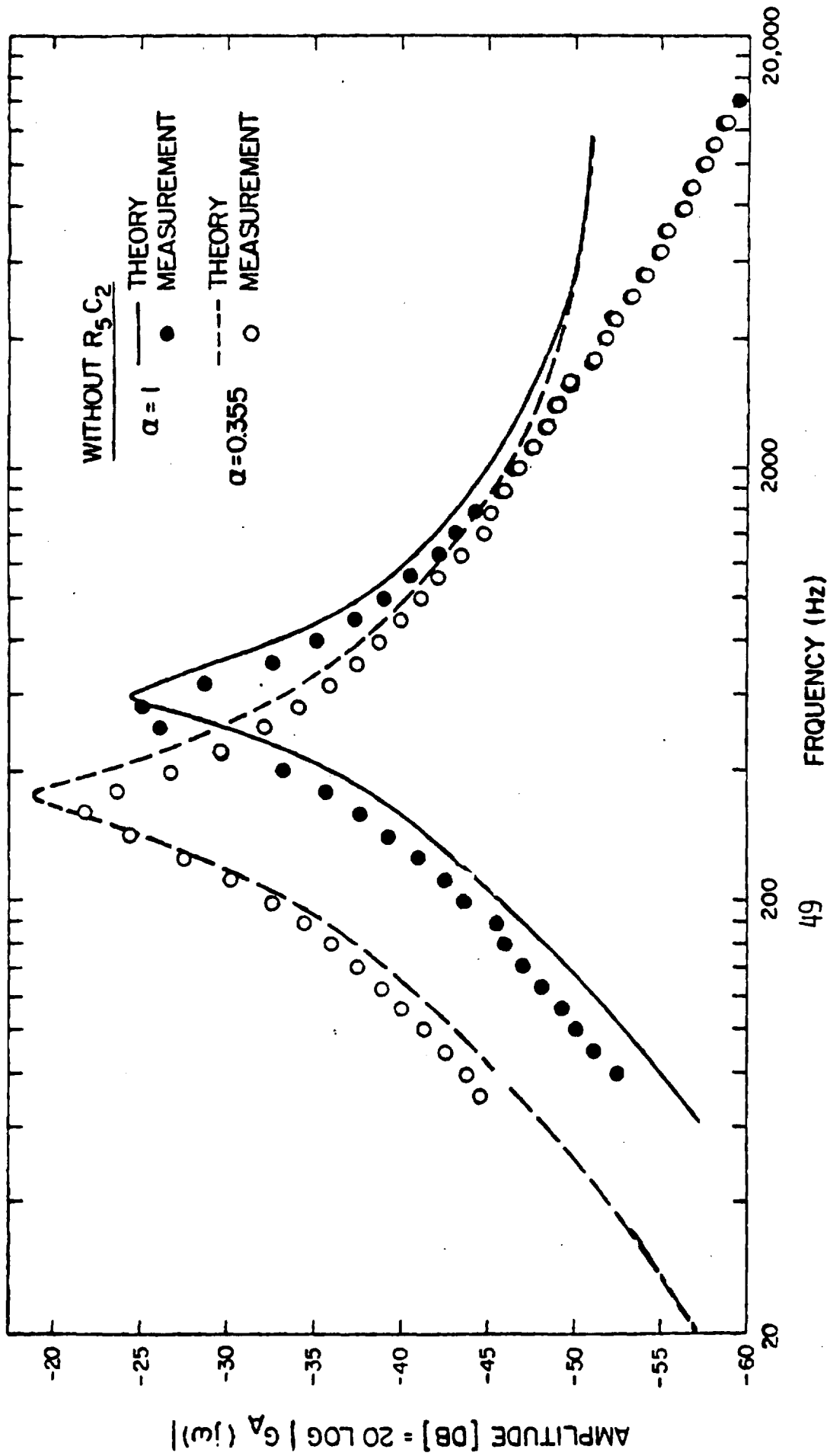


FIG. 9.6 AUDIOSUSCEPTIBILITY OF A SCM-CONTROLLER BUCK REGULATOR

This conclusion can be demonstrated analytically if one assumes that  $|G_T(s)| \gg 1$  in the frequency range considerably less than the open loop cross-over frequency. Using these assumptions, equation (9-13) can be simplified to read:

$$G_A(s) = \frac{DMs}{2V_I} \cdot \frac{(R_C Cs + 1)}{\frac{LCs^2}{\alpha} + \left(\frac{L}{\alpha R_L} + R_C C\right)s + 1} \quad (9-14)$$

The peaking of the audiosusceptibility curve in figure 9-6 is caused by the complex poles of  $G_A(s)$ . Examination of the denominator of eq. 9-14 will show that the complex poles of this simplified form of  $G_A(s)$  are the same as the complex zeros of the open loop transfer function  $G_T(s)$ , a simplified form of which is given in eq. 9-5 for the special case  $\alpha = 1$ . Hence the conclusion that the peaking of  $G_A(s)$  is caused by the complex zeros of  $G_T(s)$ .

### 9.2.2 Output Impedance

Consider a small signal sinusoidal load disturbance represented by a current source  $\hat{i}_o(s)$  placed in parallel with  $R_L$ .

The output impedance of the buck regulator can be expressed as

$$Z_o(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{Z_p(s) + F_D(s)F_p(s)F_3(s)F_4(s)F_{AC}(s)F_M}{1 + G_T(s)} \quad (9-15)$$

where  $\hat{v}_o(s)$  is the disturbance in output voltage caused by the source  $\hat{i}_o(s)$ .

Figure 9-7 illustrates two output impedance characteristics corresponding to two adaptive parameter values  $\alpha = 1$  and  $\alpha = 0.355$ . It is interesting to compare Fig. 9.7 with Fig. 9.6. Both the audiosusceptibility and output impedance are shown to have similar characteristics. In fact if one assumes  $|G_T(s)| \gg 1$  and  $R_L \gg R_C$  and  $R_L$  negligibly small, then (9-15) can be simplified to read:

$$Z_o(s) = \frac{Ls(R_L Cs + 1)}{\frac{LCs^2}{\alpha} + \left(\frac{L}{\alpha R_L} + R_C C\right)s + 1} \quad (9-16)$$

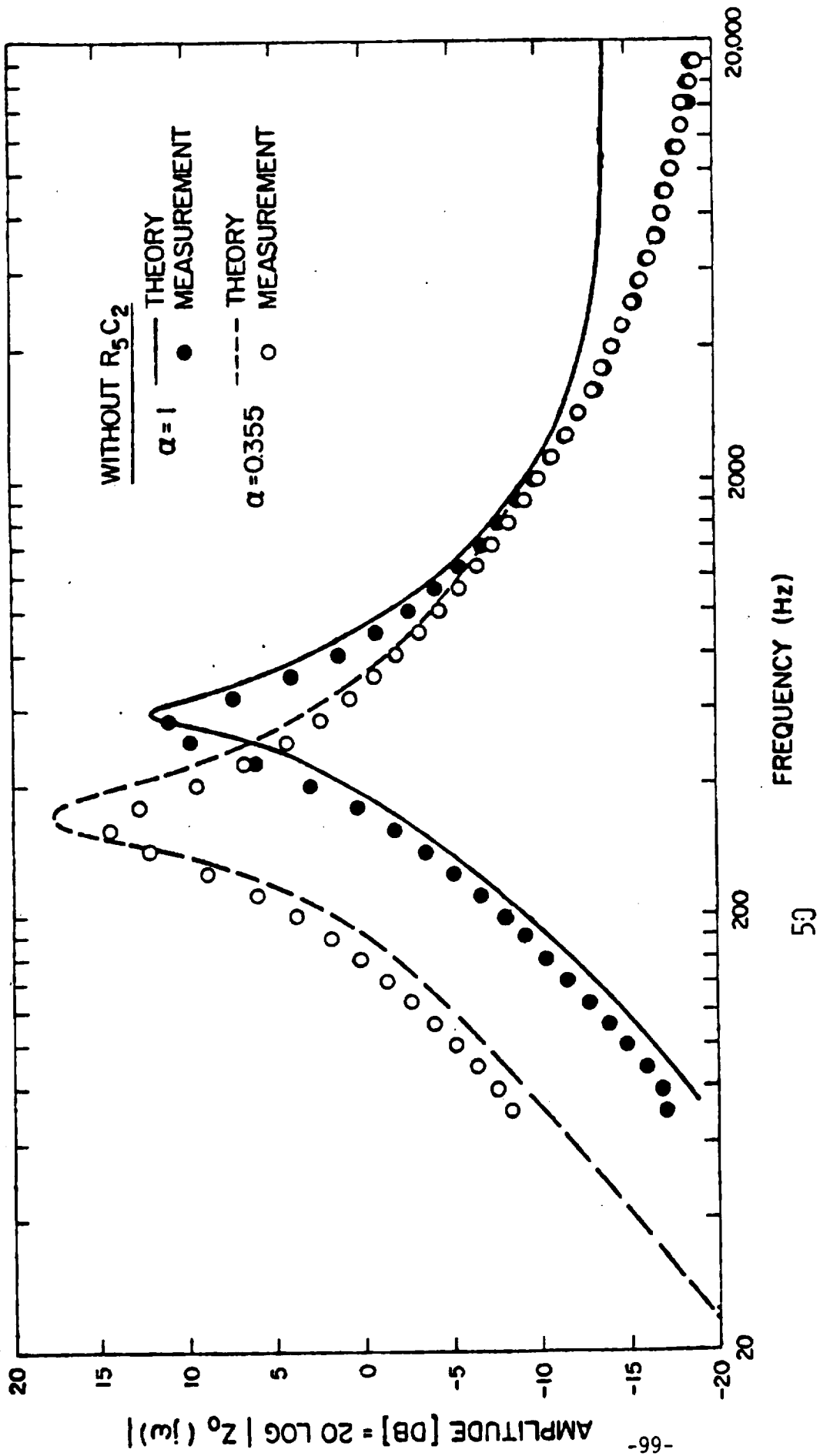


FIG. 9.7 OUTPUT IMPEDANCE CHARACTERISTIC OF A SCM-CONTROLLED BUCK REGULATOR

Equation (9-16) is very similar to equation (9-14), and can be used to interpret Fig. 9.7 in similar fashion to what was done earlier for Fig. 9.6.

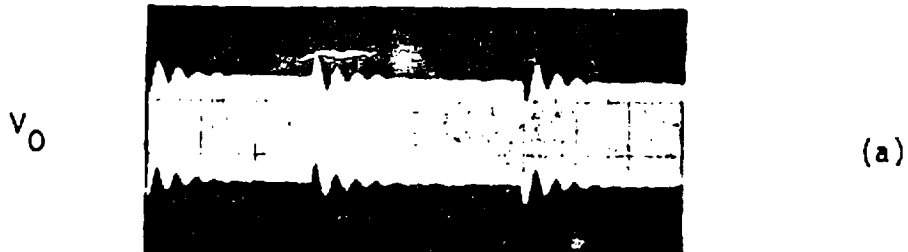
### 9.2.3 Output Transient Response

In linear systems, output impedance is often used to analyze transient response. In switching regulators, output impedance may be used the same way in certain circumstances. It may be shown that when a switching regulator is subjected to a small step-change of load, the output impedance characteristic with peaking will result in an oscillatory transient response, even though the output voltage level varies only slightly. Figure 9.8 shows two oscillograms of output voltage waveforms for a buck regulator subjected to a periodic step-change of load from 10 ohms to 11 ohms. The higher amplitude oscillation (Fig. 9.8 (b)) corresponds to the higher output impedance peaking. For this case,  $\alpha = 0.355$ .

Detailed analysis of the output transient response of a regulator using the output impedance characteristic will be discussed in chapter 12.

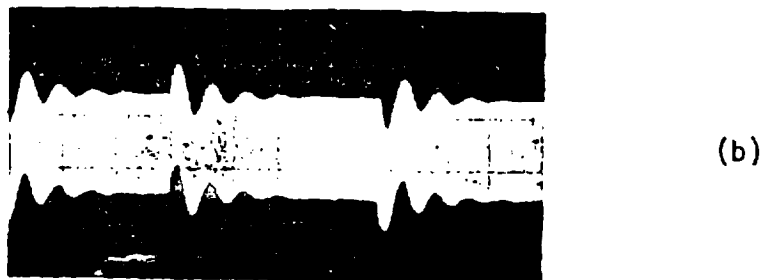


(1) WITHOUT COMPENSATION LOOP ( $\alpha = 1$ )



HORIZONTAL: 5 MS/DIV.  
VERTICAL: 0.1 V/DIV

(2) WITHOUT COMPENSATION LOOP ( $\alpha = 0.355$ )



HORIZONTAL: 5MS/DIV  
VERTIVAL: 0.1 V/DIV

FIG. 9.8 TRANSIENT RESPONSE DUE TO A STEP LOAD CHANGE  
( $R_L = 10$  OHMS TO 11 OHMS)

### 9.3 Discontinuous Inductor Current Operation

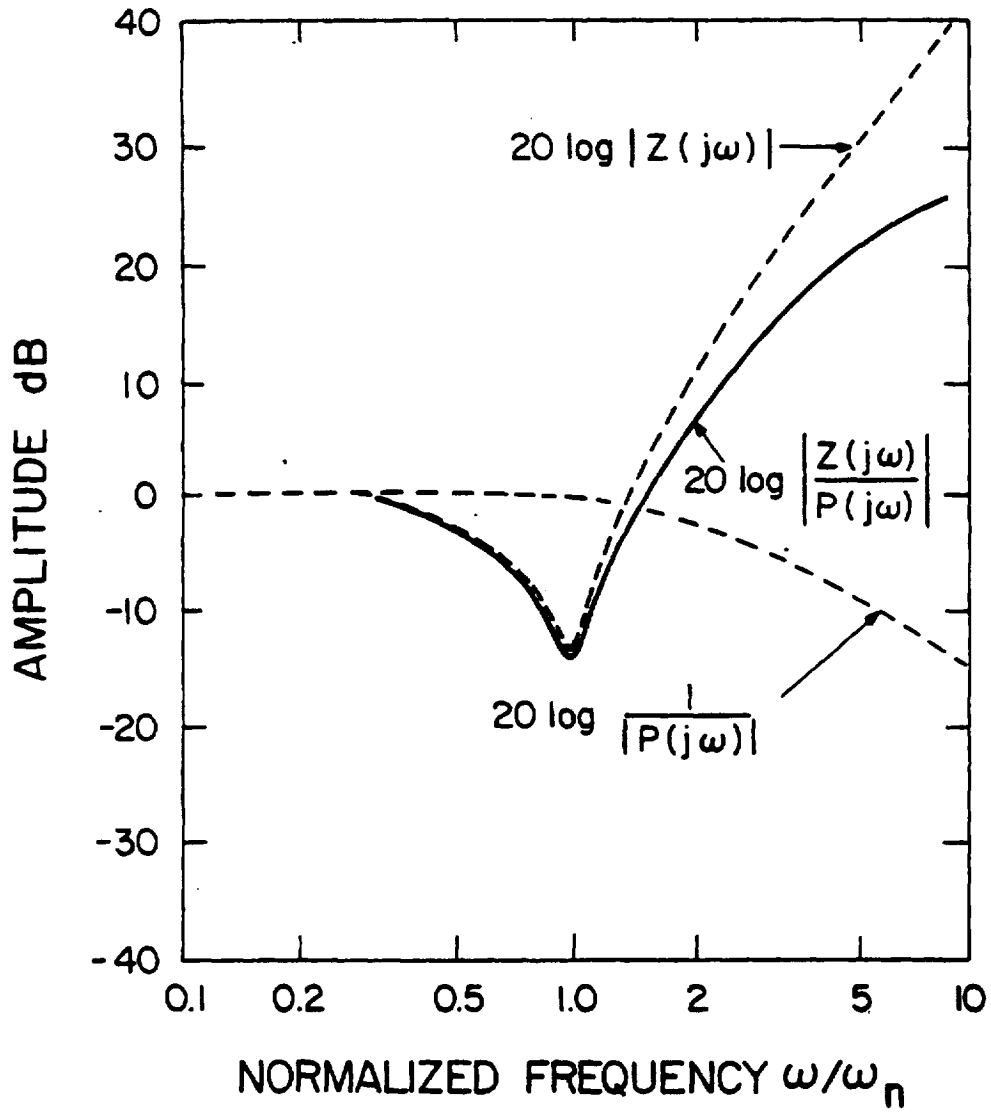
Referring to Chapter 14 for switching regulator model for discontinuous-current operation, the open-loop transfer function of the buck regulator is derived

$$G_T(s) = \frac{F_M}{\Delta R_y} \frac{2V_0}{\sqrt{K}} \frac{(1-M)^{3/2}}{M(2-M)} \frac{\frac{1}{\alpha} LCs^2 + (\frac{1}{\alpha} \frac{L}{R_L} + R_C C)s + 1}{(\frac{1-M}{2-M} R_L + R_C)Cs + 1} \quad (9-17)$$

It is clearly seen in (9-17) that when the converter is operated in discontinuous current mode, the power stage only produces a first-order pole. However, the complex zeros produced by the two feedback loops are still preserved in discontinuous current operation. The system is over compensated and, as a result, these complex zeros will present an adverse effect which is described as follows. Consider  $\alpha = 1$ . Then from eq. 9-17, the following equation is obtained:

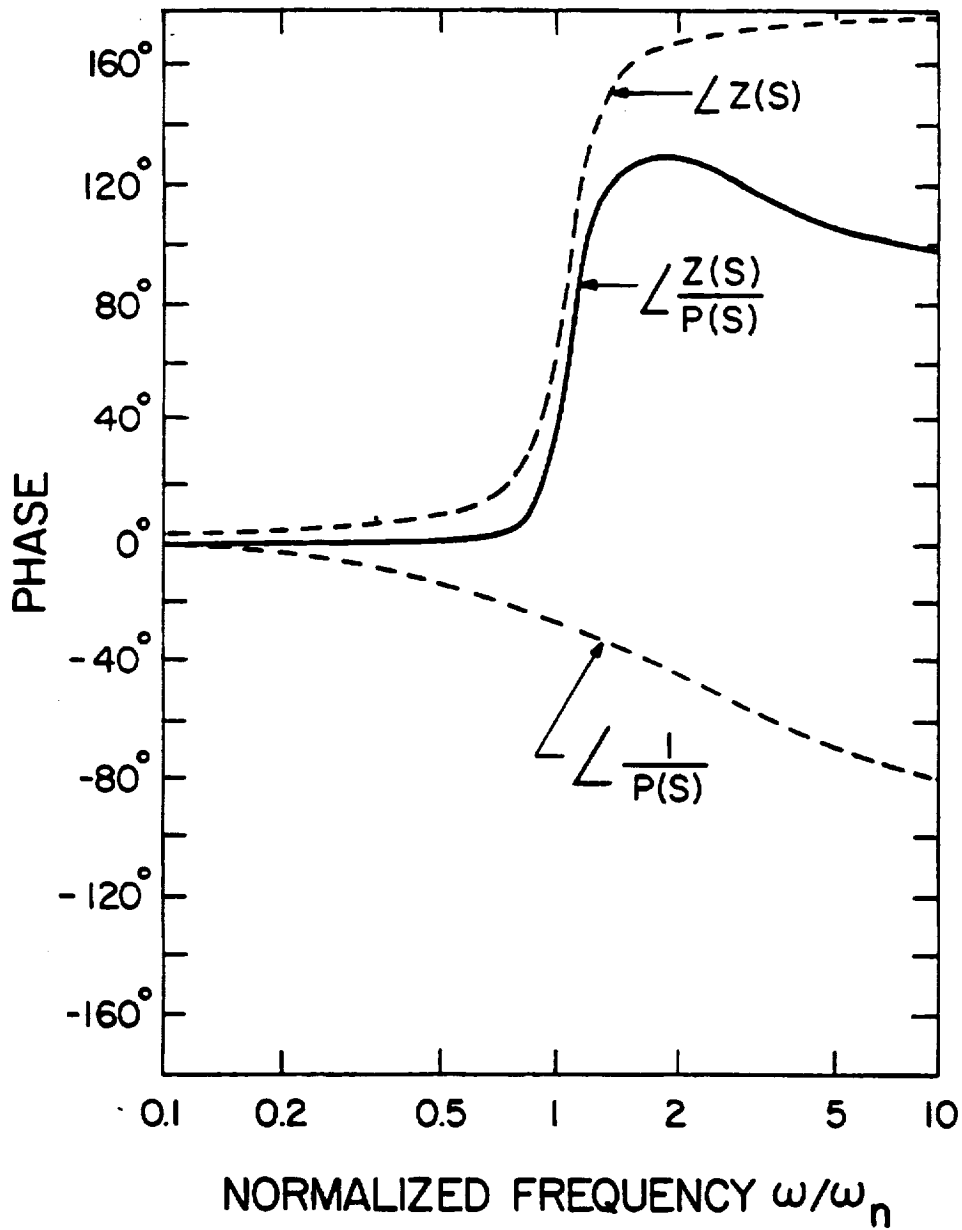
$$\frac{Z(s)}{P(s)} \triangleq \frac{LCs^2 + (\frac{L}{R_L} + R_C C)s + 1}{(\frac{1-M}{2-M} R_L + R_C)Cs + 1} \quad (9-18)$$

where  $Z(s)$  and  $P(s)$  are the polynomials containing the zeros and poles of  $G_T(s)$ . Since the pole of (9-18) varies with  $R_L$  (the converter lead), the case where the corner frequency of  $P(s)$  is twice as large as the corner frequency of  $Z(s)$  will be examined. Figures 9.9(a) and (b) show gain and phase plots. A significant reduction of the gain of  $Z(s)/P(s)$  is shown at the resonant frequency of the complex zeros. Such a gain reduction is inversely proportional to the damping ratio of the complex zeros. In this particular example, a damping ratio  $\zeta = 0.3$  is used. The sharp reduction of the gain of  $Z(s)/P(s)$  can result in severe deterioration of converter performance such as: highly oscillatory transient response and low audio signal rejection rate at the input of the converter; sometimes this reduction in gain can even



(a)

FIG. 9.9 BODE DIAGRAM OF  $P(j\omega)$  AND  $Z(j\omega)$  IN DISCONTINUOUS CURRENT OPERATION (a) GAIN



(b)

FIG. 9.9 BODE DIAGRAM OF  $P(j\omega)$  AND  $Z(j\omega)$  IN DISCONTINUOUS CURRENT OPERATION (b) PHASE.

result in converter instability.

Experimental verifications are provided employing a constant-frequency duty-cycle control where  $f = 25$  KHz. The converter is operated in discontinuous current under light load conditions, ( $R_L = 50$  ohms); other circuit parameters remain the same as in the previously tested circuit. The converter open-loop gain and phase margin are plotted in Fig. 9.10. Good correlations are shown between the measurement data and the analytical results. In the analysis, the time intervals  $T_{ON}$  and  $T_{F1}$  are calculated employing the following simplified equations.:

$$T_{ON} = \sqrt{\frac{2LT_P V_o^2}{R_L V_I (V_I - V_o)}}, \quad T_{F1} = \sqrt{\frac{2LT_P (V_I - V_o)}{R_L V_I}} \quad (9-19)$$

where the transistor drops, the diode drop and other distributed IR drops are neglected. Figure 9.10 shows the first crossover frequency occurring at 250 Hz as a result of a sharp loop gain reduction and the second crossover frequency occurring at about 10 KHz--a designed crossover frequency. The loop gain is very small between these two crossover frequencies. The converter is stable but provides very poor transient response and audio-susceptibility.

#### 9.4 Optimal Compensation

The two-loop control circuit analyzed in detail in the previous sections are shown to provide a second-order complex zero that cancels completely the complex poles produced by the LC filter of the converter. The control loops which produce the complex zeros are also shown to be adaptive to changes of the filter parameters of the converter power stage due to temperature variations or aging. Nevertheless, the two loop control

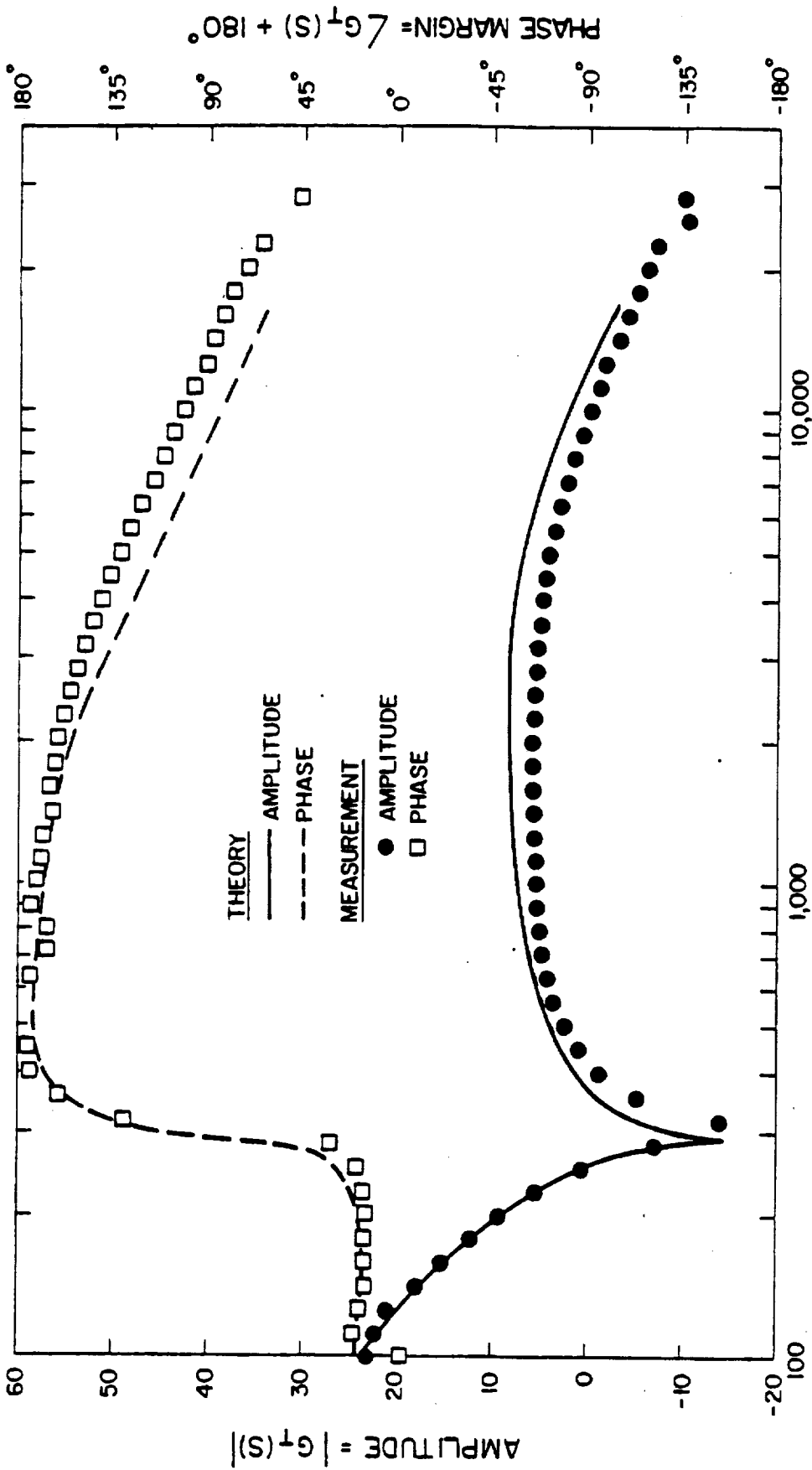


FIG. 9.10 OPEN LOOP GAIN AND PHASE FOR DISCONTINUOUS CURRENT OPERATION

scheme suffers the following dilemma:

- (A) For continuous current operation, the open-loops gain  $G_T(s) = 2V_I/Ms$  as shown in equation (9.8) is only a function of the input voltage and the type of duty cycle control chosen. For example, in the constant frequency operation,  $M = (V_I - 2V_O)T_P$ . The frequency has to be increased in order to get higher dc open-loop gain. For constant  $T_{ON}$  control,  $M = V_I T_{ON}$ , the smaller the  $T_{ON}$  interval, the larger the gain. The open loop gain is independent of other control-loop parameters. This open-loop gain is generally small and is inadequate to provide satisfactory transient response and audio susceptibility of the converter.
- (B) Due to the smaller damping ratio of the complex zeros compared to that of the complex poles, a reduction of the open-loop gain always exists. A severe reduction of loop gain can result if the two-loop control is not designed properly such that the resonant frequency of the complex zeros is not close or equal to the resonant frequency of the complex poles. ( $\alpha \neq 1$ )
- (C) For discontinuous current operation, the converter power stage only has a first order pole. The complex zeros provided by the two-loop control results in an adverse effect to the converter performances. A sharp reduction of the open-loop gain occurs at the resonant frequency of the complex zeros.

The aforescribed dilemma are inherent limitations of the particular two-loop control implementation. To improve the open loop characteristic, a third loop, a  $R_5C_2$  network, shown in Fig. 2.1, connected from the converter output to the op-amp integrator input, is proposed. The analysis of the proposed three-loop system is presented in the following.

The open loop transfer function of a converter with the  $R_5C_2$  network is presented below:

$$G_T(s) = \frac{F_M F_D}{s C_1 R_y} \frac{\frac{LCs^2}{\alpha} + \left[ (R_y + R_5) C_2 \frac{R_C Cs + 1}{R_5 C_2 s + 1} + \frac{L}{\alpha R_L} \right] s + \frac{R_C Cs + 1}{R_5 C_2 s + 1}}{LC s^2 + \left( \frac{L}{R_L} + R_\ell C + R_C C \right) s + 1} \quad (9-20)$$

This equation is too complex to provide immediate insight to the major effects of the  $R_5C_2$  network, but can be simplified considerably if one assumes

$$R_C Cs + 1 = R_5 C_2 s + 1 \quad (9-21)$$

This condition can be achieved in the design stage. In fact the effect of the term  $(R_C Cs + 1)/(R_5 C_2 s + 1)$  in the numerator of (9-20) is not significant if eq. (9-21) is not grossly violated. Detailed discussion is included in Volume II of the report. Using the above assumption together with the approximation  $\tau_{z2} \gg L/(\alpha R_L)$  Equation (9-20) is then simplified.

$$G_T(s) = \frac{F_M F_D}{s C_1 R_y} \frac{1}{\alpha} \frac{LC s^2 + \alpha \tau_{z2} s + \alpha}{LC s^2 + \left( \frac{L}{R_L} + R_\ell C + R_C C \right) s + 1} \quad (9-22)$$

$$\text{where } \tau_{z2} = (R_y + R_5) C_2$$

Figure 9.11(a) illustrates the locations of the poles and zeros of the open loop gain of equation (9-5) without the  $R_5C_2$  compensation loop. The complex zeros are adjacent to the complex poles but separated from the poles by a somewhat smaller damping ratio. When a  $R_5C_2$  compensation loop is added, the complex zeros can be reshaped as shown by the heavy lines in Figure 9-11(b) for increasing  $\tau_{z2}$ . It is interesting to note that the complete pole zero cancellation can be obtained as the locus of the complex zeros pass through the complex poles. Further increase of  $\tau_{z2}$  will eventually result to two real zeros. For reasons stated below and in the next few chapters, it is desirable to design the term  $(R_y + R_5)C_2$  so that



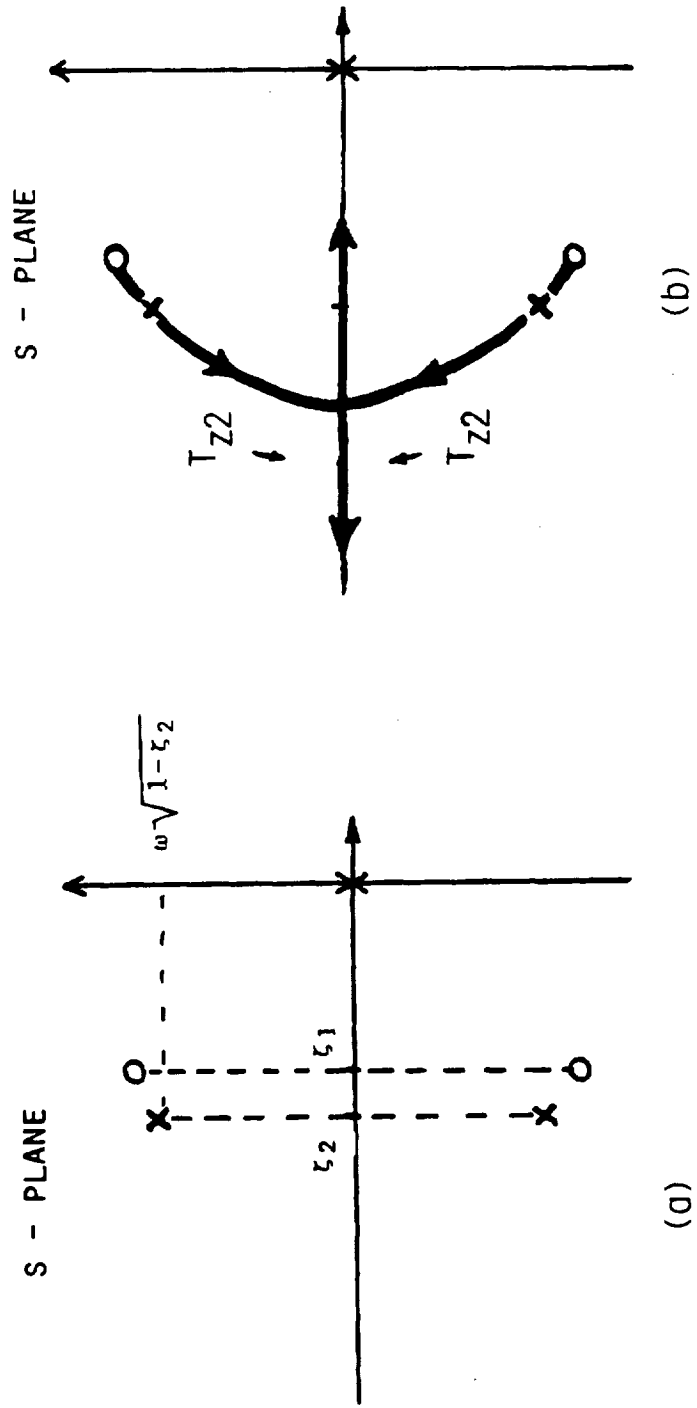


FIG. 9.11 OPEN LOOP POLES AND ZEROS (a) WITHOUT COMPENSATION LOOP (b) WITH COMPENSATION LOOP ( $\alpha=1$  AND INCREASING  $\tau_{z2}$ ). IT IS SHOWN IN FIGURE 9.11(b) THAT ZEROS MOVE BUT POLES REMAIN STATIONARY AS  $\tau_{z2}$  INCREASES.

the second-order terms in the numerator can no longer produce complex zeros but two negative real zeros.

Equation (9-22) can be simplified using the following notations

$$G_T(s) = \frac{K_1}{s} \frac{(s + s_{o1})(s + s_{o2})}{(s^2 + 2\zeta_2\omega_n s + \omega_n^2)} \quad (9-23)$$

where  $K_1 = \frac{2V_I}{M}$ ,  $\omega_n$  and  $\zeta_2$  are defined in equation (9-11), and

$$s_{o1} = \frac{1}{2LC} \{a\tau_{z2} + [(a\tau_{z2})^2 - 4\alpha LC]^{1/2}\} \quad (9-24)$$

$$s_{o2} = \frac{1}{2LC} \{a\tau_{z2} - [(a\tau_{z2})^2 - 4\alpha LC]^{1/2}\}$$

It is shown in (9-24) that the magnitude of the two zeros can be arbitrarily selected by varying the control loop parameters. Figure 9.12 shows the asymptotic curves of the open-loop gain as a function of the control parameter  $s_{o1}$  for a arbitrarily chosen  $s_{o2} = \frac{1}{5} \omega_n$ . The dotted line represents the open loop gain without the third loop and with  $\alpha$  equal to unity. Bear in mind that the objective of the third loop is to improve converter performances by increasing the open-loop gain in the particular frequency range of interest. It is clearly shown in Fig. 9.12 that larger gain can be obtained by employing  $s_{o1} = 10 \omega_n$ . For  $s_{o1} = \omega_n$ , the loop gain is less in the low frequency range than that shown as the dotted curve when only two feedback loops were employed.

Figure 9.13 provides experimental verification of the three loop system. The converter is operated at a condition same as that shown in Fig. 9.5 except a third loop is employed with  $R_5 = 500$  ohms,  $C_2 = 0.01 \mu\text{F}$ .

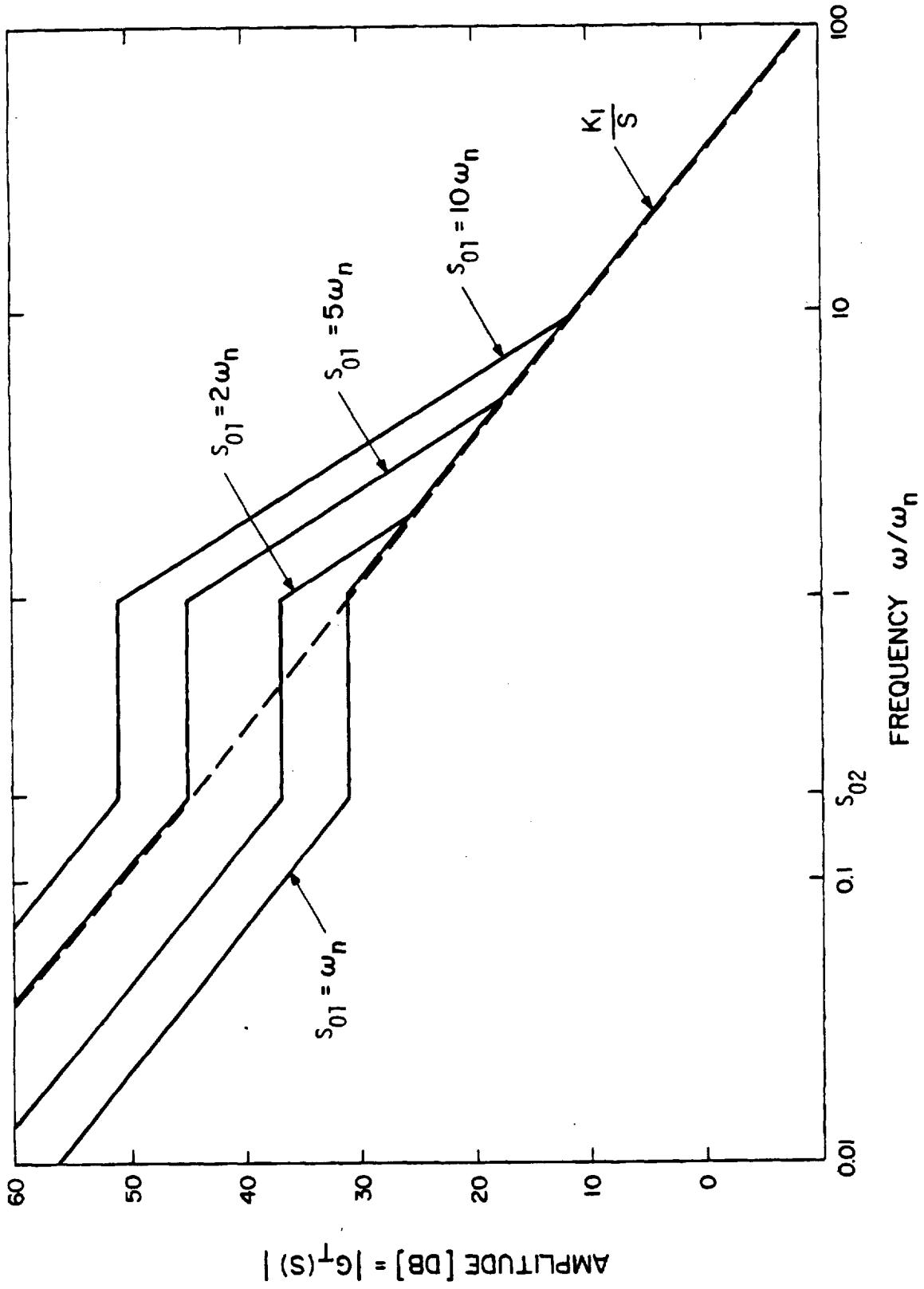


FIG. 9.12 OPEN LOOP TRANSFER FUNCTION FOR DIFFERENT VALUES OF THE ZERO  $s_{01}$

Comparing Fig. 9.13 with Fig. 9.5, it is shown that the RC loop has eliminated the loop gain reduction which otherwise results from unmatched resonant frequency and damping ratio of the complex poles and zeros of the two-loop system.

Figure 9.14 shows the open-loop transfer function of the three-loop system at a discontinuous operating condition same as that shown in Fig. 9.10. The advantage of the  $R_5C_2$  loop has been clearly demonstrated in the above illustration. The  $R_5C_2$  loop not only improves the converter performance by means of increasing the converter open-loop gain for continuous current operation, it also eliminates the adverse effect for discontinuous current operation shown as a sharp reduction of the loop gain at the resonant frequency of the complex zeros in Fig. 9.10. From the control point of view, such a RC loop is often referred to as a velocity control or rate control because it senses the change of the output voltage. Therefore, the improvement of converter load-transient response is expected. Another important aspect of the three-loop system is that the open-loop crossover frequency is generally higher than the two-loop system and the phase margin is sufficiently large as shown in the previous results. Therefore the control-loop dependent performances of the converter are optimized.

Improvement of other regulator performance characteristics such as audiosusceptibility, output impedance and transient response employing the third loop are also illustrated in the following.

Figure 9.15 shows the asymptotic curves of the audiosusceptibility characteristics. Since the two loop control provides complex poles in  $G_A(s)$ , a peaking effect is observed shown as the dotted curve of Fig. 9.15(a) and also illustrated in Fig. 9.6. Employing the  $R_5C_2$  loop the two complex poles of Eq. (9-13) are converted into two real poles as shown in Eq. (9-25) and illustrated

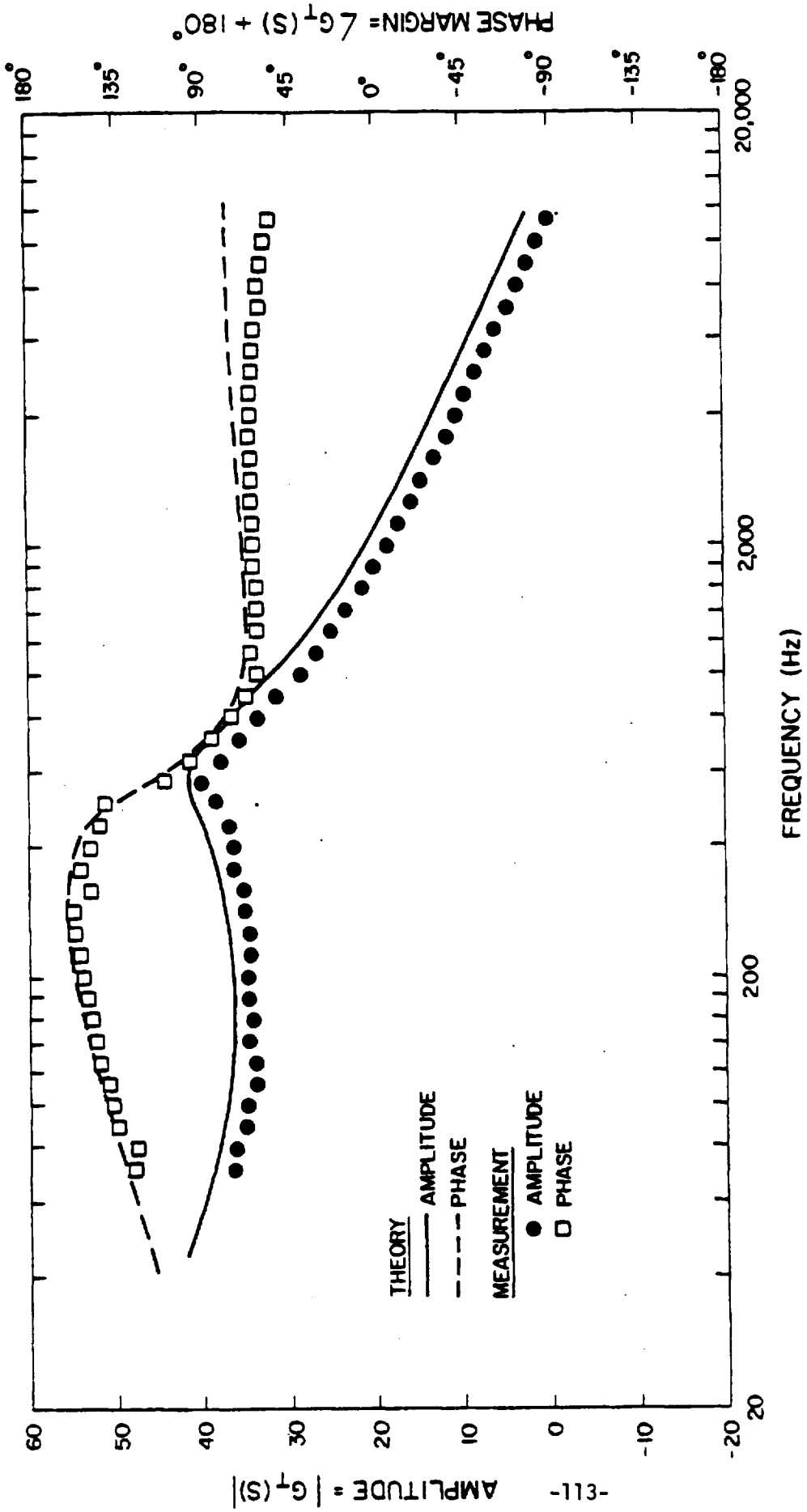


FIG. 9.13 OPEN LOOP CHARACTERISTIC WITH COMPENSATION LOOP - CONTINUOUS CURRENT OPERATION

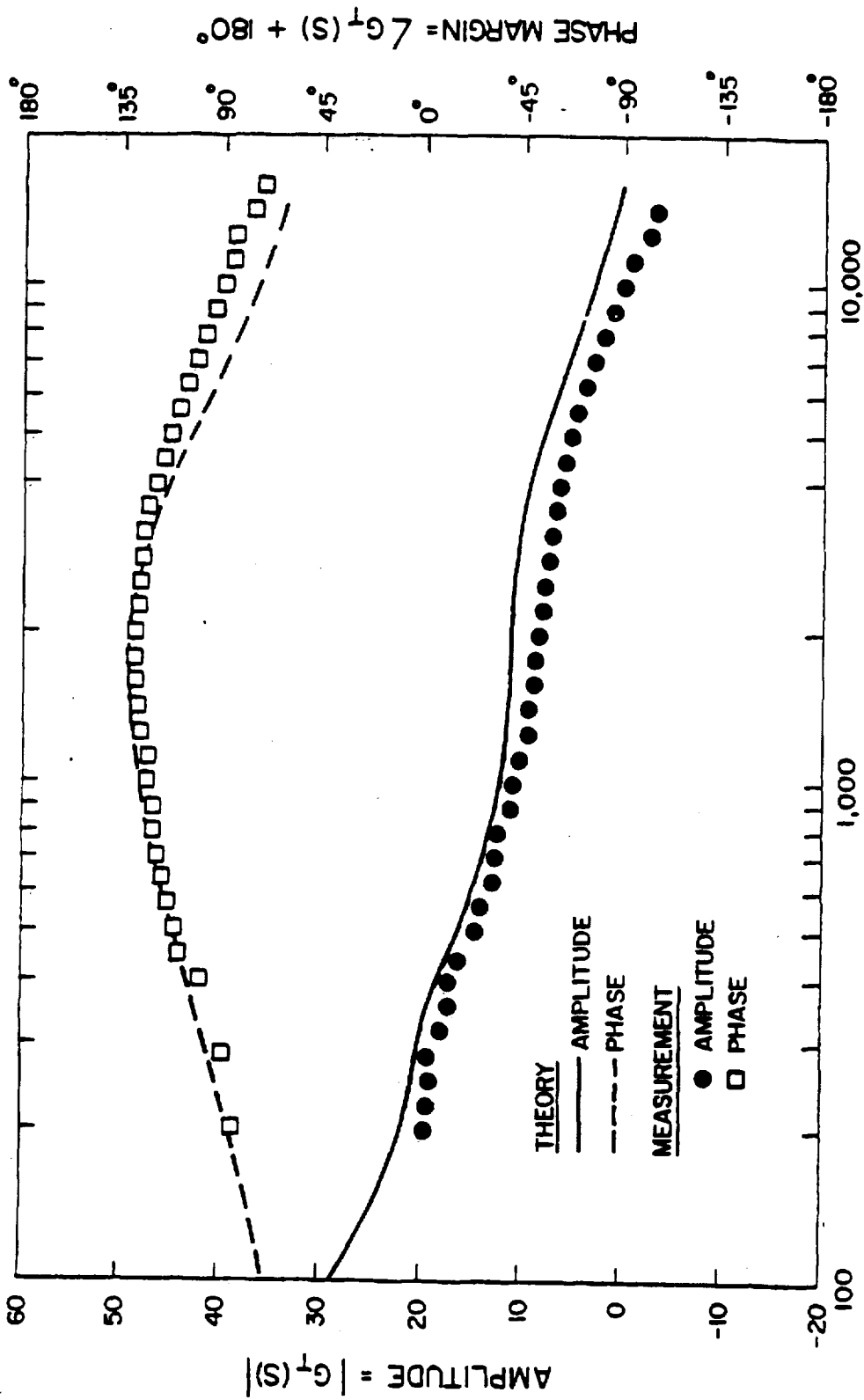


FIG. 9.14 OPEN LOOP CHARACTERISTIC WITH COMPENSATION LOOP - DISCONTINUOUS CURRENT

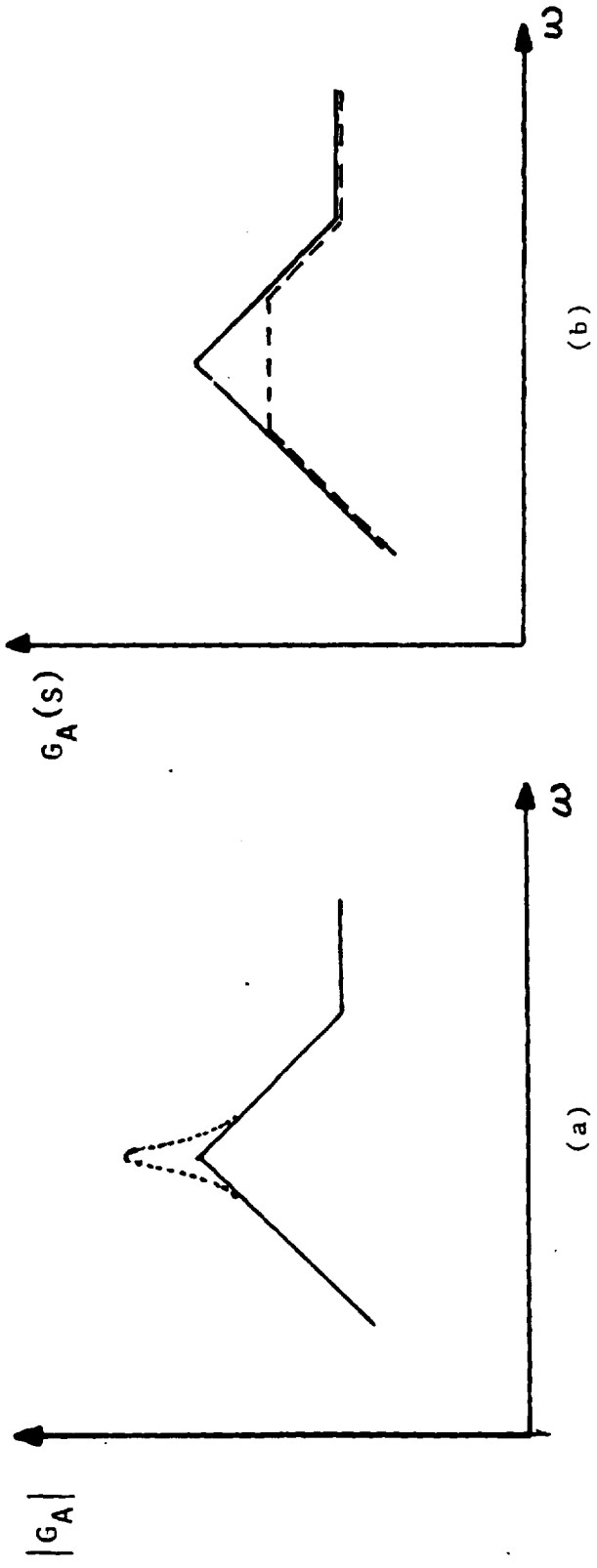


FIG. 9.15 AUDIO SUSCEPTIBILITY CHARACTERISTIC (a) WITHOUT THE COMPENSATION LOOP (b) WITH THE COMPENSATION LOOP.

in the dotted curve of Fig. 9.15(b).

$$G_A(s) = \frac{DMs}{2V_I\alpha} \frac{R_C Cs + 1}{\frac{LC}{\alpha} s^2 + \alpha\tau_{z2} s + 1} \quad (9-25)$$

Experimental measurement is presented together with the theoretical prediction of  $G_A(s)$  of (9-25) in Fig. 9.16 with parameter values same as that employed in measuring Fig. 9.13. The much improved characteristic is shown when compared with the two cases previously discussed.

The output impedance characteristic of the three-loop system is approximated by

$$Z_o(s) = \frac{Ls(R_C Cs + 1)}{\frac{LC}{\alpha} s^2 + \left(\frac{L}{\alpha R_L} + R_C C\right)s + 1} \quad (9-26)$$

The measurement results of the output impedance characteristic and the output transient response due to step load change are illustrated in Fig. 9.17 and 9.18. Significant improvement of these two performance characteristics are again demonstrated with the three-loop implementation.

### 9.5 Parameter Adaptation of the Three-Loop Control Regulator

Examining Eq. (9-5), one can conclude that an almost perfect parameter adaptation is achieved in the two loop control system. This adaptation can be illustrated by Fig. 9.19(a): as the two complex poles of  $G_T(s)$  are perturbed by the filter parameter changes, the two complex zeros track the motions of the poles the same amount. However, when the third loop is employed, the positions of the zeros change as a function of the control parameter  $\alpha\tau_{z2}$ . Pole-zero adaptation (tracking of zeros with respect to poles) can remain almost linear



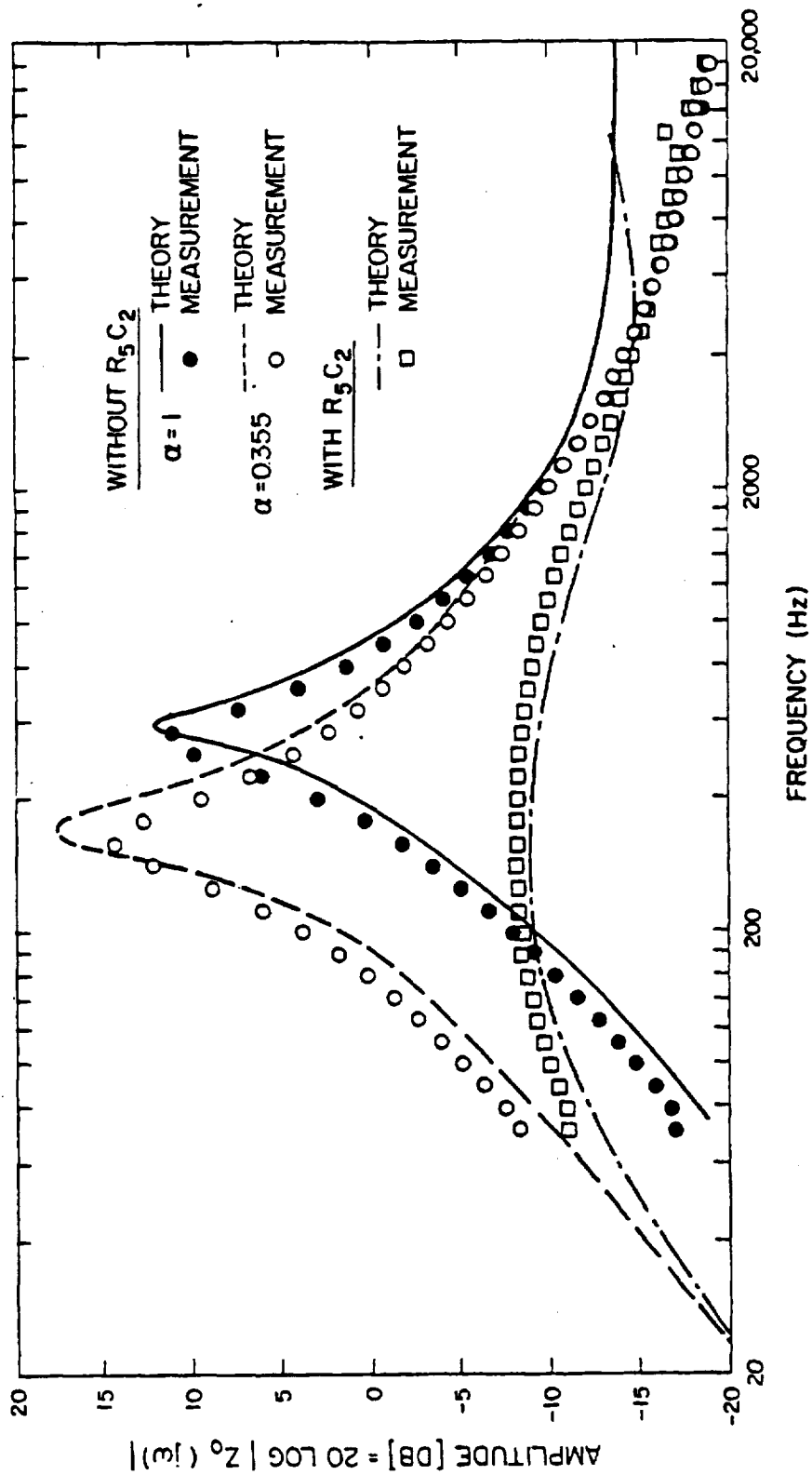


FIG. 9.16 AUDIOSUSCEPTIBILITY CHARACTERISTICS WITH AND WITHOUT THE COMPENSATION LOOP

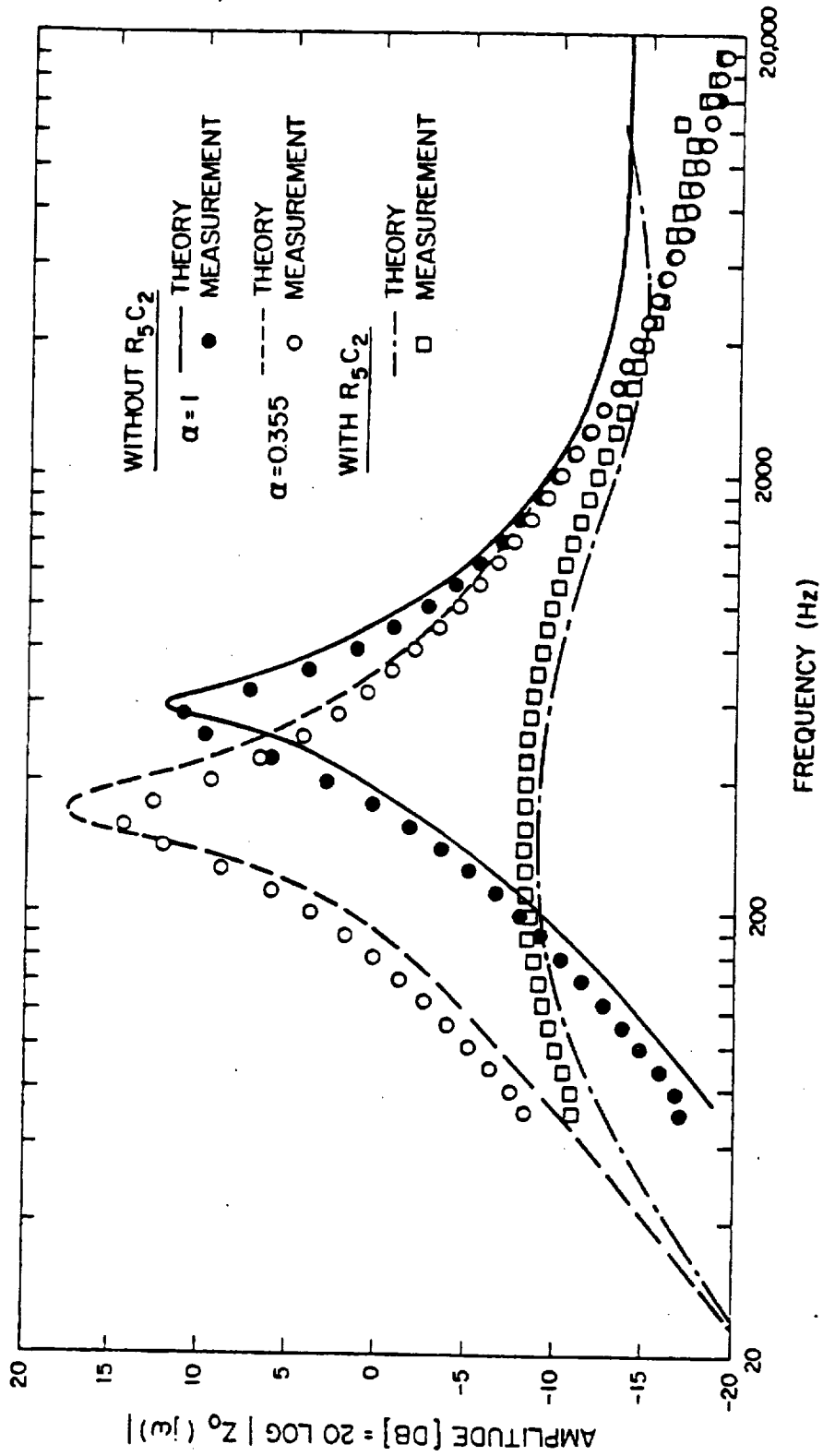
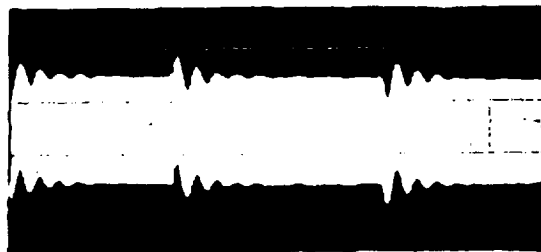
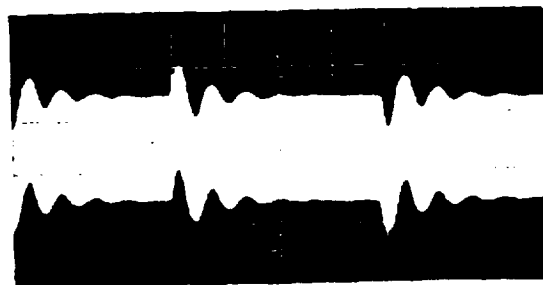


FIG. 9.17 OUTPUT IMPEDANCE CHARACTERISTICS WITH AND WITHOUT THE COMPENSATION LOOP.

(1) WITHOUT COMPENSATION LOOP

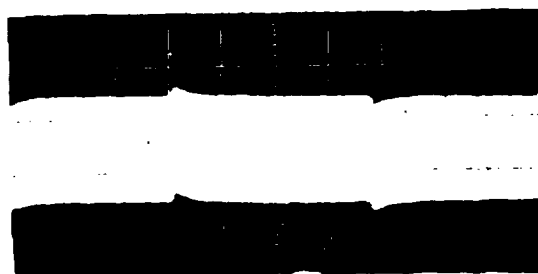


$\alpha = 1$



$\alpha = 0.355$

(2) WITH COMPENSATION LOOP



$\alpha = 0.355$

VERTICAL SCALE: 0.1 V/DIV.

HORIZONTAL SCALE: 1 MSEC/DIV.

FIG. 9.18 OUTPUT VOLTAGE TRANSIENT RESPONSE DUE TO A STEP LOAD CHANGE  $R_L = 10 \text{ OHMS} \leftrightarrow 11 \text{ OHMS}$ .

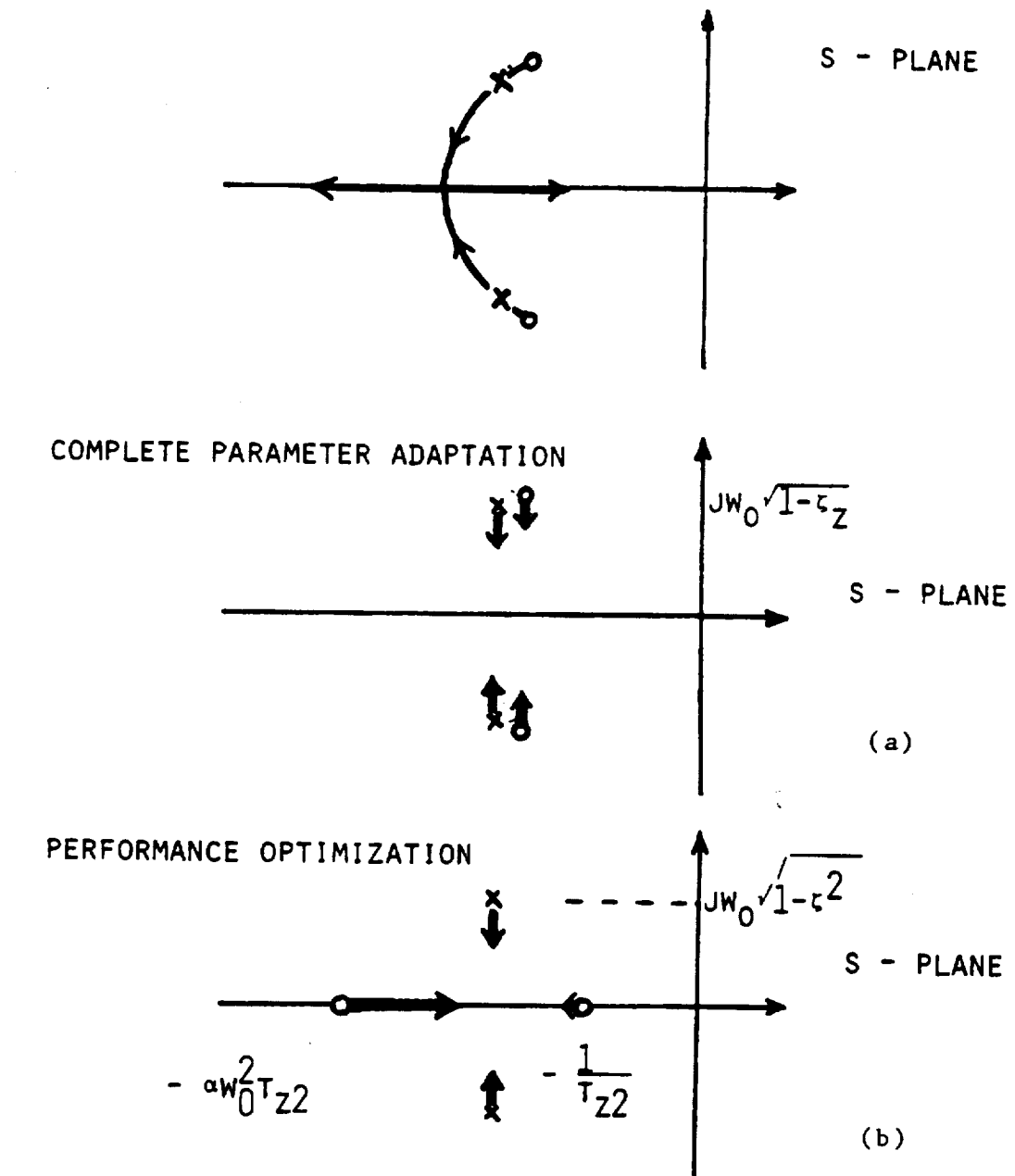


FIG. 9.19 (a) COMPLETE PARAMETER ADAPTATION (b) PARTIAL PARAMETER ADAPTATION TO OPTIMIZE REGULATOR PERFORMANCES.

as long as the zeros are sufficiently close to the poles, that is,

as long as  $\alpha\tau_{z2} \approx \frac{L}{R_L} + R_L C + R_C C$  in the numerator of equation (9-22).

It was indicated earlier that for better regulator performances it is desirable to have two real zeros instead of a complex pair. If the two real zeros are sufficiently far apart, equation (9-24) can be simplified to read:

$$s_{01} \approx \alpha\tau_{z2} \omega_o^2 \quad \text{where } \omega_o^2 = \frac{1}{LC} \quad (9-27)$$

$$s_{02} \approx \frac{1}{\tau_{z2}} \quad (9-28)$$

It is shown in the above two equations that  $s_{02}$  is no longer a function of output filter parameters, yet  $s_{01}$  is proportional to  $\omega_o^2$ . When the complex poles vary proportional to  $\omega_o$ , the zero  $s_{01}$  varies as a function of  $\omega_o^2$  as illustrated in Fig. 9.19(b). The nonlinear parameter adaptation, however, does not necessarily imply a drawback of the stability characteristic or the auto compensation nature. As discussed later in Chapter 10, the movement of the zeros in many practical concerns is often in the direction to increase the stability margin of the system.

## CHAPTER 10

### SCM-CONTROLLED REGULATOR STABILITY ANALYSIS

In this chapter, Bode analysis technique is employed to investigate the open-loop gain and phase. For a multiple-loop control system, the "loop-opening" should be performed at a place common to all feedback paths. It is clear from Figure 9.1 that such a place is the path containing the block  $F_M$ . By opening the loop at a point marked by X, the open-loop transfer function based on the various blocks of Figure 9.1 is obtained. Using this transfer function, the detailed transfer function can then be expressed in terms of circuit parameters. Subsequent to simplification, the detailed equations reveal how the various SCM parameters should be designed to achieve ample stability margin. Sample performance characteristics are given at the conclusion of the chapter.

#### 10.1 Open-Loop Transfer Function.

By opening the loop in Figure 9.1 at a place marked by "X", the open-loop transfer function becomes:

$$G_T(s) = F_M [F_{AC} F_3 F_1 + F_P F_D (F_{DC} + F_3 F_2 F_{AC})] \quad (10-1)$$

The transfer function is applicable to all three power stages.

Substituting contents of Table 8-1 into (10-1), the open-loop transfer functions  $G_T(s)$  can be derived in terms of detailed circuit parameters:

For buck power stage:

$$G_T(s) = F_M \frac{V_I}{sC_1 R_y} \frac{\omega_0^2 (1 + sCR_c)}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left[ \frac{1 + sC_2(R_y + R_5)}{1 + sC_2 R_5} + \frac{sL_e (1 + sCR_L)}{mR_L (1 + sCR_c)} \right] \quad (10-2)$$

For boost power stage:

$$G_T(s) = F_M \frac{V_I}{s C_1 R_y (D')^2} \left\{ \frac{s L_e D'}{m R_L} + \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left(1 - \frac{R_{eq} + s L_e}{R_L}\right) \cdot \left[ \frac{s^2 D'}{m \omega_0^2} + \left[ \frac{L_e D'}{m R_L} + (R_y + R_5) C_2 \frac{1 + s R_c C}{1 + s R_5 C_2} \right] s + \frac{1 + s R_c C}{1 + s R_5 C_2} \right] \right\} \quad (10-3)$$

For buck-boost power stage:

$$G_T(s) = F_M \frac{N_S}{N_P} \frac{V_I}{s C_1 R_y (D')^2} \left\{ \frac{s D D' L_e}{m R_L} + \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left(1 - D \frac{R_{eq} + s L_e}{R_L}\right) \cdot \left[ \frac{s^2 D'}{m \omega_0^2} + \left[ \frac{L_e D'}{m R_L} + C_2 (R_y + R_5) \frac{1 + s C R_c}{1 + s C_2 R_5} \right] s + \frac{1 + s C R_c}{1 + s C_2 R_5} \right] \right\} \quad (10-4)$$

In these three equations,

$$m = \frac{R_4}{n R_y} \quad (10-5)$$

$$R_y = (R_3 + R_x)/g, \quad (10-6)$$

$$R_x = \frac{R_1 R_2}{R_1 + R_2},$$

$$g = R_x / R_1$$

$$\omega_0^2 = \frac{1}{L_e C}$$

(repeat of (5-50))

$$2\zeta\omega_0 = 1/(CR_L) + (R_e + R_{ce})/L_e$$

(repeat of (5-51))

$$R_e = R_l$$

$$L_e = L$$

$$R_{ce} = R_c$$

$$* R_{eq} = R_e$$

: buck

(repeat of (5-34))

$$R_e = R_l/(D')^2$$

$$L_e = L/(D')^2$$

$$R_{ce} = R_c/D'$$

$$* R_{eq} = R_e + R_c(D/D')$$

: boost

(repeat of (5-35))

$$R_e = R_s/(D')^2$$

$$L_e = L_s/(D')^2$$

$$R_{ce} = R_c/D'$$

$$* R_{eq} = R_e + R_c(D/D')$$

: buck-boost

(repeat of (5-36))

\*Equations for  $R_{eq}$  are repeat of (5-53).



Notice that  $F_M$  is left intact so that eqs. (10-2) to (10-4) are applicable to all control laws.

## 10.2 Simplification of Open-Loop Transfer Functions

It can be immediately recognized that eqs. (10-2) to (10-4) are too complex to provide concise analytical comprehension of the effect of each control parameter. However, these equations can be simplified considerably if one chooses to adopt a design such that:

$$C_2 R_5 = C R_C = \tau_p \quad (10-7)$$

Making use of the equation (10-7), equations (10-2) to (10-4) can be shown to reduce to the following:

$$G_T(s) = \frac{F_M V_I}{s C_1 R_y} \frac{\frac{s^2}{m} + s \omega_0^2 \left[ C_2 R_y + C_2 R_5 + \frac{L_e}{m R_L} \right] + \omega_0^2}{s^2 + 2 \zeta \omega_0 s + \omega_0^2} \quad \text{buck} \quad (10-2A)$$

$$G_T(s) = \frac{F_M V_I}{s C_1 (D')^2 R_y} \left\{ \frac{s D' L_e}{m R_L} + \frac{1 - \frac{R_{eq} + s L_e}{R_L}}{s^2 + 2 \zeta \omega_0 s + \omega_0^2} \cdot \left[ \frac{s^2 D'}{m} + s \omega_0^2 \left( C_2 R_5 + C_2 R_y + \frac{D' L_e}{m R_L} \right) + \omega_0^2 \right] \right\} \quad \text{boost} \quad (10-3A)$$

$$G_T(s) = \frac{N_S}{N_P} \frac{F_M V_I}{s C_1 (D')^2 R_y} \left\{ \frac{s D D' L_e}{m R_L} + \frac{1 - D \frac{R_{eq} + s L_e}{R_L}}{s^2 + 2 \zeta \omega_0 s + \omega_0^2} \cdot \left[ \frac{s^2 D'}{m} + s \omega_0^2 \left( C_2 R_5 + C_2 R_y + \frac{D' L_e}{m R_L} \right) + \omega_0^2 \right] \right\} \quad \text{buck/boost} \quad (10-4A)$$

It will be shown in Volume II that if (10-7) is not grossly violated, (10-2A) through (10-4A) still apply to a good approximation in predicting regulator small-signal performances.

To search for commonality among these three equations, one notices that if one defines

$$\begin{aligned}
 \alpha &= m = R_4 / (nR_y) && : \text{ buck} \\
 &= m/D' = R_4 / (D'nR_y) && : \text{ boost} \\
 &= m/D' = R_4 / (D'nR_y) && : \text{ buck boost}
 \end{aligned} \tag{10-8}$$

The three transfer functions become:

$$G_T(s) = \frac{F_M V_I}{sC_1 R_y} \left\{ \frac{1}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left[ \frac{s^2}{\alpha} + s\omega_0^2 (C_2 R_y + C_2 R_5 + \frac{L_e}{\alpha R_L}) + \omega_0^2 \right] \right\} \tag{10-2B}$$

buck

$$G_T(s) = \frac{F_M V_I}{sC_1 (D')^2 R_y} \left\{ \frac{sL_e}{\alpha R_L} + \frac{1 - \frac{R_{eq} + sL_e}{R_L}}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left[ \frac{s^2}{\alpha} + s\omega_0^2 (C_2 R_y + C_2 R_5 + \frac{L_e}{\alpha R_L}) + \omega_0^2 \right] \right\} \tag{10-3B}$$

boost

$$G_T(s) = \frac{N_S}{N_P} \frac{F_M V_I}{sC_1 (D')^2 R_y} \left\{ \frac{sDL_e}{\alpha R_L} + \frac{1-D \frac{R_{eq} + sL_e}{R_L}}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \left[ \frac{s^2}{\alpha} + s\omega_0^2 (C_2 R_y + C_2 R_5 + \frac{L_e}{\alpha R_L}) + \omega_0^2 \right] \right\} \tag{10-4B}$$

buck/boost

In terms of control-loop analysis, results shown in (10-2B) to (10-4B) are sufficient as they express explicitly the open-loop transfer functions for all three regulators. However, an earlier stated objective for this program is that the analytical results are to be used as basis for the generation of concise design guidelines. Such an endeavor can only be achieved if eqs. (10-3B) and (10-4B) can be further reduced into the form exhibited by (10-2B), i.e., for all equations to exhibit the following form:

$$G_T(s) = \frac{1}{s} \frac{1}{K_1} \frac{K_2 s^2 + K_3 s + K_4}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad (10-9)$$

where  $K_1$  to  $K_4$  are constants. By so doing, one can then contemplate guidelines for selecting all constants  $k$ 's to achieve desired stability and other small-signal performances.

### 10.2.1 Open-Loop Transfer Function of An SCM-Controlled Buck Regulator

Defining

$$\tau_{z2} \triangleq C_2(R_y + R_5) + L_e/(DR_L) \approx C_2(R_y + R_5) \quad (10-10)$$

the buck-regulator open-loop transfer function of (10.2B) takes the following form:

$$G_T(s) = \frac{1}{s} \frac{F_M V_I}{C_1 R_y} \frac{\frac{s^2}{\alpha} + s\omega_0^2 \tau_{z2} + \omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad (10-11)$$

### 10.2.2 Open-Loop Transfer Function of An SCM-Controlled Boost Regulator

By defining the following identities;

$$\frac{1}{\alpha'} = \frac{1}{\alpha} \left\{ 1 - \frac{R_{eq}}{R_L} + \frac{2\zeta\omega_0 L_e}{R_L} - \frac{L_e}{R_L} \omega_0^2 \left[ \alpha C_2 (R_5 + R_y) + \frac{L_e}{R_L} \right] \right\} \quad (10-12)$$

$$\frac{1}{\alpha'} = \frac{1}{\alpha} (A_1 - A_2 \alpha \tau_{Z2}) \text{ or } \alpha = \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{Z2}} \quad (10-13)$$

$$A_1 = 1 - \frac{R_{eq}}{R_L} + \frac{2\zeta\omega_0 L_e}{R_L} - \left( \frac{L_e \omega_0}{R_L} \right)^2 \quad (10-14)$$

$$A_2 = \frac{1}{R_L C} \quad (10-15)$$

$$\alpha' = \frac{\alpha}{A_1 - A_2 \alpha \tau_{Z2}} \quad (10-16)$$

$$\begin{aligned} \tau_{Z2}' &= \left[ C_2 (R_5 + R_y) + \frac{L_{eq}}{\alpha R_L} \right] \left( 1 - \frac{R_{eq}}{R_L} \right) + \frac{L_e}{\alpha R_L} (1 - \alpha) \\ &\approx C_2 (R_5 + R_y) = \tau_{Z2} \end{aligned} \quad (10-17)$$

The open-loop transfer functions for the boost regulator can be reduced to the following form, assuming  $R_{eq} \ll sL_e$

$$G_T(s) = \frac{1}{s} \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{Z2}} \frac{F_M V_I n}{C_1 R_4 D'} \frac{\frac{s^2}{\alpha'} + s \omega_0^2 \tau_{Z2}' + \omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad (10-18)$$

### 10.2.3 Open Loop Transfer Function of An SCM-Controlled Buck-Boost Regulator

By defining the following identities:

$$\frac{1}{\alpha'} = \frac{1}{\alpha} \left\{ 1 - \frac{DR_{eq}}{R_L} + \frac{2\zeta\omega_0 DL_e}{R_L} - \frac{DL_e}{R_L} \omega_0^2 \left[ \alpha C_2 (R_5 + R_y) + \frac{L_e}{R_L} \right] \right\} \quad (10-19)$$

$$\frac{1}{\alpha'} = \frac{1}{\alpha} (A_1 - A_2 \alpha' \tau_{Z2}) \quad (10-20)$$

$$A_1 = 1 - \frac{DR_{eq}}{R_L} + \frac{2\zeta\omega_0 DL_e}{R_L} - D \left( \frac{L_e \omega_0}{R_L} \right)^2 \quad (10-21)$$

$$A_2 = \frac{D}{CR_L} \quad (10-22)$$

$$\alpha' = \frac{\alpha}{A_1 - A_2 \alpha' \tau_{Z2}} \quad (10-23)$$

$$\begin{aligned} \tau'_{Z2} &= \left[ C_2 (R_5 + R_y) + \frac{L_e}{\alpha R_L} \right] \left( 1 - \frac{DR_{eq}}{R_L} \right) + (1-\alpha) \frac{DL_e}{\alpha R_L} \\ &\approx C_2 (R_5 + R_y) = \tau_{Z2} \end{aligned} \quad (10-24)$$

the open-loop transfer functions for the buck-boost regulator can be reduced to the following:

$$G_T(s) = \frac{1}{s} \frac{A_1 \alpha' \frac{N_S}{N_P} \frac{F_M V_I^n}{C_1 R_4 D'}}{\frac{1 + A_2 \alpha' \tau_{Z2}}{s^2 + 2\zeta\omega_0 s + \omega_0^2}} \frac{\frac{s^2}{\alpha'} + s\omega_0^2 \tau_{Z2}' + \omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \quad (10-25)$$

#### 10.2.4. Experimental Verifications

To verify the analytical expressions derived above, two SCM controlled switching regulator breadboards are constructed. One is a buck regulator, the other is a buck/boost regulator. Since the characteristics of a boost regulator in many ways are quite similar to the buck/boost regulator, the authors feel that it is sufficient to verify the model for the buck/boost regulator and extended the conclusion to the boost regulator.

Example 1: The open loop characteristics of the buck regulator is verified extensively in chapter 9 with good agreement between the experimental data and analytical predictions.

Example 2: A two-winding buck/boost regulator is constructed with the following circuit parameter values:

<u>Symbols</u>	<u>Values</u>
$L_s$	220 $\mu$ H
$C$	700 $\mu$ F
$R_s$	0.087 ohms
$R_c$	0.05 ohms
$R_L$	28 ohms
$N_p$	33 turns
$N_s$	33 turns
$N_3$	22 turns
$R_1$	43.3 K-ohms
$R_2$	15.0 K-ohms
$R_3$	47.5 K-ohms
$R_4$	40.0 K-ohms
$R_5$	1.1 K-ohms
$C_1$	5600 PF
$C_2$	32000 PF
With constant $T_{ON}$ duty cycle control	
$T_{on}$	25 $\mu$ sec.
$V_I$	20 volts
$V_O$	28 volts

To measure the open-loop characteristic a small-amplitude low-frequency signal is injected between the integrator output and the threshold detector input in a series connection as shown in Fig. 10.1. The open loop gain is measured as the difference between the gains at the points C and A in this figure.

Figures 10.2(a) and (b) show the theoretical curves using equation (10-4B) and measurement data of the open loop characteristics (gain and phase) of the converter. Good correlations between the analytical prediction and experimental data are shown.

The cross-over frequency, (9.2 KHZ) is considerably higher than the filter resonant frequency ( $f_o = 170$  HZ), and yet sufficiently lower than the switching frequency (approximately 1/3 of the switching frequency) to avoid significant interference of the switching characteristics. It is shown that at such high cross-over frequency there exists a phase margin of  $62^\circ$ , sufficient to ensure the stability of the system.

### 10.3 Stabilization of SCM Control

It is interesting to point out that the duty cycle to power stage gain  $F_D F_P(s)$  for the boost and buck/boost converter derived earlier in (5-47), thru (5-49) with (5-52) has one zero in the left-half S-plane and one zero in the right-half S-plane, however, the two zeros in (10-18) and (10-25) are both located in the left-half S-plane. It is natural to postulate that the right-half S-plane zero is shifted into the left-half S-plane by the SCM control scheme. The postulation can be verified by employing the following approach. The SCM control scheme can be converted into a conventional signal loop control, if one disconnects the ac sensing loop and employs an externally generated ramp to implement the A-to-D conversion in the pulse

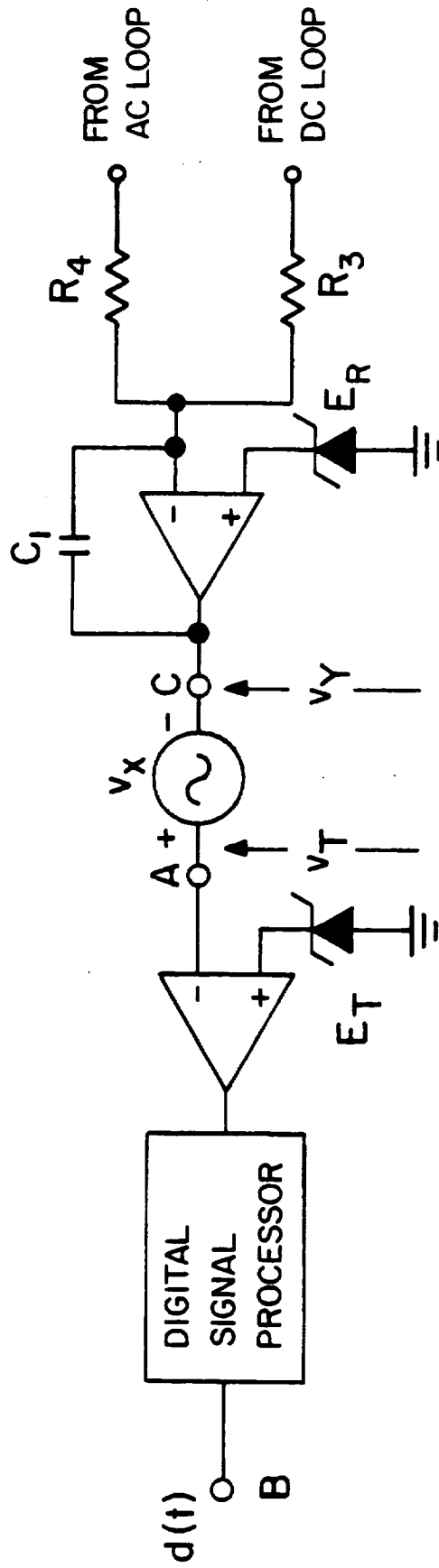
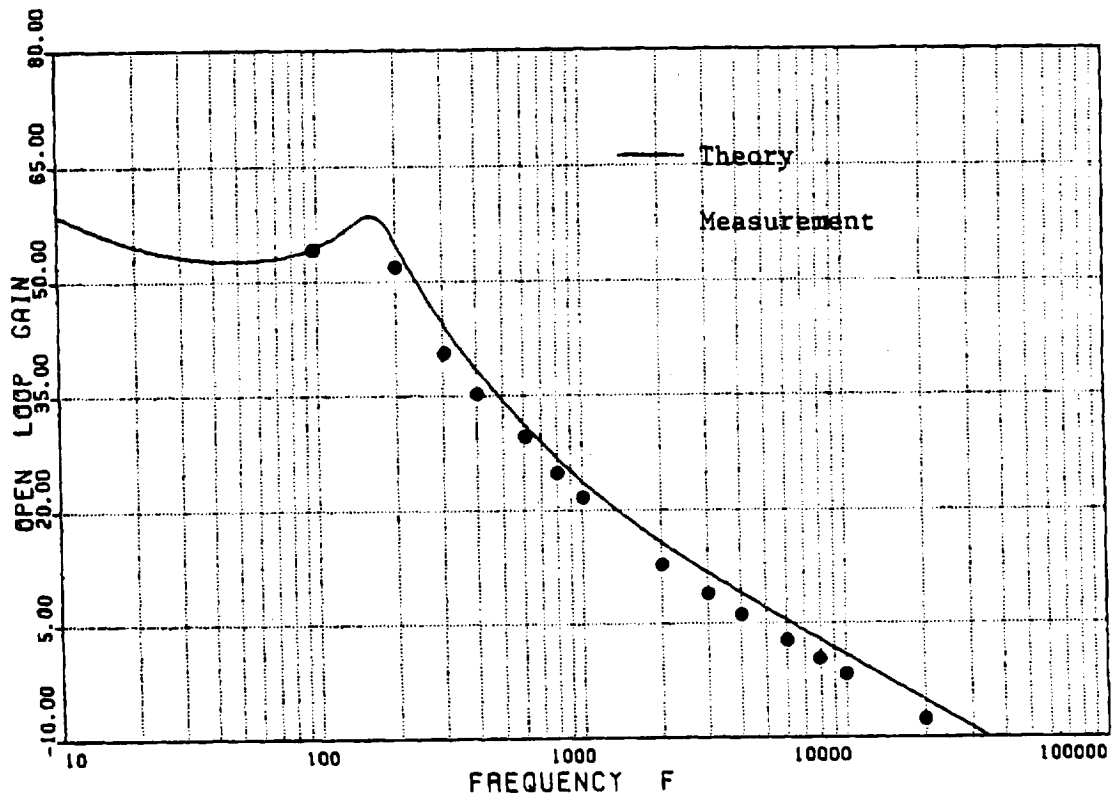


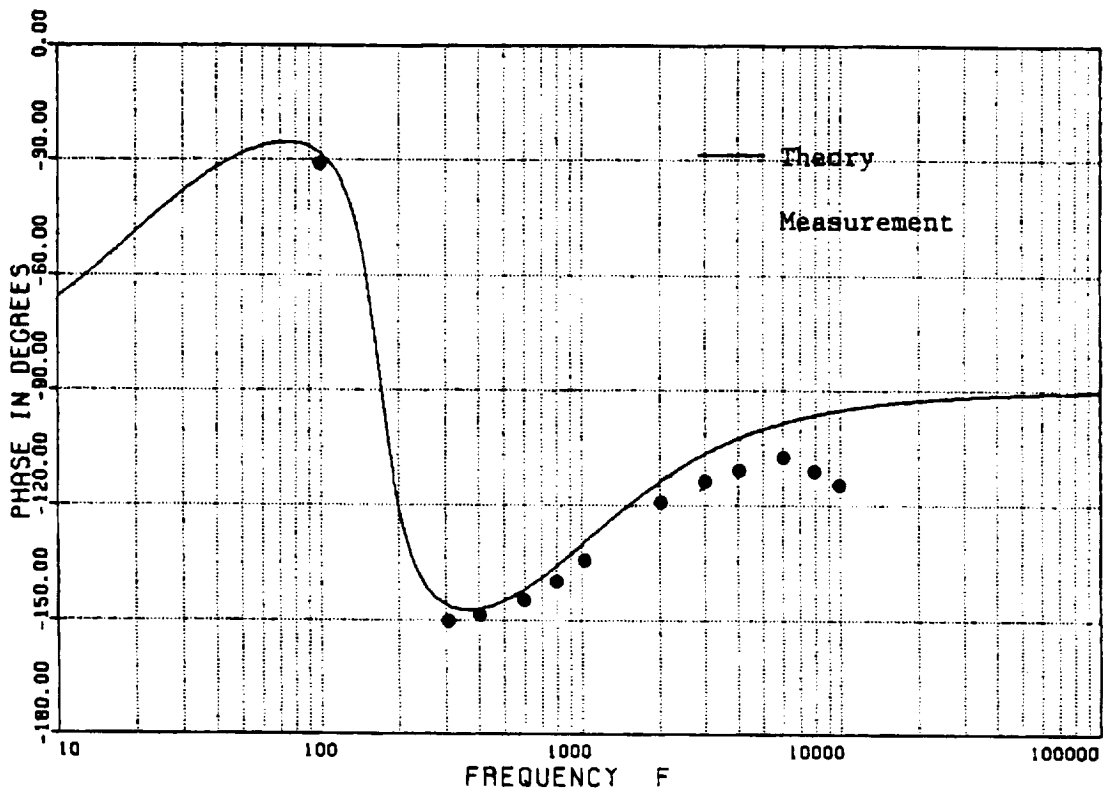
FIG. 10.1 INJECTION OF THE DISTURBANCE SIGNAL  $V_x$  BETWEEN THE OUTPUT OF THE ERROR AMPLIFIER AND THE INPUT OF THE PULSE MODULATOR.





(a)

FIG. 10.2(a) OPEN LOOP CHARACTERISTIC OF A BUCK/BOOST REGULATOR, THEORY AND MEASUREMENT (b) GAIN.



(b)

Fig. 10.2(b) Open Loop Characteristic, of a buck/boost regulator  
Theory and Measurement (b) Phase.

modulation process. Under this operating condition it is correct to assume mathematically that

$$R_4 \rightarrow \infty \text{ and}$$

$$F_M = \text{constant}$$

Also, for simplicity the compensation loop is disconnected. Employing the buck/boost converter as an example, equation (10-4) can be simplified to

$$G_T(s) = \frac{N_S}{N_P} \frac{F_M V_I}{(D')^2 C_1 s} \frac{\omega_o^2 (1-D) \frac{R_{eq} + sL}{R_L} (R_c C_s + 1)}{s^2 + 2\zeta\omega_o s + \omega_o^2} \approx \frac{N_S}{N_P} \frac{F_M V_I}{(D')^2 C_1 s} \frac{\omega_o^2 (s-s_{z1})(s+s_{z2})}{s^2 + 2\zeta\omega_o s + \omega_o^2} \quad (10-26)$$

If one compares (10-26) with (10-25), it is clear that the addition of an ac loop provides the stabilization effect by shifting the positive zero into the left-half S-plane as illustrated in Fig. 10-3, where  $s_{z1}$  and  $s_{z2}$  are

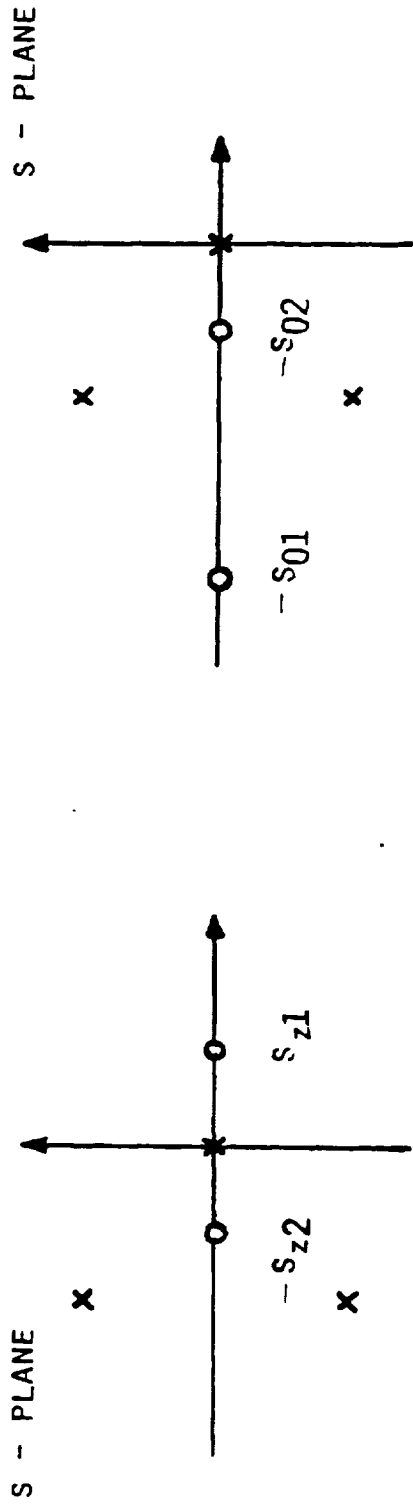
$$s_{z1} = \frac{R_L - D R_{eq}}{D L_e}$$

$$s_{z2} = \frac{1}{R_c C}$$

and  $s_{o1}$  and  $s_{o2}$  are the two zeros of the numerator of (10-25).

#### 10.4 Normalization of Open-Loop Frequency Response

It is clear from the common block diagram representation of Fig. 8.2 and from (10-11), (10-18) and (10-25) that the SCM-controlled buck, boost and buck/boost regulator all have transfer-function forms similar to (10-9). A normalization procedure is proposed such that the mathematical expression for each regulator performance category enjoys a common form for all three regulator types. The normalization procedure not only simplifies system notations for analysis purpose but also enables one to devise a unified design procedure for the standardized control module presented in Volume II of the report. The normalization procedure is described in the following.



(a)

(b)

FIG. 10.3 STABILIZATION EFFECT OF THE AC LOOP TO SHIFT THE POSITIVE ZERO TO THE LEFT HALF S PLANE.

(a) WITHOUT THE AC LOOP (b) WITH THE AC LOOP

The "s" term in all previous equations can be converted through the following normalization process to generalize the frequency-response representation:

$$s = \omega_o s \text{ (normalized)} \quad (10-27)$$

By so doing, the shape of the frequency response can be made independent of the resonant frequency  $\omega_o$  of the output filter. For simplicity the same notation  $s$  is used before and after normalization. For this reason, the "s" in all equations from here on is meant to represent  $s/\omega_o$ . With this normalization, equations (10-11), (10-18), and (10-25) become:

$$G_T(s) = \frac{F_M V_I}{C_1 R_y \omega_o s} \frac{\frac{s^2}{\alpha} + s \omega_o \tau_{z2} + 1}{s^2 + 2\zeta s + 1} \quad (10-11A)$$

$$G_T(s) = \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{z2}} \frac{F_M V_I n}{C_1 R_4 \omega_o s D'} \frac{\frac{1}{\alpha'} s^2 + \omega_o \tau'_{z2} s + 1}{s^2 + 2\zeta s + 1} \quad (10-18A)$$

$$G_T(s) = \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{z2}} \frac{N_S}{N_P} \frac{1}{D'} \frac{F_M V_I n}{C_1 R_4 \omega_o s} \frac{\frac{1}{\alpha'} s^2 + \omega_o \tau'_{z2} s + 1}{s^2 + 2\zeta s + 1} \quad (10-25A)$$

Employing (7-41),  $F_M = 2R_4 C_1 / (nM)$  the above three equations can be simplified as to one general form:

$$G_T(s) = \frac{K_1}{\omega_o s} \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{z2}} \frac{\frac{1}{\alpha'} s^2 + \tau'_{z2} \omega_o s + 1}{s^2 + 2\zeta s + 1} \quad (10-28)$$

where  $K_1 = \frac{2V_I}{M}$  buck;  $= \frac{2V_I}{D'M}$  boost;

$$= \frac{N_S}{N_P} \frac{1}{D'} \frac{2V_I}{M} \text{ buck/boost.}$$

$$\frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{z2}} = \alpha \quad (10-13)$$

$$\alpha = \frac{R_4}{nR_y} \text{ buck} \quad (10-8)$$

$$\alpha = \frac{R_4}{nR_y D'} \quad \text{boost and buck/boost} \quad (10-8)$$

$$A_1 = 1 \quad \text{buck}$$

$$= 1 - \frac{R_{eq}}{R_L} + \frac{2\zeta\omega_o L_e}{R_L} - \left( \frac{L_e \omega_o}{R_L} \right)^2 \quad \text{boost} \quad (10-14)$$

$$= 1 - \frac{DR_{eq}}{R_L} + \frac{2\zeta\omega_o DL_e}{R_L} - D \left( \frac{L_e \omega_o}{R_L} \right)^2 \quad \text{buck/boost} \quad (10-21)$$

$$A_2 = 0 \quad \text{buck}$$

$$= \frac{1}{R_L C} \quad \text{boost} \quad (10-15)$$

$$= \frac{D}{R_L C} \quad \text{buck/boost} \quad (10-22)$$

$$\tau'_{z2} = \tau_{z2} \cong C_2 (R_y + R_5) \quad \text{buck} \quad (10-10)$$

$$= \left[ C_2 (R_y + R_5) + \frac{L_e}{\alpha R_L} \right] \left( 1 - \frac{R_{eq}}{R_L} \right) + \frac{L_e}{\alpha R_L} (1-\alpha) \quad \text{boost} \quad (10-17)$$

$$= \left[ C_2 (R_5 + R_y) + \frac{L_e}{\alpha R_L} \right] \left( 1 - \frac{DR_{eq}}{R_L} \right) + (1-\alpha) \frac{DL_e}{\alpha R_L} \quad \text{buck/boost} \quad (10-24)$$

## 10.5 Qualitative Analysis of the Open-Loop Transfer Function

The two zeros in equation (10-28) can be expressed as:

$$s_{o1}, s_{o2} = \frac{\alpha' \omega_o \tau'_{z2}}{2} \left[ 1 \pm \sqrt{1 - \frac{4\alpha'}{(\alpha' \omega_o \tau'_{z2})^2}} \right] \quad (10-29)$$

where  $\alpha'$  is given by (10-13). (Notice that  $\alpha' = \alpha$  for the buck regulator.) The locus of the second-order zero of (10-29) for a fixed  $\alpha'$  and variable  $\tau'_{z2}$  is shown in Fig. 9-11(b). As the magnitude of  $\tau'_{z2}$  increases the second-order zero

changes from a complex-conjugate pairs to two negative real zeros. It was stated in section 9.4 and illustrated in Fig. 9.12 that in order to achieve higher loop gain and wider bandwidth it is desirable to have two negative real zeros instead of complex conjugated zeros. For negative real zeros, the following inequality should be satisfied

$$\frac{4}{\alpha' (\omega_o \tau'_{z2})^2} < 1$$

In practical designs generally the following inequality is observed

$$\frac{4}{\alpha' (\omega_o \tau'_{z2})^2} \ll 1 \quad (10-30)$$

The two zeros can be simplified to:

$$s_{o1} \cong \alpha' \omega_o \tau'_{z2} \cong \alpha' \omega_o C_2 (R_5 + R_y) \quad (10-31)$$

$$s_{o2} \cong 1/(\omega_o \tau'_{z2}): \quad (10-32)$$

where  $\alpha'$  is given in equation (10-13), and  $\tau'_{z2}$  is given in (10-10), (10-17), and (10-24) for each power stage.

The qualitative behavior of the open-loop transfer characteristic can now be examined based on the simplified equation:

$$G_T(s) = \frac{K_1}{\omega_o} \frac{\alpha}{s} \frac{(\frac{s}{s_{o1}} + 1)(\frac{s}{s_{o2}} + 1)}{s^2 + 2\zeta s + 1} \quad (10-33)$$

A typical asymptotic curve of eq. (10-33) is given in Figure 10.4. Arrangements of zeros  $s_{o1}$  and  $s_{o2}$  by selection of different control parameter values can result in all types of open-loop characteristics. Figure 10.5 illustrates the effect of changing the location of  $s_{o1}$  by varying  $\alpha'$ , while keeping  $s_{o2}$  fixed. Conversely, Figure 10.6 illustrates the effect of changing the location of  $s_{o2}$  by varying  $\tau'_{z2}$  while keeping  $s_{o1}$  fixed by maintaining

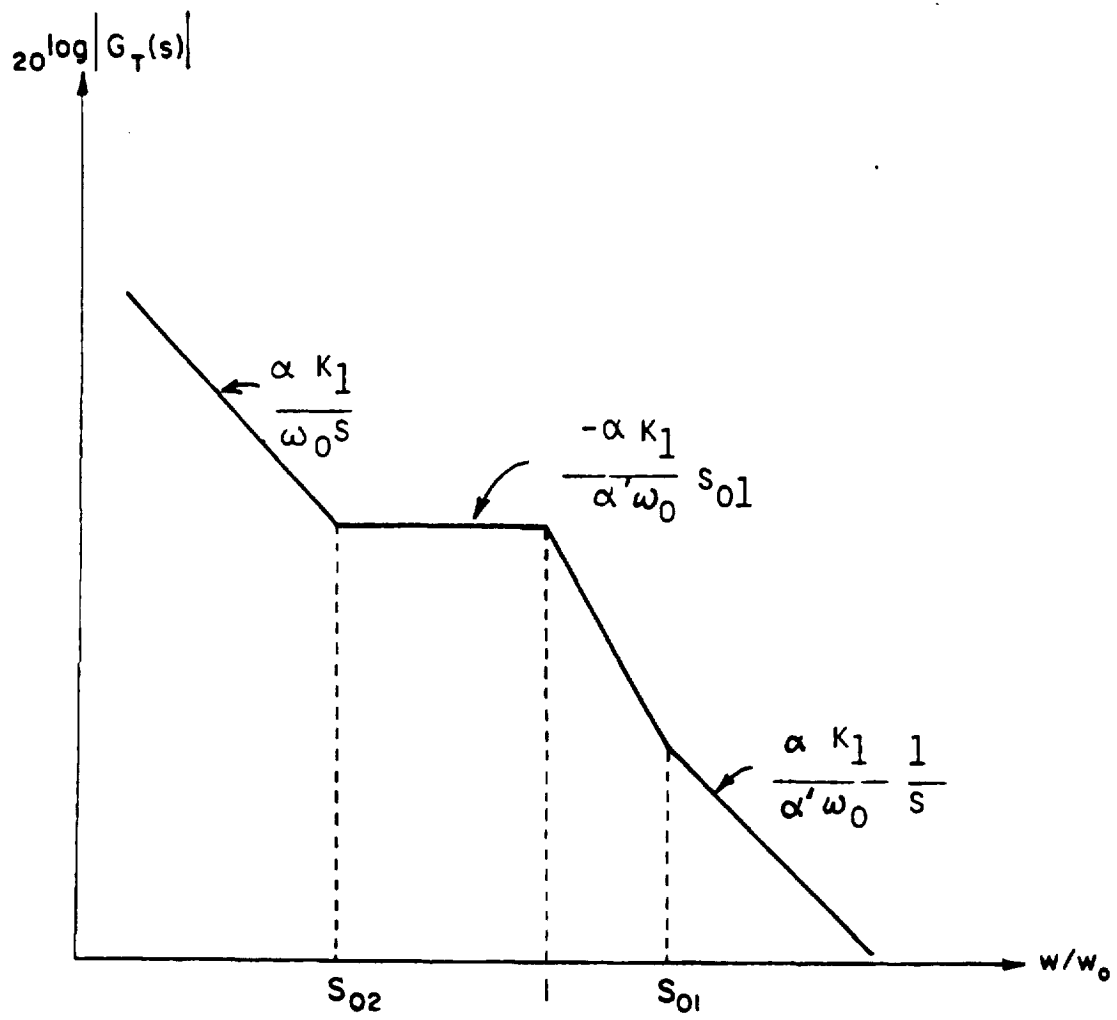


FIG. 10.4 ASYMPTOTIC CURVE OF THE OPEN LOOP TRANSFER FUNCTION



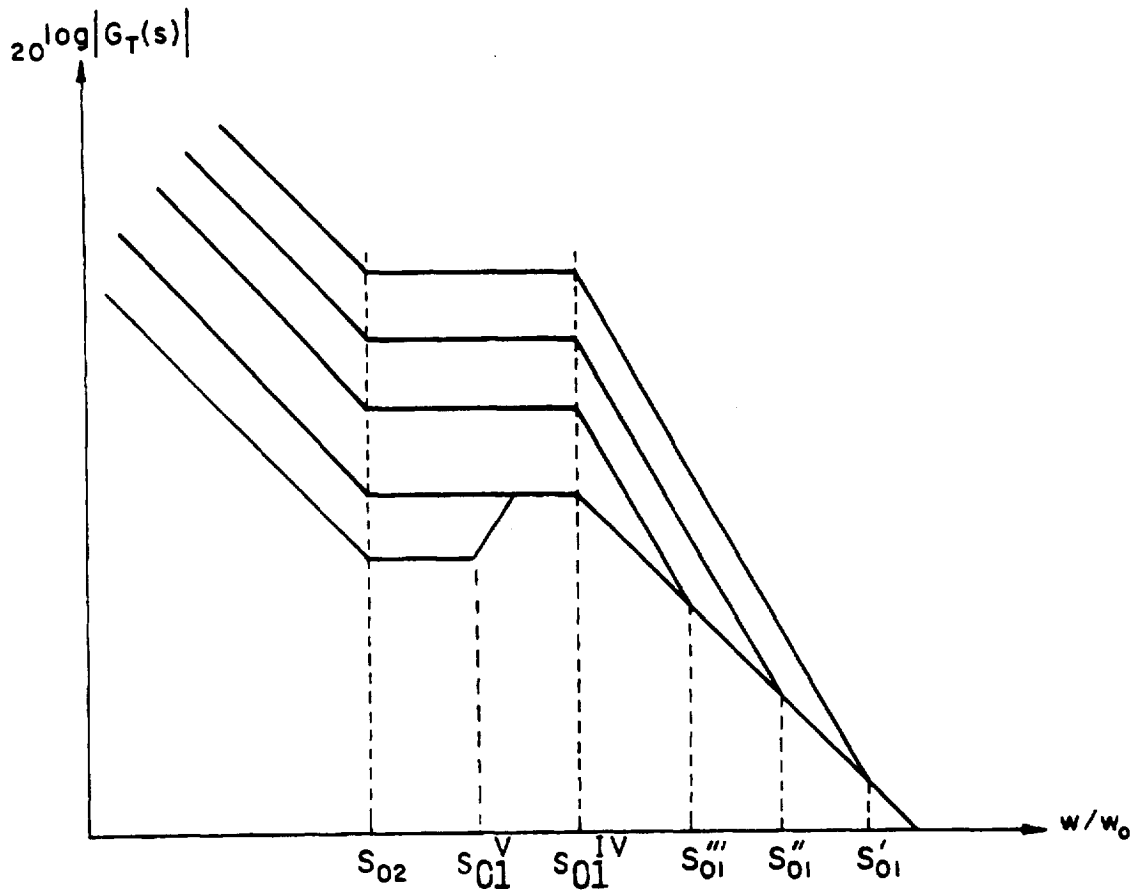


FIG. 10.5 OPEN LOOP TRANSFER CHARACTERISTIC FOR DIFFERENT VALUES OF THE ZERO  $s_{01}$

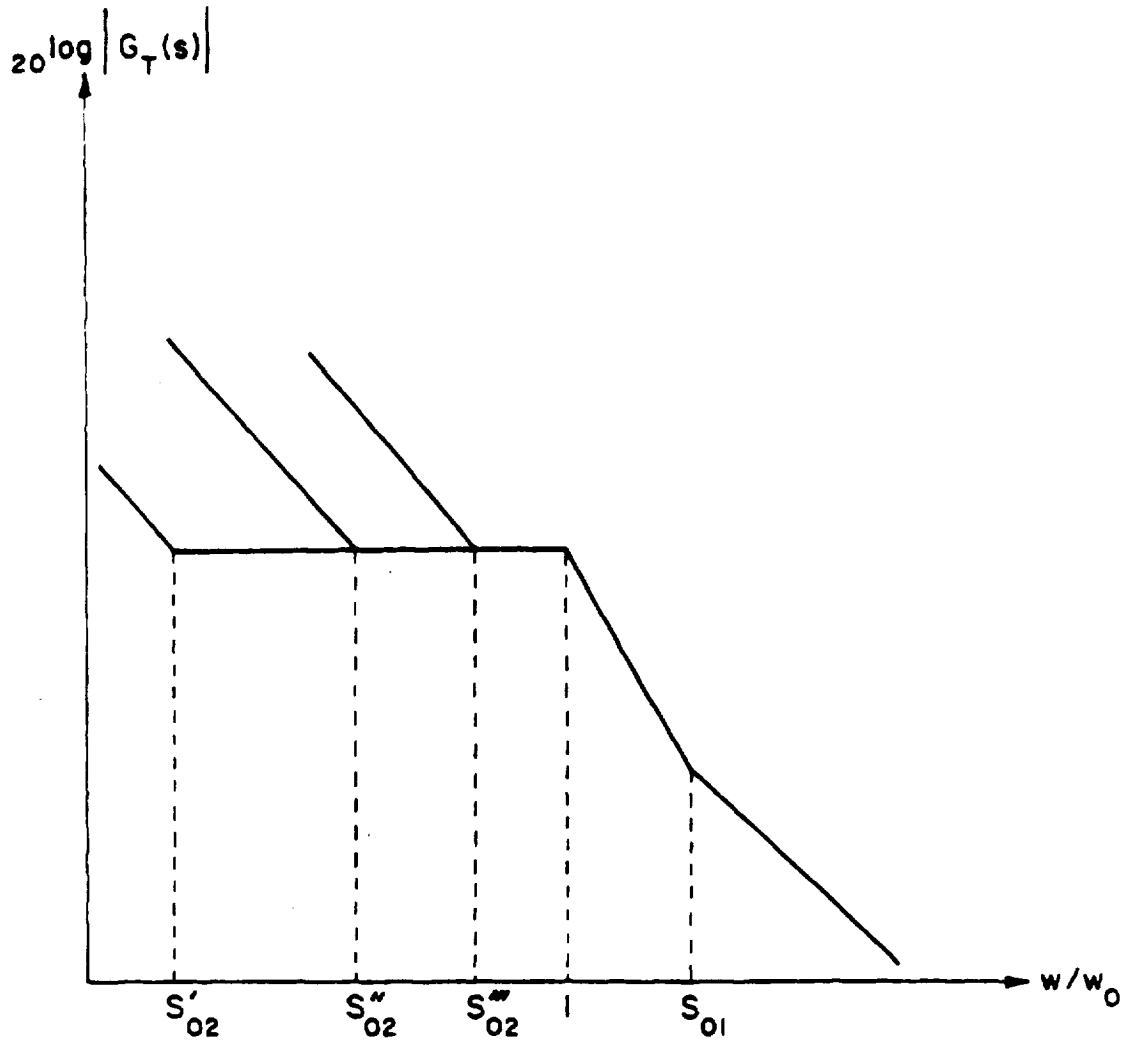


FIG. 10.6 OPEN LOOP TRANSFER CHARACTERISTIC FOR DIFFERENT VALUES OF THE ZERO  $S_{02}$

a constant product  $\alpha' \tau'_{22}$  .

A set of illustrative computer plots for gain and phase based on actual circuit parameters is given in Figure 10.7. Here, a fixed  $s_{o2}$  is argued by twelve different values for  $\alpha'$ : 0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, and 6. Except for the filter resonance in Figure 10.7, which the asymptotic plot of Figure 10.5 cannot reveal, similarities between the two figures are evident. In the gain plot of Figure 10.7(A), a higher  $\alpha'$  produces a higher gain. Higher gain is accomplished in the phase plot of Figure 10.7(B), by a correspondingly higher phase angle, resulting in a smaller phase margin.

The effects of the parameter  $\alpha'$  to the open-loop gain and phase are vividly displayed in the three-dimensional plots Fig. 10.8(A) and (B). The family of curves shown in Fig. 10.7 is represented by a three-dimensional surface by introducing the variable  $\alpha'$  along a third orthogonal axis.

In the above example, a buck/boost converter with the following parameter values is employed.

$$V_I = 20 \text{ volts}$$

$$V_o = 28 \text{ volts}$$

$$T_{on} = 25 \text{ } \mu\text{sec}$$

$$R_e = 0.5 \text{ ohms}$$

$$R_c = 0.05 \text{ ohms}$$

$$R_L = 28 \text{ ohms}$$

$$L_s = 220 \text{ } \mu\text{H}$$

$$C = 0.7 \times 10^{-3} \text{ F}$$

$$M = V_I T_{on} \\ = 0.5 \times 10^{-3} \text{ V-sec.}$$

$$\tau_{p1} = R_5 C_2 = 0.16 \times 10^{-4} \text{ sec.}$$

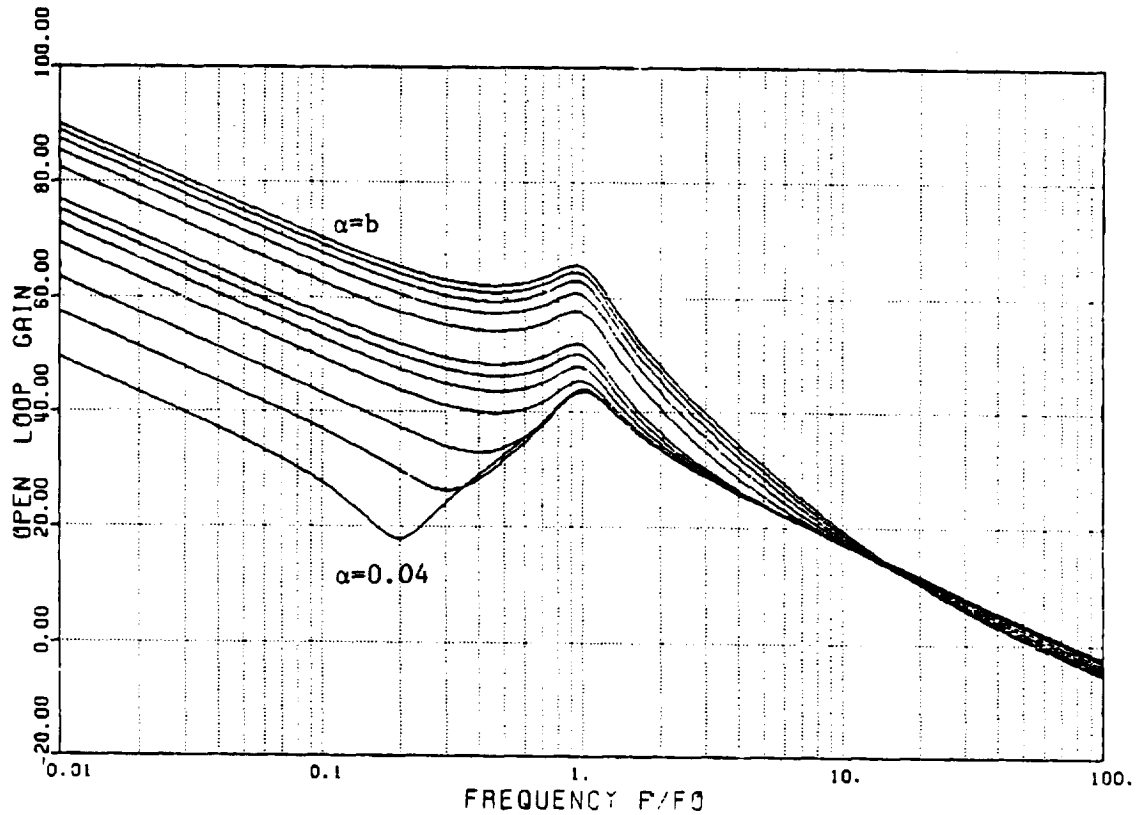


Fig. 10.7 (a) Open Loop Gain Characteristic for Different Values of the Parameter  $\alpha'$ ;  $\alpha' = 0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, 6$  from the bottom curve up, respectively.

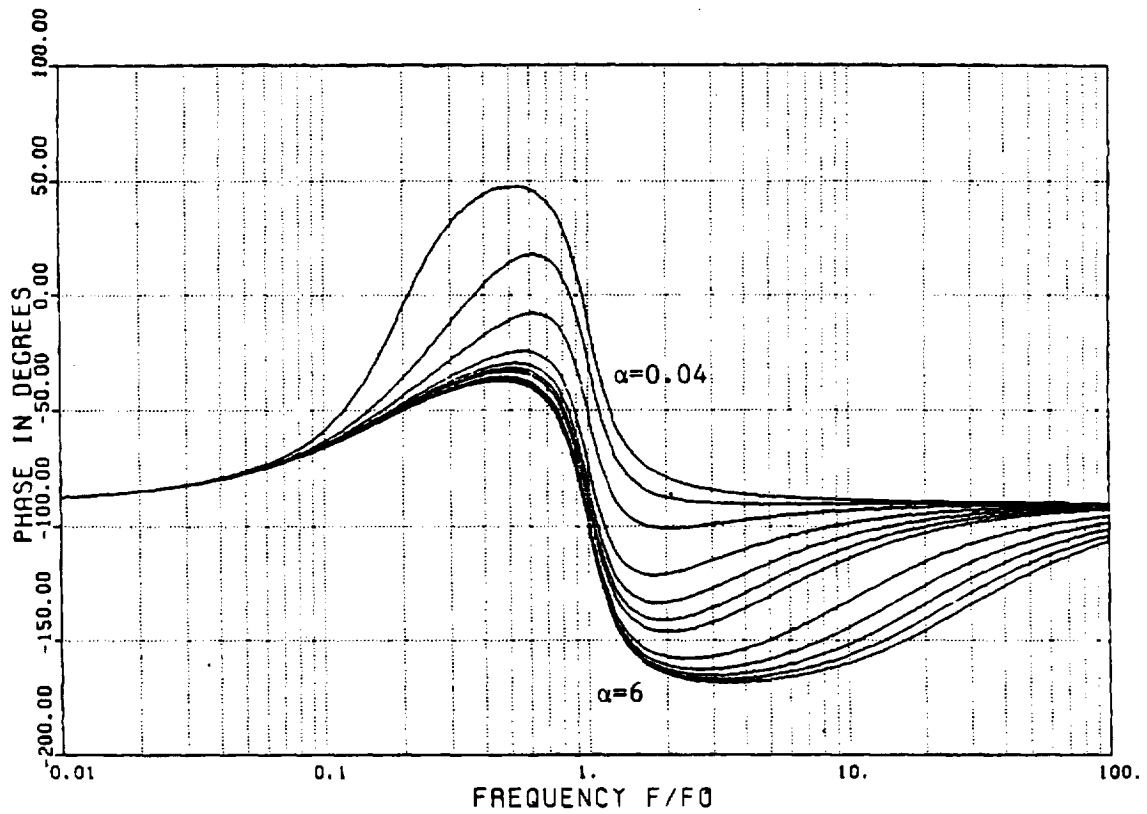


Fig. 10.7 (b) Open Loop Phase Characteristic for Different Values of the Parameter  $\alpha'$ ;  $\alpha' = 0.04, 0.1, 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, 6$  from the top curve down, respectively.

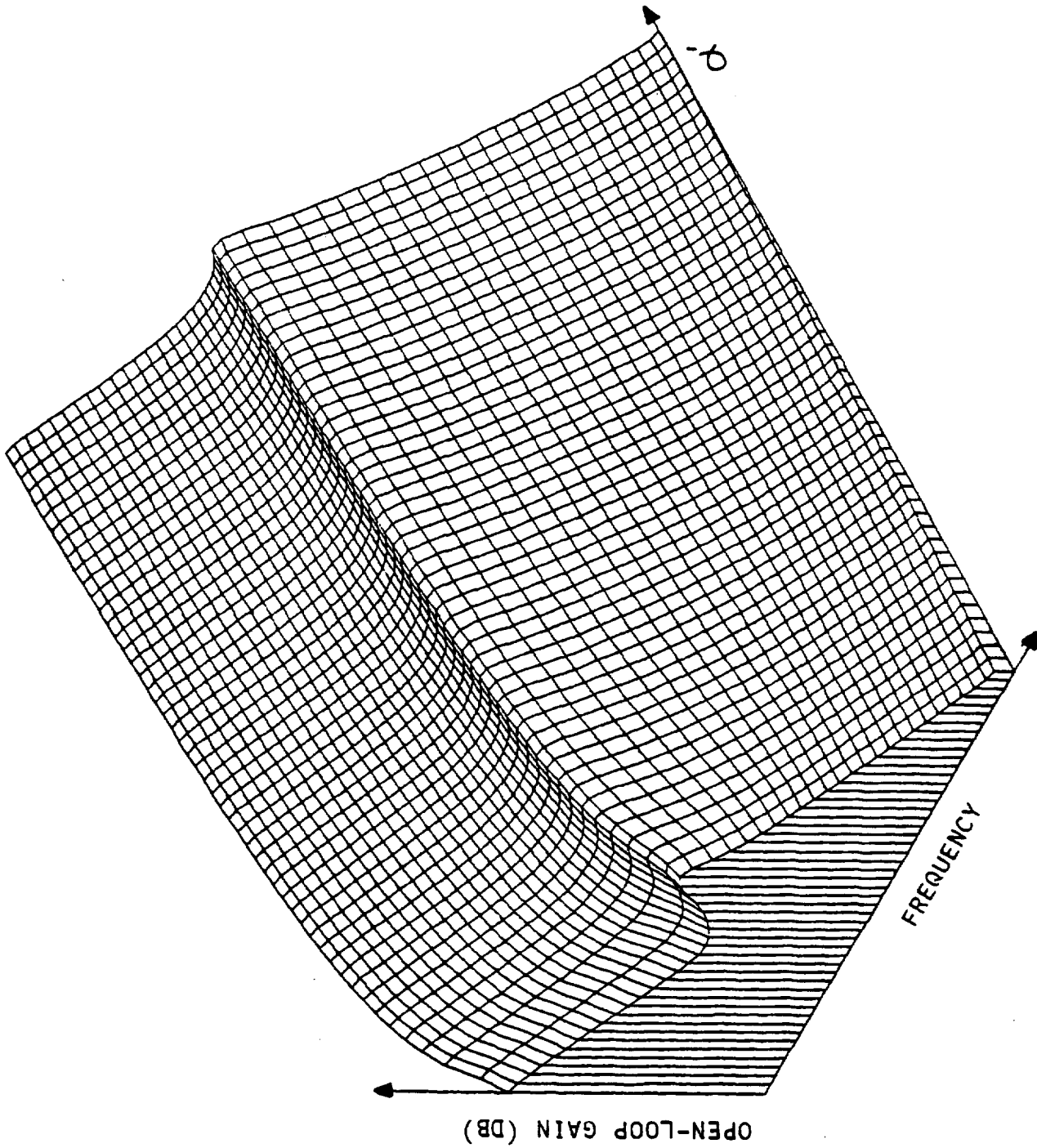


FIG. 10.8 (a) THREE DIMENSIONAL PLOT OF THE OPEN-LOOP GAIN.

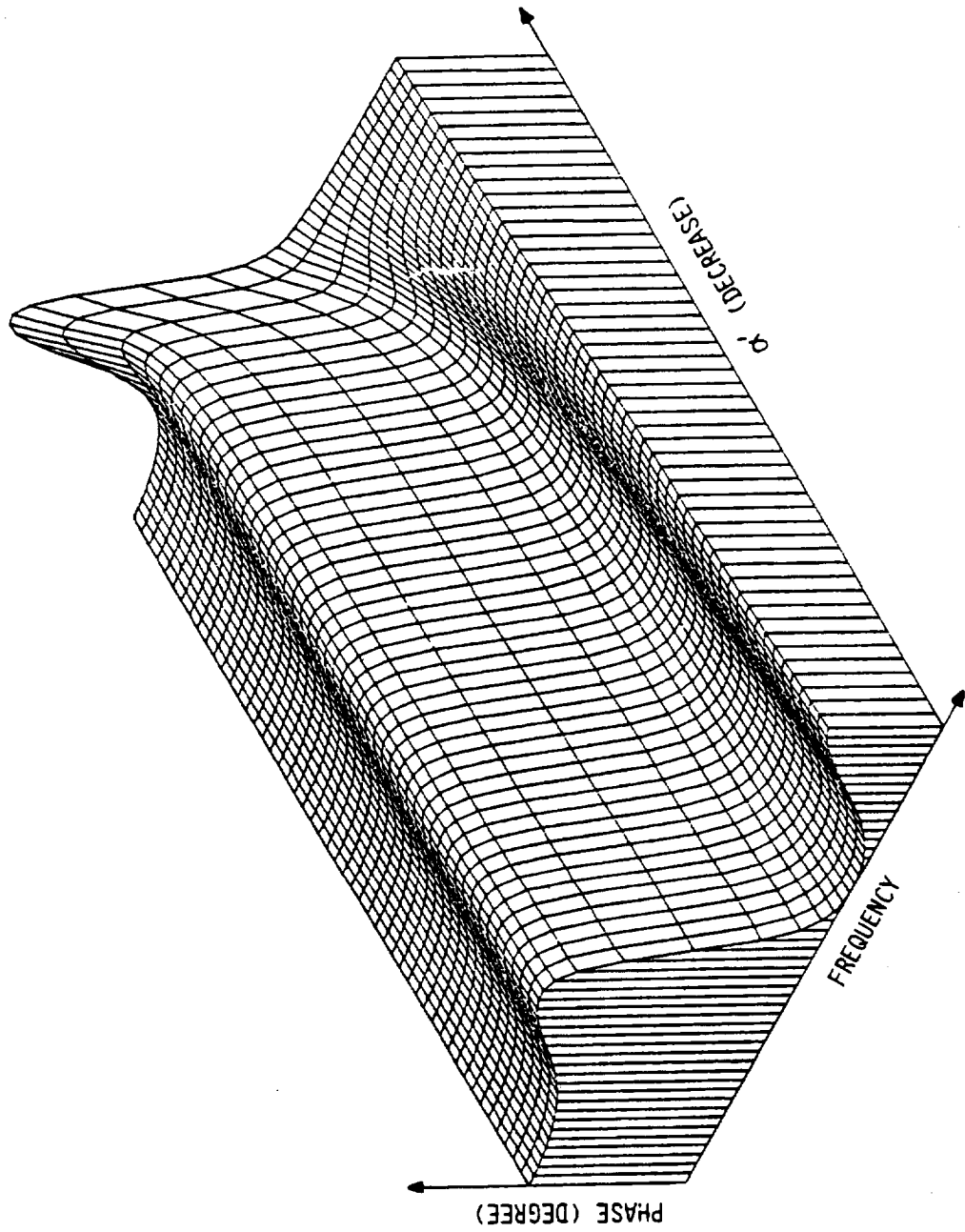


FIG. 10.8 (b) THREE-DIMENSIONAL PLOT OF THE OPEN-LOOP PHASE.

## 10.6 Adaptive SCM-Control.

The effect of the output filter parameters  $L_s$  and  $C$  on the regulator performances can be examined using the simplified open loop equation (10.33). It is shown that the two zeros can be expressed in the un-normalized scale as

$$s_{o1} = \omega_o^2 \alpha' \tau'_{z2} \quad (10.34)$$
$$s_{o2} = \frac{1}{\tau'_{z2}}$$

when  $\omega_o$  increases (or decreases), the corner frequency  $s_{o1}$  increases (or decreases) in a faster rate nearly proportional to  $\omega_o^2$ , while  $s_{o2}$  remains almost constant. Figure 10.9 illustrates the changes of the open loop characteristics due to the output filter capacitor variations of a buck/boost converter. It is shown that when  $\omega_o$  varies ranging from  $\omega_o/2$  to  $2\omega_o$ , the two new zeros  $s_{o1}$  and  $s_{o2}$  change in nonlinear fashion as predicted. Nevertheless, the open loop cross-over frequency and the phase margin only change slightly. It is important to point out that there is almost no change in the cross-over frequency and phase margin between curves a and b. However, when  $\omega_o$  is doubled as shown in curve c, the phase delay is also increased accordingly. As a result, the stability margin of the system is reduced. In practice, the output filter capacitor value is likely to increase its magnitude due to the addition of a capacitive load. A judicious design choice could minimize the effect of capacitor variations.

In a different regard, the variations on the output filter  $\omega_o$  could have been caused by changing the second parameter  $L_e (= L_s/D'^2)$  due to the duty cycle variations. Figure 10.10 illustrates the changes of the open loop



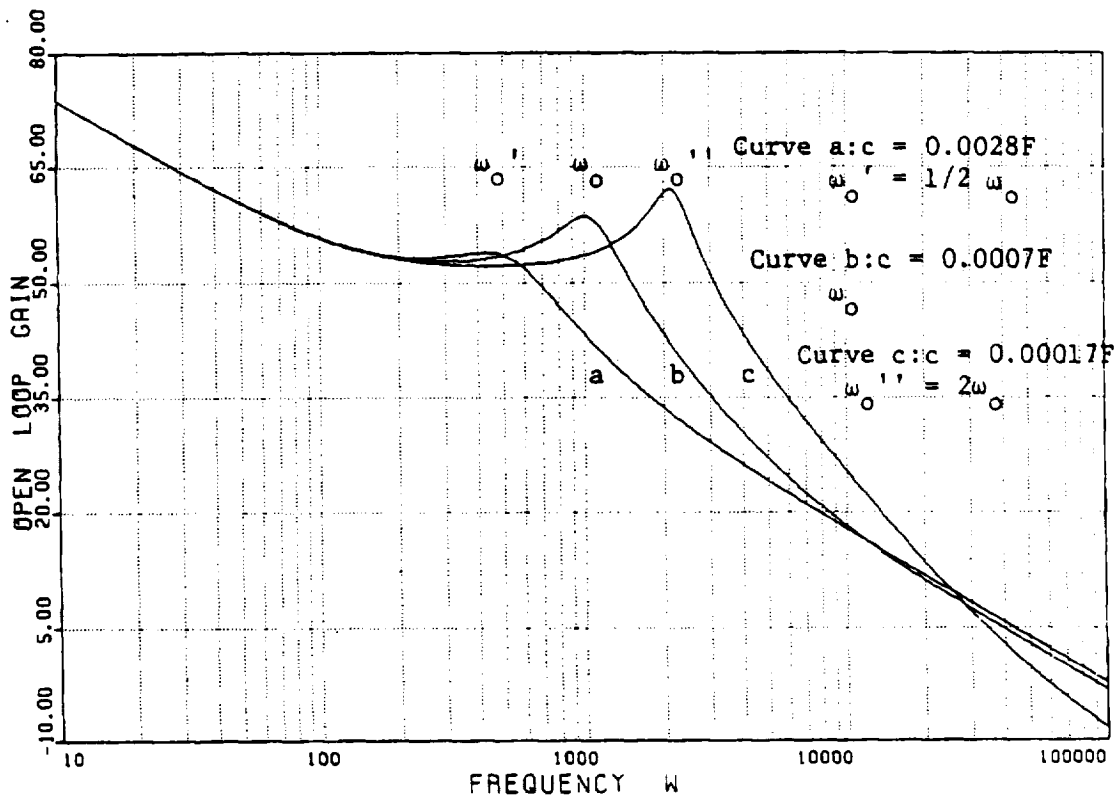


Fig.10.9(a) Open Loop Gain Characteristic for Different Values of  $\omega_0$  by Varying the Output Filter Capacitor  $C$ .

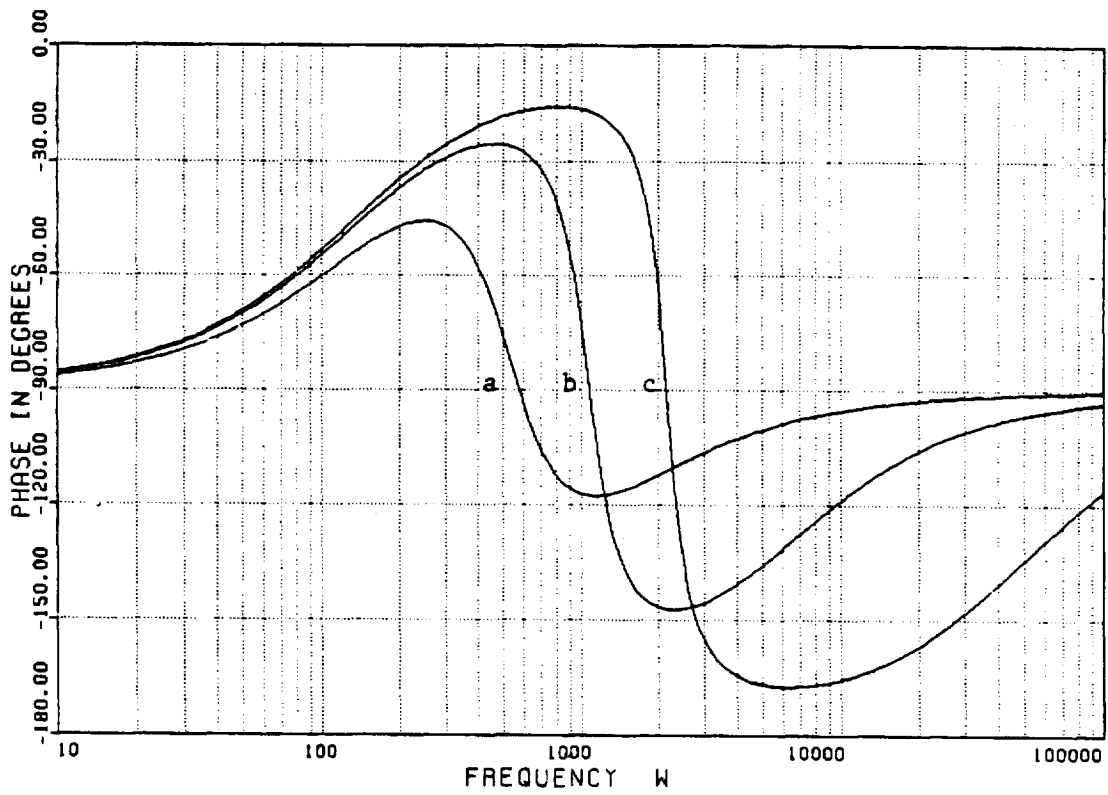


Fig.10.9(b) Open Loop Phase Characteristics for Different Values of  $\omega_0$  by Varying the Output Filter Capacitor C.

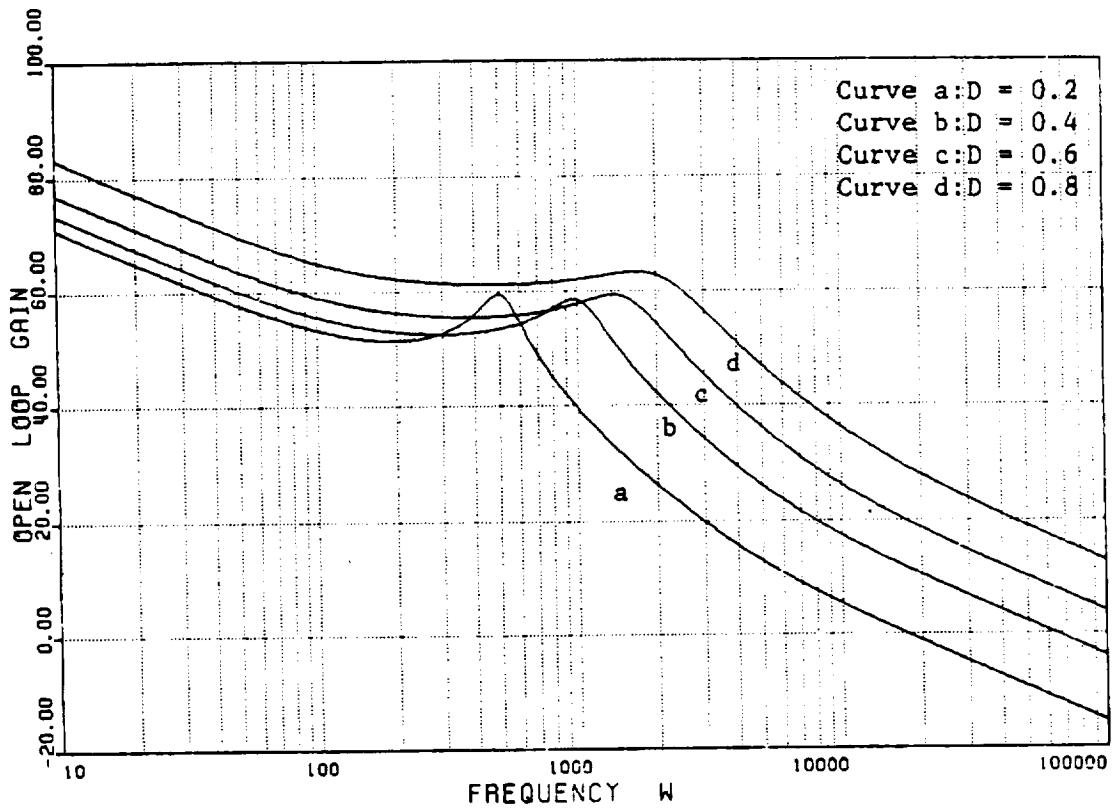


Fig. 10.10(a) Open Loop Gain Characteristic for Different Values of  $\omega_o$  by Varying the Output Filter Inductor  $L_e$

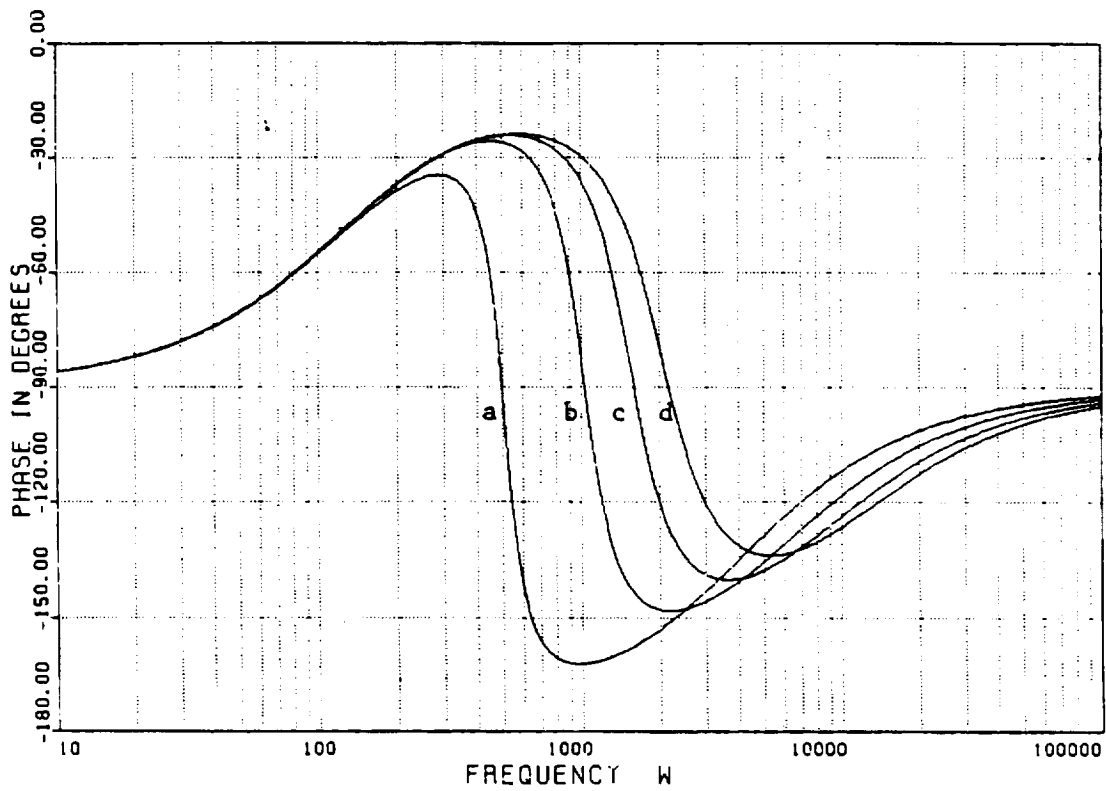


Fig.10.10(b) Open Loop Phase Characteristics for Different Values of  $\omega_o$  by Varying the Output Filter Inductor  $L_e$

characteristics due to variations of the duty cycle  $D(=0.2, 0.4, 0.6, 0.8)$ . It should be noted that the vertical movement of these characteristics is the result of dc loop gain changes. Although there are noticeable changes in the cross-over frequency, the phase margins at their corresponding cross-over frequencies are almost unaffected by the duty cycle changes. This effect can be verified by examining the following relations.

$$\omega_o = \frac{D'}{\sqrt{L_s C}} \quad (10.35)$$

and as a first order approximation

$$\alpha' \approx \alpha = \frac{R_4}{nR_y} \frac{1}{D'}$$

Substituting the above relations into (10.34), one obtains

$$s_{o1} \approx \frac{D'}{L_s C} \frac{R_4}{nR_y} \tau_{z2}'$$

One can conclude from the above argument that both  $\omega_o$  and  $s_{o1}$  are linearly proportional to the duty cycle  $D'$ . The SCM control is therefore adaptive to the duty cycle variations in regard to its effect of modulating the output filter inductance.

## CHAPTER 11

### SCM-CONTROLLED REGULATOR AUDIOSUSCEPTIBILITY ANALYSIS

The audiosusceptibility refers to the regulator's ability in attenuating small-signal sinusoidal disturbances propagating from the regulator input to its output. The audiosusceptibility performance is of considerable importance, as the regulator generally shares the input bus with other on-line equipment. The steady-state and dynamic operations of this equipment generates noise voltages on the input line which must be attenuated by the closed-loop regulator so that operations of the various payloads at the regulator output will not be detrimentally compromised. Since the passive filters in the regulator generally can provide adequate attenuation of disturbances at higher frequencies, the interest in the audiosusceptibility capability from a feedback-control-performance viewpoint is more often confined to a lower frequency range within, say, zero to ten times the output filter resonant frequency of the regulator.

The audiosusceptibility analysis utilizes the same block diagram of Figure 8.2 previously used for the stability analysis. Interest is focussed on  $\hat{v}_o/\hat{v}_i$ , with output-current disturbance  $\hat{i}_o$  assumed to be zero. It is clear that the  $\hat{v}_i$  to  $\hat{v}_o$  propagation actually portrays the closed-loop frequency response of the regulator.

It is easily shown from Figure 8.2 that the closed-loop frequency response  $G_A(s)$  can be expressed as:

$$\frac{\hat{v}_o}{\hat{v}_i} = G_A(s) = \frac{F_I F_P (1 + F_1 F_3 F_{AC} F_M)}{1 + G_T(s)} \quad (11-1)$$

where  $F_I$ ,  $F_P$ ,  $F_1$ ,  $F_3$ ,  $F_{AC}$ , and  $F_M$  have been defined in Table 8.1, and  $G_T(s)$  is the open-loop frequency response derived previously in eqs. (10-11), (10-18), and (10-25) for the three regulators. Substituting the defined parameters in Table 8-1 into (11-1) and applying the normalization prescribed in equation (10-27) one has,

$$G_A(s) = \frac{1}{1+G_T(s)} \cdot K_2 \cdot \frac{\tau_{z1}\omega_o s+1}{s^2+2\zeta s+1} \quad (11-2)$$

$$\text{where } K_2 = D \quad \text{buck} \quad (11-3)$$

$$= \frac{D}{D'} \left(1 + \frac{2V_{IL}e}{R_L M}\right) \quad \text{boost}$$

$$= \frac{N_s}{N_p} \frac{D}{D'} \left(1 + \frac{2V_{IL}e}{R_L M} D\right) \quad \text{buck/boost}$$

$$\tau_{z1} = R_c C$$

Substituting (10-33) into (11-2) and using (10-31) and (10-32),

$$G_A(s) = \frac{K_2}{K_1} \frac{\omega_o}{\alpha} \frac{s(\tau_{z1}\omega_o s+1)}{\frac{\omega_o}{\alpha K_1} s^3 + \left(\frac{1}{\alpha'} + \frac{\omega_o}{\alpha K_1}\right) s^2 + \left(\tau_{z2}\omega_o + \frac{\omega_o}{\alpha K_1}\right) s + \left(1 + \frac{\omega_o}{\alpha K_1}\right)} \quad (11-4)$$

The closed loop transfer function  $G_A(s)$  has two zeros and three poles. For sufficiently large  $K_1$ , the three poles are generally negative, real, and sufficiently apart. However, by increasing the control parameter  $\alpha'$  for large loop gain and wider bandwidth as illustrated in Fig. 10.7, the root-locus follows the pattern shown as Fig. 11-1. Notice, in Fig. 11-1, that the symbols  $s_{o1}$  and  $s_{o2}$ , previously used for the zeros of  $G_T(s)$ , are now used for the poles of  $G_A(s)$ . This is permissible because the poles of the closed-loop transfer function  $G_A(s)$  and the zeros of the open-loop transfer function  $G_T(s)$  are approximately the same. In the closed-loop transfer function  $G_A(s)$ , an additional high-frequency pole is generated and is represented by the symbol  $s_{o3}$ . For smaller  $\alpha'$ , the roots  $s_{o1}$  and  $s_{o2}$  form a complex pair. As  $\alpha'$  increases,  $s_{o1}$  and  $s_{o2}$  move toward the real axis where they merge, then move apart. As  $\alpha'$  increases still more,  $s_{o1}$  crosses the high-frequency zero, then merges with  $s_{o3}$  to form another complex pair.

The complex roots can result in severe peaking of the audio-susceptibility characteristic. For sufficiently small  $\alpha'$ , the peaking of  $G_A(s)$  characteristic occurs at low frequency as illustrated in Fig. 9-15 and Fig. 9-16. For sufficiently large  $\alpha'$ , the peaking of  $G_A(s)$  characteristic occurs at high frequencies. This phenomenon is illustrated in Fig. 11-2 employing a buck/boost converter with parameter values identical to that used in Fig. 10.7. It is interesting to note that while higher loop gain and wider bandwidth can always be achieved by increasing the  $\alpha'$  parameter values as shown in Fig. 10.7, the effect of the parameter  $\alpha'$  to the  $G_A(s)$  characteristic is quite dissimilar. In fact, optimum audio-



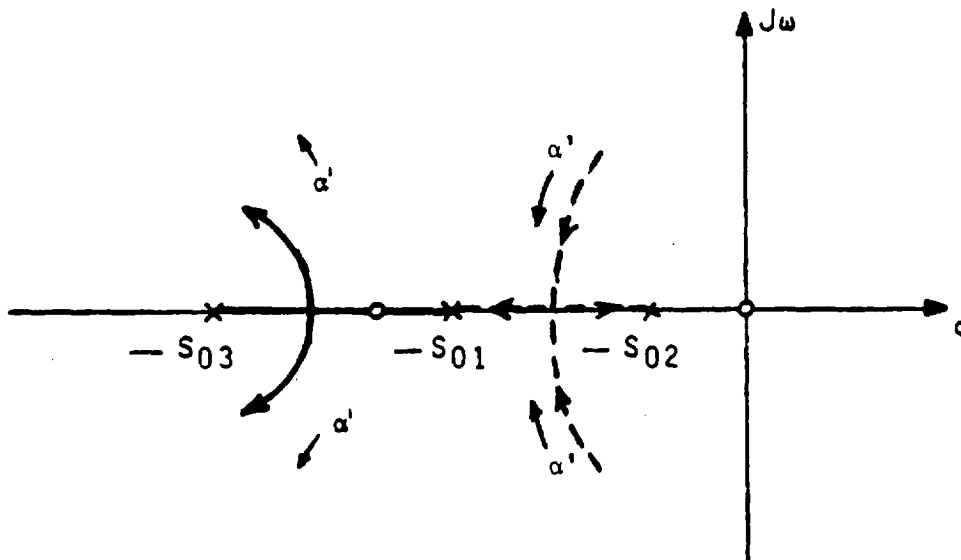
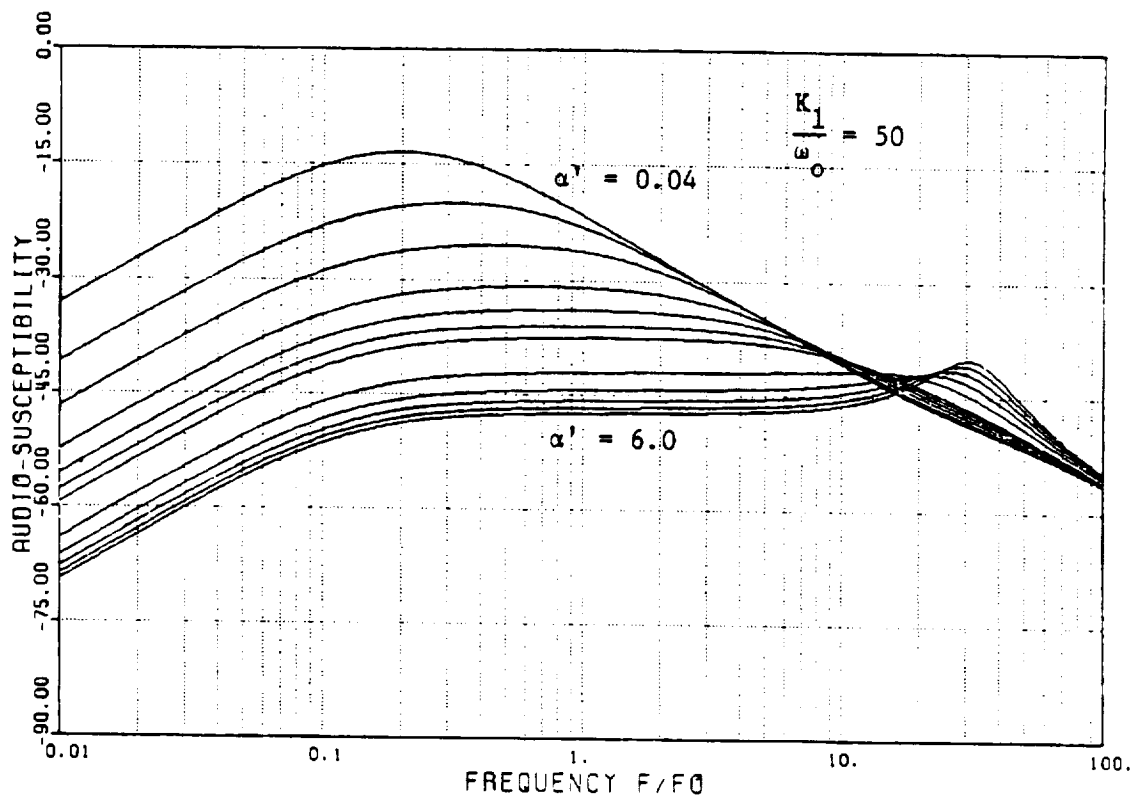


FIG. 11.1 POLES AND ZEROS OF THE AUDIOSUSCEPTIBILITY CHARACTERISTIC  $G_A(s)$



(a)

FIG. 11.2 AUDIOSUSCEPTIBILITY CHARACTERISTIC  $G_A(s)$  OF A BUCK/BOOST CONVERTER AS A FUNCTION OF  $\alpha'$

susceptibility performance, that is, performance without peaking, can only be achieved by judicious selection of  $\alpha'$  as illustrated in Fig. (11-2). Figures 11-3 and 11-4 provide 3-D plots of the  $G_A(s)$  characteristics as a function of frequency and the control parameter  $\alpha'$ . Detailed design guidelines for selecting the control parameters to optimize the audiosusceptibility characteristic are presented in Volume II of this report.

If one assumes that the proper value for the control parameter  $\alpha'$  can be selected to avoid high-frequency peaking, then the effect of the high frequency root can be neglected. Under this condition, the worst audiosusceptibility usually occurs at low frequencies. In the low-frequency range, equation (11-4) can be simplified if one employs the following inequality relation

$$G_T(s) \gg 1$$

which yields

$$G_A(s) = \frac{K_2}{K_1} \frac{\omega_o}{\alpha} \frac{s(\tau_{z1}\omega_o s + 1)}{\frac{s^2}{\alpha^2} + s\omega_o\tau'_{z2} + 1} \quad (11-5)$$

where  $K_1$  and  $K_2$  are given in (10-28) and (11-3) and

$$\alpha = \frac{A_1 \alpha'}{1 + A_2 \alpha' \tau_{z2}} \quad \text{same as (10-13)}$$

where  $A_1$ ,  $A_2$ ,  $\tau_{z2}$ ,  $\tau'_{z2}$  and  $\alpha$  are specified under (10-28). Equation (11-5) can be expressed as (11-6) if the two roots of the characteristic equations are real values

$$G_A(s) = \frac{K_2}{K_1} \frac{\omega_o}{\alpha} \frac{s(\tau_{z1} \omega_o s + 1)}{\left[ \frac{s}{s_{o1}} + 1 \right] \left[ \frac{s}{s_{o2}} + 1 \right]} \quad (11-6)$$

A sketch of asymptotic curve of eq. (11-5) is given in Figure 11.5. The worst audio-susceptibility performance occurs between  $s_{o1}$  and  $s_{o2}$ . The denominator of (11-6) produces second-order poles which are identical to

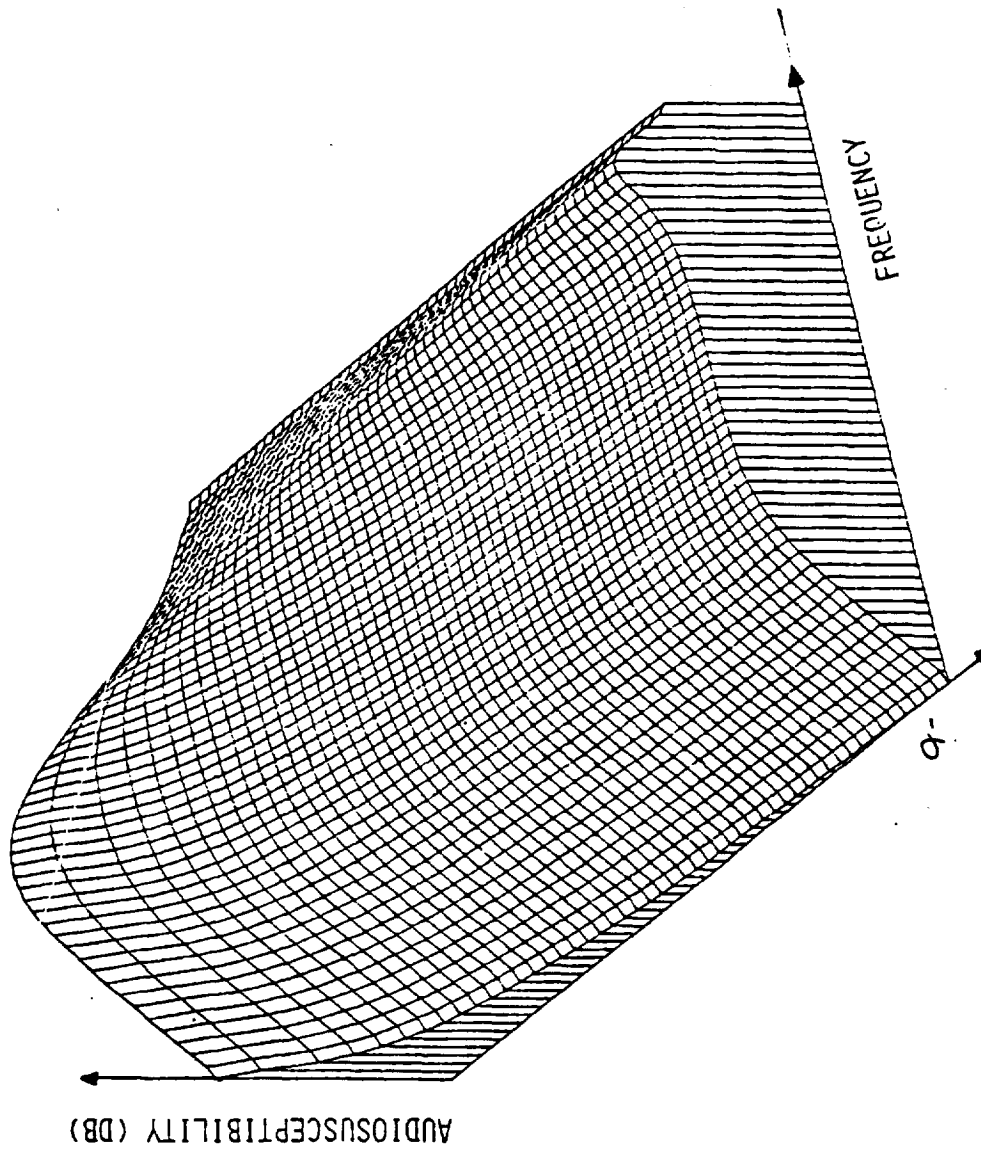


FIG. 11.3 THREE-DIMENSIONAL PLOT OF THE AUDIOSUSCEPTIBILITY CHARACTERISTIC AS SHOWN IN FIG. 11.2.

ORIGINAL FACETS  
OF POOR QUALITY

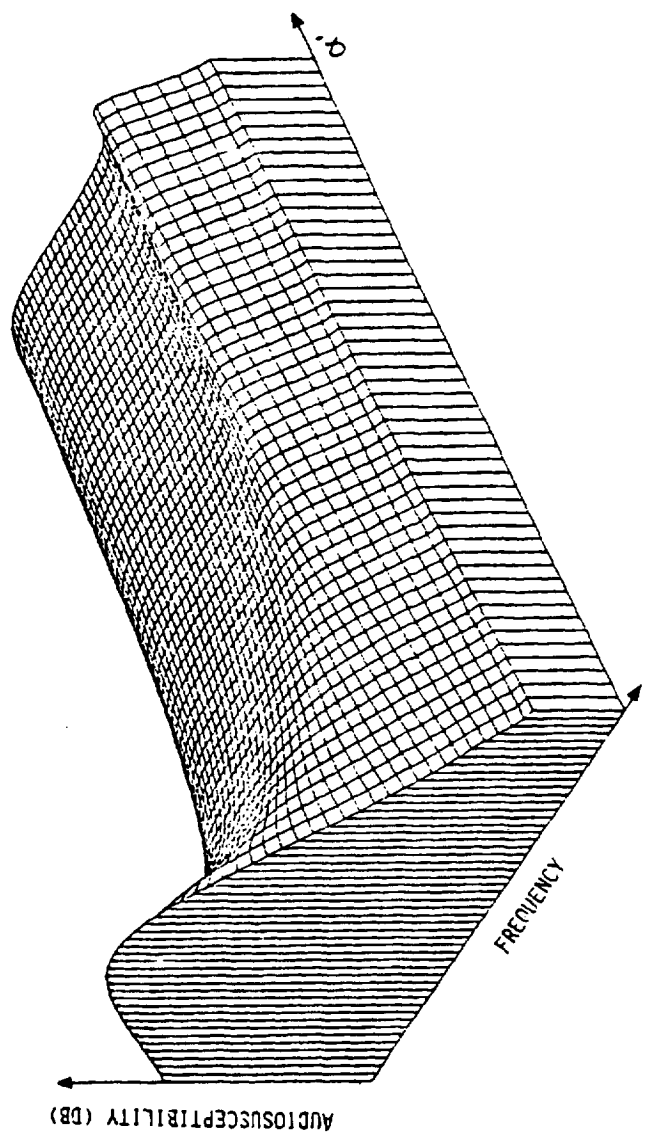


FIG. 11.4 THREE-DIMENSIONAL PLOT OF  $G_A(s)$  - A DIFFERENT ANGLE.

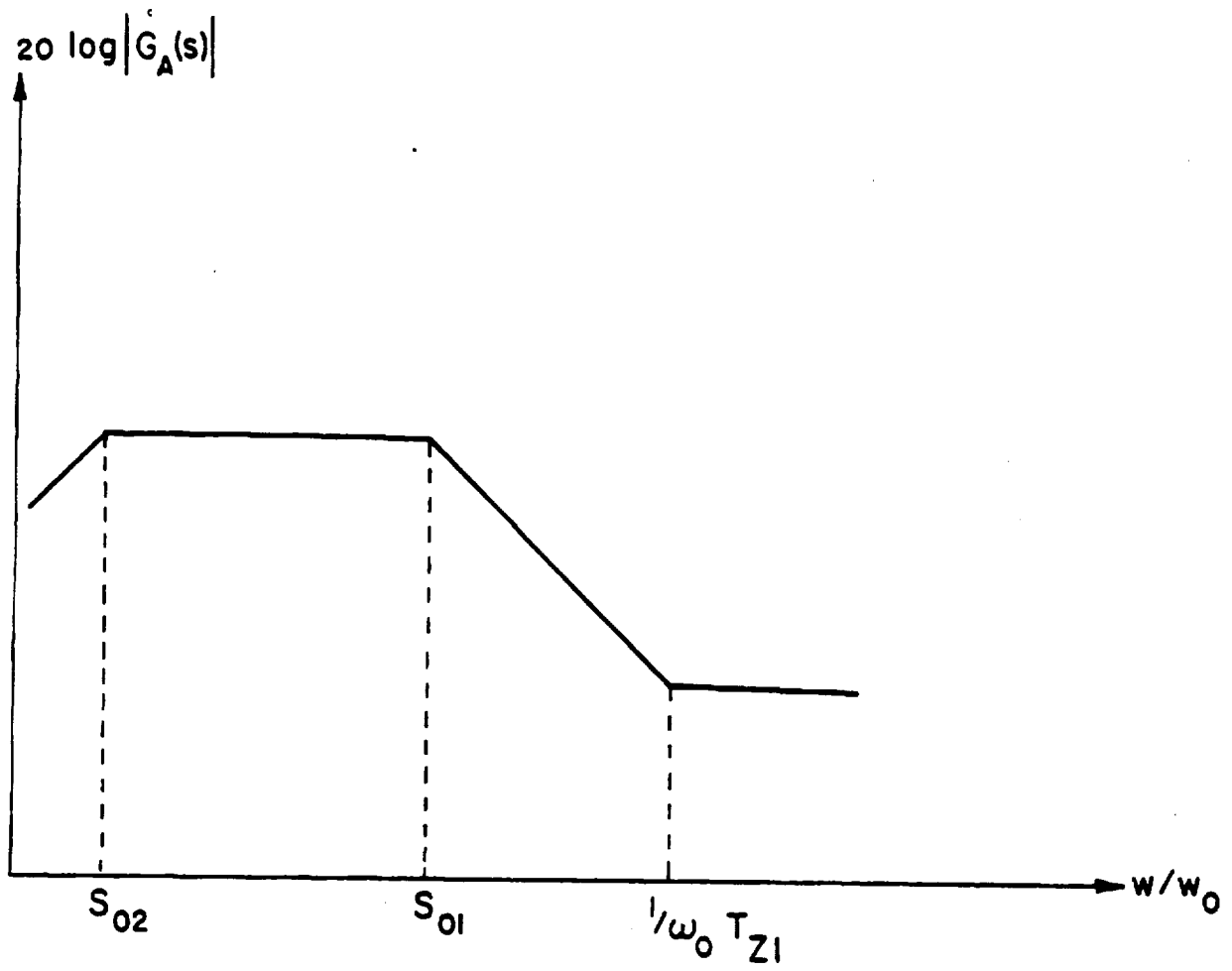


FIG. 11.5 CLOSED LOOP TRANSFER CHARACTERISTIC

to the numerator of (10-33).

Experimental verification of the audiosusceptibility characteristic was provided for both buck and buck/boost converters. The closed-loop input-to-output transfer function is measured with a variable-frequency sinusoidal voltage source superimposed on the nominal dc voltage as illustrated in Fig. 11-6. The verification of the audiosusceptibility characteristic for the buck converter has already been elaborated in chapter 9, with excellent correlation between analysis and measurement. Experimental verification for the buck/boost converter is shown in Fig. 11-7. In both cases, the flat top of the  $G_A(s)$  characteristic is evident.

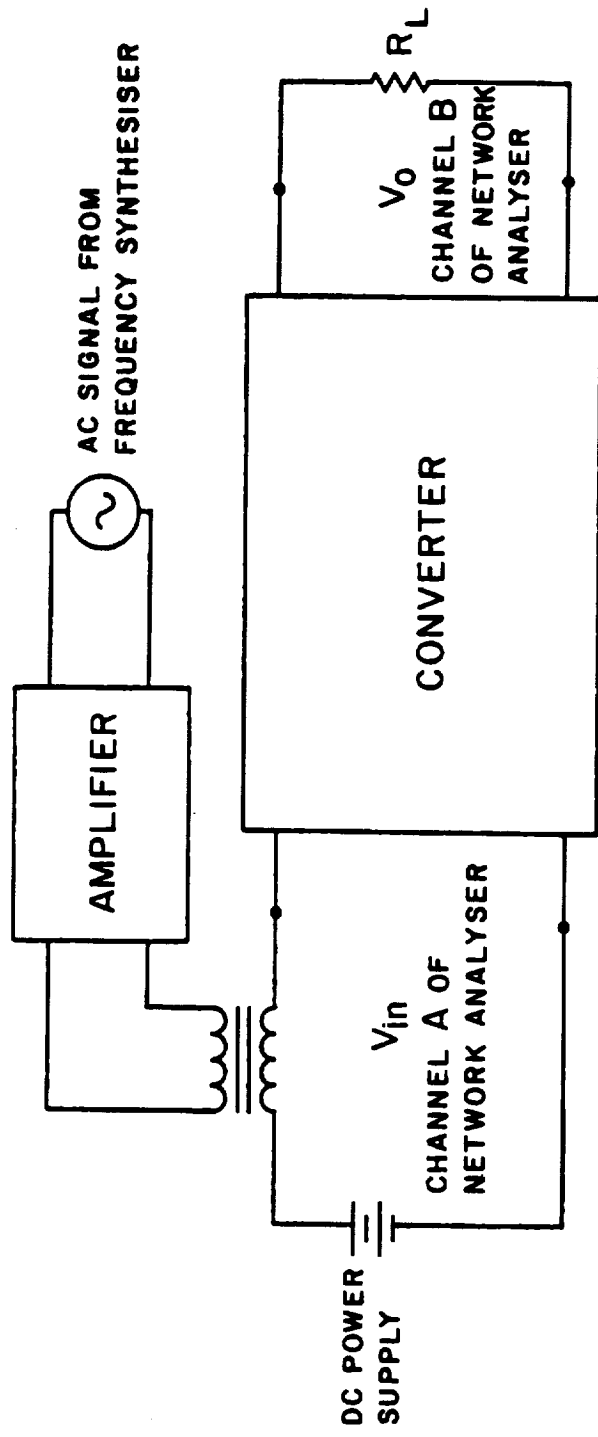


FIG. 11.6 AUDIOSUSCEPTIBILITY MEASUREMENTS



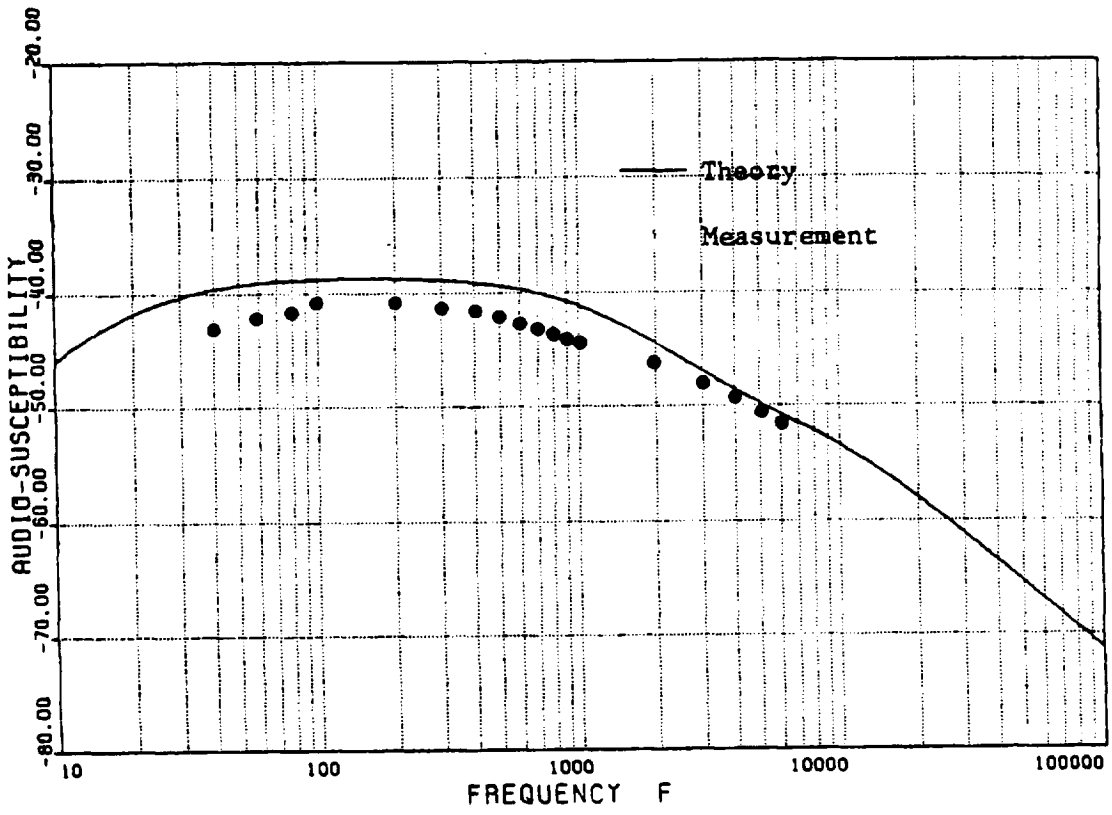


Fig. 11.7 Audio-Susceptibility Characteristic

Theory and Measurement

Mode 1 Operation

CHAPTER 12  
OUTPUT IMPEDANCE AND LOAD TRANSIENT

The converter performance due to sinusoidal disturbance of the output current can be investigated using the output impedance characteristic. The output impedance is measured as the ratio of  $\hat{v}_o(s)/\hat{i}_o(s)$ , where  $\hat{i}_o(s)$  is the sinusoidal disturbance at the converter output. The output impedance is employed to measure dc or dynamic performance of a switching regulator subjected to sinusoidal load variations. The output impedance characteristic of an open-loop regulator usually has its maximum value at the output filter resonant frequency. The undesirable large output impedance can be reduced effectively by properly designing the control loop parameters of SCM. It is desirable that the switching regulator has a minimum output impedance to imitate an ideal voltage source.

In order to derive an analytical expression for the closed-loop output impedance of the switching regulator, it is necessary to include the disturbance from the output current into the small signal model. The two-winding buck/boost regulator is employed as an example to demonstrate the small signal model incorporating the disturbance from the load.

### 12.1 Small Signal Model Including Load Disturbance

The two-winding buck/boost power stage, can be simplified into an equivalent single winding buck/boost in the following way: First the two-winding buck/boost, as shown in Fig. 12.1(a), is equivalent to the circuit configuration shown in Fig. 12.1(b) where the number of turns of the primary winding is equal to that of the secondary winding. Second, the circuit shown in Fig. 12.1(c), is identical to Fig. 12.1(b), by simple reversing the secondary winding polarity. This consequently necessitates moving the diode to the lower terminal and the positive side of  $v_o$  is connected to the lower terminal.

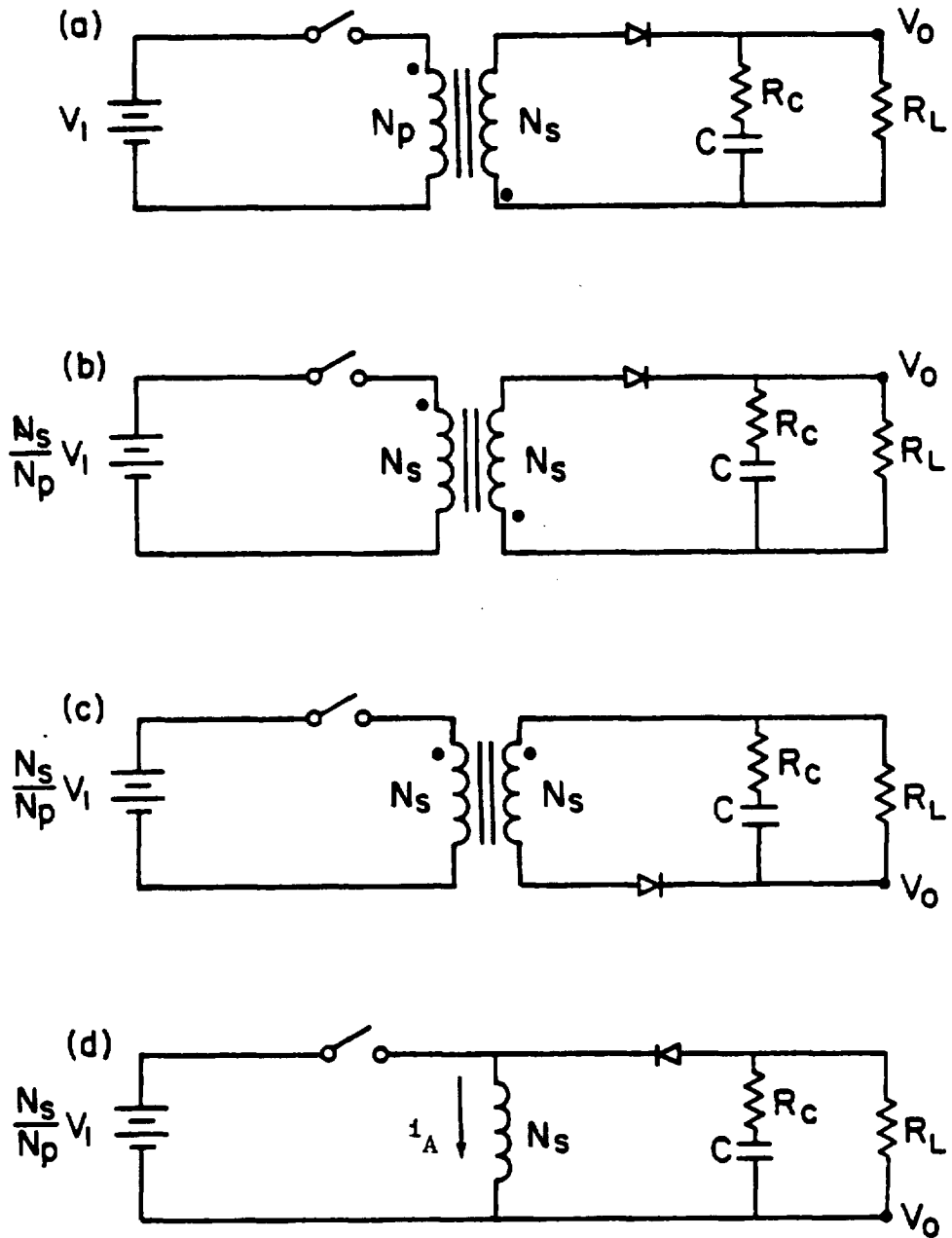


FIG. 12.1 TWO-WINDING BUCK/BOOST IS SIMPLIFIED INTO AN EQUIVALENT SINGLE WINDING BUCK/BOOST

Third, if one neglects the input and output isolation of the circuit shown in Fig. 12.1(c), the two-winding energy storage inductor can be replaced by a simple winding inductor as shown in Fig. 12.1(d).

The linear circuit model equations obtained in Ref. [9] for a single-winding buck/boost shown in Fig. 12.1(d) are listed in the following:

$$\frac{1}{\mu} = \frac{V_0}{V_I} = \frac{D}{D'} \cdot \frac{N_s}{N_p} \quad (12-1)$$

$$e_s = \frac{V_0}{D^2} \cdot \frac{N_p}{N_s} \left[ 1 - D \frac{L_e s}{R_L} \right] \quad (12-2)$$

$$J(s) = \frac{V_0}{D'^2 R_L} \quad (12-3)$$

the parasitic elements such as  $R_c$  and  $R_s$  are neglected in equations (12-1) to (12-3). If the parasitic elements are considered, equation (12-2) should be expressed as

$$e_s = \frac{V_0}{D^2} \cdot \frac{N_p}{N_s} \left[ 1 - D \frac{L_e s + R_{eq}}{R_L} \right] \quad (12-4)$$

Consider  $\hat{v}_1(s) = 0$ . The dual-input describing function shown in Fig. 5.3 can be reduced to Fig. 12.2 or represented by the canonical circuit model shown in Fig. 12.3 (similar to reference 9, Fig. 4.3).

The equivalent small-signal averaged inductor current  $\hat{i}_a(s)$  of the single-winding buck/boost can be calculated as follows:

$$\hat{i}_a(s) = \frac{1}{D'} \left[ \frac{I_o \hat{d}(s)}{D'} + \frac{\hat{v}_o(s)}{R_c + \frac{1}{sC}} + \frac{\hat{v}_o(s)}{R_L} - \hat{i}_o(s) \right] \quad (12-5)$$

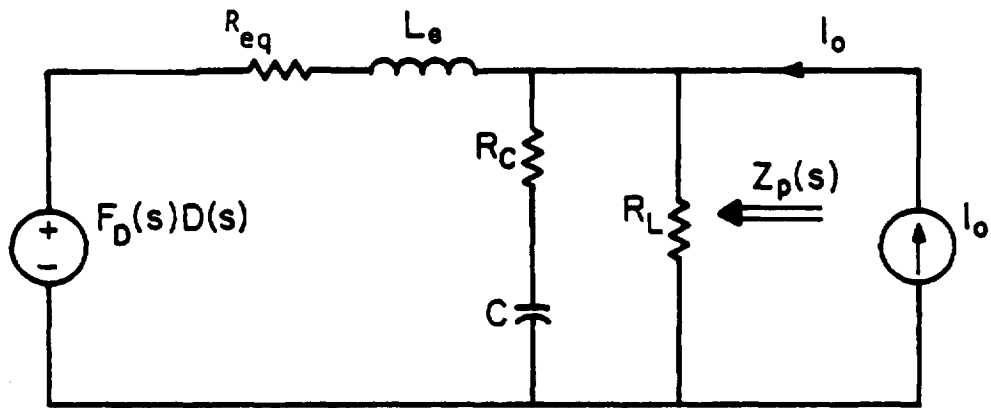


FIG. 12.2 A SINUSOIDAL DISTURBANCE AT THE CONVERTER OUTPUT REPRESENTED BY A CURRENT SOURCE  $i_o$  TO DERIVE  $Z_o(s)$

By superposition from Fig. 12.3

$$\hat{v}_o(s) = Z_p(s) \hat{i}_o(s) + F_D(s) F_p(s) \hat{d}(s) \quad (12-6)$$

where  $Z_p(s)$  is the output impedance of the power stage with the loop open.

$$Z_p(s) = \frac{(R_{eq} + L_e s)(R_c Cs + 1)R_L}{(R_{eq} + L_e s)[(R_L + R_c)Cs + 1] + (R_c Cs + 1)R_L} \quad (12-7)$$

Substituting (12-6) and the equations for F taken from Table 8.1 into equation (12-5), one can easily prove

$$\begin{aligned} \hat{i}_a(s) &= \frac{1}{D'} \left[ I_{\frac{o}{D'}} \hat{d}(s) + D' F_2(s) [Z_p(s) \hat{i}_o(s) + F_D(s) F_p(s) \hat{d}(s)] - \hat{i}_o(s) \right] \\ &= [F_1(s) + F_2(s) F_D(s) F_p(s)] \hat{d}(s) + [F_2(s) Z_p(s) - F_4(s)] \hat{i}_o(s) \end{aligned} \quad (12-8)$$

$$\text{Let } F_4(s) = \frac{1}{D'} \quad (12-9)$$

Based on equation (12-8), the small signal block diagram as shown in Fig. 8.2 can be constructed to derive the output impedance.

Apply Mason's gain formula [20] to the modified block diagram Fig. 8.2. Consider  $\hat{i}_o(s)$  is the only input and  $\hat{v}_o(s)$  is the output. The forward gain paths are:

- (1)  $Z_p(s)$  does not touch loop #1
- (2)  $F_4(s) F_3(s) F_{AC}(s) F_M(s) F_D(s) F_p(s)$  touches all the three loops

The loops are:

- #1 -  $F_M(s) F_1(s) F_3(s) F_{AC}(s)$
- #2 -  $F_M(s) F_D(s) F_p(s) F_2(s) F_3(s) F_{AC}(s)$
- #3 -  $F_M(s) F_D(s) F_p(s) F_{DC}(s)$

$$Z_o(s) = \frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{Z_p (1 + F_M F_1 F_3 F_{AC}) + F_4 F_3 F_{AC} F_M F_D F_p}{1 + G_T} \quad (12-10)$$

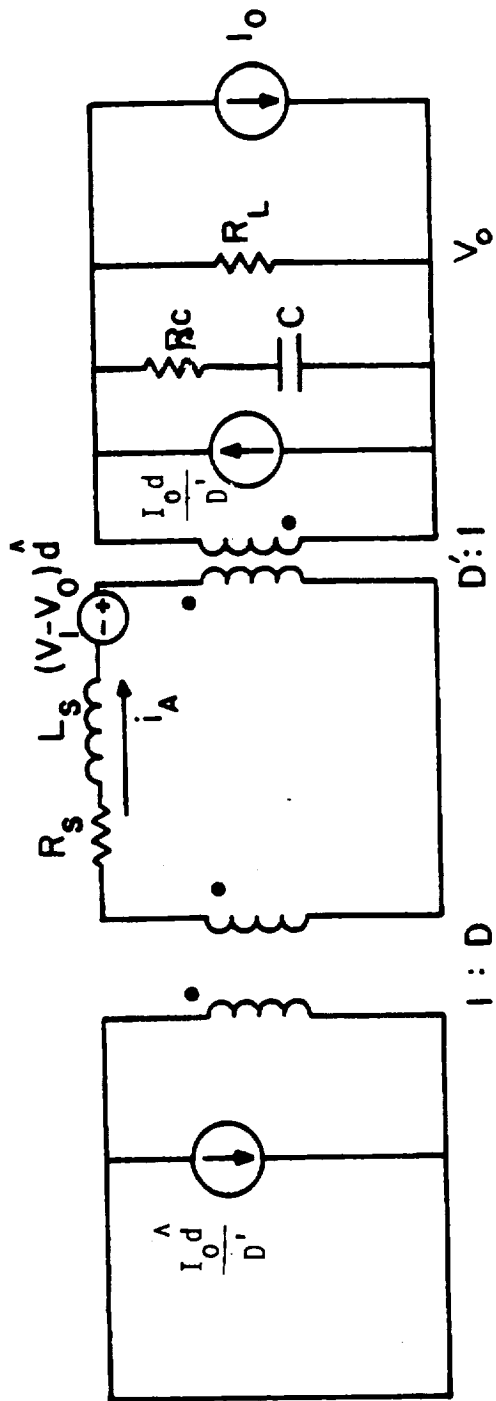


FIG. 12.3. EQUIVALENT CIRCUIT TRANSFORMATIONS OF THE FINAL CIRCUIT AVERAGED MODEL

The above equation for the closed-loop output impedance and the block diagram of Fig. 8-2 are also applicable to the buck and boost converters with

$$\begin{aligned}
 F_4 &= 1 && \text{buck} && (12-11) \\
 &= \frac{1}{D} && \text{boost and buck/boost}
 \end{aligned}$$

Substituting the equations for  $F'$  from Table 8.2 and normalizing the frequency by letting

$$s = \omega_o s \text{ (normalized),}$$

equation (12-10) becomes

$$Z_o(s) = \frac{\omega_o \tau_{z1} s + 1}{(s^2 + 2\zeta s + 1)(1 + G_T(s))} \left\{ s\omega_o L_e + \left( R_{eq} + \frac{2V_I L_e}{M} \right) \right\}$$

or

$$Z_o(s) = K_3 \frac{\omega_o \tau_{z1} s + 1}{(s^2 + 2\zeta s + L)(1 + G_T(s))} \left[ \frac{\omega_o L_e}{K_3} s + 1 \right] \quad (12-12)$$

where

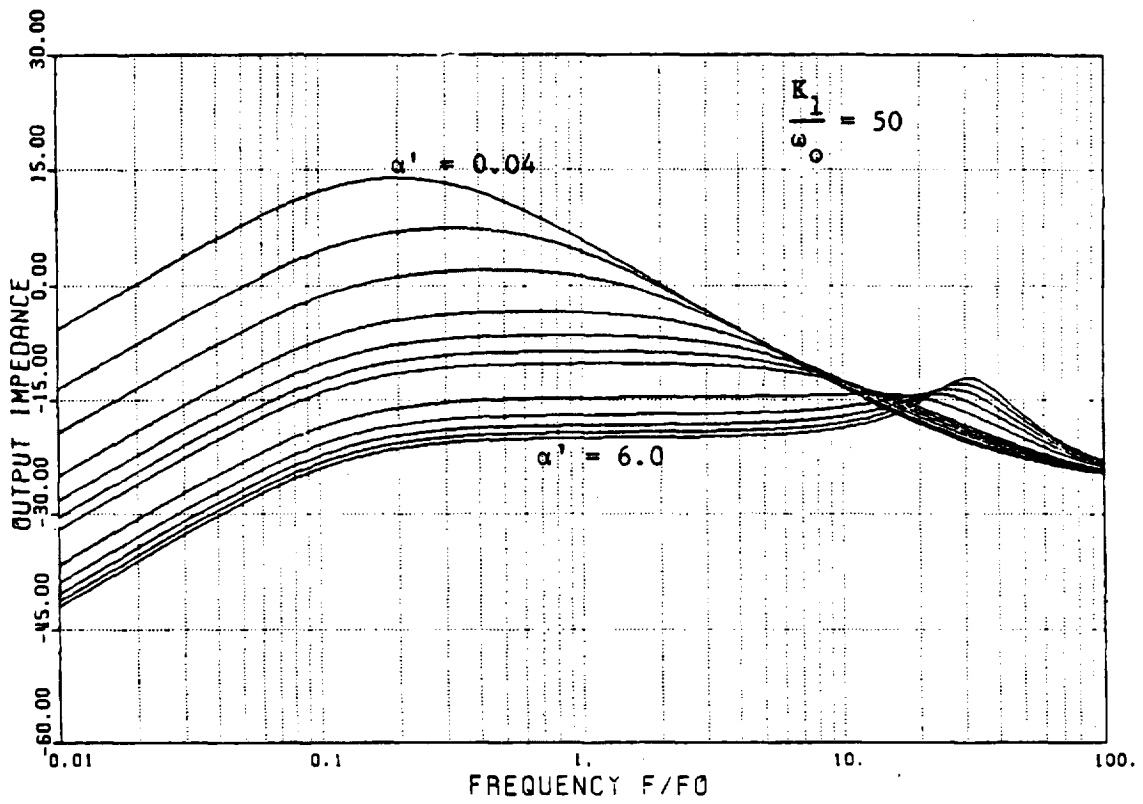
$$K_3 = R_{eq} + \frac{2V_I L_e}{M} \quad (12-13)$$

To simplify equation (12-12), assume that  $K_1$  is sufficiently large, and that the zero in the brackets in equation (12-12) has insignificant effect in the low frequency range. Then, equation (12-12) can be simplified for low frequency approximation to:

$$Z_o(s) = \frac{\omega_o L_e s}{\alpha} \frac{\omega_o \tau_{z1} s + 1}{\left( \frac{s}{s_{o1}} + 1 \right) \left( \frac{s}{s_{o2}} + 1 \right)} \quad (12-14)$$

The above simplified  $Z_o(s)$  characteristic has the same form as that of  $G_A(s)$  in (11-5). Figure 12.4 illustrates the computer plot of (12-12) for a two-





(a)

FIG. 12.4(a) OUTPUT IMPEDANCE CHARACTERISTIC OF A BUCK/BOOST CONVERTER EMPLOYING THE SAME CIRCUIT PARAMETER VALUES AS FIG. 11.2

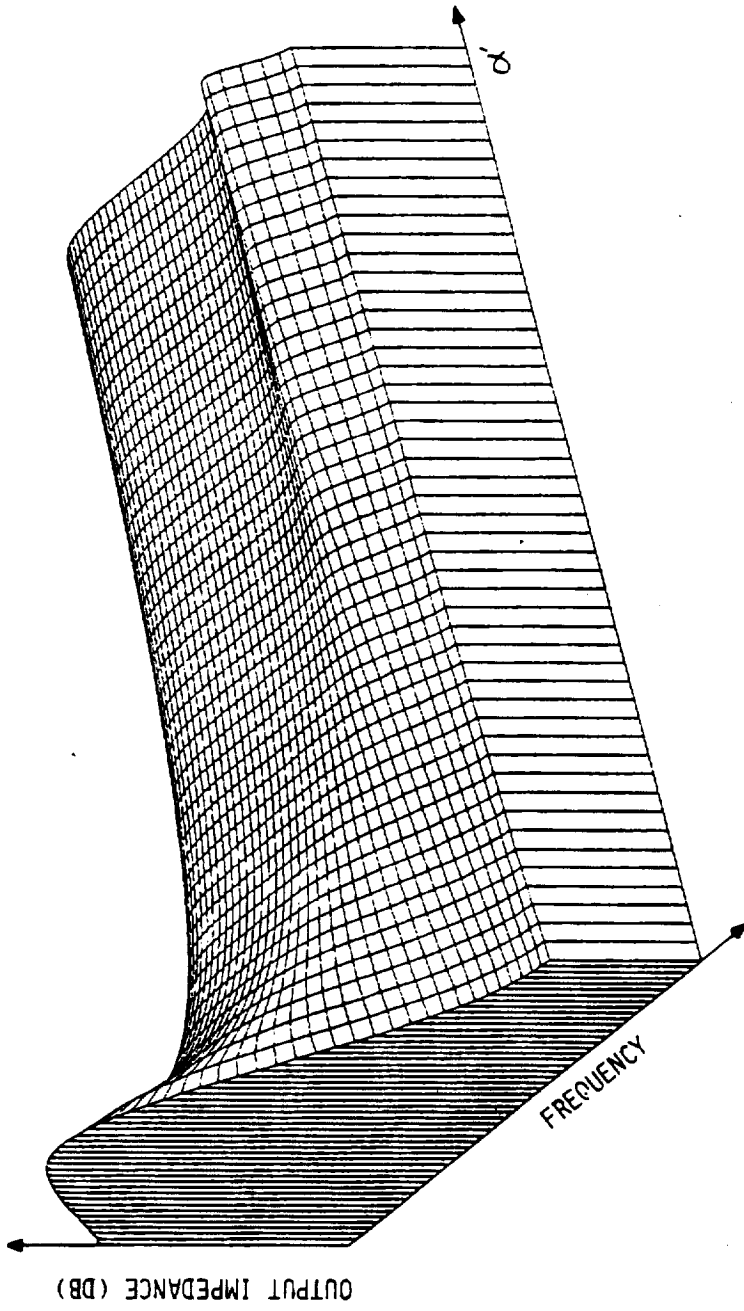


FIG. 12.4(b) THREE DIMENSIONAL PLOT OF (a)

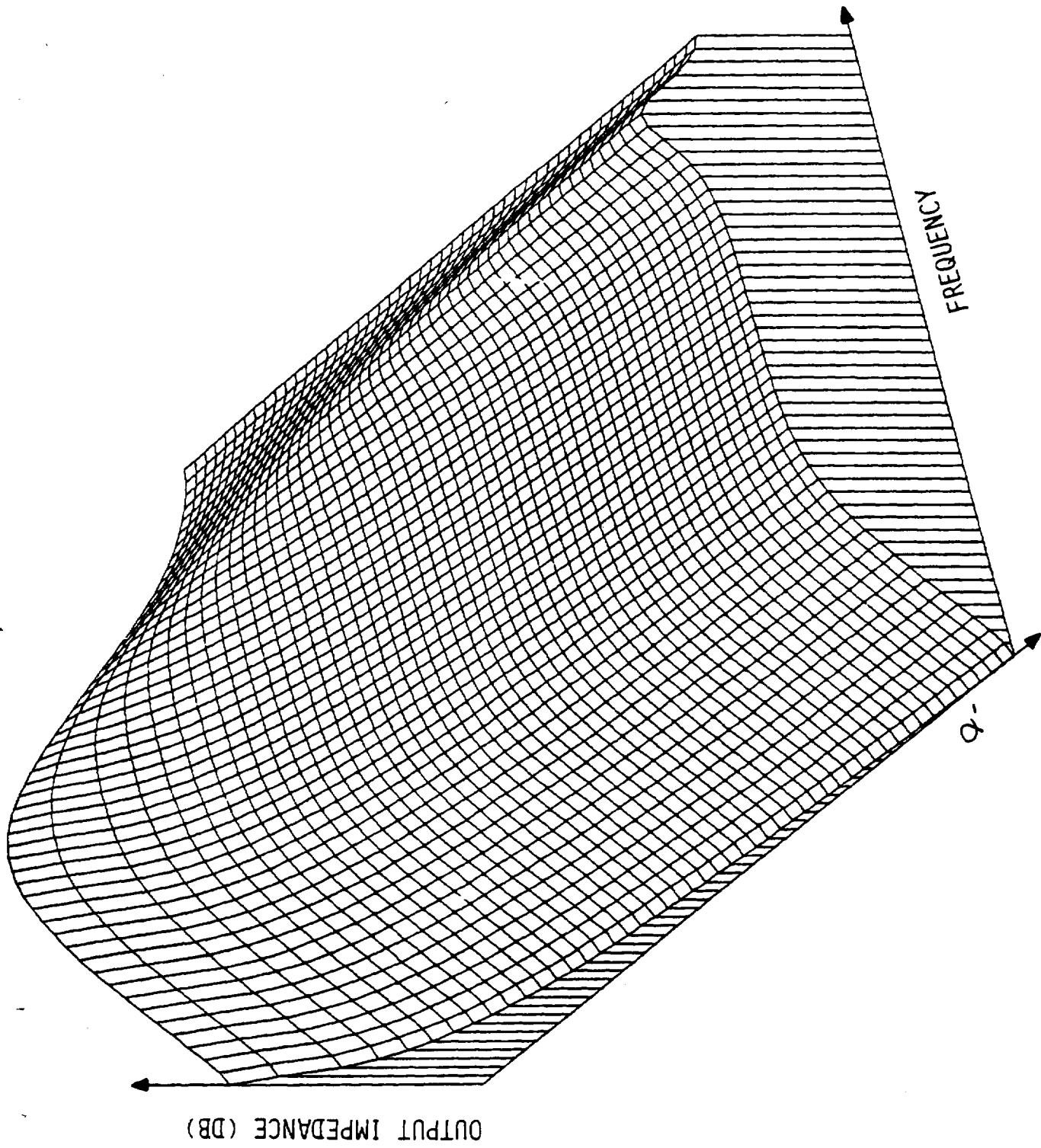


FIG. 12.4(c) THREE-DIMENSIONAL PLOT OF (a)

winding buck/boost converter having the same parameter values as employed in Fig. 11.2.

Experimental verification of the analytical model is provided in Fig. 12.5 employing the same circuit parameter values as those used in Fig. 10.2. Good correlations are shown.

## 12.2 Transient Response to Step Load Change.

Since the converter load is often subjected to step load changes, undesirable resonance between the load and the regulator due to these load changes may result in excessive disturbance of the output voltage. For this reason, the time constant of the transient responses and the amount of peaking are specified for each application. If the load change is not a severe one, such as a sudden short at the output, the output voltage of the converter usually changes only slightly. Also, the duty cycle ratio changes slightly during the entire transient. The output impedance derived in the previous section for the small model can be used to examine the transient response of the converter. For a step change of the load current  $\Delta I_o/s$ , equation (12-14) can be rewritten as

$$\Delta V_o(s) = \Delta I_o \omega_o^2 L_e \frac{\alpha'}{\alpha} \left[ \frac{B_1}{s + s'_{o1}} + \frac{B_2}{s + s'_{o2}} \right] \quad (12-15)$$

Equation (12-15) is not normalized in  $s$ . Therefore,

$$s'_{o1}, s'_{o2} = \frac{\alpha' \tau'_{z2} \omega_o^2}{2} \left[ 1 \pm \sqrt{\frac{4\alpha'}{(\alpha' \tau'_{z2} \omega_o)^2}} \right] \quad (12-16)$$

$$B_1 = \frac{-\tau_{z1} s'_{o1} + 1}{-s'_{o1} + s'_{o2}} \quad (12-17)$$

$$B_2 = \frac{\tau_{z1} s'_{o2} - 1}{-s'_{o1} + s'_{o2}} \quad (12-18)$$

where  $s'_{o1} = \omega_o s_{o1}$  and  $s'_{o2} = \omega_o s_{o2}$

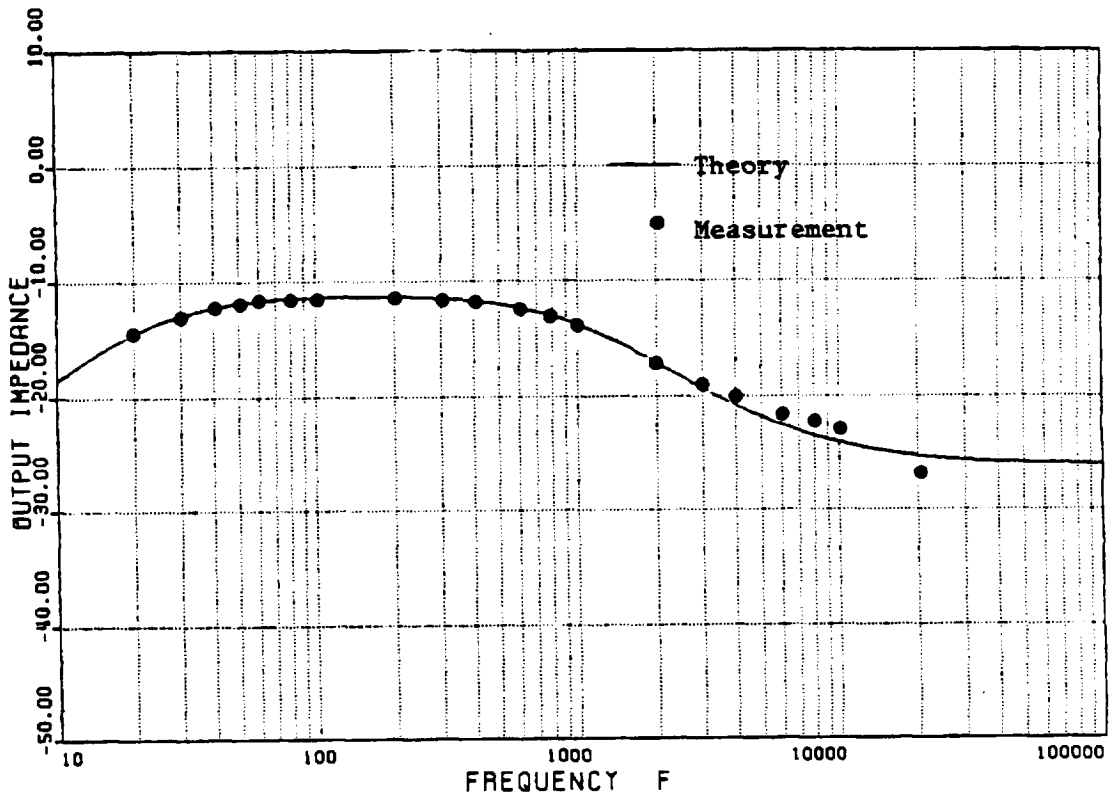


Fig. 12.5 Output Impedance Characteristic  
Theory and Measurement  
Mode 1 Operation

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The inverse transform results in the transient response as a sum of two exponential terms as follows:

$$AV_o(t) = I_o \frac{\alpha'}{\alpha} \omega_o^2 L_e [B_1 e^{-s'_{o1}t} + B_2 e^{-s'_{o2}t}] \quad (12-19)$$

The transient response of the output voltage is illustrated in Fig. 12-6. The settling time and the peaking can be determined analytically from (12-19). The time constant of transient response is usually dominated by the lower frequency term of (12-19). It is true for all practical designs that the corner frequencies are sufficiently apart ( $s'_{o1} \gg s'_{o2}$ ) as suggested in earlier chapters. It is evident from equation (12-19) that the time constant  $1/s'_{o2}$  determines the decay rate of the transient response due to a step change of load current. As a matter of fact, the smaller the time constant, the faster the transient response. However, if  $s'_{o1}$  and  $s'_{o2}$  form a complex conjugate pair as illustrated in Fig. 9.11, the transient response will be oscillatory instead of decaying exponentially. The load transient response for complex conjugate  $s'_{o1}$  and  $s'_{o2}$  as well as negative real  $s'_{o1}$  and  $s'_{o2}$  were demonstrated in Fig. 9.18.

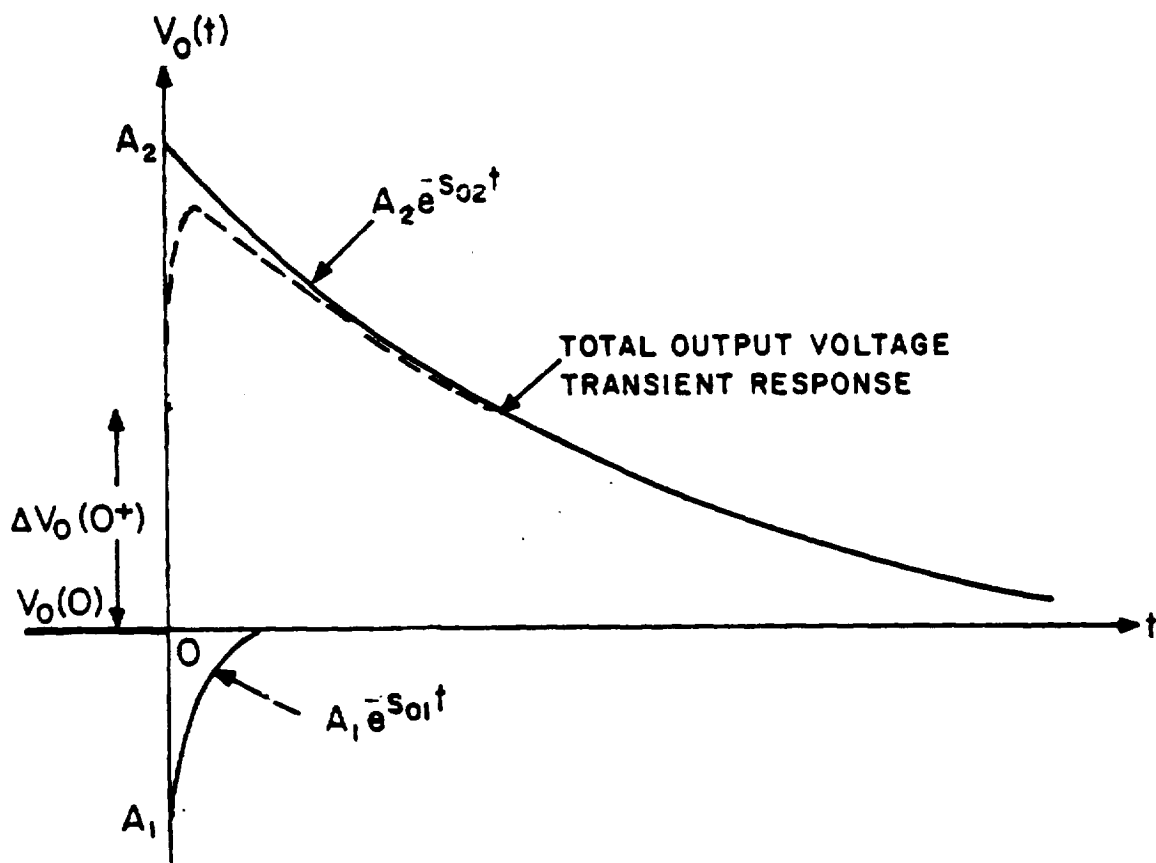


FIG. 12.6 THE OUTPUT VOLTAGE TRANSIENT RESPONSE DUE TO OUTPUT CURRENT STEP CHANGE

C-3

## CHAPTER 13

### INPUT FILTER EFFECTS TO SWITCHING REGULATOR PERFORMANCES

#### 13.1 Introduction.

The presence of the input filter often constitutes potential performance difficulties in a switching regulator. This is mostly due to an insufficient understanding of the complex interactions among input filter, output filter and the control loops. Results of significant importance have shown that the interactions between the input filter and the control loop can result in an oscillatory, or even an unstable, positive feedback system [16-20]. The objective of the present chapter is to study the interaction between the power stage and control loop in the presence of a single stage input filter. Based on the results of the analysis, design guidelines for the input filter are then formulated.

The dual input describing function is employed to analyze various small signal performances of the converter with the input filter, such as stability, audiosusceptibility, and output impedance. Employing this dual input describing function, the interaction of circuit parameters among the input filter, output filter and SCM control loops can be investigated.



### 13.2 Modeling of Power Stages With An Input Filter

The effect of the input filter is characterized by the following two parameters: the forward transfer characteristic of the input filter,  $H_F(s)$ , when the input filter is disconnected from the switching regulator and the output impedance of the input filter,  $Z_F(s)$ . The continuous mmf power stage canonical circuit model [9], including an input filter as shown in Fig. 13.1, will be analyzed. The dual inputs presented to the power stage, as shown in Fig. 13.2 can be obtained by manipulating the canonical circuit model of Fig. 13.1 (ignoring the dc components) as follows: Since the canonical equivalent circuit model preserves the input and output terminal properties, we can insert an input filter into the input side of the circuit model as shown in Fig. 13.3(a). This circuit can be simplified to the form presented in Fig. 13.3(b) where

$$H_F(s) \triangleq \frac{\hat{V}_j(s)}{\hat{V}_j(s)} \quad (13-1)$$

$$Z_F(s) \triangleq \frac{\hat{V}_j(s)}{\hat{I}_j(s)}$$

In other words, the input filter and the dc source are represented by their Thevenin equivalent circuit. The circuit model in Fig. 13.3(b) can be reduced to that shown in Fig. 13.3(c) by replacing the circuit elements to the left of the dotted line with a Thevenin equivalent circuit as shown in Fig. 13.3(c). It should be noted that the circuit model in Fig. 13.3(a) contains two independent voltage sources  $\hat{V}_j(s)$  and  $\hat{d}(s)$ . The output voltage can be expressed in terms of these two voltage sources and the transfer functions  $F'_I(s)$ ,  $F'_D(s)$  and  $F'_P(s)$  defined on page 185:

$$\hat{V}_O(s) = (F'_I(s) \hat{d}(s) + F'_D(s) \hat{V}_j(s)) F'_P(s) \quad (13-2)$$

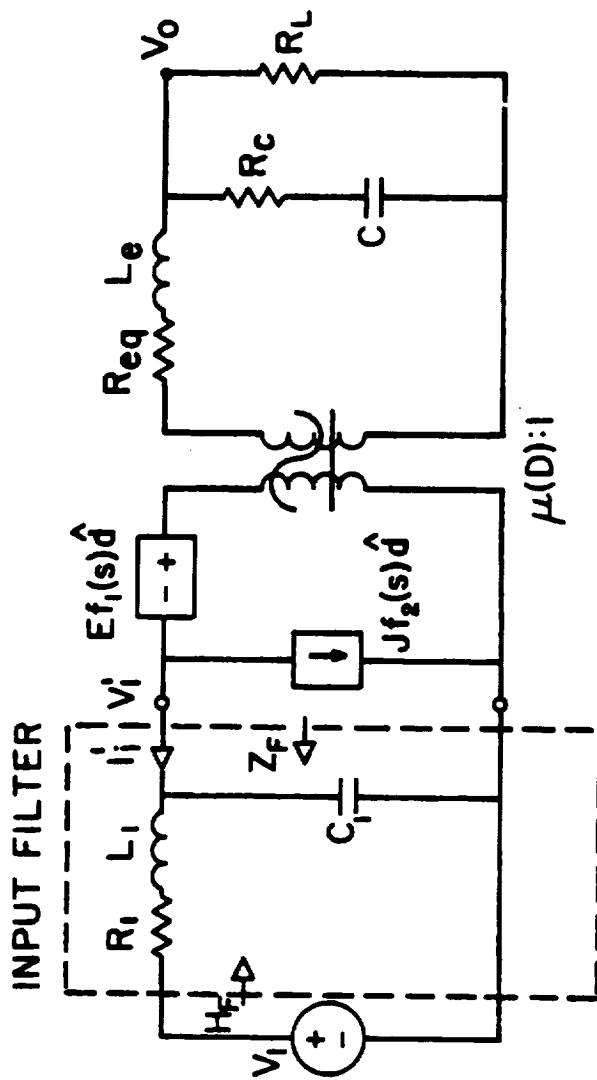


FIG. 13.1 CONTINUOUS MMF MODEL WITH INPUT FILTER

The dual-input transfer function of the power stage enjoys the same form as that shown in Fig. 5.3, except with the following modifications of  $F_I'(s)$ ,  $F_D'(s)$  and  $F_P'(s)$  where the prime sign denotes the transfer function incorporating the effect of an input filter.

$$\text{Let } \mu = \frac{1}{D} \quad (13-3)$$

$$= D'$$

$$= \frac{N_P}{N_S} \frac{D'}{D}$$

$$F_I'(s) = \frac{1}{\mu} H_F(s) \quad (13-4)$$

$$F_D'(s) = \frac{V_o}{D} \left( 1 - \frac{Z_F(s)}{\mu^2 R_L} \right) \quad \text{buck} \quad (13-5)$$

$$= \frac{V_o}{D'} \left[ \left( 1 - \frac{R_e + s\omega_o L_e}{R_L} \right) - \frac{Z_F(s)}{\mu^2 R_L} \right] \quad \text{boost}$$

$$= \frac{V_o}{DD'} \left[ \left( 1 - D \frac{R_e + s\omega_o L_e}{R_L} \right) - \frac{Z_F(s)}{\mu^2 R_L} \right] \quad \text{buck/boost}$$

and

$$F_P'(s) = \frac{\tau_{z1} \omega_o s + 1}{\frac{Z_F(s)}{\mu^2 R_L} (R_L C \omega_o s + 1) + s^2 + 2\zeta \omega_o s + 1} \frac{1}{\omega_o^2} \quad (13-6)$$

### 13.3 Input Filter Interactions

The common block diagram as shown in Fig. 8.2 is still valid for switching regulator with an input filter, simply if  $F_I(s)$ ,  $F_D(s)$  and  $F_P(s)$  are replaced by  $F_I'(s)$ ,  $F_D'(s)$  and  $F_P'(s)$  given in (13-4), (13-5) and (13-6), respectively. Employing the small signal model of Fig. 8.2, interactions

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among input filter, output filter and control loops are analyzed. The detrimental effects of the input filter to the regulator performances are investigated in the following categories.

13.3.1 Loop Stability. The stability of a switching regulator can be examined by the open-loop gain  $G_T(s)$ :

$$G_T(s) = F_M(s)F_D'(s)F_p'(s)F_{DC}(s) + F_M(s)F_3(s)F_{AC}(s)[F_1(s)+F_2(s)F_D'(s)F_p'(s)] \quad (13-7)$$

The input-filter design parameter central to the loop gain is the filter output impedance  $Z_F(s)$  which affects the transfer function  $F_D'(s)$  and  $F_p'(s)$ .

1) The output impedance  $Z_F(s)$  is related to the duty-cycle power-stage gain  $F_D'$  through equation (13-5) which can be rewritten for the normalized  $s$  as

$$F_D'(s) = \frac{DV_o}{R_L} [\mu^2 R_L - Z_F(s)] \quad \text{buck} \quad (13-8)$$

$$= \frac{1}{D^2} \frac{V_o}{R_L} [\mu^2 R_L (1 - \frac{R_{eq} + s\omega_o L_e}{R_L}) - Z_F(s)] \quad \text{boost}$$

$$= \left( \frac{N_s}{N_p} \right)^2 \frac{D}{D^2} \frac{V_o}{R_L} [\mu^2 R_L (1 - D \frac{R_{eq} + s\omega_o L_e}{R_L}) - Z_F(s)] \quad \text{buck/boost}$$

where  $\mu^2 R_L$  is the absolute value of the negative resistance of a switching regulator at a given operating condition. As a rule of thumb for the input filter design, the peak magnitude of  $Z_F(s)$  (which occurs at resonance) should not be greater than the absolute value of the negative impedance of the regulator

$$Z_F(j\frac{\omega_1}{\omega_o}) < \mu^2 R_L \quad (13-9)$$

Excessive output impedance  $Z_F(s)$  at the resonant frequency  $\omega_1$  of the input filter can result in a negative duty-cycle power-stage gain. The negative

duty-cycle power-stage gain  $F'_D(s)$  together with the negative feedback loop will contribute to an unstable positive feedback system.

2) The output impedance is related to the power-stage transfer function  $F'_p(s)$  through equation (13-6) which can be expressed as

$$F'_p(s) = \frac{(R_c + \frac{1}{s\omega_o C}) \parallel R_L}{Z_F(s) + Z_1(s)} \frac{1}{\omega_o^2} \quad (13-10)$$

where  $Z_1(s) = R_{eq} + s\omega_o L_e + (R_c + \frac{1}{s\omega_o C}) \parallel R_L$  (13-11)

is the input impedance of the equivalent output filter of the power-stage.

Excessive  $Z_F(s)$  at the resonant frequency can significantly reduce  $F'_p(s)$ , therefore, the loop gain.

Figure 13.4 (a) and (b) illustrates the duty-cycle-to-output transfer function  $F'_D(s) \cdot F'_p(s)$  of a buck converter when an improperly designed input filter is employed. The filter parameters are  $L_1 = 77\mu\text{H}$ ,  $R_1 = 39.6\text{m}\Omega$  and  $C_1 = 412\mu\text{f}$ . The buck converter power stage parameters are  $V_I = 12\text{V}$ ,  $V_O = 5\text{V}$ ,  $R_L = 0.86\Omega$ ,  $L = 200\mu\text{H}$ ,  $R_e = 20\text{m}\Omega$ ,  $C = 1540\mu\text{F}$ ,  $R_c = 7\text{m}\Omega$  and switching period  $T_p = 50\mu\text{s}$ . (For detailed information please refer to Reference 17.) The solid curves of Fig. 13.4(a) and (b) represent the transfer characteristic without an input filter and the dotted curves represent that with an input filter. A sharp reduction of the gain accompanying with a rapid change of phase occurs at the input filter resonant frequency which not only causes loop instability but also severely degrades the transient response from a presumably well-damped system to an oscillatory one. Figure 13.5 illustrates the open-loop gain and phase plot of a buck/boost regulator with the same circuit parameter valued employed for Figure 10.7. The same input filter design as given in the previous example is used which

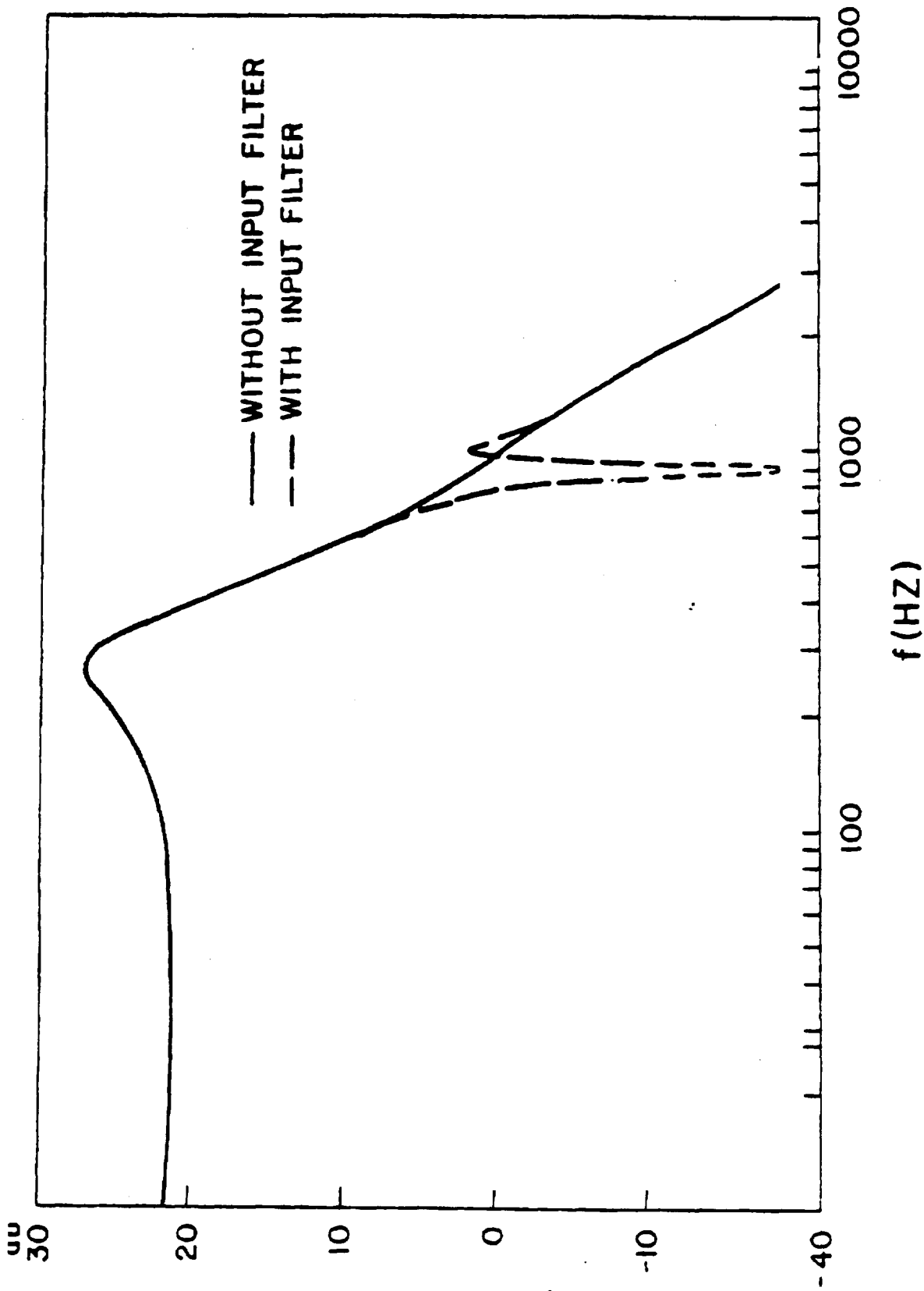


Fig.13.4 Duty-cycle-to-output voltage transfer characteristic with and without an input filter (a) gain

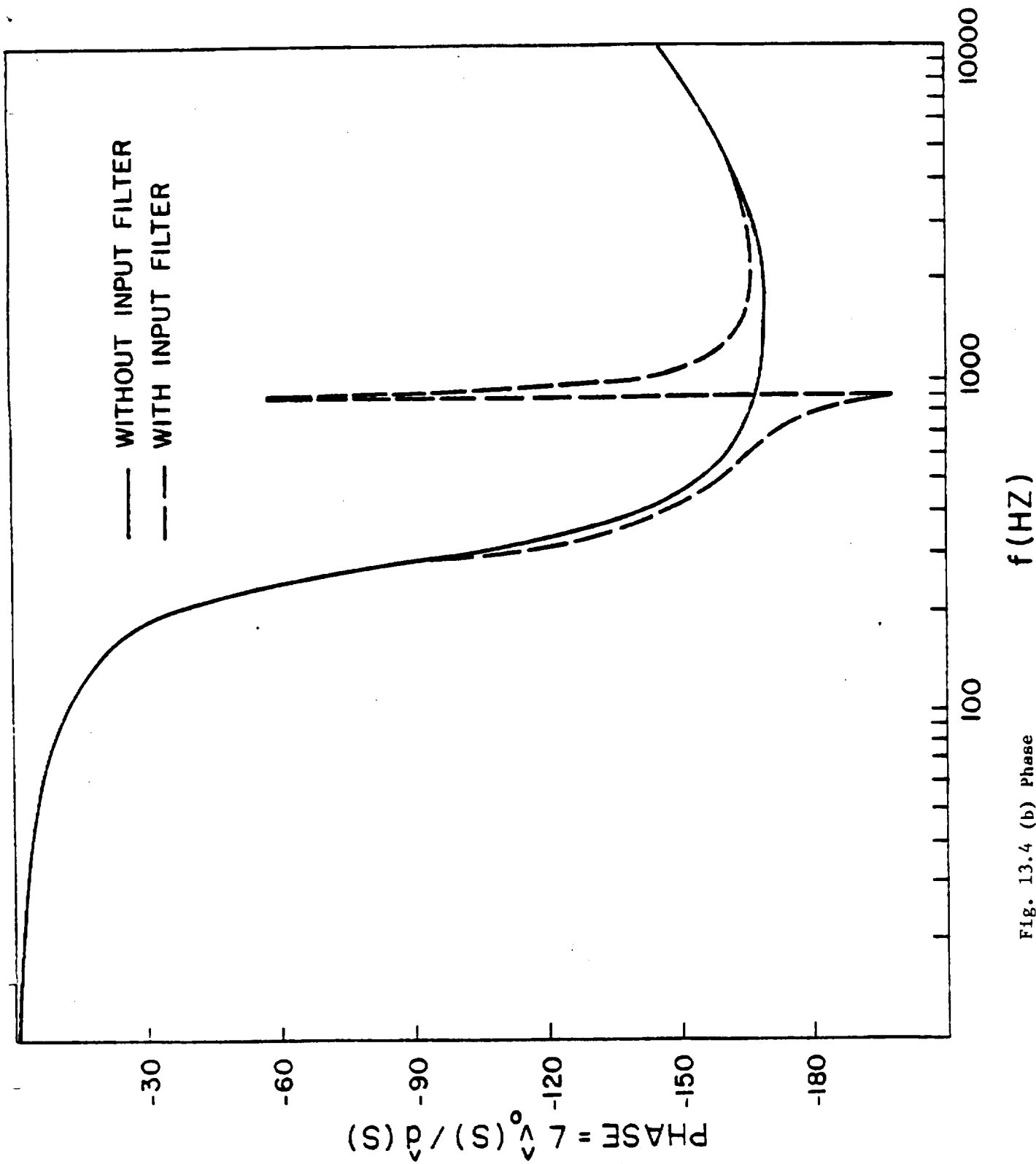
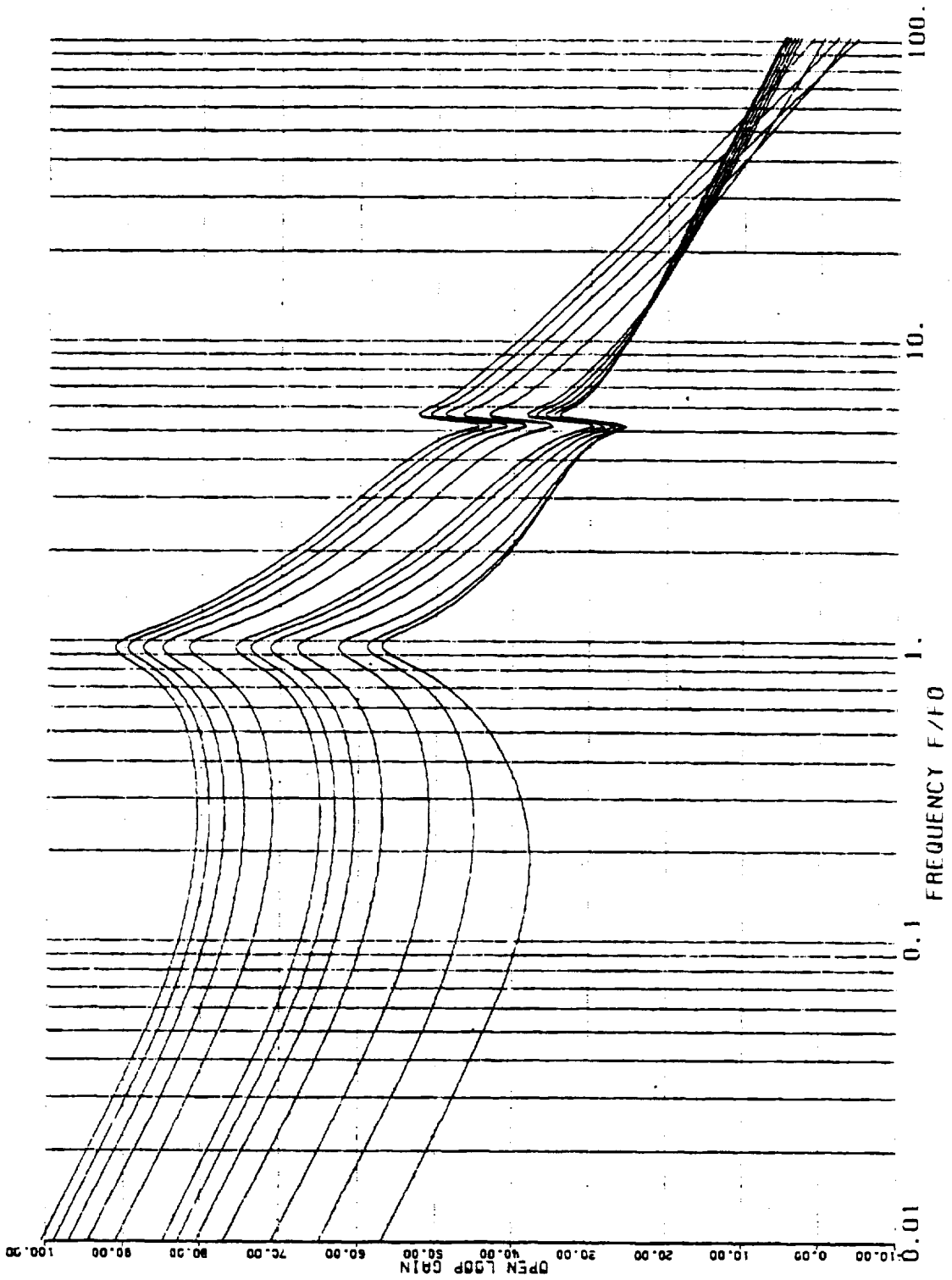


Fig. 13.4 (b) Phase



$$H_F(j\omega_1) = 11 \quad z_F(j\omega_1) = 4.75$$

Fig. 13.5(a) The effect of the Input Filter on the Open Loop Characteristic (Gain)



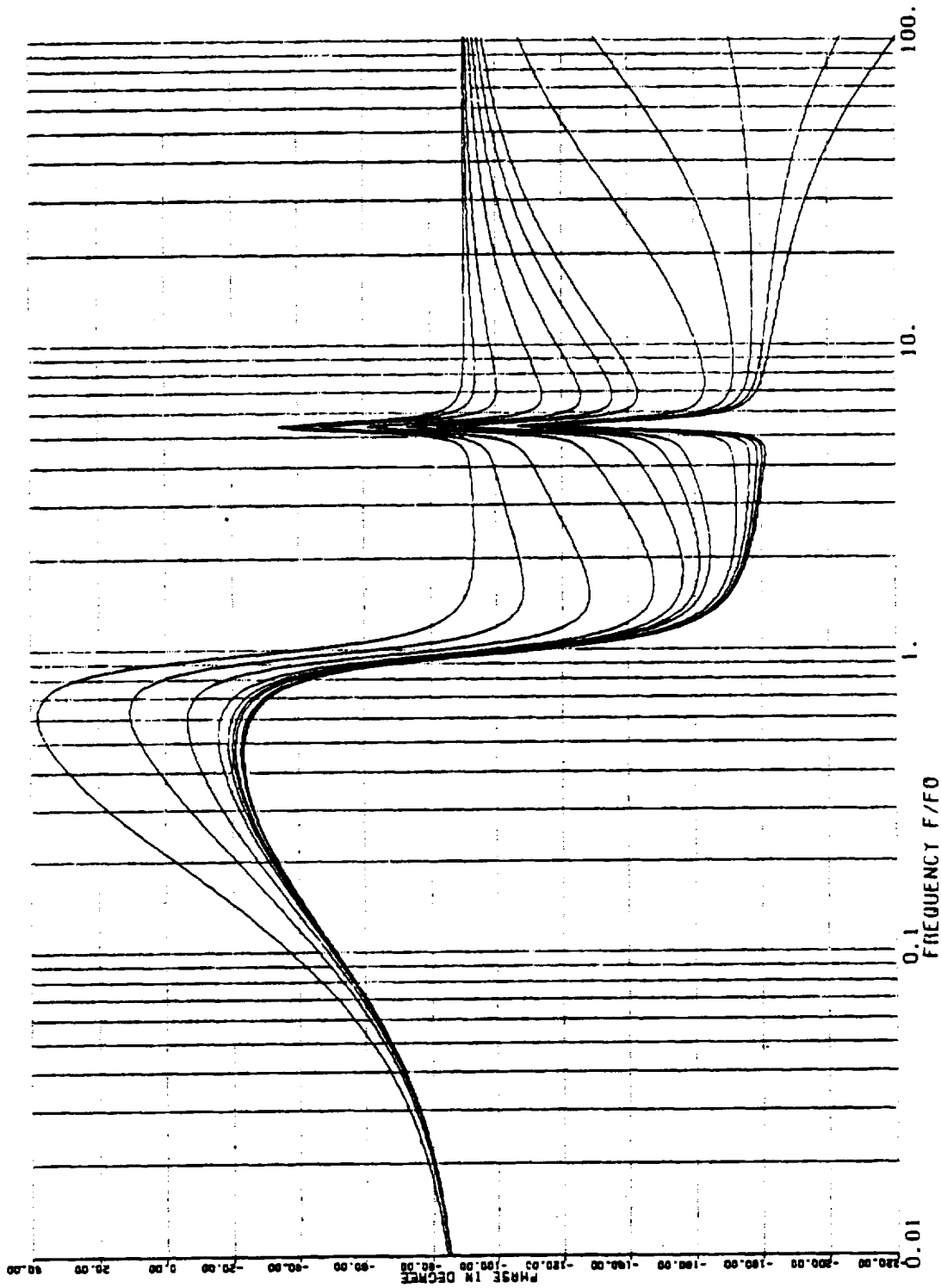


Fig. 13.5(b) The Effect of the Input Filter on the Open Loop Characteristic (Phase)

gives an exaggerated  $Z_F(j\omega_1) = 4.75$  and  $H_F(j\omega_1) = 11$  to demonstrate the effect of an input filter. It is interesting to note that although there are significant gain and phase disturbances at the input filter resonant frequency, the high cross over frequencies and phase margins are nevertheless unperturbed. This is primarily due to the high-gain wide-bandwidth nature of the open-loop characteristic contributed by the particular SCM control scheme. Therefore, the loop instability due to the input filter interaction is alleviated with SCM control.

13.3.2 Audiosusceptibility. The audiosusceptibility is expressed as

$$G'_A(s) = \frac{F'_I(s)F'_P(s)[1+F_1(s)F_3(s)F_{AC}(s)F_M(s)]}{1 + G'_T(s)} \quad (13-12)$$

The forward transfer function  $H_F(s)$  is related to the transfer function  $F'_I(s)$  as given in equation (13-4). Excessive peaking of  $H_F(s)$  can result in severe degradation of the audiosusceptibility of the regulator. Figure 13.6 illustrates the audiosusceptibility of a buck/boost converter with an input filter for different values of  $\alpha'$ . For  $\alpha' = 1$ , approximately 23 dB of the peaking is observed. This peaking is caused to a large extent by the peaking of  $H_F(s)$  shown in the transfer function  $F'_I(s)$ .

The particular peaking effect at very high frequency as discussed in Fig. 11.2 is unimportant since it is largely attenuated by the input filter.

13.3.3 Output Impedance Characteristic.

The output impedance, as given in Chapter 12, is:

$$Z_O(s) = \frac{Z_P(s)[1 + F_1(s)F_3(s)F_{AC}(s)F_M(s)]}{1 + G'_T(s)} + \frac{F_D(s)F'_P(s)F_3(s)F_{AC}(s)F_M(s)F_4(s)}{1 + G'_T(s)} \quad (13-13)$$

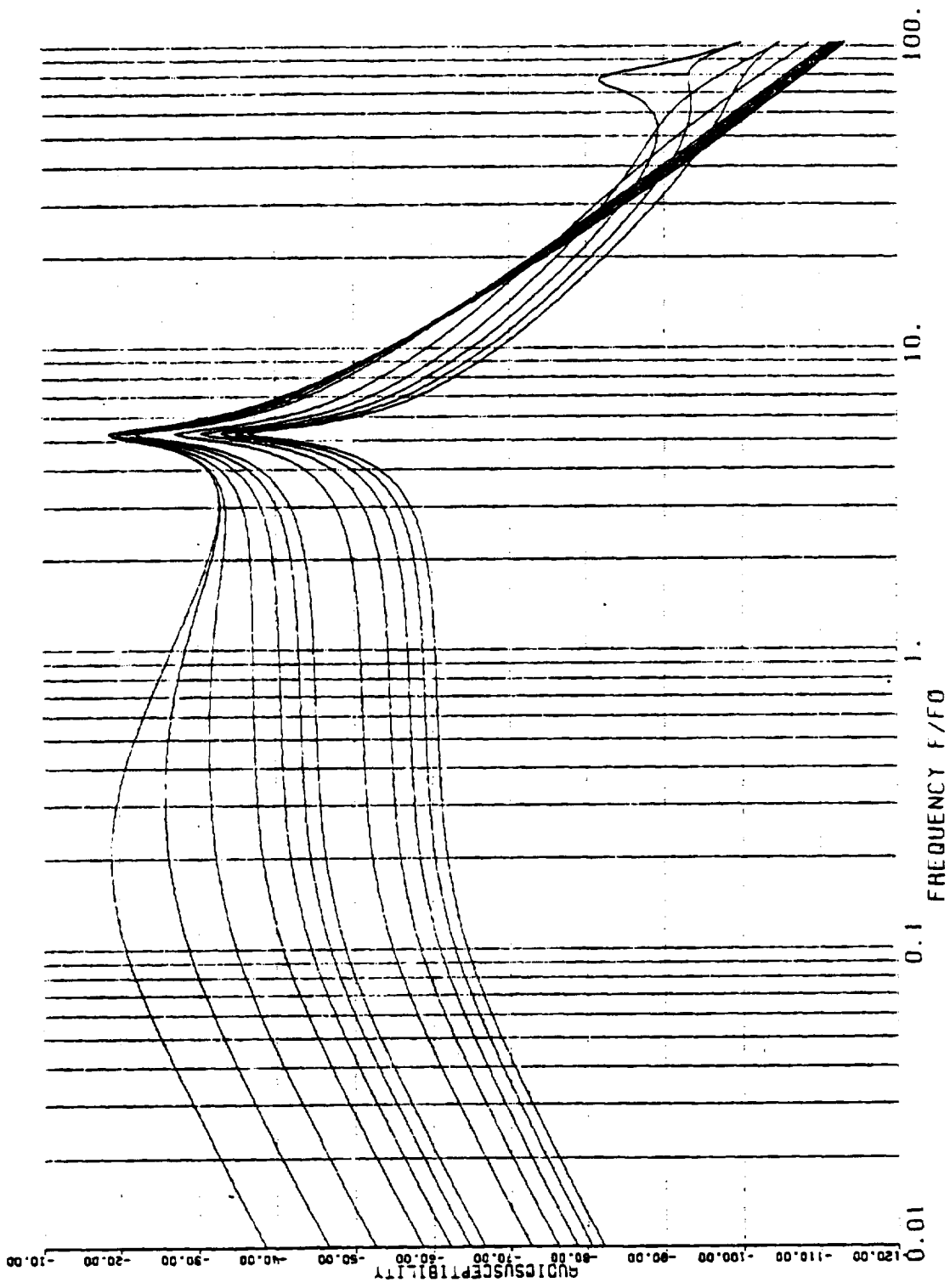


Fig. 13.6 The effect of the Input filter on the Audio-susceptibility Characteristic

Fig. 13.7 illustrates the output impedance characteristic of the converter with an input filter for different values of  $\alpha'$ . The filter interaction is less noticeable here than in the audiosusceptibility of the open loop characteristic because the output impedance of the power stage  $Z_p(s)$  is less sensitive to the input filter peaking effect.

#### 13.4 Input Filter Design Constraints.

The effect of the input filter interaction on the regulator performances was briefly discussed in the previous sections. The following significant results are drawn:

- (1) Insufficient damping at the resonant frequency of an input filter can result in an unstable system.
- (2) A necessary condition to avoid system instability due to the input filter interaction is to maintain the inequality derived from eq. (13-8)

$$\frac{V_I}{I_I} \left( 1 - D \frac{R_{eq} + s\omega L_o}{R_L} \right) - Z_F(s) > 0 \quad (13-14)$$

- (3) The resonant peaking of  $H(s)$  is the dominating factor in determining the degradation of the audiosusceptibility characteristics
- (4) The degradation of the output impedance due to the input filter interaction is usually negligible in SCM-controlled switching regulators.

Due to the high-loop-gain wide-bandwidth nature of the SCM controlled switching regulators, the performance degradation in the presence of an input filter is considerably less pronounced compared to that of the conventional single-loop control system. As illustrated in Fig. 13.5, the loop-gain reduction due to the input filter interaction occurs at a frequency less than one-tenth of the open-loop crossover frequency where there exists a sufficiently large gain (about 40 db) to off-set the loop-gain reduction due to

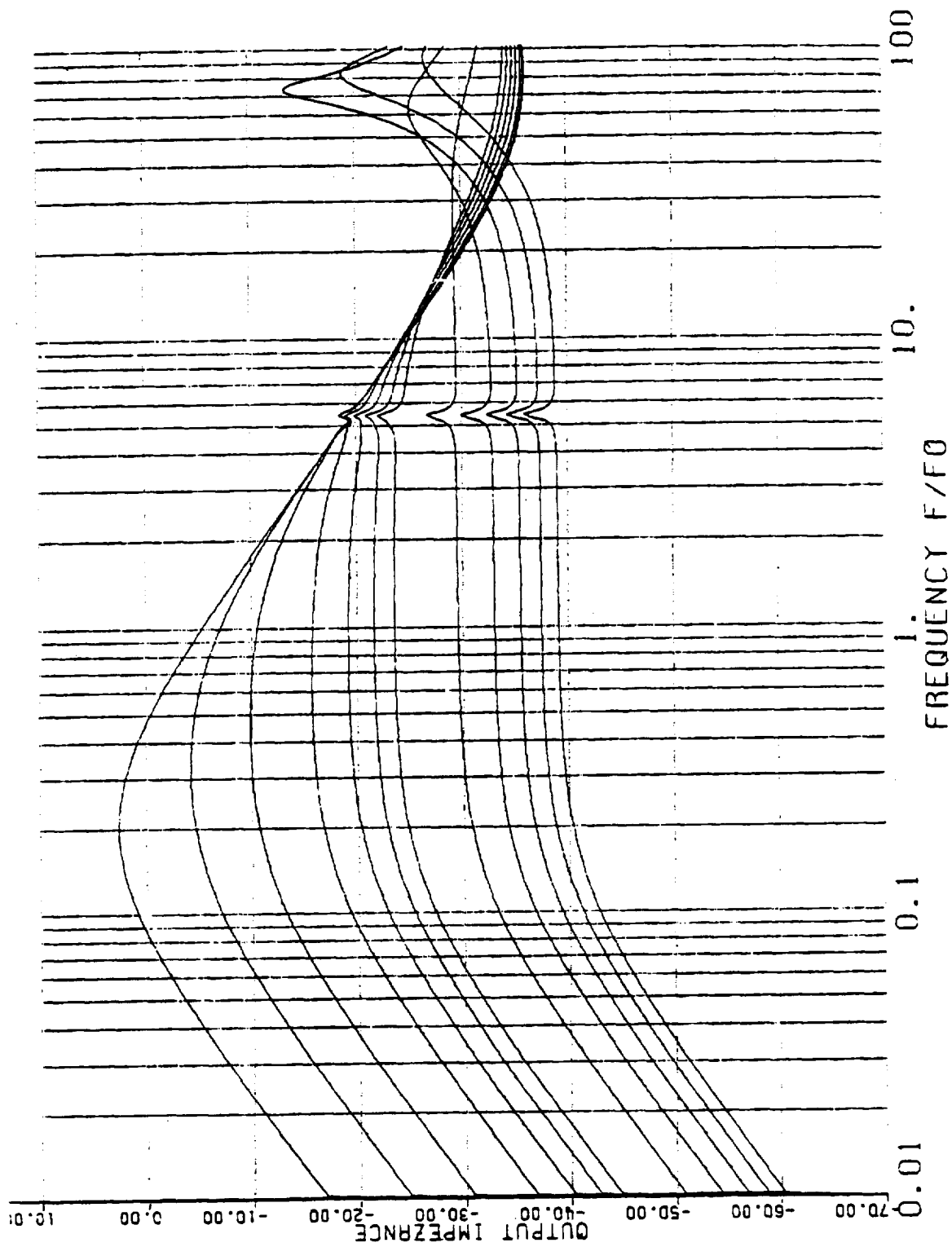


FIG. 13.7 THE EFFECT OF THE INPUT FILTER ON THE OUTPUT IMPEDANCE CHARACTERISTIC

an input filter.

Some basic design constraints are presented in Volume II of the report to alleviate the detrimental effect of the input filter on switching regulator performances.

If the reader desires further information on the material contained in this chapter, consult reference [17].

CHAPTER 14  
MODELING AND ANALYSIS OF SWITCHING REGULATORS  
IN DISCONTINUOUS INDUCTOR MMF OPERATION

The average models of switching regulators operating in a continuous inductor mmf mode (Mode 1) have been presented in the previous chapters. The models are no longer valid if the inductor mmf reduces to zero and dwells at zero for a fraction of a cycle (Mode 2). It is demonstrated in Fig. 3.1 that during one cycle of operation, there exist three different circuit topologies of the power stage, each corresponding to a certain specified time interval. The time interval  $T_{on}$  represents the time when the power switch is on and the diode is off,  $T_{f1}$  represents the time when the power switch is off and the diode is on, and  $T_{f2}$  represents the time when both the power switch and the diode are off. If the converter is restricted to operate only at continuous inductor mmf, the time interval  $T_{f2}$  does not exist, and the order of the system remains uniform throughout the cycle. Recently Ćuk [10] has presented an approach which is capable of representing switching regulators operating in both Mode 1 and Mode 2 by a linearized average model.

In Chapter 5, the canonical circuit models for the power stage of the three basic regulators were derived for Mode 1 operation by employing the state-space averaging technique. For Mode 2 operation, the average models for SCM-controlled regulators are derived using the averaging techniques in conjunction with topology manipulation. The two-winding buck/boost converter is chosen as an illustrative example. The results for the other two converter types are also summarized.

It should be noted that the average models for Mode 2 operation are derived here to permit analytical investigation of the switching regulator characteristics in the discontinuous mode of operation. Recall that the switching regulator model and characteristics for Mode 2 operation are quite different from that of Mode 1 operation and utilization of Mode 2 is rather limited. Because of the higher component stress and larger output ripples, the authors feel that it

is impractical to extend the SCM design guideline to include Mode 2 operation. It is recognized, however, that the regulator performance characteristics and stability margins are usually improved instead of deteriorated in Mode 2 compared over that of Mode 1. For design purpose and worst case consideration, the Mode 2 operation can be generally ignored. The SCM design guidelines to be presented in Volume II of the report are constrained to only Mode 1 operation. It is intended that the analytical models presented in this chapter be used only for the purpose of analyzing the regulator characteristics in Mode 2 operation.

#### 14.1 Power Stage Model of the Buck/Boost Converter with Discontinuous MMF

The average model for the three basic power stages operating in the discontinuous mmf mode were derived by Cúk (10), and expressed in the canonical circuit form shown in Figure 14.1. This canonical circuit model is seen to be of first order only. The inductor mmf no longer constitutes a state variable since it always reduces to zero at the end of each cycle and no longer possesses the free boundary properties. The input of Figure 14.1 has been modified to include the effect of the input filter. Parameter values for the canonical circuit model are summarized in Table 14.1 for the three basic power stages in Mode 2 operation. It should be noted that the letter M carries a new significance in this chapter.

Since the canonical model was derived for a single-winding buck/boost power stage in reference 10, the circuit topology manipulation discussed in chapter 13 was used to derive an equivalence between the two-winding buck/boost and a single-winding buck/boost. The expressions for elements  $j_1$ ,  $r_1$ ,  $g_1$ ,  $j_2$ ,  $r_2$ ,  $g_2$ , M, and K in the canonical circuit model for the two-winding buck/boost power stage were readily obtained from the earlier modeling effort. These expressions are listed in eq.14.1 through 14.3 along with expressions for  $Z(s)$  and  $H(s)$ .



TABLE 14-1 PARAMETER VALUES FOR THE CANONICAL CIRCUIT MODEL OF  
FIGURE 14.1 IN MODE 2 OPERATION

TYPE	M	K	$j_1$	$r_1$	$g_1$	$j_2$	$r_2$	$g_2$	Z	H
BUCK	$\frac{P}{D+D_2}$	$\frac{2L}{R_L T_P}$	$\frac{2V_0 \sqrt{1-M}}{R_L \sqrt{K}}$	$\frac{1-M}{M^2} R_L$	$\frac{M^2}{1-M} \frac{1}{R_L}$	$\frac{2V_0 \sqrt{1-M}}{R_L \sqrt{K}}$	$(1-M)R_L$	$\frac{M(2-M)}{1-M} \frac{1}{R_L}$	$Z_F$	$H_F$
BOOST	$\frac{D+D_2}{D_2}$	$\frac{2L}{R_L T_P}$	$\frac{2V_0 \sqrt{M}}{R_L \sqrt{K(M-1)}}$	$\frac{M-1}{M^3} R_L$	$\frac{M}{M-1} \frac{1}{R_L}$	$\frac{2V_0}{R_L \sqrt{KM(M-1)}}$	$\frac{M-1}{M} R_L$	$\frac{M(2M-1)}{M-1} \frac{1}{R_L}$	$Z_F$	$H_F$
BUCK/ BOOST	$\frac{D}{D_2}$	$\frac{2L_S}{R_L T_P}$	$\frac{2V_0}{R_L \sqrt{K}}$	$\frac{R_L}{M^2}$	0	$\frac{2V_0}{R_L \sqrt{KM}}$	$R_L$	$\frac{2M}{R_L}$	$\left(\frac{N_S}{N_P}\right)^2 Z_F$	$\frac{N_S}{N_P} H_F$

where  $D \triangleq \frac{T_{on}}{T_P}$ ,  $D_2 \triangleq \frac{\Delta}{T_P}$ ,  $D_3 \triangleq 1-D-D_2$

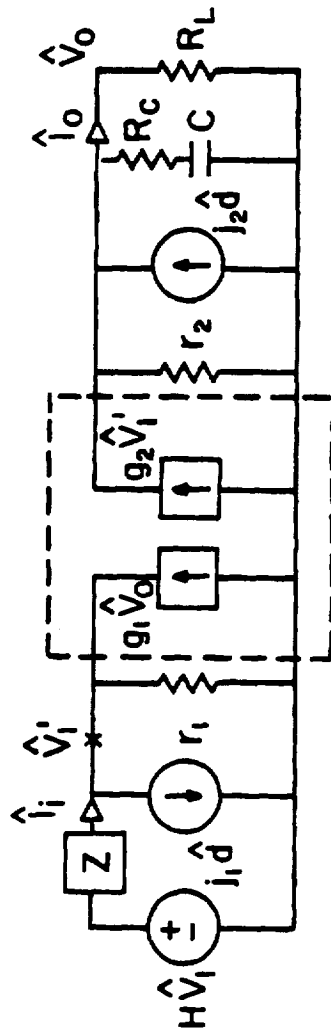


FIG. 14.1 FINAL AC SMALL SIGNAL CIRCUIT MODEL FOR CONVERTERS IN THE DISCONTINUOUS CONDUCTION MODE [10]

$$\left. \begin{aligned}
 j_1 &= \frac{2V_0}{R_L \sqrt{K}} \\
 r_1 &= \frac{R_L}{M^2} \\
 g_1 &= 0 \\
 j_2 &= \frac{2V_0}{R_L \sqrt{KM}} \\
 r_2 &= R_L \\
 g_2 &= \frac{2M}{R_L} \\
 Z(s) &= \left( \frac{N_s}{N_p} \right)^2 Z_F(s) \\
 H(s) &= \left( \frac{N_s}{N_p} \right) H_F(s)
 \end{aligned} \right\} \quad (14.1)$$

where

$$M = \frac{D}{D_2} \quad (14.2)$$

$$K = \frac{2L_s}{R_L T_p} \quad (14.3)$$

Since there exists three switching time intervals during one complete cycle of operation, the duty cycle ratio  $D$  and  $D_2$  are defined

$$D \triangleq \frac{T_{on}}{T_p} \quad (14.4)$$

$$D_2 \triangleq \frac{T_{fl}}{T_p}$$

where  $T_{on}$ ,  $T_{fl}$  and  $T_p$  are defined in Fig. 3.1(b).

The dual input describing function of the power stage, as

shown in Fig. 14.2, can be derived from the canonical circuit model. A brief derivation from the circuit model to the block diagram transfer function is presented in the following.

It is straightforward to show from Fig. 14.1 that:

$$\hat{v}_o(s) = \frac{\frac{1}{Z(s) + r_1} \{ [j_1 r_1 - Z(s)(j_1 g_2 r_1 - j_2)] \hat{d}(s) + g_2 r_1 H(s) \hat{v}_1(s) - v_o(s) \}}{\frac{1}{R_L} + \frac{1}{r_2} + \frac{1}{R_c + 1/sC} - \frac{g_1 g_2 Z(s) r_1 + 1}{Z(s) + r_1}} \quad (14-5)$$

Equation (14.5) can be expressed as

$$\hat{v}_o(s) = F_P(s) [F_I(s) \hat{v}_1(s) + F_D(s) \hat{d}(s)] \quad (14.6)$$

where

$$F_P(s) = \frac{Z_x(s)}{Z(s) + r_1 + Z_x(s)} \quad (14.7)$$

where

$$Z_x(s) = R_L // r_2 // (R_c + 1/sC) // \frac{-(Z(s) + r_1)}{1 + g_1 g_2 Z(s) r_1} \quad (14.8)$$

$$F_I(s) = g_2 r_1 H(s) \quad (14.9)$$

$$F_D(s) = j_2 r_1 - Z(s)(j_1 g_2 r_1 - j_2) \quad (14.10)$$

Substituting from (14.1) into (14.7), (14.8), (14.9) and (14.10), and using (14.8) in (14.7):

$$F_P(s) = \frac{R_L (R_c Cs + 1)}{2 \left[ \left( \frac{R_L}{2} + R_c \right) Cs + 1 \right] \left[ Z(s) + \frac{R_L}{M^2} \right]} \quad (14.11)$$

$$F_I(s) = \frac{2}{M} H(s) \quad (14.12)$$

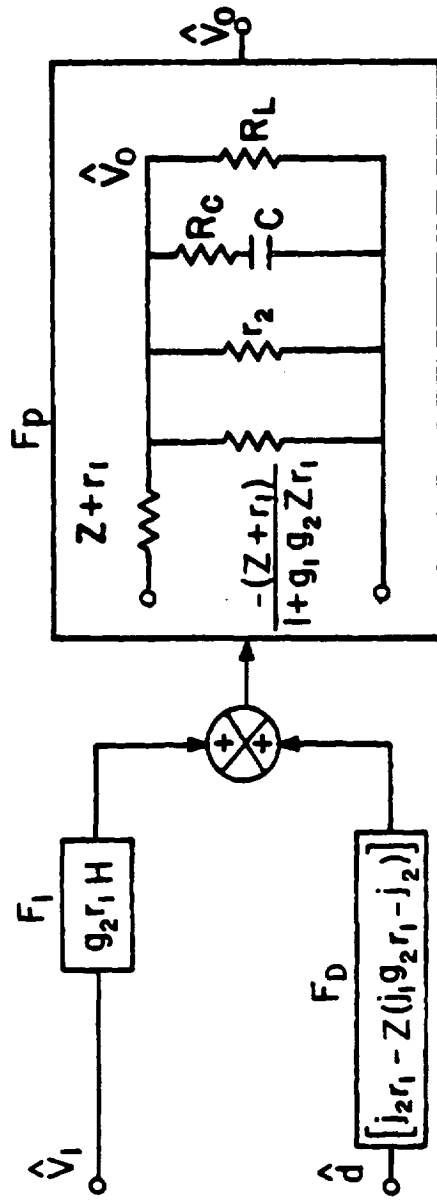


FIG. 14.2 BLOCK DIAGRAM REPRESENTATION FOR FIG. 8.2.1

$$F_D(s) = \frac{2V_o}{MR_L \sqrt{K}} \left[ \frac{R_L}{M^2} - Z(s) \right] \quad (14.13)$$

It can be concluded from equations (5.52) and (14.11) that the transfer characteristic of the power stage,  $F_p(s)$ , (ignoring the effect of the input filter) changes from second order to first order when the zero inductor mmf dwell time starts to emerge. It is obvious that the Bode plot of  $F_p(s)$  as shown in Fig. 14.3 often has a lower corner frequency followed by -20 db/decade roll-off and a phase lag no greater than 90°.

#### 14.2 Development of ASP Transfer Function:

In Chapter 6, the standard ASP, including three sensing loops and an operational amplifier integrator, and characterized by (6.9) and (6.10) is also applicable for Mode 2 operation. However, the characteristics of the voltage of the ac sensing loop changes abruptly from Mode 1 to Mode 2 operation. The voltage of the ac sensing loop for Mode 2 is derived as follows:

Since the canonical circuit model preserves both the input and output properties of the converter power stage, the circuit in Fig. 14.1 is employed to derive the input and output currents. The current through the energy storage inductor would be simply equal to the input current  $\hat{i}_i$  plus the output current  $\hat{i}_o$  as shown in the canonical circuit model in Fig. 14.1.

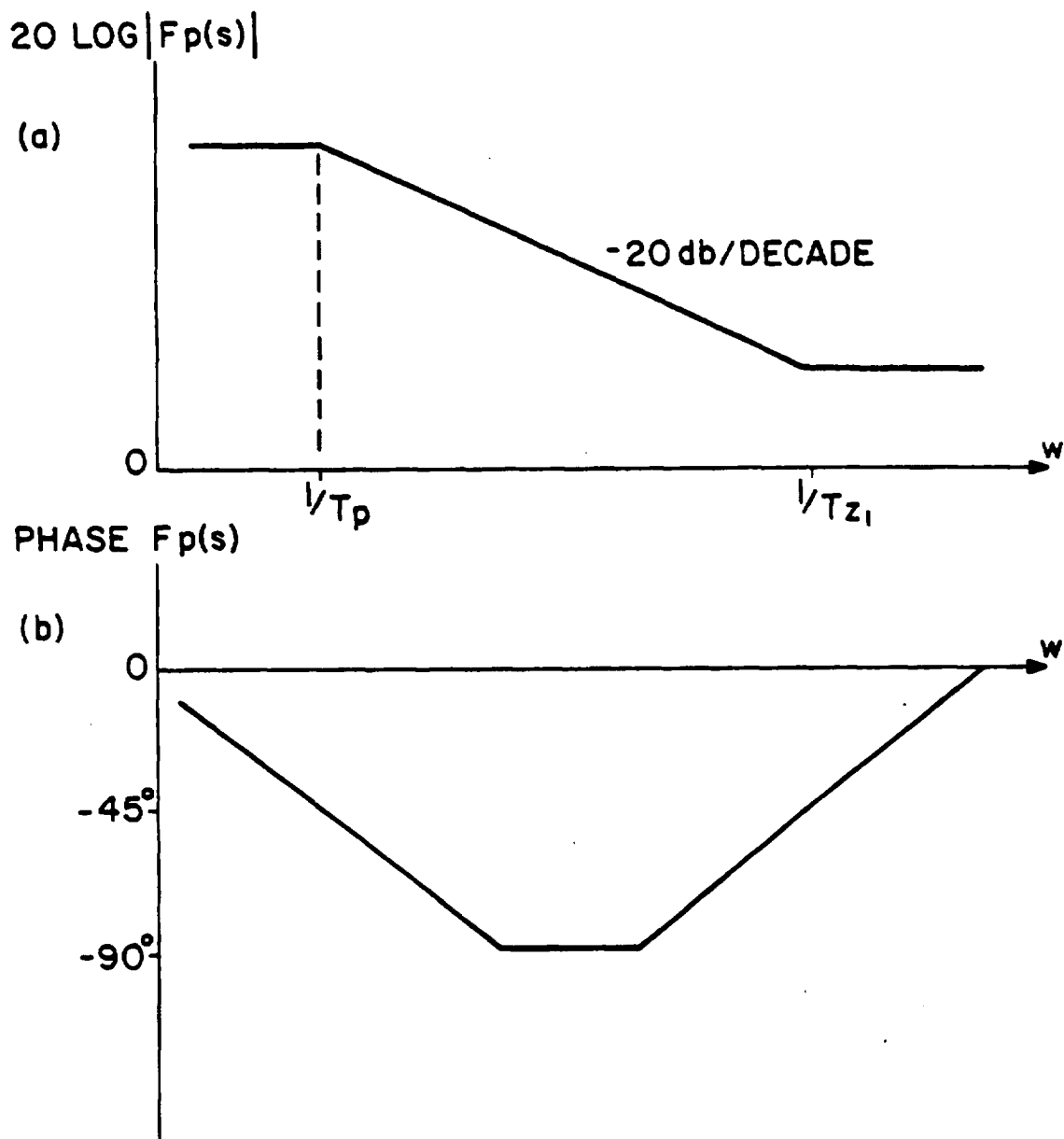


FIG. 14.3 THE MAGNITUDE (a) AND PHASE (b) OF  $F_p(s)$

It is possible to derive the following expressions for  $\hat{i}_1(s)$  and  $\hat{i}_o(s)$ :

$$\begin{aligned} \hat{i}_1(s) &= [j_1 - j_2 \frac{1}{r_1 g_2}] \hat{d}(s) \\ &+ \left\{ \frac{1}{g_2 r_1} \left[ \frac{1}{r_2} + \frac{1}{R_L} + \frac{1}{R_c + sC} \right] - g_1 \right\} \hat{v}_o(s) \end{aligned} \quad (14.14)$$

$$\hat{i}_o(s) = \frac{\hat{v}_o(s)}{R_c + 1/sC} + \frac{\hat{v}_o(s)}{R_L} \quad (14.15)$$

Combining these expressions, we can obtain the inductor current  $\hat{i}_l(s)$ :

$$\hat{i}_l(s) = \hat{i}_1(s) + \hat{i}_o(s) \quad (14.16)$$

Employing equations (14.1), equation (14.16) can be reduced to the following form in the frequency domain:

$$\hat{i}_l(s) = \frac{V_0}{R_L \sqrt{K}} \hat{d}(s) + \left[ \frac{M+1}{R_L} + \frac{sC(M/2+1)}{R_c Cs + 1} \right] \hat{v}_o(s) \quad (14.17)$$

The voltage  $\hat{v}_{ac}(s)$  across the sensing inductor is given by the equation:

$$\hat{v}_{ac}(s) = nsL_s \hat{i}_l(s) \quad (14.18)$$

It is now convenient to define the following three terms:

$$F_1 = \frac{V_0}{R_L \sqrt{K}} \quad (14.19)$$

$$F_2 = \frac{M+1}{R_L} + \frac{(M/2+1)sC}{R_c Cs + 1} \quad (14.20)$$

$$F_3 = nsL_s \quad (14.21)$$

Using these terms and using (14.17) in (14.18), the following expression for the voltage  $\hat{v}_{ac}(s)$  may be obtained:

$$\hat{v}_{ac}(s) = F_3(s) [F_1(s) \hat{d}(s) + F_2(s) \hat{v}_o(s)] \quad (14.22)$$

#### 14.3 Duty Cycle Pulse Modulator Model:

For Mode 2 operation, the integrator output voltage waveform is shown in Fig. 14.4. During the time interval  $T_{f2}$  when the inductor mmf vanishes, the integrator output voltage increases



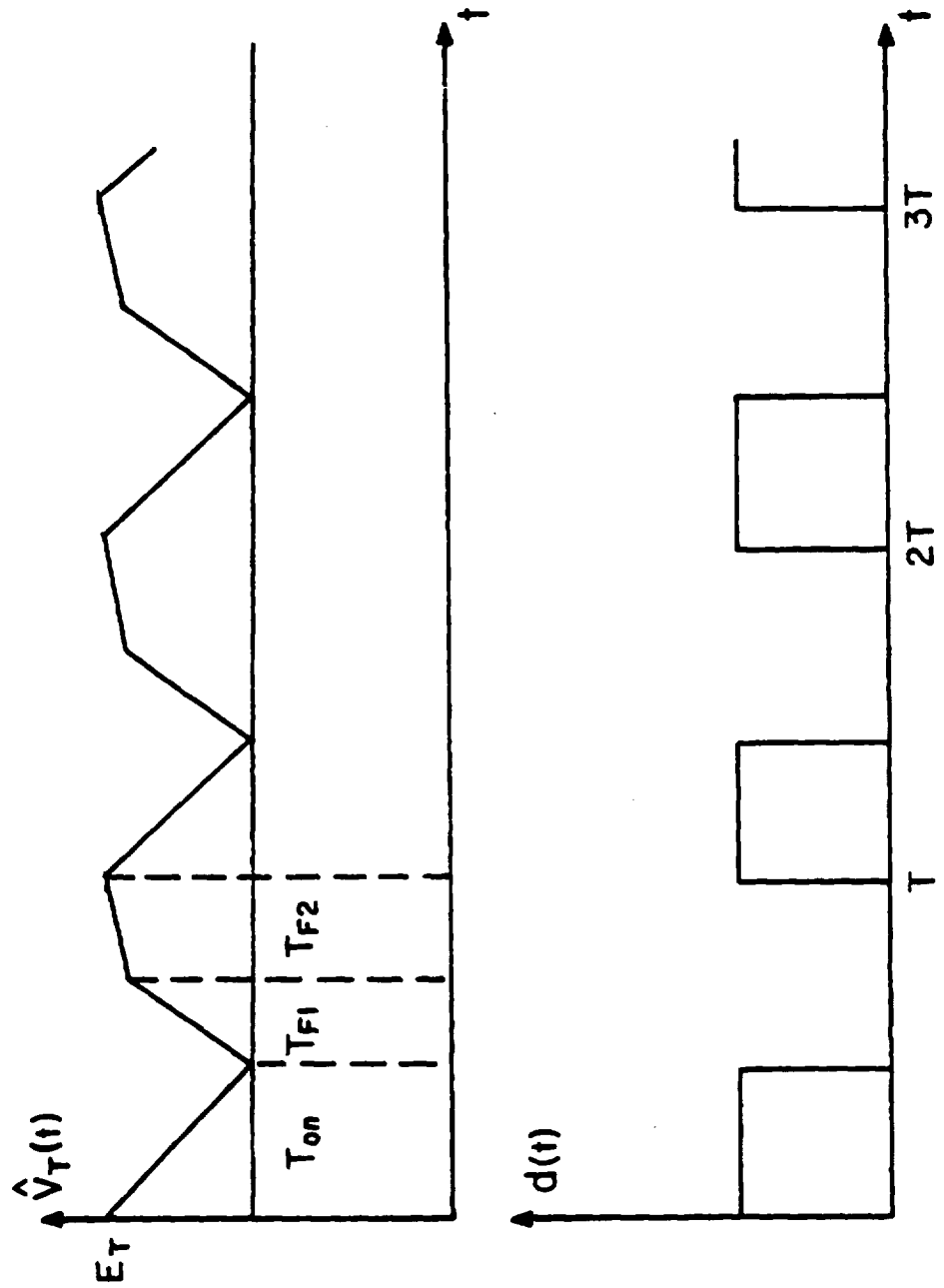


FIG. 14.4 THE INTEGRATOR OUTPUT VOLTAGE WAVEFORM FOR MODE 2 OPERATION

only slightly, as a result of integrating the output ripple voltage through the dc feedback loop.

The constant  $T_{on}$  duty cycle control method is rarely used in Mode 2 operation. Since the termination of the off time of each switching cycle is determined by the intersection of the ascending ramp voltage  $v_T(t)$  with the threshold voltage  $E_T$ , the implementation of constant  $T_{on}$  control with Mode 2 operation is susceptible to noise and disturbance in the loop. As a result, the cycle can be terminated prematurely. Therefore, a constant frequency or constant  $t_{off}$  operation are commonly used for duty cycle control in Mode 2.

The transfer function of the constant frequency pulse width modulator is derived here as an illustrative example.

$$F_M = \frac{\hat{d}}{\hat{v}_t} \quad (14.23)$$

where

$$\hat{d} = (a_2^2 + b_2^2)^{1/2} \sin(\omega t + \theta_2) \quad (14.24)$$

$$\hat{v}_t = (a_1^2 + b_1^2)^{1/2} \sin(\omega t + \theta_1) \quad (14.25)$$

$$a_2 = \frac{A}{T_P S_N} (1 + T_{on}^2 \omega^2) \quad (14.26)$$

$$b_2 = \frac{A}{T_P S_N} (\omega T_{on})$$

$$\theta_2 \approx \frac{\omega T_{on}}{(1 + T_{on}^2 \omega^2)} \quad (14.27)$$

$$a_1 = A \frac{T_{f2}}{T_p} \left\{ 1 - \frac{\omega}{2} \left( T_p - \frac{T_{f2}}{2} \right) - \frac{\omega^2}{2} \cdot \frac{T_{f1}}{T_{f2}} (T - T_{f2})^2 \right\}$$

$$b_1 = A \frac{\omega T_{f2}}{2} \left\{ 1 + 2 \frac{T_{on}}{T_p} + \frac{T_{f1} - T_{on}}{T_{f2}} \right\} \quad (14.28)$$

$$\theta_1 = \tan^{-1} \frac{\frac{\omega T_p}{2} \left( 1 + 2 \frac{T_{on}}{T_p} + \frac{T_{f1} - T_{on}}{T_{f2}} \right)}{1 - \frac{\omega}{2} \left( T_p - \frac{T_{f2}}{2} \right) - \frac{\omega^2}{2} \left( T_p - T_{f2} \right)^2 \frac{T_{f1}}{T_{f2}}} \quad (14.29)$$

$$(a_2^2 + b_2^2)^{\frac{1}{2}} = \left\{ \left( \frac{A}{T_p S_N} (1 + T_{on}^2 \omega^2) \right)^2 + \left( \frac{A}{T_p S_N} \omega T_{on} \right)^2 \right\}^{\frac{1}{2}}$$

$$= \frac{A}{T_p S_N} [1 + 3T_{on}^2 \omega^2]^{\frac{1}{2}}$$

$$= \frac{A}{T_p S_N} \left[ 1 + \frac{3T_{on}^2 \omega^2}{2} \right] \quad (14.30)$$

Using (14-23) through (14-30), the expression for  $F_M$  may be obtained.

$$F_M = \frac{\frac{\Delta}{d}}{\frac{\Delta}{V_T}} = \frac{(a_2^2 + b_2^2)^{\frac{1}{2}} \sin(\omega T + \theta_2)}{(a_1^2 + b_1^2)^{\frac{1}{2}} \sin(\omega T + \theta_1)} \quad (14.31)$$

The analytical expressions for the time intervals  $T_{ON}$ ,  $T_{f1}$ , and  $T_{f2}$ , and the slope  $S_N$  employed in equation (14.31) are given in the following.

The time interval  $T_{f2}$  is shown as follows:

$$T_{f2} = T - T_{on} - T_{f1} \quad (14.32)$$

It can be shown that the time intervals  $T_{ON}$  and  $T_{f1}$  can be expressed as the converter operating condition and circuit parameter values [21].

$$T_{on} = \frac{N_p}{V_I - V_Q} \left[ \frac{2\mu_m T_p P_o A_C (V_O + V_D)}{l V_O} \right]^{\frac{1}{2}}$$

$$T_{f1} = N_s \left[ \frac{2\mu_m T_p P_o A_C}{l V_O (V_O + V_D)} \right]^{\frac{1}{2}}$$

where  $A_C$  and  $l$  are the cross section area and mean magnetic path of the core and  $\mu_m$  is the permeability of the magnetic core.

Ignore the transistor drop  $V_Q$  and the diode drop  $V_D$ , and use the following equations:

$$\frac{\mu_m A_C}{l} = \frac{L_s}{N_s^2} = \frac{L_p}{N_p^2}$$

$$P_o = \frac{V_o^2}{R_L}$$

$$\frac{V_o}{V_i} = M \cdot \frac{N_s}{N_p}$$

$$K = \frac{2L_s}{R_L T_p}$$

$$\left( \frac{1}{s} \left( \frac{1}{s} - 1 \right) \frac{1}{s} + \frac{1}{s} \right) \left( \frac{1}{s} - 1 \right) \frac{1}{s} + \frac{1}{s} = \frac{1}{s} \quad (14.33)$$

M is defined in Table 7-1.

Equation (14.32) can be simplified to the following form:

$$T_{f2} = T_p [1 - \sqrt{K(1 + M)}] \quad (14.34)$$

The slope  $s_N$  has been derived in Chapter 7, equation (7-38), as

$$s_N = -n \frac{N_s}{N_p} \cdot \frac{1}{R_4 C_1} V_i \quad (14.35)$$

14.4 Small Signal Performance Characteristic:

Small-signal performance characteristics of a switching regulator for Mode 2 operation are examined including the following three categories: stability, audio-susceptibility and output impedance.

In order to derive closed-forms for the above mentioned characteristics, the same block diagrams used in Chapter 8 in

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where A and B are the cross section area and mean magnetic path of the core and  $\mu$  is the permeability of the magnetic core.

Fig. 8.1 and 8.2 are used, except the expressions for the transfer functions  $F_I(s)$ ,  $F_D(s)$ ,  $F_P(s)$ ,  $F_1(s)$ ,  $F_2(s)$ ,  $F_3(s)$  and  $F_M(s)$  used in these block diagrams are given in sections 14.1, 14.2, and 14.3. For simplicity, the input filter will not be included in the following analysis.

#### 14.4.1 Stability Analysis:

The open loop transfer function for Mode 2 is expressed as:

$$G_T(s) = F_M(s) [F_{DC}(s)F_P(s)F_D(s) + F_{AC}(s)F_3(s)(F_1(s) + F_2(s)F_P(s)F_D(s))] \quad (14.36)$$

$$\text{Let } R_y = \frac{R_x + R_3}{g}$$

$$m = \frac{R_4}{nR_y}$$

$$\tau_{z2} = C_2(R_5 + R_y)$$

$$\tau_{z1} = R_C C$$

$$\tau_{p1} = R_5 C_2$$

$$R_x = \frac{R_1 R_2}{R_1 + R_2}$$

$$g = \frac{R_x}{R_1}$$

(14.37)

Substitute the transfer function  $F$ 's derived in the previous section of this chapter into equation (14.36).

$$G_T(s) = F_M(s) \left\{ \frac{nL V_0}{R_4 C_1 R_L (K)^{\frac{1}{2}}} + \frac{V_0 (\tau_{z1} s + 1)}{M(K)^{\frac{1}{2}} [(R_L/2 + R_c)Cs + 1]} \left[ \frac{\tau_{z2} s + 1}{s C_1 R_y (\tau_{p1} s + 1)} + \frac{nL s}{R_4 C_1} \times \frac{[(M+1)R_c + (M/2 + 1)R_L]Cs + (M+1)}{R_L (\tau_{z1} s + 1)} \right] \right\} \quad (14.38)$$

Assuming that  $\tau_{z1} = \tau_{p1}$ ,  $G_T(s)$  becomes: (14.39)

$$G_T(s) = \frac{V_0}{M C_1 R_y (K)^{\frac{1}{2}}} \frac{F_M}{s [(R_L/2 + R_c)Cs + 1]} \left\{ \frac{L C}{\alpha R_L} [(M+1) + \frac{R_c}{R_L} (2M+1)] s^2 + [\tau_{z2} + \frac{L s}{m R_L} (2M+1)] s + 1 \right\} \quad (14.40)$$

If the following terms are now defined,

$$\frac{1}{\alpha'} = \frac{L C}{m R_L} [(M+1) + \frac{R_c}{R_L} (2M+1)]$$

$$\tau'_{z2} = \tau_{z2} + \frac{L s}{\alpha R_L} (2M+1) \quad (14.41)$$

$$\beta = (\frac{R_L}{2} + R_c) C$$

$G_T(s)$  becomes:

$$G_T(s) = \frac{V_0}{M C_1 R_y (K)^{\frac{1}{2}}} F_M(s) \left\{ \frac{(1/\alpha')s^2 + \tau'_{z2} s + 1}{s(\beta s + 1)} \right\} \quad (14.42)$$

Fig. 14.5 illustrates the plot of the open loop gain given in (14.42), with the same values of the circuit parameters given in section 10.2.4 with the following additional values to satisfy Mode 2 operation, and constant frequency control.

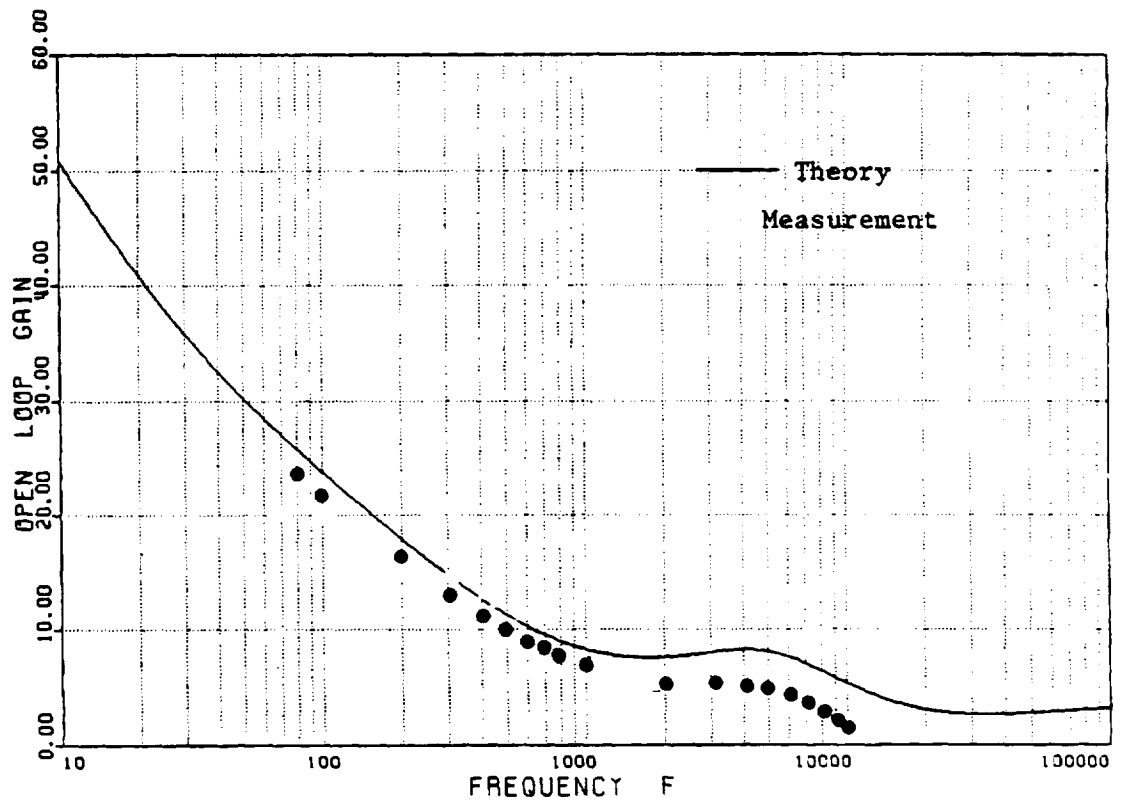


Fig. 14.5: Open Loop Gain Characteristic, Theory and Measurement  
Mode 2

$$R_L = 160 \text{ ohms}$$

$$T_p = 37.5 \text{ usec.}$$

$$V_0 = 27.45 \text{ volts.}$$

The discrepancies between the theoretical prediction and measurement data of the open-loop gain at high frequencies are perhaps due to the low frequency approximations of the power stage and the pulse width modulator model.

#### 14.4.2 Audio-Susceptibility Analysis:

It can be proved using the block diagram representation in Fig.

8.2 that

$$G_A(s) = \frac{F_I(s)F_P(s)[1 + F_1(s)F_3(s)F_{AC}(s)F_M(s)]}{1 + G_T(s)} \quad (14.43)$$

Using the previously derived expressions for the F's, equation (14.43) can be simplified to read:

$$G_A(s)[1 + G_T(s)] = \frac{M(\tau_{z1}s + 1)}{(\beta s + 1)} \left[ 1 + \frac{nV_o}{2R_4 C_1 F_M} \right] \quad (14.44)$$

For low frequency approximation, assume:

$$1 + G_T(s) \approx G_T(s) \quad (14.45)$$

Using equation (14.42) together with equation (14.45), equation

(14.44) can be simplified as:

$$G_A(s) = \frac{s(\tau_{z1}s + 1)M^2(K)^{\frac{1}{2}}}{(1/\alpha')s^2 + \tau'_{z2}s + 1} \left[ \frac{1}{2m} + \frac{C_1 R_y}{V_o F_M} \right] \quad (14.46)$$



The plot for the audio-susceptibility characteristic for the same circuit parameters as used in Figure 14.5 is shown in Figure 14.6 with both theoretical prediction and experimental verification.

#### 14.4.3 Output Impedance

It was proved in Chapter 12 that the output impedance may be expressed as:

$$Z_o(s) = \frac{Z_P(s)[1 + F_M(s)F_1(s)F_3(s)F_{AC}(s)] + F_{AC}(s)F_D(s)F_M(s)F_P(s)F_4(s)F_3(s)}{1 + G_T(s)} \quad (14.47)$$

where  $Z_P(s)$  is the output impedance of the power stage with the loop open. From the canonical circuit model for Mode 2 in Fig. 14.1

$$Z_P(s) = r_2 \parallel R_L \parallel (R_c + 1/sC) \quad (14.48)$$

where  $r_2 = R_L$  as in equation (14.1). Eq. (14.48) may be written

$$Z_P(s) = \frac{(1 + R_c Cs) R_L/2}{1 + (R_L/2 + R_c)Cs} \quad (14.49)$$

Using equation (14.42) and (14.49), equation (14.47) can be simplified as:

$$Z_o(s) = \frac{1}{((1/\alpha')s^2 + \tau'_{z2}s + 1)} \left[ \frac{R M(K)^{1/2} C_1}{V_o F_M} + \frac{nLs}{2R_4} [(MR_y \tau_{z1} + 2R_4 \tau_{z2})s + (MR_y + 2R_4)] \right] \quad (14.50)$$

The above equation can be employed to analyze the output impedance characteristic of the converter.

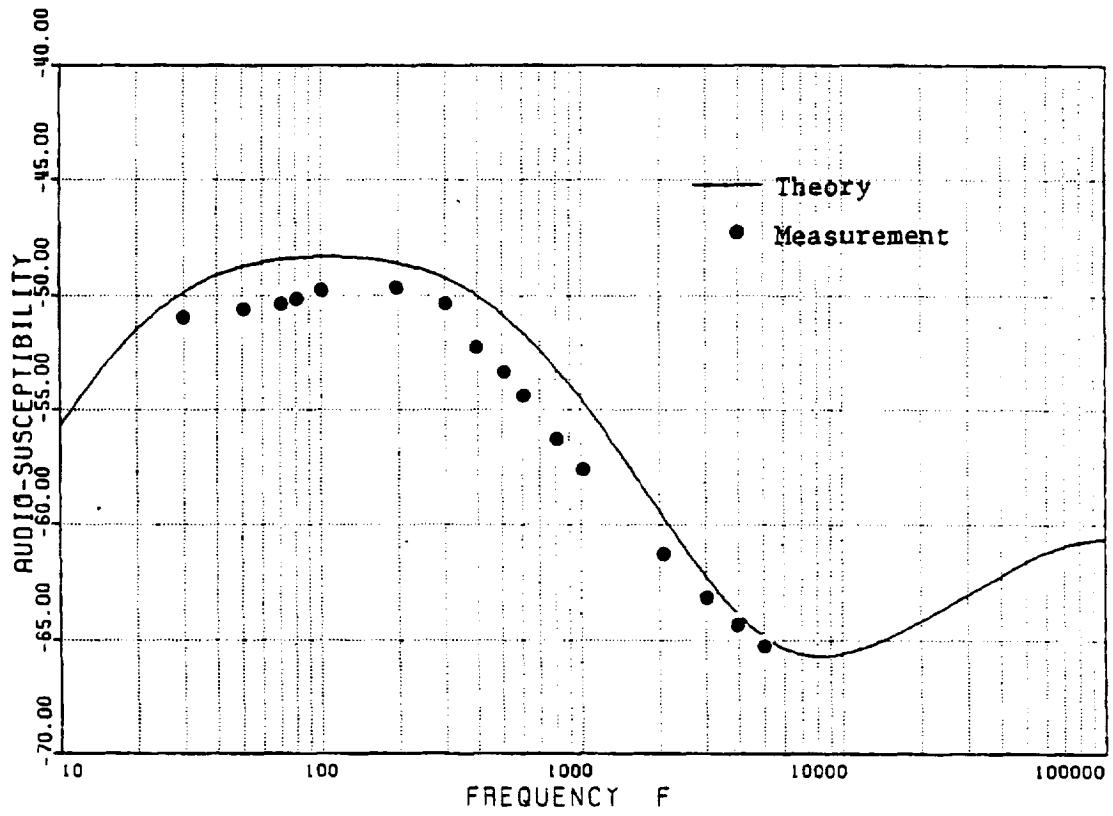


Fig. 14.6 Audio-Susceptibility Characteristic. Theory and Measurement.

Mode 2

#### 14.5 Summary of discontinuous current models

The dual input describing function model as shown in Fig. 14.2 is valid for all three switching regulator types. The complete block diagram representation of Fig. 8.2 is also applicable for the three regulator types in the discontinuous Mode 2 operation. The analytical expressions for the F's in Fig. 8.2 are provided in the following:

$$F_I = g_2 r_1 H \quad (14.51)$$

$$= \frac{2-M}{M} H_F \quad \text{buck}$$

$$= \frac{2M-1}{M^2} H_F \quad \text{boost}$$

$$= \frac{N_S}{N_P} \frac{2}{M} H_F \quad \text{buck/boost}$$

$$F_D = j_2 r_1 - Z(j_1 g_2 r_1 - j_2) \quad (14.52)$$

$$= \frac{2V_0}{R_L} \frac{1-M}{M} \sqrt{\frac{1-M}{KM}} \left( \frac{R_L}{M^2} - Z_F \right) \quad \text{buck}$$

$$= \frac{2V_0}{R_L M} \sqrt{\frac{M-1}{KM}} \left( \frac{R_L}{M^2} - Z_F \right) \quad \text{boost}$$

$$= \frac{2V_0}{M R_L \sqrt{K}} \left[ \frac{R_L}{M^2} - \left( \frac{N_S}{N_P} \right)^2 Z_F \right] \quad \text{buck/boost}$$

$$F_P = \frac{1-M}{2-M} \frac{(R_C Cs + 1)R_L}{\left[\left(\frac{1-M}{2-M} R_L + R_C\right)Cs + 1\right]\left(Z_F + \frac{1-M}{M_2} R_L\right) - MZ_F(R_C Cs + 1)} \quad (14.53)$$

buck

$$F_P = \frac{M-1}{2M-1} \frac{(R_C Cs + 1)R_L}{\left[\left(\frac{M-1}{2M-1} R_L + R_C\right)Cs + 1\right]\left(Z_F + \frac{M-1}{M^3} R_L\right) - \frac{Z_F}{M}(R_C Cs + 1)}$$

boost

$$= \frac{1}{2} \frac{(R_C Cs + 1)R_L}{\left[\left(\frac{R_L}{2} + R_C\right)Cs + 1\right]\left[\left(\frac{N_S}{N_P}\right)^2 Z_F + \frac{R_L}{M^2}\right]}$$

buck/boost

$$F_1 = 0 \quad \text{buck} \quad (14.54)$$

$$= \frac{2V_0}{R_L} \sqrt{\frac{M(M-1)}{K}} \frac{1}{2M-1} \quad \text{boost}$$

$$= \frac{V_0}{R_L \sqrt{K}} \quad \text{buck/boost}$$

$$F_2 = \frac{1 + (R_L + R_C)Cs}{R_L (1 + R_C Cs)} \quad \text{buck} \quad (14.55)$$

$$= \frac{M(M-1)}{R_L (2M-1)} + \frac{M^2}{2M-1} \frac{1 + (R_L + R_C)Cs}{R_L \left(R_C + \frac{1}{sC}\right)} \quad \text{boost}$$

$$= \frac{M+1}{R_L} + \frac{(M/2 + 1) sC}{R_C Cs + 1} \quad \text{buck/boost}$$

$$\begin{aligned}
 F_3 &= nLs && \text{buck and boost} && (14.56) \\
 &= nL_s s && \text{buck/boost}
 \end{aligned}$$

$$F_4 = 1 \quad \text{buck} \quad (14.57)$$

$$= Z_P F_2 + g_1 r_2 F_P \quad \text{boost}$$

$$= Z_P F_2 + g_1 r_2 F_P + 1 - \frac{Z_P (R_L C s + 1)}{R_L (R_C C s + 1)} \quad \text{buck/boost}$$

$$Z_P = (Z + r_1) // - \left( \frac{Z + r_1}{1 + g_1 g_2 z r_1} \right) // r_2 // \frac{R_L (R_C C s + 1)}{(R_L + R_C) C s + 1}$$

The analytical expressions for  $F_{DC}$  and  $F_{AC}$  as given in (6-9) and (6-10) remain unchanged for the discontinuous current operation.

## CHAPTER 15

### CONCLUSIONS

Three basic switching regulators, buck, boost, and buck/boost, employing a standardized multi-loop control module (SCM) were characterized by a common small-signal block diagram. The model consists of three transfer functions, characterizing, respectively, the power stage, the analog signal processor (ASP), and the digital signal processor (DSP). The power stage model incorporates all possible forms of small signal disturbances from the line, the load and the control loops. The ASP model consists of three feedback loops: dc, ac and RC compensation loops which sense and process the output voltage and the ac voltage across the energy storage inductor to provide an adaptive-compensation for stabilization and performance optimization. The DSP model implements a variety of duty cycle control modes, such as constant  $T_{on}$ , variable  $T_{off}$ ; constant  $T_{off}$ , variable  $T_{on}$ ; constant frequency with and without an external ramp.

The common block diagram model was employed to examine, in detail, SCM-controlled switching regulator performance categories, including stability, audiosusceptibility, output impedance and the transient response due to a step load change. Summarized in the following are some of the significant contributions of the multi-loop SCM control scheme:

- (1) High-gain wide-bandwidth stable operation. The open-loop crossover frequency is usually in the range of 1/3 to 1/2 of the switching frequency and is accompanied by ample phase margin.
- (2) Stabilization effect by shifting the positive zero from the right-half s-plane into the left-half s-plane for the boost and the buck/boost regulators.

- (3) Second-order compensation adaptive to the moving poles of the boost and buck/boost converter power stage due to duty cycle modulations.
- (4) Autocompensation adaptive to output filter parameter changes due to component tolerance, temperature variation, aging and capacitive loading effect.
- (5) Mitigation of the input filter destabilization effect and performance degradations.
- (6) Unification of modeling and performance characterization for the three basic switching regulator types by nullifying the positive zero and adaptively compensating the moving poles of the boost and buck/boost converters. The SCM control enables the performance characteristics of all three regulators to enjoy a common form. This finding has greatly facilitated developing a uniform analysis and design procedure.

In addition to the above described performance characteristics of SCM-controlled regulators, the analysis also reveals the following features unique to SCM control scheme.

- (1) Key control parameters including dc-loop gain, ac-loop gain and RC compensation-loop parameters and their ranges in order to optimize switching regulator performances.
- (2) Theoretical limitations of regulator performances for any given power stage configuration and parameter values.
- (3) Impact of the output filter capacitor ESR to the switching regulator performances and control circuit design.
- (4) Performance degradation in the form of high frequency resonance

between the power stage and the control loops due to improperly designed control circuit parameters and suggestions for eliminating the high frequency resonant peaking.

- (5) Input filter effect to the SCM-controlled switching regulator performances.

To facilitate developing a unified analysis and design procedure for the three converter types, a normalization procedure for the power stage parameters was proposed. Employing the normalized model, regulator performances such as stability, audiosusceptibility, output impedance and step load transient are analyzed and key performance indexes are expressed in simple analytical forms. More importantly, the performance characteristics of all three regulators are shown to enjoy common properties due to the particular SCM control scheme and the normalization procedure. This normalization procedure allows a simple unified design procedure to be devised in Volume II of the Report: "Users' Design Handbook of the Standardized Control Module (SCM) of DC-DC Converters". In the Handbook, simple design guidelines and procedures are presented for an arbitrarily given power stage configuration and parameter values. The key SCM control parameters can be selected such that all regulator performance specifications can be met and optimized concurrently in a single, non-iterative design attempt.



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