Application Independent Module Generation in Analog Layouts

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Abstract

This paper presents a new feature for a module generator environment that performs application independent module description in analog layouts. With the help of a special capacitance sensitivity matrix one module description can be used for different applications.

1 Introduction

Today most analog layouts are still hand drafted by specialists. In recently developed tools analog layout generation [1] usually starts with an optimized circuit schematic. In the first step the devices are grouped or clustered according to special analog layout requirements like matching, crosstalk, etc. Then the layout can be generated automatically with predefined modules for these blocks. These modules are placed and routed in subsequent steps.

In analog circuit design, only a few basic modules (e. g. current mirrors, differential pairs) exist from a schematic point of view. However, the modules differ in their functionality. For instance a biasing network current mirror has a different optimal layout (maximal parasitic capacitances) compared to a current mirror for an active load in an operational amplifier (minimal parasitic capacitances). The node capacitances determine the location of poles and zeros in analog circuits and the crosstalk limits the signal to noise ratio. Thus a relatively large analog module library has to be provided for high quality circuit layouts. In order to limit the number of modules their description will be application independent in this approach.

2 Application Independent Description

The designer has to define a capacitance sensitivity matrix determining the allowed or desired overlap between rectangles on different nodes. This can be obtained from a simulation or from the knowledge of the designer. During module generation which is performed in an environment [2] by abutting objects with a special compactor these constraints will be kept automatically. The router of this environment will also regard these constraints. In Fig. 1 two different results of *one* module description for a folded transistor are depicted with their according matrices. In (a) only the overlap of gate over drain has been allowed while in (b) all overlaps are possible. Therefore the coupling capacitances increase from (a) to (b). The description of this module is application independent because the different module topologies result from the external matrices.

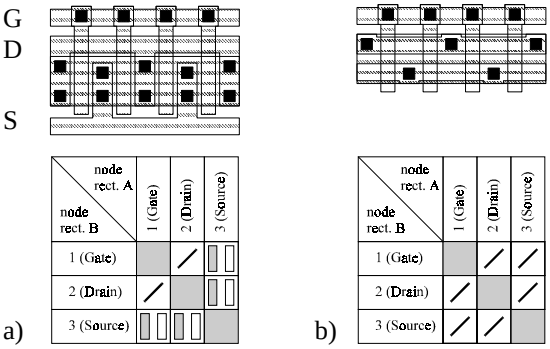

Fig. 1: Different folded transistors with according matrices

In a more complex example for a cascode current mirror for low voltage applications the use of the contrary matrices results in different topologies with an area reduction by 30 % if all overlaps are allowed. But simultaneously the total amount of coupling capacitances has increased by 530 %. The choice of the correct matrix depends on the function of this module. The benefit is to have an identical module description for different applications.

3 Conclusion

The presented methodology for application independent module description allows to keep the number of modules in an analog library small and increases the maintainability of this library by that.

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References

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