

Application of Automated Design Migration to Alternating Phase Shift Mask Design

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ABSTRACT

The use of phase shifted mask (PSM) has been demonstrated to be a powerful resolution enhancement technique (RET) for the printing of features at dimensions below the exposure wavelength in deep submicron technologies. Its implementation in physical design has introduced non-conventional design ground rules, which impact the traditional layout migration process and designers' productivity. In this panel discussion paper, we propose a solution to extend the traditional constraint-based layout migration and legalization approach. The solution has been demonstrated to be very effective in practice.

Keywords

Phase-shifting mask, resolution enhancement technique, design migration.

1. Introduction

As semiconductor manufacturing technology becomes increasingly sophisticated and feature sizes continue to shrink into the deep submicron regime, more and more stratagems have to be applied in order to maintain high yields and generally improve IC manufacturability. We have long been accustomed to standard design rules intended to prevent failures such as electrical opens or shorts, to reduce sensitivity to defects, or to accommodate overlay tolerances between levels. As process technology advances, manufacturability requirements are directed less at preventing gross yield loss and more toward improving performance yields and preserving reasonable process windows. Certain newer technologies, such as chemical mechanical polishing (CMP) have introduced specific new design rules intended, for example, to allow the process to achieve better planarity by restricting pattern density. Other design mandates may be aimed at reducing long term yield problems such as electromigration, e.g. by putting constraints on linewidths or via sizes and placement. By far, the majority of design for manufacturability techniques reside in the arena of optical

lithography, where prolonging the lifetime of a generation of tools is literally of capital importance. Known collectively as resolution enhancement techniques (RET), these methods include, among others, optical proximity correction (OPC), sub-resolution assist features (SRAF) [10], and alternating phase shift masks (altPSM).

Each of the strategies described above has technological challenges associated with it. Each also requires manipulation of the layout design data in order to achieve the desired manufacturability improvement. All of these methods also necessitate the use of new types of automated design tools to realize or assist with these layout modifications. What the methods do not share is the level of designer intervention that is required. In some cases, the design data can be manipulated as a post-processing step in the mask house - the designer need not even know that it is happening. OPC and SRAF typically fall into this category. For meeting new design rules regarding, say, linewidths or pattern densities, all that may be needed is designer awareness. Automated design tools may assist in this effort, for example, via an addition to a typical design rule checker (DRC) which also now calculates and reports pattern densities. At the far opposite end of the spectrum lies alternating phase shifted mask design, which requires substantial investment by the design community [9]. The greater the level of designer involvement in a given manufacturability improvement technique, the greater the resource required. This resource may take the form of additional design staff, more advanced CAD tools, or both of these. Lack of this resource is likely to result in longer turn around time for designs and greater time to market for new products. Clearly one of the most significant needs for the implementation of altPSM and other manufacturability techniques is the development of design tools that improve designer productivity and reduce design cycle time.

In this paper we describe the application of a constraint-based automatic design migration tool to alternating phase shifted mask design. We first briefly describe the altPSM concept and why it necessitates heavy designer involvement. We describe a basic layout legalization technique and its application to standard design migration. We then show a general mechanism to use it in conjunction with a topology recognition shape algorithm to repair altPSM design conflicts. Finally, we report the results of the application of this tool to a number of actual logic designs to demonstrate its efficacy in the automation of altPSM design and follow by some discussions on future challenges.

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2. Alternating Phase Shifted Masks

Alternating phase shifted masks are a powerful RET which can effectively double the resolution of a conventional optical lithography system. AltPSM achieves this feat by introducing a 180° phase shift in the light transmitted between adjacent features on a photo mask. This phase shifting is accomplished by creating a path length difference for the exposing light in the high index of refraction mask material between adjacent features on the mask. The path length difference, in turn, is created by recessing the transparent mask material appropriately (to a depth of $0.5\lambda/(n-1)$, where λ is the source wavelength and n is the refractive index of the mask material). While the initial concept of altPSM was introduced for alternating apertures in a dark background [7], the same principle can be applied to imaging dark lines in clear backgrounds [6], as is needed in the lithography of the polysilicon conductor ("PC"), or gate level, of IC processes.

To utilize the destructive interference of phase shifted light to enhance the resolution of isolated lines, a topography step needs to be introduced in the photo mask as shown in Figure 1. This topography step is accomplished by selectively etching into the mask substrate, which in turn requires a CAD data level to define the location of the desired phase region. Speaking from the point of view of the mask layout, there must be a PHASE1 shape on one side of each PC feature to be phase shifted and a PHASE2 shape on the other side. The PHASE1 shape would represent, for example, the portion of the mask which is transparent with 0° phase, and the PHASE2 shape the portion of the mask which is transparent with 180° phase. Figure 1 shows the relationship between the drawn layout shapes and the physical mask.

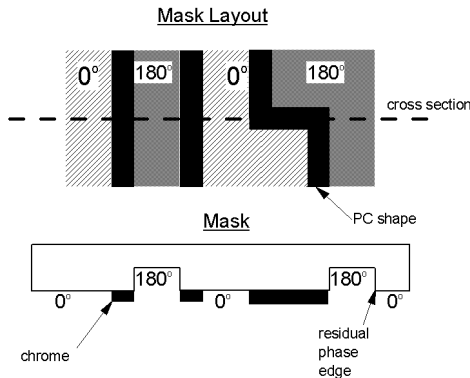


Figure 1. Relationship between altPSM layout and physical mask

Thus, the design effort for altPSM can be reduced to the relatively "simple" task of drawing the desired phase region adjacent to every shape requiring the lithographic enhancement afforded by altPSM. In reality, there are considerable challenges associated with the implementation of altPSM for logic design. These are treated at length in [9]. One of the first problems is deciding what to phase shift. Critical features are those which, based on their nominal size and required linewidth control, must be phase shifted in order to achieve an acceptable process window. Since the benefits of phase shifting decrease with increasing feature size, at some large feature size phase shifting becomes unnecessary. A second issue is the derivation of the design rules which govern both the level to be shifted and the phase shapes themselves. It should be noted that there are certain topological constructs which

cannot be phase shifted, regardless of the design rules imposed. For example, the three-way intersection or T-junction of critical dimension lines depicted in Figure 2 cannot be converted to an altPSM design such that all three critical lines receive the required phase transition. Figure 3 shows another forbidden topology which is the *odd-even* run. It creates a conflict when a contiguous phase shape along a pair of adjacent critical lines (even run) is divided by an odd number of critical line(s).

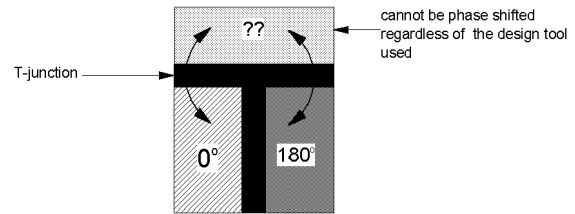


Figure 2. Phase conflict in a T-junction

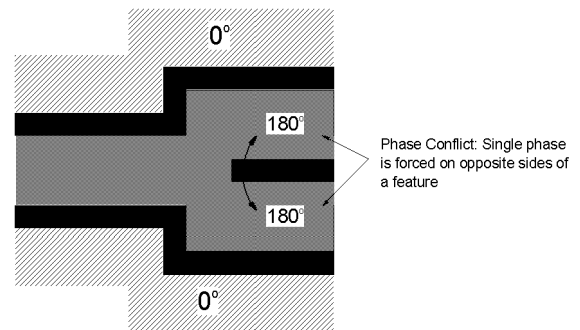


Figure 3. Phase conflict in an odd-even run

A third challenge is to check a design against these design rules [2]; a fourth is to actually create and assign phases to the phase shapes.

A good survey for RET is presented in [4]. Dark field altPSM conflict resolution techniques are examined in [1][12]. Bright field altPSM conflict resolution is treated in [5]. It uses a feature graph to capture the necessary condition for altPSM conflicts, but the sufficiency condition is not captured because the legality of phase shapes is not modeled explicitly. Because of the complexity of creating legal phase shapes, designing altPSM compliant layouts is becoming a very demanding task. Without automated layout legalization software, the productivity of layout designers is seriously impacted.

3. Layout Migration and Legalization

The forbidden layout topologies of an altPSM layout break down the conventional migration techniques which use linear shrink in conjunction with minimum perturbation DRC violation cleanup [3]. New layout migration capabilities need to be developed to address re-use of layouts designed in conventional CMOS design ground rules.

Traditional design migration techniques use a constraint graph to capture design rules that govern the legality of a conventional CMOS layout. A ground rule is typically represented by a two-variable linear constraint, which describes the minimum or maximum distance between two interacting layout edges. The

constraint is generated by analyzing the relationship between two adjacent layout elements.

The minimum perturbation formulation of a layout legalization problem seeks to minimize the final locations of layout objects from their respective original locations, i.e.

$$\begin{aligned} \text{Minimize: } & w_i \bullet \|x_i - x_i^{\text{old}}\| \text{ for each layout element } i \\ \text{Subject to: } & x_i - x_j \geq d_{ij} \end{aligned}$$

where x_i is a variable that denotes the final location of a layout element i , x_i^{old} is a constant that denotes the original location of the object and w_i is a weight that controls the desired movement the object. A violation $x_i - x_j < d_{ij}$ is relaxed and a cost term $f(x_i, x_j)$ with a negative slope is introduced in the objective function such that $f(x_i, x_j)$ is less than 0 when $x_i - x_j$ is less than d_{ij} and $f(x_i, x_j)$ equals 0 when $x_i - x_j$ is greater than or equal to d_{ij} . The set of two-variable constraints is represented by a constraint graph. This legalization technique has been used successfully to migrate layouts in real life design migration projects [3].

4. Marker Shape Generation

Most altPSM conflicts of a layout cannot be described by simple relationships between adjacent layout elements, for example, the T-junction conflict is caused by a forbidden topology and the topology needs to be discovered explicitly. The traditional constraint generation techniques discover constraints between layout elements by analyzing simple relationships between adjacent layout elements. They are not able to capture the conflicts without a priori knowledge of the conflicts. We use a separate geometric operations to create *marker shapes*, which are shapes derived from the original layout shapes, to denote the conflicts. Artificial design rules are then used to ensure that marker shapes will have appropriate influence on actual layout shapes during the legalization process. In this section, we outline the marker shapes generation process and describe how T-junction markers and *critical line-end to projecting critical line* markers are created. We will use these two markers to illustrate how the corresponding altPSM conflicts can be resolved using our layout legalization technique in the following section.

The process of generating marker shapes that not only flag problematic layout configurations is broken into 3 distinct steps. First, the layout is separated into critical and non-critical shape segments. The primary distinguishing characteristic in determining feature criticality is feature width relative to a predetermined cutoff dimension. It is extremely important, however, to capture all the details of the altPSM design process in the feature classification. All features classified as critical will receive phase shift designs but, for the purpose of layout verification, all shape segments that will receive phase shapes have to be classified as critical, capturing all details of the phase shift design process, e.g. some phase shift design approaches call for critical classification of a feature edge over its entire length if any segment of the feature drops below the dimensional cutoff. The second step involves relatively standard design rule checking (DRC). Based on the breakdown of the layout into critical and non-critical segments, error vectors are created for shapes topologies or layout configurations that are non-phase-shiftable. Finally, the conflict specific error vectors are converted into

marker shapes that convey the various possible layout corrections, the minimum dimensional alterations for each correction option, and the spatial extent of each correction option.

To create a marker shape for a T-junction, after classifying the critical feature segments using a variant of the patented Galan-checker [2], small non-critical feature segments that contain an odd number of critical segment ends are identified as non-phase-shiftable intersections. After the intersections are identified, they are expanded and intersected with the original shapes to create the markers. See Figure 4.

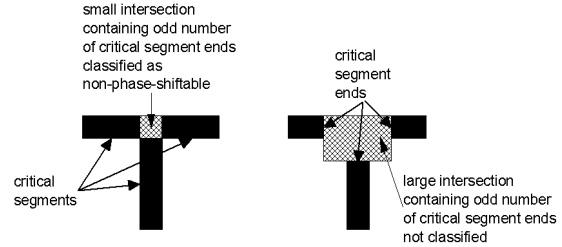


Figure 4. Non-phase-shiftable Intersection

To create a set of marker shapes for a critical line-end to projecting critical line violation, first the layout problem is identified by the DRC code, then 3 marker shapes are created: one marker shape communicates the need to grow the space between the critical line-end and the projecting line to the appropriate value, the second indicates the length over which the line end needs to be widened to form a non-critical line end, and the third indicates the length of feature segment over which the projecting critical line needs to be widened to avoid the conflict. See Figure 5.

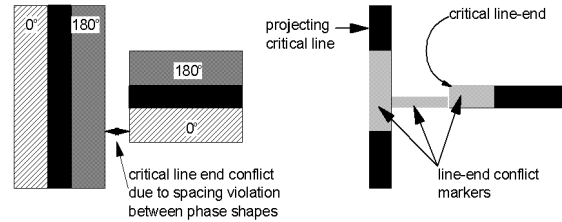


Figure 5. Markers for a critical line-end violation

5. AltPSM Conflict Resolution

In general, an altPSM conflict is resolved by one of three ways. The first is by increasing the width of a critical feature, the second is by introducing a *phase breaking block* (a non-critical design shape that breaks the unwanted interaction between phase shapes) on a portion of a critical feature and the third is by increasing the spacing between critical features.

We formulate a minimum perturbation problem to realize each resolution. After the marker shapes are created, we devise a set of conventional design rules to describe the relationships between the marker shapes and the design shapes. With the marker shapes and new rules in place, the constraint generation process and the layout legalization are carried out as before. We provide a general scheme to prioritize the resolutions for each conflict. The prioritization based on design preference and empirical experience can be implemented readily using the scheme.

5.1 T-junction Conflict Resolution

To resolve the conflict caused by a T-junction, we require the width of the T-junction marker to be at least W_{NC} , where W_{NC} denotes the minimum width when a feature is classified as non-critical, i.e. a width when the feature is not required to be phase-shifted. In addition, the marker is required to be enclosed inside the original polysilicon shape. These requirements are described by traditional width and enclosure rules. They translate into the following constraints during the constraint generation process,

$$\begin{aligned} m_R - m_L &\geq W_{NC} && \{\text{marker is at least non-critical}\} \\ m_L - s_L &\geq 0 && \{\text{marker is inside shape}\} \\ s_R - m_R &\geq 0 \end{aligned}$$

where m_L, m_R denote the left and right edges of a marker and s_L, s_R denote the left and right edges of the shape that it marks. See Figure 6. In practice, the edges of the marker shape are coincident with the corresponding shape edges. The marker is drawn to be smaller to illustrate the indented topological relationships between the edges of the marker and the edges of the shape.

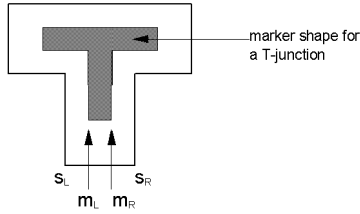


Figure 6. Marker shape of a T-junction

Since the constraint $m_R - m_L \geq W_{NC}$ is originally not satisfied, it is relaxed into the objective function during the minimum perturbation optimization process. One could expand the width of any of the three legs of the junction or introduce a phase breaking block in the middle of the junction. We found that in practice, the former formulation is sufficient, since the width of the gate-length portion of the shape is pre-constrained and only the non-gate portion of polysilicon shapes are widened in the optimization. See Figure 7.

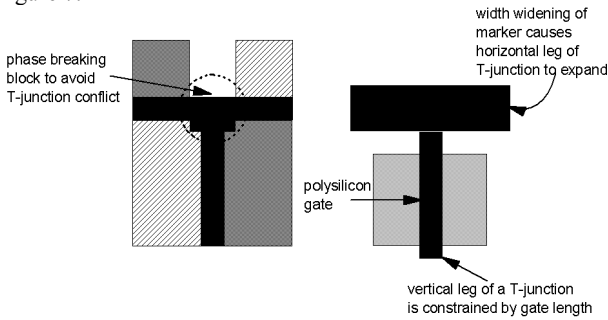


Figure 7. Gate-length constraint eases problem setup

5.2 Critical Line-end Conflict Resolution

There are three solutions to resolve the critical line-end to projecting critical line conflict as shown in Figure 8. We will describe how they can be achieved by appropriate addition of rules to the markers and the use of the minimum perturbation legalization technique.

In the first solution, the conflict is resolved by adding a phase breaking block (expanding the line-end). It is achieved by requiring the width of the line-end marker to be W_{NC} and the length of it to be L_{NC} , where W_{NC} denotes the non-critical width, and L_{NC} denotes the non-critical length. Further more, the marker is required to

- (1) cover a distance L_{NC} from the line end.
- (2) cover at least the width of the original shape.
- (3) inherit all the spacing rules of the polysilicon level.

These requirements translate into the following constraints:

$$\begin{aligned} m_R - m_L &\geq L_{NC} \\ m_R - s_L &\geq L_{NC} \end{aligned}$$

during the x-direction optimization and:

$$\begin{aligned} m_T - m_B &\geq W_{NC} \\ m_T - s_B &\geq W \\ s_T - m_B &\geq W \end{aligned}$$

during the y-direction optimization. m_L, m_T, m_R, m_B denote the left, top, right and bottom edges of a marker respectively, s_L, s_T, s_R, s_B denote the corresponding edges of the shape it marks, W denotes the width of the shape. See Figure 9. In practice, the three edges of the line-end marker along the critical line-end are coincident with the corresponding line-end edges. The marker is drawn to be larger to illustrate the intended topological relationships between the edges of the marker and the edges of the line-end.

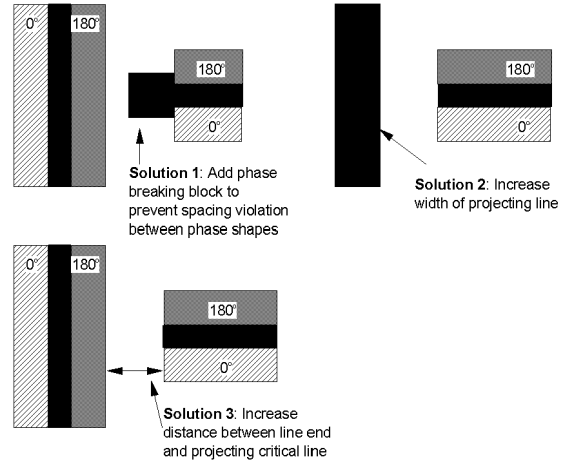


Figure 8. Solutions for critical line end conflict

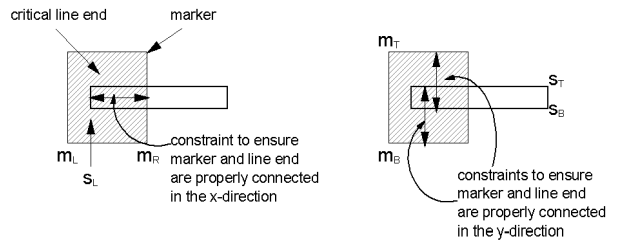


Figure 9. Constraints between marker and critical line end

These constraints essentially allow the creation of a phase breaking block at the critical line end. Similar to the case of the T-junction, initially non-satisfied constraints are relaxed into the objective function during the minimum perturbation legalization process. After the legalization process, the line-end marker is converted to a shape in the polysilicon level to complete the creation of the phase breaking block. Note that the phase breaking block does not have to center along the critical line-end, its location is determined by the perturbation cost of the layout. See Figure 10.

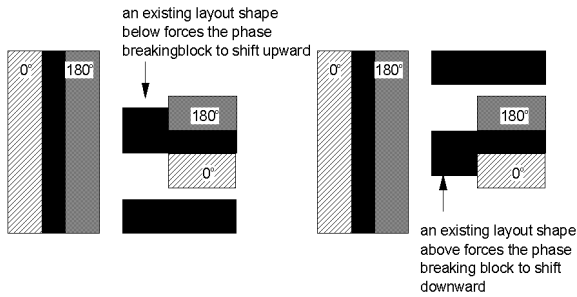


Figure 10. Phase breaking block shifted accordingly

In the second solution, the conflict is resolved by modifying the width of the projecting critical line. It is achieved by requiring the width of the marker shape on the projecting critical line to be at least W_{NC} and requiring that the marker shape be enclosed in the projecting line.

In the third solution, the conflict is resolved by increasing the spacing between the critical line-end and the projecting critical line. It is achieved by requiring the length of the spacing marker to be at least the distance required to resolve the spacing violation between the phase shapes.

Each desired conflict resolution can be formulated as a layout legalization problem using marker shapes and carefully devised rules. In some cases, the marker shapes are required to be completely enclosed in the original design shapes; in other cases, the marker shapes are converted to design shapes after the optimization.

5.3 Prioritization of Conflict Resolutions

We now describe the general prioritization scheme and its implementation. The scheme adjusts the objective function of the minimum perturbation problem for a layout. It manipulates layout variables in the layout constraint set to control the degree of modification allowed in the layout. The degrees of freedom for the modification are described below:

- (1) Expand marker shapes (and abutting edges of original shapes) only.
- (2) Move and/or expand marker shapes only without increasing the size of the layout
- (3) Move and/or expand marker shapes and affected predefined non-critical levels without increasing the size of layout, e.g. alter only the polysilicon level.
- (4) Move and/or expand marker shapes and affected predefined non-critical levels without increasing the size of the layout more than a predetermined percentage.

We achieve (1) by *freezing* all layout variables that are not associated with the marker shapes. Tying those variables with the source node of the constraint graph does the freezing of the variables. In theory, the layout size can increase due to the expansion of the marker shapes.

To achieve (2), we *un-freeze* the variables associated with the critical features and add an upper bound constraint between the source node and the sink node of the constraint graph. We also assign high weights to layout variables associated with the critical features to limit their movement and give preference to the movement of the marker shapes.

To achieve (3), we un-freeze shapes in some predefined design levels, e.g. all polysilicon shapes and diffusion shapes.

To achieve (4), the upper bound constraint between the source node and the sink node is expanded by a predetermined percentage.

We solve a minimum perturbation problem for each of the four layout modification problems described above in sequence. If no more conflict is detected after an optimization, the process is stopped and a final result is obtained.

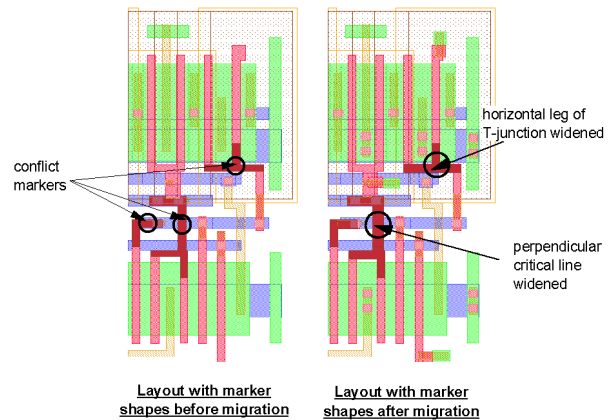


Figure 11. A layout before and after migration

Figure 11 shows a layout before and after it is migrated. The layout on the left is a layout with marker shapes denoting altPSM conflicts before it is migrated. The layout on the right shows how the marker shapes get expanded to remove the conflicts.

We have shown a general technique to resolve a T-junction conflict and a critical line-end to projecting critical line conflict. There are other altPSM conflicts that cannot be easily discovered by traditional constraint generation techniques. See [9] for a more complete discussion of altPSM conflicts. We have also used this technique to resolve the other altPSM conflicts successfully.

6. Results

The layout legalization capability described above was developed and used to migrate conventional CMOS layouts to altPSM compliant layouts. We tested this migration approach on a variety of designs from custom layouts to standard cells in order to assess area impact of the altPSM design rules. The migrated layouts were verified by an altPSM enabled DRC checker [2]. The results for automatically migrated layouts were comparable with those for

manually adjusted layouts, except in a few very compact designs where layout topologies needed to be altered. The migration of a typical standard cell took between 1 to 30 seconds depending on the size of the cell and the nature of the conflicts. It took less than 5 minutes to migrate a sample of 20 standard cells. During our assessment, a custom multiplexer layout with about 50 devices was migrated in less than 1 minute. The same layout took a custom layout designer 8 hours to make altPSM compliant!

The layout migration and legalization software described above could also be use as a productivity tool to assist in the designing of new altPSM layouts. This will help lower the barrier of introducing altPSM design rules to the designers.

7. Future Challenges

Legalizing altPSM layouts is an important part of the altPSM layout design process. It enables the reusability of conventional CMOS layouts and enhances the productivity of designers. Our solution establishes a feasibility milestone for the altPSM layout migration problem. There are still open issues and challenges.

- It is an open problem to see if the traditional constraint generation process using a scanline approach can be extended to discover the forbidden altPSM topologies. Conceivably, some secondary structures need to be built during the scanline process to keep track of the bad topologies. A unifying constraint generation process can potentially improve the efficiency of the constraint generation process.
- The altPSM conflict resolution problem is examined in [5] in a topological context¹ and is shown to be NP-hard by formulating it as a Graph Bipartization Problem. We show that a practical legalization can be accomplished by solving a series of minimum perturbation problems in some predetermined order. A hybrid approach could potentially improve the legalization process.
- When altPSM compliant standard cells are assembled in a place and route process, the phase shapes in the cells may interact and create phase conflicts. To guarantee the integrity of the place and route process, e.g. adjacent cells can always be abutted, in an altPSM setting; new place and route methodologies need to be developed. Conceivably, the new methodologies will impose some new phase related boundary conditions for the standard cells. These boundary conditions need to be carefully examined and taken into consideration when standard cells are migrated to altPSM compliant cells.
- In a hierarchical layout, a cell needs to maintain its identity and interacts with other shapes legally in every layout context. In a highly nested hierarchical layout, it is desired to create the phase shapes in the cell to maintain the compactness of the layout data. In practice, it may not be possible to find a legalization of a layout without flattening

¹ The optimization criterion is to minimize the number of nodes to delete in the feature graph proposed, using timing information to choose between widening a critical feature and increasing spacing between features, it does not consider the effects of the actual movements of shapes in the layout.

the phase shapes of the cells. A very interesting research topic is to find a conflict resolution technique to minimize the flattening of phase shapes.

There are more physical design challenges beyond the narrow context of design migration. The polarities of phase shapes in altPSM layouts add a new level of interacting constraint when layout cells are assembled, either in a place and route environment or in a hierarchical environment. This new constraint forces all stages of physical design to be integrated more tightly than ever before in order to produce altPSM compliant layouts. This opens up a whole new area for research and development, either in new methodologies development or in new tools integration.

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