

Application of Integral Analysis Technique to Determine Signal- and Power Integrity of Advanced Packages

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Abstract

In this paper an application of an integral analysis technique is demonstrated for determining Signal Integrity (SI) and Power Integrity (PI) of complex and advanced package solutions. A representative System-in-Package (SiP) product has been selected as a carrier for our study, which is focused on analysis methodology, tools and flow. In particular, possibility to easily support what-if simulations for SI and PI, including analysis with distributed on-chip decoupling capacitors is investigated and highlighted. Importance of balancing between accuracy, CPU time and ease-of-use is also underlined.

Introduction

Simultaneous requests for miniaturization and improved functionality of semiconductor products, has lead to a significant increase of their complexity. This trend is present both on a chip and package level, with approaches called System-on-Chip (SoC) and System-in-Package (SiP). An important aspect of designing such complex packages is the availability/accessibility to methodologies, flows and tools that would allow engineers to physically and electrically design and verify such products. A single semiconductor package with a size of around 1 cm², very often contains RF, analog and digital blocks or ICs. This makes the electro-magnetic coupling between these blocks both on IC and package level extremely important for the overall functionality. These parasitic interactions are in most cases strongly undesired, and thus packages have to be carefully analyzed with respect to so-called signal integrity (SI) and power integrity (PI). Unfortunately, the interactions and coupling does not end at the package-board interface; they can also occur through the PCB.

Both the semiconductor and EDA vendor communities have recognized an increasing importance of signal and power integrity analysis of advanced packages. The result is that new EDA solutions for electrical what-if analysis and verification are emerging on the market.

There are two use-models/methodologies that can be distinguished for SI and PI analysis of advanced packages. In the first, sequential (or cascaded) use-model, an engineer has a full control over extraction of electrical models of passive elements and important interconnects (e.g. wirebonds, package/PCB traces, selected traces on IC, distributed on-chip decoupling capacitors, etc). The user is also supposed to create a simulation test-bench in which extracted electrical models of interconnects in S-parameter or SPICE format are combined along with behavior models of active IC's.

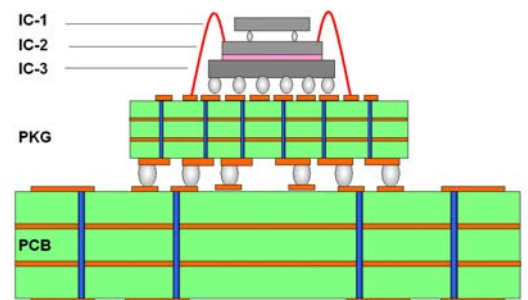
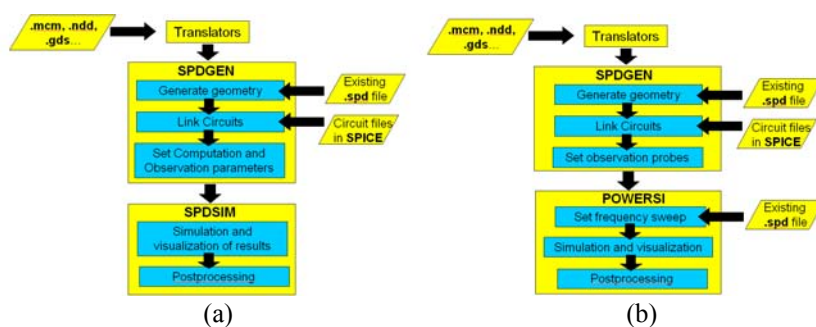


Figure 1. Flow diagrams of Sigrity's integral approach for SI/PI analysis: (a) time-domain and (b) frequency-domain.

Figure 2. Schematic cross section of the carrier design.

In the second, integral use-model, an engineer creates a unified physical database of IC/package/PCB combination by merging available physical data in a single design file. This should be followed by defining electrical excitation of the system within the same physical database, and setting up the simulation parameters. One major difference between the two use-models is that in the integral approach, the user does not have a control over partitioning the overall system for the purpose of extraction of electrical models of interconnects and connecting those models in a simulation test-bench. The tool automatically takes care of this, once the physical database is assembled and current/voltage signatures of active parts are assigned. This appealing feature of the integral approach implies correct modeling of the return current loops of the total structure, which is very difficult, if not impossible with the cascaded approach.

In this paper we investigate capability and functionality of integral analysis technique to determine signal and power integrity of advanced packages. This is done by exercising flows of Sigrity [2] solution for SI and PI analysis (shown in Figure 1), on a relevant System-in-Package carrier design.

Carrier design

A schematic cross-section of the carrier design is shown in Figure 2. It is a SiP product with three stacked ICs on 4-layer laminate substrate. The top BiCMOS die with RF functionality (IC-1) is flipped on a passive silicon die (IC-2) that contains high-density (HD) deep-trench decoupling capacitors [3] for each supply domain of IC-1. IC-2 die is wirebonded directly to the substrate. The bottom die in the stack (IC-3) is a CMOS IC with primarily digital functionality. This die is flip-chipped onto the package. The package is mounted on a 4-layer PCB test-board.

Database creation

For integral SI/PI analysis technique, easy creation of a single database with IC's, package and PCB is one of the most important challenges. For the selected carrier, the IC designs are available in .gds2 format, the package in Cadence .mcm/.sip or Encore BGA .na2 formats and the PCB in Mentor Graphics Expedition PCB/.nnd formats.

The integral flow must enable a straightforward procedure for creation of a single database, with data conversion and merging utilities readily available in the tool suite. Prior to conversion from the available data formats into the native format of the analysis tool suite (for Sigrity it is the .spd format), reduction of IC physical databases has to be done. This requires knowledge of the functionality of the IC's. Only after this step, an amount of data from IC's will be reduced to a level that can be handled by the tools. We have limited the IC-1 to its bumps and IO info; IC-2 to technology stack-up, simplified layout of decoupling capacitors, ground plane, sensitive differential RF input lines and wirebonds; IC-3 to redistribution layer (RDL) in top metal layer, ground plane underneath the RDL, and the technology stack-up.

Our experience shows that although the data conversion procedure is automatic, the user has to check/inspect the design, and does some necessary modifications and database adaptations. It should be noted that after conversion, the native .spd file lives its own life and is not in synchronization with the original design. After conversion, the merging utilities are applied and the resulting physical database of the carrier design is shown in Figure 3.

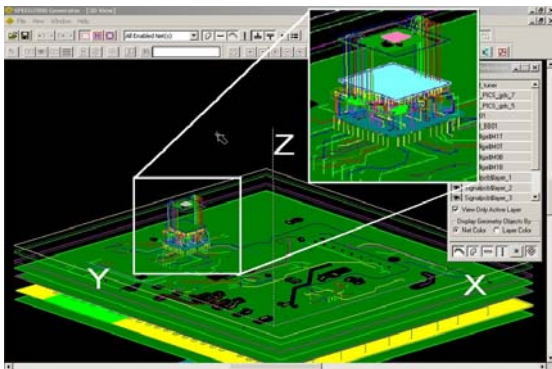


Figure 3. PCB, package and IC physical models in a single integral database; simplified 3D view.

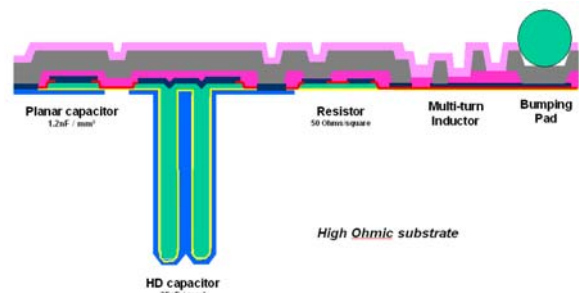


Figure 4. Schematic cross section of passive silicon IC with high-density trench capacitors.

Some objects of the original design have to be re-shaped in the analysis tool. Almost each and every true-3D object has to be re-defined: wire bond profile has to be recreated, while bumps and balls have to be replaced by vias, which properly model the physical geometry.

An important feature of the selected carrier design is that it contains passive silicon die with high-density (HD) deep-trench decoupling capacitors [3], shown in Figure 4. Due to its planar character, the used analysis tool cannot handle the 3D nature of the trench capacitors. Therefore, the geometry of such capacitors has to be simplified by a parallel-plate capacitor with the same top area and an effective dielectric constant that would ensure the same capacitance density. To do this, we have successfully used a unique feature of the Sigrity tool for SI/PI analysis, which is the ability to modify dielectric properties of a layer only across the selected area (see Figure 5). It should be noted that capacitance density has to be known upfront, since the goal here is not to extract the capacitance, but to model its effect on overall system performance.

After building a complete physical database, further tests are done to demonstrate analysis capabilities of the integral SI/PI analysis flows. It should be noted that integral SI/PI analysis tools, represented here by the Sigrity tool suite, are not intended to be used as tools of choice for accurate modelling of general 3D structures, such as integrated inductors or antennas. For model extraction of such structures, full-wave 3D EM solvers of CST, Ansoft [5] and Optimal [6] offer highest accuracy. Nevertheless, such tools consume significant amount of memory and time. However, when analyzing and verifying SI and PI behaviour of complete SiP's or advanced packages, a balance between accuracy and speed of analysis is of paramount importance. That is where the tools like Sigrity's could be very useful; it is shown in Figure 6, that Sigrity's hybrid approach of combining different methods of simulation, results in acceptable accuracy, while at the same time offering a very high speed of simulation. Note that an example from Figure 6 is simulated on a transmission-line test structure, which is geometrically simple enough to be analyzed by the general purpose full-wave 3D EM tools in real time. With the tools supporting integral analysis method, significantly more complex structures can also be easily analyzed, which is demonstrated in the following sections of the paper.

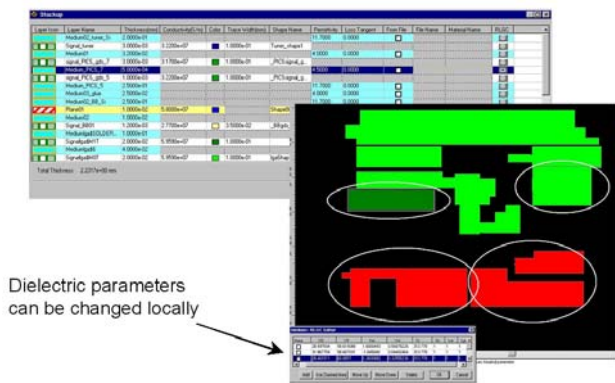


Figure 5. Dielectric properties can be locally changed to model high-density of 3D decoupling capacitors.

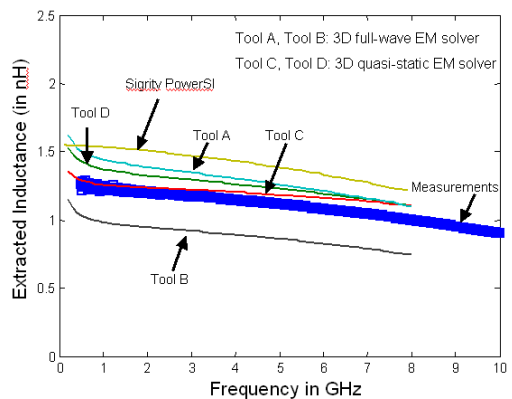


Figure 6. With the hybrid simulation approach, Sigrity offers a balance between accuracy and speed.

Simulation Test Case

A simulation test case is set up for the chosen carrier product. Both time-domain and frequency-domain simulation flows have been investigated. For time-domain simulations, SPICE models are introduced which describe switching current activity of supply domains of the aggressor, the digital CMOS IC-3. We have used a simplified, first-order switching current activity models described by the triangular-like shapes, where the amplitude is calculated to meet the average power obtained by the measurements. The rise- and fall times are taken from the technology-node information, in this case 90nm CMOS. In addition, the switching frequencies (20 MHz, 60 MHz, and 480 MHz) are also taken from the measurements. Such activities of IC-3 are expected to introduce power/ground bounce as well as noise at sensitive RF inputs of IC-1. It should be noted that the tool also supports usage of more accurate current activity descriptions, e.g. in a form of a table or a model created by applications such as Apache RedHawk [6]. For frequency-domain analysis, impedances are calculated at different locations of the design in reference to the excitation points at supply domains of the digital IC-3 die.

Simulation Results and Discussions

In this section, a selection of SI/PI analysis results is presented and discussed. All simulations are performed on HP Proliant BL25p G1 blade server with CPU 2x AMD Opteron (2600MHz), RAM of 16 GB and OS Red Hat Enterprise Linux WS release 3 (Taroon Update 8).

Time-domain simulation and analysis

First, for PI analysis, voltage noise at supply domains of the victim die IC-1 is simulated in time-domain, and plotted versus time in Figure 7. Four supply domains at 2.8V are included in the graph. The noise is a result of switching activity at all supply domains of the aggressor die IC-3. All decoupling capacitors from the original design are included in the analysis. This means that on-chip decoupling capacitors of IC-3, distributed deep-trench capacitors of IC-2 and PCB decoupling capacitors are all included in the analysis. We have observed that simulation runs to the end without any convergence problems and that it took a record short 2 hours and 20 minutes to complete. Note that we haven't included any net coupling in horizontal direction, which would otherwise increase the simulations time.

Noise levels from Figure 7 are zoomed upto 3 ns along time axis, and shown in Figure 8(a). Ease-of-use of the integral approach for what-if analysis is demonstrated through making changes in the physical design and excitation sources, and repeating simulations. In Figure 8(b), the noise is plotted for the same supply domains, but now for the case in which deep-trench decoupling capacitors from IC-2 are replaced by planar capacitors, which naturally have much smaller capacitance density. A clear advantage for the overall system performance is clearly visible when deep-trench HD capacitors are included in the design: it can be seen that the noise levels are predicted to be reduced more than 10 times. In another experiment, the most aggressive switching among IC-1 supply domains (with respect to amplitude) is excluded from the simulation setup, and the results are shown in Figure 8(c). Observe tremendous reduction in the noise, which demonstrate importance of 1) proper activity modeling for IC's, 2) proper estimation of on-chip decoupling capacitance of the aggressor die, and 3) proper design of decoupling scheme (on-chip and off-chip) for each supply domain. The same conclusions are supported by Figure 9, where noise at the sensitive differential input of IC-1 is plotted for the case with and without the most aggressive switching at IC-3.

Frequency-domain analysis

An important value of the integral frequency-domain simulation approach is capability to simultaneously optimize decoupling scheme on different design domains: IC, package and PCB. Making changes in decoupling schemes and simulate the system with such modifications is almost straightforward. Figure 10 shows capability of the tool to probe each point in the design in simulation post-processing mode, locate hot spots, and optimize decoupling capacitance. Optimized decoupling of the system with involvement of deep-trench decoupling capacitors is illustrated in Figure 11, where high transimpedance curve with peaks is simulated for the case in which HD capacitors of IC-2 are not present in the design. The flattened characteristics without peaks at amplitude ~ 0 is hardly visible in the graph and characterizes the system in which HD capacitors of IC-2 are present.

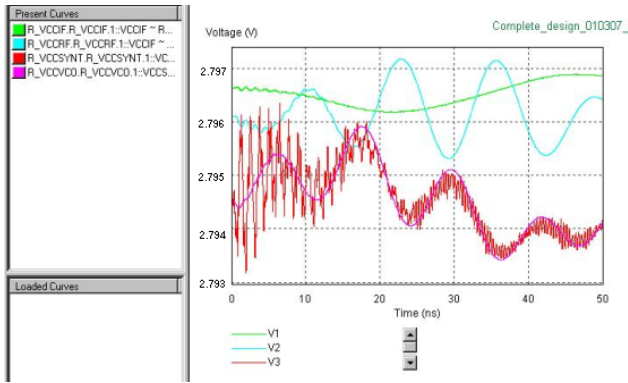


Figure 7. Voltage noise at 2.8 V supply domains at IC-1, as a result of switching activity of IC-3.

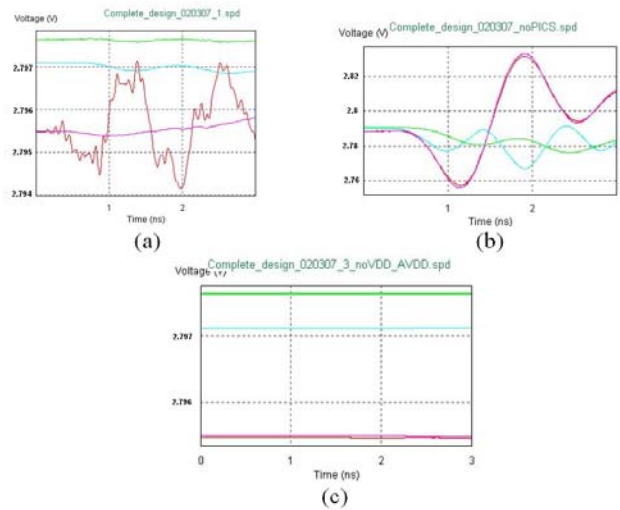


Figure 8. Noise at 2.8V supply domains of IC-1 for: (a) original design, (b) when deep-trench HD capacitors of IC-2 are excluded from design, and (c) when switching of most aggressive supply domain of IC-3 is switched off.

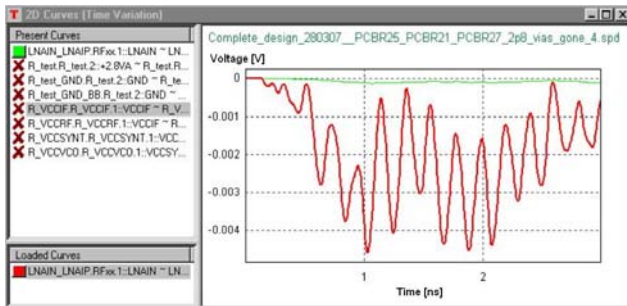


Figure 9. Noise at differential RF input of IC-1 as a result of switching activity of supply domains of IC-3. Observe suppression of the noise in the case when most aggressive switching is excluded from simulations.

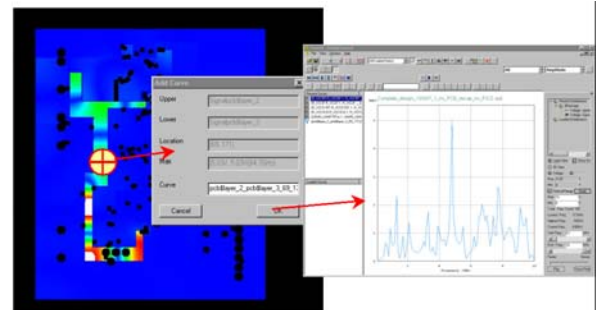


Figure 10. Impedance at each point of design can be analyzed and used for optimization of decoupling scheme: probing across PCB, package and IC domains.

Conclusions

In this paper an integral analysis technique to determine signal and power integrity of SiP's and advanced packages has been investigated through applying the flow and methodology on a representative carrier design. It has been shown that for the integral SI and PI analysis approach, defining a correct physical database that contains all the relevant physical and electrical information from PCB, package and IC domains is of paramount importance. In addition, capability of the applied tool-suite to account for distributed capacitors on passive silicon IC has been demonstrated to be an important aspect of the flow. Accuracy of the activity models of IC's has also been shown to be very important for simulation results and aligning with measurements. Finally, considering the complexity of the system, it has been demonstrated that speed and accuracy of analysis have to be in a very good balance to allow easy SI and PI what-if simulations and verifications.

Acknowledgements

Authors would like to acknowledge Sauer Sinaga and Xavier Lecoq for their support and help.

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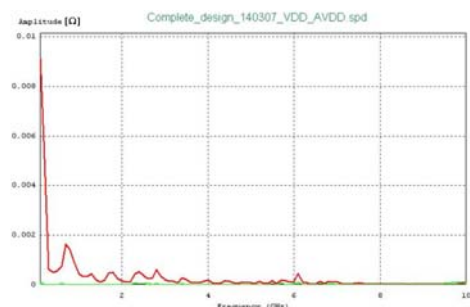


Figure 11. Transimpedance of a supply domain at IC-1 with respect to an excitation point at IC-3, with and without HD decoupling capacitors of IC-2. Reduction of impedance to very low values (flattened characteristics without peaks at ~0 amplitude hardly visible) is a result of involvement of HD decoupling capacitors.