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Application of Steinberg Vibration Fatigue Model for Structural Verification of Space Instruments

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Abstract. Electronic components in spaceships are subjected to vibration loads during the ascent phase of the launcher. It is important to verify by tests and analysis that all parts can survive in the most severe load cases. The purpose of this paper is to present the methodology and results of the application of the Steinberg's fatigue model to estimate the life of electronic components of the EPT-HET instrument for the Solar Orbiter space mission. A Nastran finite element model (FEM) of the EPT-HET instrument was created and used for the structural analysis. The methodology is based on the use of the FEM of the entire instrument to calculate the relative displacement RDSD and RMS values of the PCBs from random vibration analysis. These values are used to estimate the fatigue life of the most susceptible electronic components with the Steinberg's fatigue damage equation and the Miner's cumulative fatigue index. The estimations are calculated for two different configurations of the instrument and three different inputs in order to support the redesign process. Finally, these analytical results are contrasted with the inspections and the functional tests made after the vibration tests, concluding that this methodology can adequately predict the fatigue damage or survival of the electronic components.

INTRODUCTION

Spaceships are subjected to several mechanical loads during the ascent phase of the launcher generated by the different causes such as rocket propulsion, aerodynamic effects and pyro-shocks actuations. It is necessary to verify by analysis and tests that all parts and equipment can survive during this severe environment. Electronic components are quite susceptible to be damaged by fatigue due to random vibration and shock loads, and therefore, they need to be verified during the qualification and acceptance phases of the project. In recent years, the need for fatigue analyses in space projects has been increased due to the development of new reusable launchers as Falcon 9 [1], where their electronic equipment are subjected to the vibration loads of various ascent phases. Therefore, fatigue analysis should be implemented in the structural verification plan of the electronic equipment.

Steinberg, in Ref. [2], developed a fatigue model that predicts the life of electronic components attached to a printed circuit board (PCB), where only a few parameters of the component and the PCB need to be known. Steinberg model has the advantage of estimating in a simple way the survival of the joints between electronic components and the PCB subjected to dynamic loads like random vibration and shock. This fatigue model has been implemented in several applications as Vibrationdata [3], where the maximum relative displacement spectral density (RDSD) curve of the PCB expected from random vibration environment is used as input to obtain the cumulative damage index (CDI). Recent research works studied the influence of the input parameters [4] and validated the Steinberg's model [5] in order to demonstrate that can be applied for engineering projects. In Ref. [6] the Steinberg's model is compared with the Steinberg's three-band method by finite element analysis (FEA) with the objective of calibrating the parameters. Other research works [7]–[11] developed and used more sophisticated fatigue analysis methods that need detailed finite element models and the results of several tests. With the aim of

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improving the accuracy of simplified FEM, it is necessary to find an adequate modeling approach to take into account the influence of the electronic components on the mass and stiffness of the PCB [12], [13] and to correlate with the test results [14].

In this paper, the application of the Steinberg's model to predict the fatigue life of the electronic components is presented for the process of structural verification of the EPT-HET instrument of Solar Orbiter space mission. All the steps to calculate the fatigue life are indicated and the results are contrasted with the inspections performed after the vibration tests to find the possible damage on the pins of electronic components. The results show that the application of this method can prevent the damage caused by random vibration loads and can help in the structural verification of the PCB assemblies for future space programs.

THEORETICAL BACKGROUND

The principal formulation used for this analysis can be found in the book of Dave S. Steinberg 'Vibration Analysis for Electronic Equipment' [2]. In addition, the software created by Tom Irvine (Vibration Data) has a module of fatigue of electronic components that has been used for more precise calculations in this paper. It employs an extension of the Steinberg approach to take into account the RDSD curve of each PCB in the fatigue analysis [3].

Steinberg's Fatigue Limit Equation

Equation (1) determines the maximum relative displacement (3σ-RMS) at the center of a PCB that will give a fatigue life of 20 million of cycles in a random vibration environment for a particular component mounted on the PCB. The input data for this equation (see Table 1) are the dimensions of the PCB and the length, position (Table 2) and type (Table 3) of the electronic component.

$$Z_{3\sigma\text{limit}} = \frac{0.02816B}{Chr\sqrt{L}} \tag{1}$$

Derivation of the Fatigue Curve

Equation (2) relates the 3σ-RMS value of the maximum relative displacement ($Z_{3\sigma}$) obtained from FEA and the number of cycles (N) of fatigue life associated to this value. The parameters are summarized in Table 4.

$$N = 20x10^6 \left(\frac{Z_{3\sigma\text{limit}}}{Z_{3\sigma}} \right)^b \tag{2}$$

TABLE 1. Parameters of Steinberg's Fatigue Limit Equation [2]

Parameter Symbol	Parameter Name	Units
$Z_{3\sigma\text{limit}}$	Maximum relative displacement (3σ-RMS) of the PCB	mm
B	Length of the circuit board edge parallel to the component	mm
L	Length of the electronic component	mm
h	Thickness of the circuit board	mm
r	Relative position factor for the component mounted on the board (Table 2)	-
C	Constant for different types of electronic components (Table 3) $0.75 \leq C \leq 2.25$	-

TABLE 2. Relative position factor values for the electronic components on the PCB [2]

r	Component Location (Board Simply Supported on All Sides)
1	Component located at the center of the PCB
0.707	Component located near one side of the PCB
0.5	Component located near one corner of the PCB

TABLE 3. Constants for different types of electronic components [3]

C	Type of Electronic Component
0.75	Axial leaded through hole or surface mounted components, resistors, capacitors, diodes.
	Fine-pitch surface mounted axial leads around perimeter of component with four corners bonded to the circuit board to prevent bouncing.
1.0	Standard dual inline package (DIP).
	Through-hole Pin grid array (PGA) with many wires extending from the bottom surface of the PGA.
1.26	DIP with side-brazed lead wires.
	Surface-mounted leaded ceramic chip carriers with thermal compression bonded J wires or gull wing wires.
	Any component with two parallel rows of wires extending from the bottom surface, hybrid, PGA, very large scale integrated (VLSI), application specific integrated circuit (ASIC), very high scale integrated circuit (VHSIC), and multichip module (MCM).
1.75	Surface-mounted ball grid array (BGA).
2.25	Surface-mounted leadless ceramic chip carrier (LCCC).

TABLE 4. Parameters of fatigue curve [2]

Parameter Symbol	Parameter Name
N	Number of cycles of fatigue life of the electronic component related to the results of the random vibration analysis.
$Z_{3\sigma limit}$	Maximum relative displacement (3σ-RMS) of the PCB related to a fatigue life of 20 million of cycles.
$Z_{3\sigma}$	Maximum relative displacement (3σ-RMS) of the PCB obtained from FEA.
b	Fatigue exponent. Takes a value of 6.4 for the Steinberg's model.

Number of Cycles Accumulated during Random Vibration Test

In order to calculate the number of cycles (n) that are accumulated during the random vibration test, Steinberg assumes only the main natural frequency of the PCB (f_1), and multiplies this value by the duration of the random vibration test (T) as shown in Eq. (3).

$$n = f_1 T \tag{3}$$

Tom Irvine's software [3] takes into account more than one mode of the PCB with the Relative Displacement Spectral Density (RDSD) curve, which is introduced as input to calculate the number of cycles (n). In the next sections, the results obtained from this software are compared with the results obtained with the Eq. (3).

Miner's Cumulative Fatigue

Equation (4) determines the accumulated fatigue of the electronic components subjected to different mechanical vibration environments. It compares the number of cycles (n_i) that a component mounted on a PCB is subjected by a particular mechanical environment with the number of cycles (N_i) that the same component can withstand in the same environment. Later, each fraction is added to get the total accumulated fatigue damage. The standards for European space projects recommend applying the safety factor of 4 to take into consideration the uncertainties of the results. In theory, the component should fail when CDI = 1.0.

$$CDI = 4\sum_{i=1}^{m} \frac{n_i}{N_i} \tag{4}$$

STRUCTURAL VERIFICATION AND REDESIGN PROCESS FOR EPT-HET INSTRUMENT

The institute IDR/UPM participates in different space missions performing structural and thermal analyses of various instruments. One of these instruments is the Electron Proton Telescope – High Energy Telescope instrument (EPT-HET), which is a unit that belongs to the Energetic Particle Detector (EPD) payload of the Solar Orbiter spacecraft.

The EPT-HET instrument has the mission of measuring the energetic particles (electrons and protons) expelled from the sun. The instrument includes three PCBs of 120x100 mm assembled inside the housing: LVPS (Low Voltage Power Supply), Digital and Analogic boards. The thicknesses of LVPS, Digital and Analogic boards are 1.51, 1.53 and 1.57 mm respectively. They are made of layers of FR4 (glass-reinforced epoxy composite) and copper, and each PCB is joined to the housing by 16 bolts on the contour. For the Steinberg's method estimations, each PCB is considered as simply supported plate at the four edges, which is a boundary condition similar to that of the design.

The initial verification plan of the EPT-HET instrument included the creation of two models: the Qualification Model (QM) to be tested in the qualification test campaign and the Flight Model (FM), which must be tested in the acceptance test campaign before being integrated into the Solar Orbiter spaceship. After qualification vibration tests, some anomalies were detected during the functional test. The later inspections revealed that some pins and glued spots of the main electronic components were broken by fatigue during the random vibration tests (see Fig.1). These failures couldn't be prevented because fatigue analysis wasn't considered necessary before the qualification test. Because of this, the qualification tests must be repeated, but on the Flight Model, becoming the Protoflight Model (PFM). With the aim of avoiding the same failures for the next test campaign, the following actions were implemented:

- Modification of the PCBs assembly design by adding stiffeners attached to center points of the PCBs. These structural elements get the decrease of the maximum deflections of the PCBs during vibration environment, and therefore, they can improve the fatigue life of the electronic components. The original design without these stiffeners corresponds to the Qualification Model, and the second design, with the stiffeners, is the Protoflight Model.
- Review and change of the levels of the random vibration specifications. The first random vibration input, estimated conservatively by the European Space Agency (ESA) with a 1σ-RMS value of 26.2 g, is referred as 'Input 1' in this paper. This environment was applied for the qualification tests and provoked cracks in the pins of some electronic components. After the qualification tests, ESA proposed a second environment ('Input 2') from a more realistic estimation, with a RMS value of 11.6 g. Finally, the levels of this second specification were reduced in a frequency band that includes the main natural frequencies of the instrument and of its PCBs in a notching procedure to prevent the over-testing. As a result, a third input ('Input 3') with a RMS value of 10.9 g was obtained and finally applied for the protoflight vibration tests. All specifications are shown in Fig. 2.
- Implementation of the fatigue analysis explained in this study to evaluate the fatigue damage considering all these changes of the design and input levels.

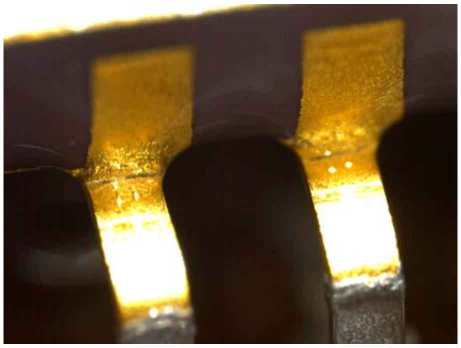


FIGURE 1. Broken pins found during the visual inspections after qualification vibration tests (Courtesy of University of Kiel)

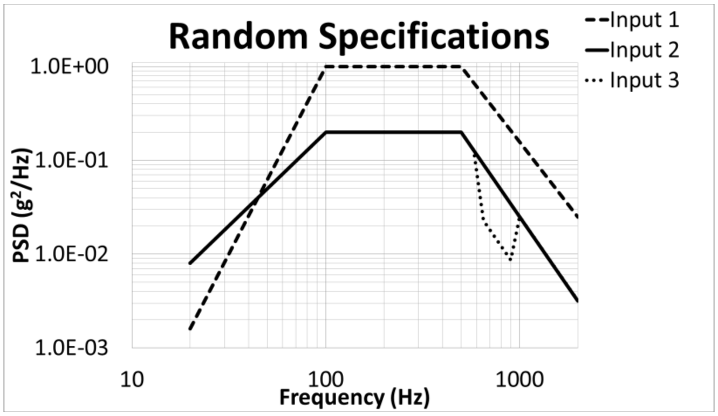
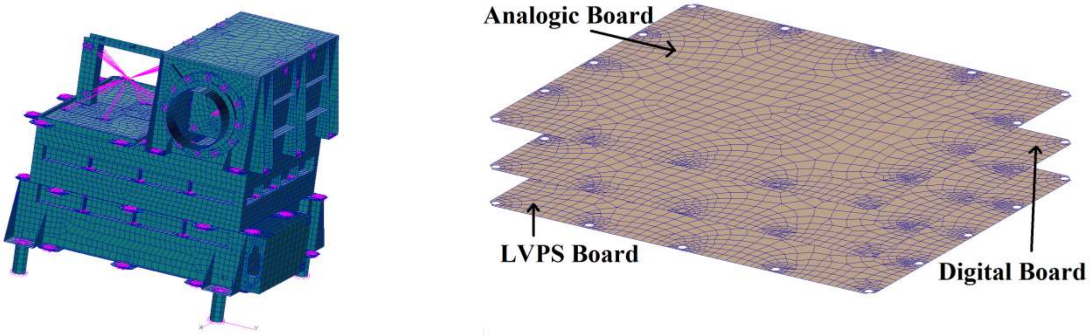


FIGURE 2. Random vibration input specifications. The 1σ-RMS values are 26.2g for 'Input 1', 11.6g for 'Input 2' and 10.9g for 'Input 3'

The methodology explained here was applied in order to get estimations for the fatigue life of the electronic components in a simple and rapid way for all the combinations considering the two design configurations and the three different random vibration loads. Only the random excitation along the axis perpendicular to the PCBs (Z-axis) is considered in this paper, because it is the most severe load condition. However, all random excitations in each of the three principal axes can also be taken into account. The advantage of this procedure is that the same finite element model of the entire instrument used for the typical structural analyses (to calculate stresses and IF forces) is also employed to obtain the maximum relative displacements (RDSD curves and RMS values). This option avoids the creation of finite element models where every electronic component has to be modeled in detail, as explained in various studies [7], [8], which requires more time of analysis and more amount of data.

FATIGUE ANALYSIS OF THE ELECTRONIC COMPONENTS

The first step is to run the random vibration analyses on the finite element model of the instrument (Fig.3) to obtain the relative displacement results of the PCBs. Two versions of the FEM were created and analyzed with MSC Patran/Nastran: the first one (see Figs. 4a and 5a) without PCB stiffeners (Qualification Model) and the second one (see Figs. 4b and 5b) with the PCB stiffeners (Protoflight Model). The approach of modeling the PCBs was the globally smeared technique, where the electronic components are not explicitly represented, but their total mass is taking into account with the Non Structural Mass (NSM) parameter for each PCB. The finite element model is correlated with the results of the qualification vibration tests in order to get the same natural frequencies and modal damping factor.



(a) (b)

FIGURE 3. Finite element model of the EPT-HET instrument (a) and the PCBs (b)

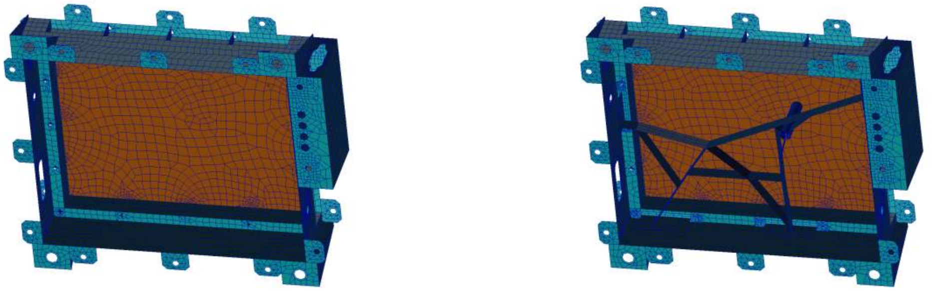

(a) (b)

FIGURE 4. FEM of the Digital Board assembled into the Instrument Housing – QM (a) and PFM (b)

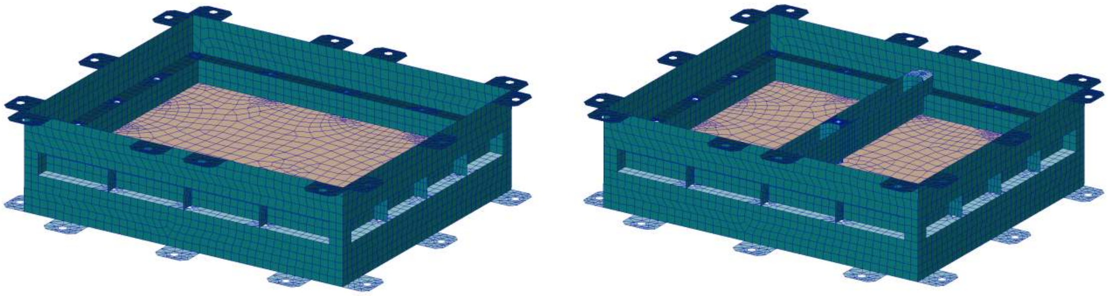

(a) (b)

FIGURE 5. FEM of the Analogic Board assembled into the Instrument Housing – QM (a) and PFM (b)

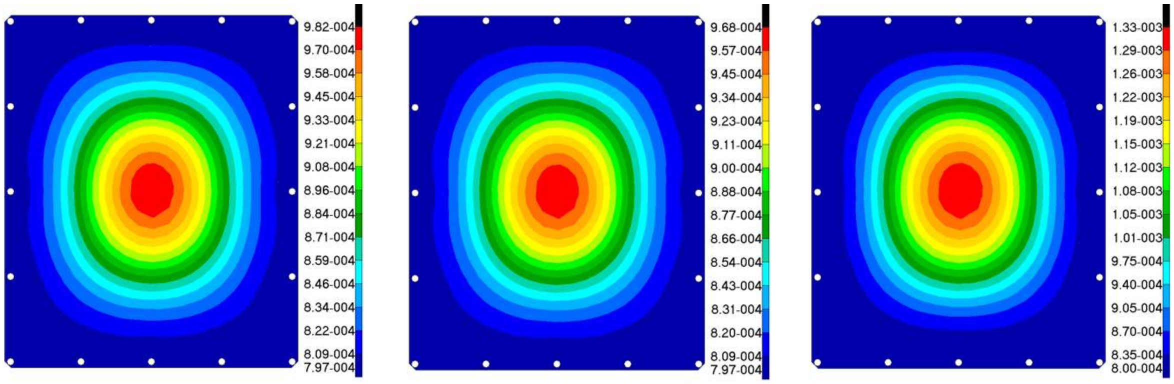
The maximum relative displacement results (RMS values) obtained from FEA are shown in Tables 5 and 6. Figure 6 shows the distributions of the absolute displacement on the three PCBs of the Qualification Model when 'Input 1' random load is applied. These distributions indicate that the maximum displacements are located at the center of each PCB. Figure 7 shows the Relative Displacement curves between the center node and the boundary of the Digital Board (see Fig. 7a) and Analogic Board of the QM (see Fig. 7b). Each one of these PCB has one Field Programmable Gate Array (FPGA) electronic component attached on the center, whose pins were broken during the qualification tests.

TABLE 5. Maximum relative displacement (3σ-RMS) for Qualification Model

PCB	**Maximum Relative Displacement $Z_{3\sigma}$ (mm)**		
	Input 1	**Input 2**	**Input 3**
LVPS Board	0.5623	0.2410	0.1448
Digital Board	0.5336	0.2287	0.1377
Analogic Board	1.1167	0.4811	0.3042

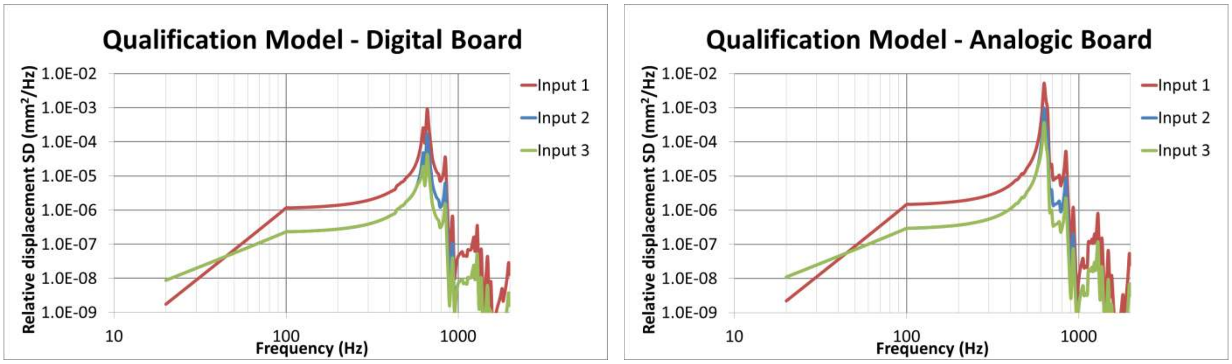
TABLE 6. Maximum relative displacement (3σ-RMS) for Protoflight Model

PCB	**Maximum Relative Displacement $Z_{3\sigma}$ (mm)**		
	Input 1	**Input 2**	**Input 3**
LVPS Board	0.4458	0.1871	0.1007
Digital Board	0.4637	0.1945	0.1042
Analogic Board	0.1314	0.0550	0.0396



(a) (b) (c)

FIGURE 6. Absolute displacement distributions (in meters) for the Qualification Model on the LVPS Board (a), Digital Board (b) and Analogic Board (c)



(a) (b)

FIGURE 7. Relative displacement spectrum density (RDSD) curves for the center node of Digital Board (a) and Analogic Board (b) in the QM configuration

TABLE 7. Values of the parameters for the Steinberg's fatigue limit equation

Electronic Component	**PCB**	**B (mm)**	**h (mm)**	**L (mm)**	**r**	**C**	**$Z_{3\sigma limit}$ (mm)**
FPGA	Digital Board	100	1.5326	40	1.0	1.26	0.2306
FPGA	Analogic Board	120	1.5702	40	1.0	1.26	0.2701

TABLE 8. Number of cycles of fatigue life (N) for FPGA component on Digital Board

Random Input	**Number of Cycles of Fatigue Life (N)**	
	Qualification Model	**Protoflight Model**
Input 1	$9.310\text{x}10^4$	$2.288\text{x}10^5$
Input 2	$2.109\text{x}10^7$	$5.944\text{x}10^7$
Input 3	$5.426\text{x}10^8$	$3.237\text{x}10^9$

TABLE 9. Number of cycles of fatigue life (N) for FPGA component on Analogic Board

Random Input	**Number of Cycles of Fatigue Life (N)**	
	Qualification Model	**Protoflight Model**
Input 1	$2.268\text{x}10^3$	$2.008\text{x}10^9$
Input 2	$4.966\text{x}10^5$	$5.273\text{x}10^{11}$
Input 3	$9.341\text{x}10^6$	$4.315\text{x}10^{12}$

The second step is to calculate with Eq. (1) the maximum relative displacement ($Z_{3\sigma limit}$) related to 20 million of cycles of fatigue life for the more susceptible electronic components (in this case, two FPGA components). Table 7 summarizes the main parameters and results of the Steinberg's fatigue limit equation.

The next step is to determine the number of cycles of fatigue life of each electronic component with Eq. (2) for the three different random inputs and for the two design configurations, taking into account the values of $Z_{3\sigma}$ provided from FEM random analysis and the values of $Z_{3\sigma limit}$ calculated in the previous step. The fatigue exponent is 6.4 for electronic structures. The results are indicated in Tables 8 and 9.

In order to calculate the number of cycles accumulated during random vibration tests (n), two methods have been taking into account. The first one consists in assuming only the first main natural frequency of each PCB (f_1) with the Eq. (3). The second method consists in using the fatigue module of the Vibrationdata software [3], introducing as input the RDSD curves (see Fig. 7 as example) and the maximum relative displacement ($Z_{3\sigma limit}$) from Steinberg's fatigue limit equation (see Table 7). This second estimation takes into account the whole relative displacement spectrum.

The specified duration of random vibration test for each axis is 120 seconds for qualification and 60 seconds for acceptance. In order to better compare the different cases (two designs and three random inputs) among them and with the qualification tests, the value of 120 seconds has been considered in the following calculations. In Table 10 are indicated the main natural frequencies obtained by FEA for each PCB for both design configurations.

The obtained results with both methods are the number of cycles accumulated during random vibration environment (see Tables 11 and 12) and the corresponding CDI values (see Tables 13 and 14). The results from these two different methods are very similar each other, showing the same order of magnitude for the CDI values.

TABLE 10. Main natural frequencies of the PCBs

PCB	Main Natural Frequency (Hz)	
	Qualification Model	**Protoflight Model**
Digital Board	660.8	745.2
Analogic Board	628.6	1048.3

TABLE 11. Number of accumulated cycles for random vibration Z-axis for FPGA component on Digital Board

Random Input	Number of Accumulated Cycles (n) with Eq. (3)		Number of Accumulated Cycles (n) with Vibrationdata Software	
	QM (120 s)	**PFM (120 s)**	**QM (120 s)**	**PFM (120 s)**
Input 1	7.930×10^4	8.942×10^4	8.051×10^4	9.118×10^4
Input 2	7.930×10^4	8.942×10^4	8.020×10^4	9.097×10^4
Input 3	7.930×10^4	8.942×10^4	7.871×10^4	9.076×10^4

TABLE 12. Number of accumulated cycles for random vibration Z-axis for FPGA component on Analogic Board

Random Input	Number of Accumulated Cycles (n) with Eq. (3)		Number of Accumulated Cycles (n) with Vibrationdata Software	
	QM (120 s)	**PFM (120 s)**	**QM (120 s)**	**PFM (120 s)**
Input 1	7.543×10^4	1.258×10^5	7.650×10^4	1.122×10^5
Input 2	7.543×10^4	1.258×10^5	7.637×10^4	1.098×10^5
Input 3	7.543×10^4	1.258×10^5	7.560×10^4	1.226×10^5

TABLE 13. Miner's cumulative fatigue (CDI) values for random vibration Z-axis for FPGA component on Digital Board

Random Input	CDI Considering Only the First Mode of Each PCB		CDI Obtained with Vibrationdata Software	
	QM (120 s)	PFM (120 s)	QM (120 s)	PFM (120 s)
Input 1	3.4	1.6	3.5	1.7
Input 2	$1.5x10^{-2}$	$6.0x10^{-3}$	$1.5x10^{-2}$	$6.3x10^{-3}$
Input 3	$5.8x10^{-4}$	$1.1x10^{-4}$	$5.5x10^{-4}$	$1.1x10^{-4}$

TABLE 14. Miner's cumulative fatigue (CDI) values for random vibration Z-axis for FPGA component on Analogic Board

Random Input	CDI Considering Only the First Mode of Each PCB		CDI Obtained with Vibrationdata Software	
	QM (120 s)	PFM (120 s)	QM (120 s)	PFM (120 s)
Input 1	$1.3x10^{2}$	$2.5x10^{-4}$	$1.4x10^{2}$	$1.9x10^{-4}$
Input 2	$6.1x10^{-1}$	$9.5x10^{-7}$	$6.5x10^{-1}$	$7.0x10^{-7}$
Input 3	$3.2x10^{-2}$	$1.2x10^{-7}$	$3.3x10^{-2}$	$8.4x10^{-8}$

As can be appreciated in Tables 11 and 12, the results obtained using Eq. (3) are independent of the input environment, whereas the results from Vibrationdata software vary slightly for the different input environments.

The final results are the accumulated fatigue damage index (CDI) values. There are some CDI values that exceed the limit of 1.0, which are considered as cases with risk of fatigue damage. This risk is higher for the worst combination of random input load ('Input 1') and design configuration (QM without PCB stiffeners) for both electronic components. There is also risk of fatigue damage for the FPGA on the Digital Board for the combination of 'Input 1' load and PFM design.

Although the method that only takes into account the first natural frequency of each PCB is simpler than using the Vibrationdata software, which considers the whole Relative Displacement Spectrum Density curve, both methods lead in very similar CDI values for each case.

SUMMARY OF THE RESULTS

The following conclusions of the fatigue analysis for the EPT-HET instrument have been deduced from the results obtained in this paper:

- For the FPGA component on the Digital Board, the most determinant action to improve its fatigue life is the reduction of the random input levels. For the most severe random input load ('Input 1'), there is high risk of fatigue damage for both design configurations. This fact agrees with the failures observed on the pins of the FPGA component after the random vibration test performed with this load on the Qualification Model. On the other hand, the stiffener for this PCB slightly decreases the fatigue damage risk, but not as much as with the reduction of the input levels. This fact can be explained because although it gets the decrease of the maximum relative displacement, this benefit is minimized by the increment of the number of the accumulated cycles during random vibration environment (n) produced by the increase of the first natural frequency of the PCB.
- For the FPGA component on the Analogic Board, the stiffener contributed the most to reduce the fatigue damage risk. This action reduces the CDI values about 6 orders of magnitude, while the change of random specification input can only reduce the CDI values by 4 orders of magnitude as much. The high value of CDI for the Qualification Model design with 'Input 1' random specification indicates a serious risk of fatigue damage, which agrees with the broken pins found after the vibration tests performed with this load on the Qualification Model.
- The final design configuration was the Protoflight Model (with stiffeners). The protoflight campaign was performed applying the random vibration environment identified in this paper as 'Input 3'. No anomalies were detected during the functional tests performed after these vibration tests. This fact confirms the low CDI values calculated applying the method explained in this paper, but considering the duration of the random test of 60 seconds for each axis for protoflight tests. The resulting CDI values for this case are the half of the values indicated in the bottom right cell of the Tables 13 and 14, which are far below of the limit of 1.0.

CONCLUSIONS

The objective of this study is to present the application of the Steinberg's method to predict the fatigue life of electronic components of the EPT-HET instrument for the Solar Orbiter program. The advantage of this methodology lies in the fact that the order of magnitude of the CDI values can indicate in a quick way the risk of fatigue damage of the electronic components avoiding the need to create a new and more detailed finite element model. Therefore, it is a useful method that can be implemented in the structural verification procedure for future space projects to get an easy estimation about the fatigue damage of the electronic components before the vibration tests.

In this study, this analytical estimation is made for different combinations of designs and random inputs and agrees with the fatigue damage on some pins of electronic components found during the inspections and functional tests made on the EPT-HET instrument after the vibration tests. Additionally, this method was able to predict the survival of the electronic components for the tests on the Protoflight Model.

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