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Application of Transmission Line Models to Backpanel Plated Through-Hole Via Design

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***Abstract*—This paper introduces an approach of using a Plated through-hole (PTH) via transmission-line model in the design of a thick printed circuit board, such as a backpanel. Full wave FEM modeling of a section of backpanel containing a differential via pair was compared with a transmission model. Computed values of the differential transmission loss agreed within an acceptable range for engineering studies, yet the transmission line model results required less than 2% of the computation time that the full wave model required. Effects of via spacing, via diameter and trace thickness were also examined.**

I. INTRODUCTION

Plated through-hole (PTH) vias are commonly used in printed circuit boards, even thick boards, such as backpanels, due to their ease of manufacturing, layout, and cost. Since backpanels are typically thicker than other printed circuit boards, the electric effects of a via may be more acute on backpanels than on thinner types of boards [1]. Typically, backpanels have signal vias even when the signal transmission is confined to a single layer. For instance, a signal transmitted through a backpanel often originates on a daughter card, goes into the backpanel through a mated pair of connector pins, and continues to another daughter card in reverse sequence. PTH vias are used to connect the connector pins to board traces and are present even when the signal on the backpanel is confined to a single layer.

As signal transmission speeds increase, the design of PTH vias becomes increasingly critical in determining the overall signal transmission quality. Full wave numerical modeling, such as finite element method (FEM), can be useful and accurate for anticipating signal quality problems in backpanels. However, full wave numerical methods can require significant computer resources (such as memory and CPU speed) to model an entire backpanel and can require significant computation time to complete a simulation analysis. Furthermore, because backpanel layouts can be complicated, the construction of full wave numerical models can be time-consuming. In practical backpanel designs, engineers usually require only an approximate estimation of the signal transmission quality. A transmission line model may be helpful in providing via characterizations to a sufficient degree of accuracy in a much shorter time than full wave numerical modeling.

The typical structures in backpanels include both signal traces and vias. It is well known that signal traces can be modeled effectively as transmission lines. The behavior of vias has also been modeled using transmission lines [2]. This work examines the use of transmission-line models for vias as well as traces.

Transmission-line models require that the cross-sectional field distribution be invariant along the axial direction. This assumption is valid for many PCB via structures. Therefore, differential vias can be treated as a multi-conductor transmission line immersed in the PCB dielectric substrate in a manner that is perpendicular to the PCB copper layers.

II. APPROACH

To validate the proposed approach, a backpanel with a pair of PTH vias, a pair of differential signal traces on layer #1 and another pair of differential signal traces on layer #18 is modeled. The geometry of a 500 x 500 mil section of the backpanel that is modeled is shown in Fig. 1. The vias are located in the center of the section. The stackup detail is shown in Fig. 2. In the real design, copper layers #2 and #17 are cut off and replaced by the adjacent fill dielectric layer material (relative permittivity: 4.06), in order to achieve a specific characteristic impedance of the top layer signal trace. The inner radius and the outer radius of the PTH vias are 13 mils and 18 mils respectively. The center-to-center distance of the two vias is 50 mils. The length of the vias is 215.6 mils. There are rectangular antipads on each of the copper layers except layers #1 and #17. The dimensions of the antipads are 68.8 x 118.8 mils. The bottom signal traces on layer #18 are parallel to each other from the vias to the edge of the backpanel. The width of the traces is 4 mils and they are 46 mils away from each other. Due to board layout restrictions, the top signal traces on layer #1 are also extended towards the edge of the backpanel, but are perpendicular to the bottom signal traces. There are also some bends in the top traces. The top signal trace width is 6 mils, and the overall length of each trace is approximately 220 mils.

An equivalent circuit for this geometry using a transmission line model is shown in Fig. 3. Transmission line h_1 is the widely-spaced portion of the top traces on layer #1 (h_1 = 110 mils) and transmission line h_2 is the narrowly-spaced portion of the top traces

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on layer #1 (h_2 = 110 mils). Transmission line h_3 is the PTH vias in the backpanel (h_3 = 215.6 mils) and transmission line h_4 is the bottom signal trace on layer #18 (h_4 = 236 mils). C_1 and C_2 represent the capacitance between the PTH vias and the adjacent ground structure layers. The value of the C_1 and C_2 is approximately 0.06 pF [3]. The equivalent circuit is simulated with HSPICE to study S_{21} of the two-port system [4]. Dielectric and skin-effect losses are included. The transmission line RLGC parameters are calculated using the XFX field solver according to the given geometry and material properties.

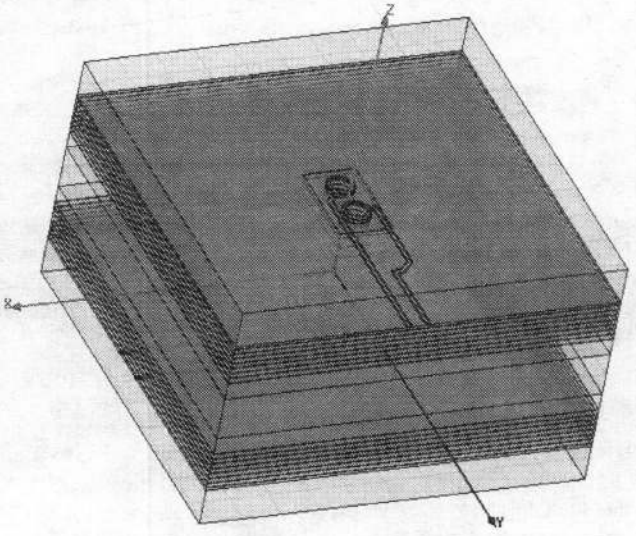

Figure 1. Modeled backpanel design with a pair of differential PTH vias and signal traces.

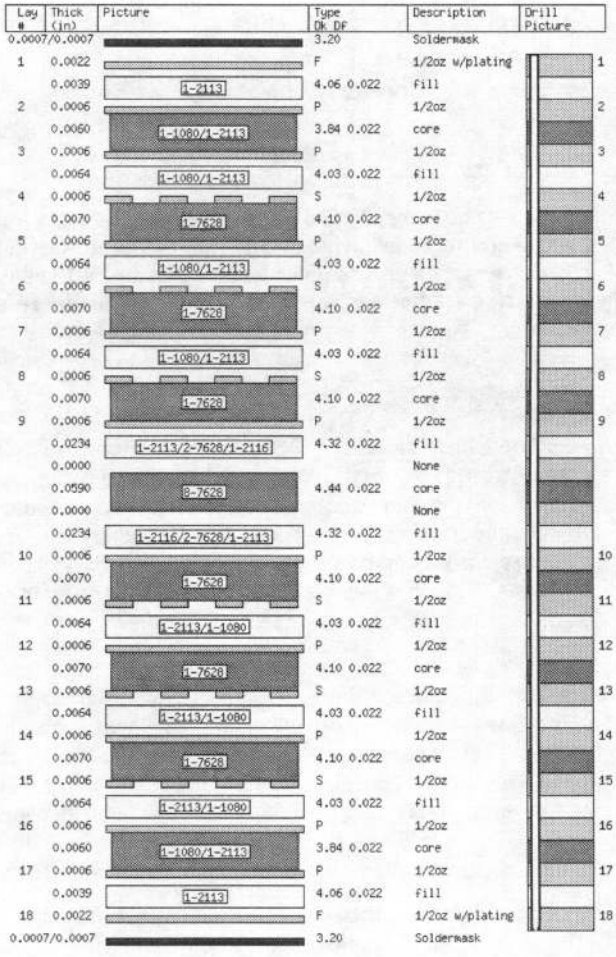

Figure 2. An 18 layer stackup for backpanels.

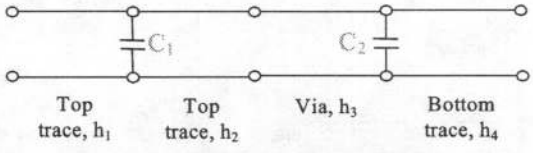

Figure 3. An equivalent circuit for the geometry shown in Fig. 1.

An FEM simulation for the same geometry shown in Fig. 1 is conducted using Ansoft HFSS. Dielectric and skin-effect losses are included in the HFSS and transmission line models. The boundary condition on the outer surface of this entire model is set to be "radiation", which makes the board appear to be infinitely large in the simulation so that there are no reflections at the boundary. In HFSS, the wave port excitation is chosen for this simulation. It is more accurate for transmission lines than the lumped port excitation, since the fields of the wave port excitation are closer to the real field distributions. The wave port excitation simulates the 2-dimensional ports at first, and uses the results to set the boundary conditions for the 3-dimensional simulation. Thus, terminal port impedance versus frequency results can be generated [5]. In the HFSS model, the reference impedance on the two wave ports is 150 ohms. Accordingly, the source impedance and load impedance in the HSPICE transmission line model are also 150 ohms.

The scattering parameter $|S_{21}|$ is calculated for both the transmission-line model and the HFSS numerical model with port 1 at the end of the top layer trace and port 2 at the end of the bottom layer trace. The comparison of the modeled $|S_{21}|$ in the frequency range 0 - 10 GHz using HFSS and the transmission-line approach is shown in Fig. 4. Instead of the smooth behavior exhibited by a typical board trace, the modeled $|S_{21}|$ shows a resonance due to the mismatches between the traces, the via pair, and the reference impedance. This resonance is undesirable for signal transmission because of increased signal losses at frequencies near it. The two modeling results agree within 1 dB for most frequency points in the 0 - 10 GHz range. There is a slight discrepancy in the resonant frequency, which may partly result from approximating the length of the top signal trace and approximating the RLGC parameters for the via transmission-line model (The influence from the copper layers and the different dielectric layers in the backpanel stackup was ignored in generating the via transmission line RLGC parameters).

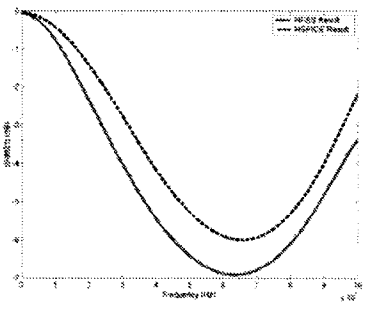

Figure 4. Compairson of HFSS and trasnsmission-line approach for backpanel geometry shown in Fig. 1.

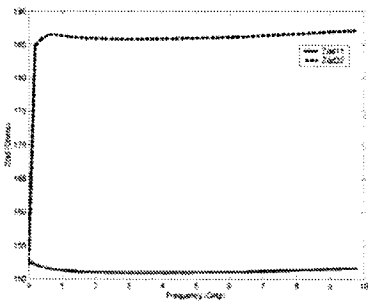

Figure 5. Terminal port impedances in the HFSS model.

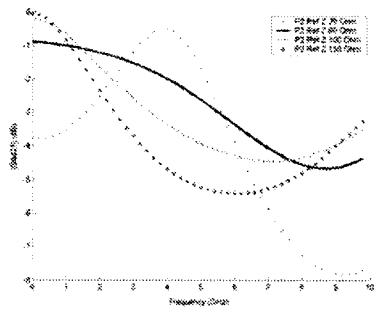

Figure 6. Comparison of S_{dd21} with different port reference impedances.

Fig. 5 shows the wave port terminal impedance calculated using HFSS. (Z_{dd11} represents the terminal impedance on the top trace on layer #1, and Z_{dd22} represents the terminal impedance on the bottom trace on layer #18.) This result also coincides with the XFX result (188 ohms for the bottom trace and 152 ohms for the top narrowly-spaced trace). The characteristic impedance for the PTH via transmission line is 110 ohms from the XFX simulation results. As stated previously, the terminal impedance is 150 ohms for the signal trace pairs on the top and bottom layers, which aggravates the mismatches between the traces, the via pair, and the reference impedance.

A slightly different HFSS model is simulated to investigate the effect of different reference impedances on the transmission quality. The length of the top layer trace is decreased from 220 mils to 170 mils (h_1 = 60 mils in Fig. 3), and the length of the bottom layer trace is decreased from 236 mils to 30 mils. All other geometric features of the new model are the same as the original. The reference impedance at port 2 on the bottom layer in the new model is changed to 20 ohms, 60 ohms, 100 ohms and 150 ohms respectively. Fig. 6 shows how the reference impedance on the bottom trace port affects the transmission quality of the backpanel.

III. Application

The transmission-line model approach can be utilized widely in backpanel designs. Here are several examples.

A. Effect of the via spacing

In order to investigate the relation between the spacing between a pair of differential vias and the scattering parameters, another model was constructed with the center-to-center distance between the two vias increased from 50 mils to 70 mils. All other geometric features of the new model were the same as the original model. Results for the new model are shown in Fig. 7. Fig. 7 can be compared with Fig. 4 to view the effects of increasing the spacing between the differential via pair from 50 to 70 mils.

As the space between the vias increases, the capacitance between the differential vias decreases. The differential vias impedance is closer to the top and bottom trace impedances. Thus, the magnitude of S_{dd21} is supposed to increase for a wider via space. As shown in Fig. 7 and Fig. 4, the comparison result supports this assumption. The resonance frequency is decreased from 6.3 GHz for the 50-mil-spacing vias to approximate 5.9 GHz for the 70-mil-spacing vias. This is due to the decrease of the space between the vias and the copper layers, which will result in the greater value of C_1 and C_2, capacitance between the PTH vias and the adjacent ground layers. The relocation of the vias also slightly affects the length and the RLGC parameters of the top and bottom trace transmission lines, which is not included in the corresponding HSPICE model. This may explain the increased difference between the HFSS result and the HSPICE result.

B. Effect of the via diameter

In order to investigate the relation between the via diameter and the scattering parameters, another model was constructed with the via outer radius decreased from 36 mils to 26 mils and inner radius decreased from 26 mils to 16 mils. In the HPICE model, the

value of the C_1 and C_2 are approximated to be 0.03 pF because the capacitance is determined by the size of the vias and thinner vias will result in lower capacitance. All other geometric features of the new model are the same as the original one. The effect of the smaller via structure can be observed by comparing Fig. 8, to Fig. 4.

The decrease in via diameter increases the inductance of the differential via pair resulting in an increase of the differential impedance. Thus, the S_{dd21} magnitude is assumed to increase with a smaller via size. Comparing Fig. 8 and Fig. 4, supports this assumption. In the frequency range from 0 to 10 GHz, the magnitude of S_{dd21} for the model with smaller via size is greater than that for the model with bigger vias.

C. *Effect of the trace width*

The width of the trace on the bottom layer was increased from 4 mils to 8 mils to investigate the effect of trace width on the S_{dd21} magnitude. All other geometric features of the new model were the same as the original one.

Increasing the width of the bottom traces increases the capacitance of the differential traces, resulting in a decrease in the differential impedance making it closer to the reference impedance (150 ohms). Thus, the S_{dd21} magnitude increases with a greater bottom trace width. A comparison of Fig. 9 and Fig. 4 demonstrates this. If the bottom trace width were decreased to 2 mils, HFSS would have trouble modeling this geometry due to the limitations of the algorithm and the available memory. However, the transmission line model could still be applied.

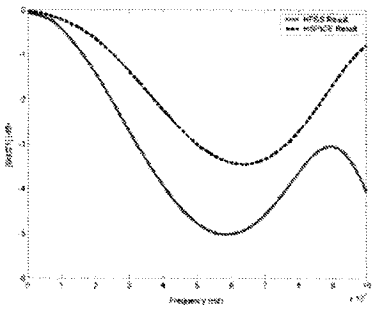

Figure 7. Comparison of S_{dd21} from 70-mil-spacing vias.

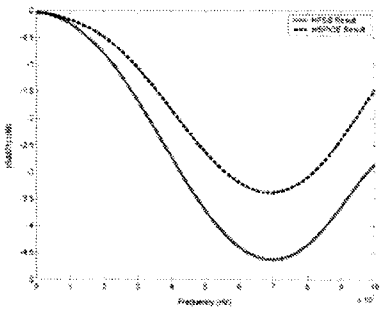

Figure 8. Comparison of S_{dd21} for smaller via size

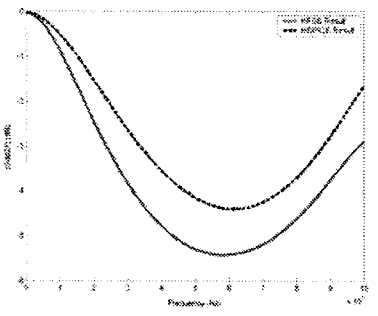

Figure 9. Comparison of S_{dd21} for 8-mil-wide bottom trace

IV. Summary and Conclusions

A transmission-line approach was used to model the effects of differential vias in a practical backpanel design. This approach used transmission-line segments to model vias and signal traces. Modeled scattering parameters compared favorably with those from a full-wave FEM method, demonstrating that modeling PTH vias in backpanels as transmission line segments can be sufficiently accurate for engineering studies and backpanel design. In the backpanel example, the two modeling results agree within 1 dB for most frequency points in the 0 - 10 GHz range. The signal transmission loss due to the mismatch between the traces, the via pairs, and the reference impedance can be determined quickly and effectively using the transmission-line approach. For the example described, it took several hours to construct the numerical model and more than 10 hours to complete each simulation on a UNIX workstation. In contrast, the transmission line model analysis can be completed within minutes once the transmission line parameters have been determined.

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