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Applications of Graphene Devices in RF Communications

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ABSTRACT

Graphene, a one-atom-thick layer of carbon atoms arranged in a honeycomb lattice, has recently attracted great interest among physicists and engineers. The combination of the unique properties of graphene with new device concepts and nanotechnology can overcome some of the main limitations of traditional radio frequency electronics in terms of maximum frequency, linearity, and power dissipation. In this article we review the current status of research on graphene-based electronic devices for RF applications. The future challenges facing this rising technology and its feasibility for a new generation of applications in RF communications and circuits are also discussed.

INTRODUCTION

In 2004 scientists from the University of Manchester isolated graphene, a one-atom-thick layer of carbon atoms arranged in a honeycomb lattice through sp² bonding (Fig. 1) [1]. Considered for many years an impossible goal, the isolation of graphene triggered a revolution not only among condensed matter physicists but also among chemists and engineers, eager to take advantage of its unique properties [2, 3].

The symmetry of its honeycomb lattice structure confers to graphene very unique transport properties [4]. For example, the carriers in graphene lose their effective mass and can be described by a Dirac-like equation instead of by the Schrödinger equation used in traditional semiconductors. This very low effective mass is responsible for a very high electron and hole mobility in excess of 200,000 cm²/Vs at T = 5 K [5] and in excess of 100,000 cm²/Vs at T = 240 Kin suspended graphene [6], the highest ever reported for any semiconductor. Second, graphene is a zero-bandgap material where the conduction and valence bands touch each other at a point called the Dirac point. In addition to this zero bandgap, the density of states in graphene is zero at the Dirac point and increases linearly for energies above and below it, which allows for carrier modulation. Third, the carriers in graphene are confined to a layer that is only one atom thick. This allows unprecedented electrostatic confinement, and also makes graphene extremely flexible and transparent.

These unique properties of graphene have motivated intense work among physicists and engineers who have seen in this material new opportunities to improve digital and radio frequency (RF) electronics, advanced sensors, transparent electronics, low-power switches, solar cells, and even battery energy storage. In this article we review some of the recent progress made in the use of graphene devices for communication applications. The next section discusses the various growth techniques currently used to synthesize graphene, and we then introduce the basic fabrication technology common to many graphene devices. We then describe several graphene devices with the potential to impact future communication systems. In particular, we summarize the current effort on graphene low noise amplifiers, graphene nonlinear electronics, and focus on the use of graphene in RF electromechanical resonators and switches. The final section offers some conclusions and future prospects of this amazing new material.

GRAPHENE GROWTH

Graphene was first discovered through the successive peeling of highly oriented pyrolytic graphite (HOPG) using scotch tape [1]. This amazingly simple method, also known as mechanical exfoliation, has been effective at producing graphene flakes 20-1000 µm in length, and has been the primary source material for most papers reporting graphene's extraordinary physical and electronic properties. Unfortunately, while these flakes have generated impressive performance, working with them involves consuming effort to locate and identify single-layer flakes. Furthermore, electron beam lithography is necessary to pattern graphene transistors in these randomly arranged flakes, and it usually has a throughput of only a couple of transistors per sample.

Therefore, extensive research and interest have focused on developing methods for large area synthesis of graphene. The two most common methods are silicon carbide (SiC) sublimation and chemical vapor deposition (CVD). The first method is the process of heating silicon carbide substrates under vacuum [7]. By heating up these substrates to about 1400°C, the silicon at the surface sublimates, leaving behind carbon

that forms thin crystalline graphene sheets. By controlling the crystal orientation of the SiC, one can control the number and mobility of graphene layers. The growth on the Si-face of SiC renders a few-layer graphene sheet with mobilities around 1500 cm²/Vs, while the growth on the C-face results in much thicker multilaver graphene with mobilities as high as 200,000 cm²/Vs. The screening of charged impurities by the outermost graphene layers is believed to be responsible for the very high mobility reported in the thick graphene grown on C-face SiC. In spite of the higher mobility of graphene grown on C-face, Si-face is typically used for RF devices due to the much higher carrier modulation resulting from the thinner graphene layer [8]. Unfortunately, the high cost and relatively small size of available SiC wafers (up to 4" in diameter) does not make this process amenable to large wafer scale processing.

Conversely, CVD graphene can be grown on arbitrary sized wafers coated with thin film catalysts. These metal catalysts serve to help decompose hydrocarbon gases into elemental carbon and hydrogen, and provide a substrate for carbon deposition. The observation of carbon depositions on metal catalysts has been known for many years due to their reduction of catalytic efficiency of nickel. It is only with the discovery of graphene that this effect has been harnessed for large area synthesis. The two most common metal catalysts used today are nickel and copper, each of which can be deposited as a thin film or rolled into thin foils. Initial work focused on ambient pressure CVD (AP-CVD) on nickel films [9, 10]. Carbon deposited on the surface of the catalyst diffuses into the bulk, creating a solid solution of metal and carbon. Due to the change in solubility with respect to temperature, carbon begins to precipitate out of solution as the sample is cooled down. Through careful control of the cooling rates, the surface coverage of single and bilayer graphene can be controlled, yielding > 80 percent coverage. Recently it has been shown that due to the lower bulk solubility of carbon in copper, the reaction of graphene on copper is surface limited, producing almost complete coverage of single-layer graphene [11]. Furthermore, copper growth is done with lowpressure CVD (LP-CVD), and thus allows for higher throughput growth and conserves on source materials.

As with HOPG graphene, CVD grown graphene needs to be transferred onto an insulating substrate before processing. This is done by spin coating a thin polymer layer such as PMMA on top of the graphene followed by chemical etching of the catalyst — thus freeing the graphene/PMMA film from the substrate (Figs. 2 and 3a). The film can then be transferred to any arbitrary substrate. The PMMA is then removed using solvents and forming gas annealing to burn off any organic residue. This process has no fundamental limitations on size and has already been demonstrated on 4-in wafers. Observed mobilities are also on the same order as SiC of 1000-2500 cm²/Vs. Most recent work has been focused on optimizing the catalyst and growth conditions to achieve the highest quality and largest grain sized graphene. Fur-

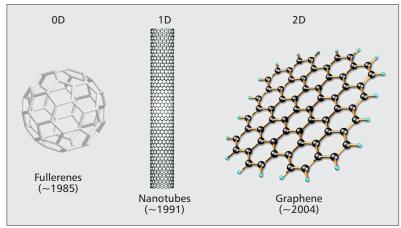


Figure 1. Diagram of different low-dimensional carbon structures and the year of their discovery/isolation.

thermore, transferless processes and direct growth on insulating substrates similar to SiC are being investigated to further simplify the growth and fabrication process.

GRAPHENE FABRICATION TECHNOLOGY

Although graphene shares many of its outstanding properties with carbon nanotubes, graphene devices are strongly preferred from a commercial point of view because their fabrication is very similar to traditional planar wafer-size Si processing. Devices are patterned using standard photolithography tools or electron-beam lithography. Metal contacts are deposited through liftoff, and graphene is subsequently etched with oxygen plasma. Finally, a gate dielectric is deposited and the gate metal is patterned (Fig. 3b). Most of the fabrication technology mirrors all the work done on carbon nanotube field effect transistors (CNT-FETs) in terms of selection of ohmic metals, gate dielectrics, and so on. However, there are four main issues for graphene fabrication that still require optimization: substrate selection, contact resistance, gate dielectric deposition, and band gap engineering.

Every atom in a graphene film is at the surface and strongly interacts with the surrounding environment, which opens numerous opportunities for new device concepts, but also new sources of performance degradation. So far the most dominant mechanism for mobility degradation in graphene is charged impurities. Therefore, much work has been dedicated to studying various high-k dielectric materials and substrates to screen the effects of any charged impurities and reduce surface phonon effects. By carefully controlling the graphene-substrate interface, mobilities as high as 20,000 cm²/Vs have been demonstrated. In spite of some partial success in identifying suitable substrates, more work is needed in this area as the reported mobilities are still far from the record mobility recorded in suspended graphene, where the substrate underneath the graphene film was etched away [5]. The lack of substrate in these measurements prevents any degradation through surface vibraGraphene is uniquely suited for high frequency low noise amplifiers. Its extremely high mobility offers the potential of ultra low source-to-drain resistances, extremely high current densities, and high efficiency operation.

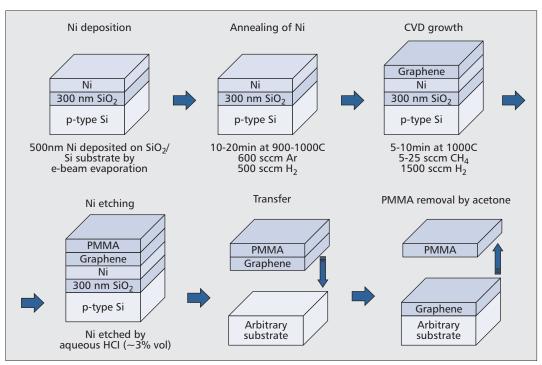


Figure 2. *Main steps in the CVD growth and transfer of graphene.*

tions (phonons) or nearby charged impurities, both of which greatly reduce graphene's intrinsic properties. However, most practical applications require that a substrate allows for proper heat dissipation; therefore, the choice of substrate and its interaction with graphene are of utmost importance.

A second important processing issue in graphene devices is to optimize the metallization for reducing contact resistances. Most work has been done on matching work functions of graphite and the metal. The most common metal combinations are Cr/Au, Ti/Pt, and Ti/Pd/Au. Based on experiments done in our laboratory, Cr/Au contacts give contact resistances in the range $1 \times 10^{-4} - 2 \times 10^{-4}$ ohm.cm². Ti/Pt gives similar contact resistance as Cr/Au contacts. Ti/Pd/Au contacts give contact resistances in the range $0.5 \times 10^{-4} - 1 \times 10^{-4}$ ohm.cm². However, there is still no consensus as to which one provides the lowest contact resistance. Furthermore, since graphene is so easily doped by its environment, metal on graphene may end up doping the underlying graphene, creating a potential barrier into the undoped graphene channel. This increased resistance is detrimental towards highspeed operation due to the increased RC time to charge and discharge all of the capacitances.

One of the most difficult problems with graphene processing has been finding the appropriate gate dielectric material. Atomic layer deposition (ALD) is the most commonly used deposition method due to the accurate control of the layer thickness that it allows. Unfortunately, ALD relies upon alternating pulses of water and precursor materials. Graphene is hydrophobic and thus the deposition of high quality pinhole-free ALD is very difficult. Various approaches have been attempted utilizing chemical functionalization with NO2, aluminum

oxidation, or seed layers to provide a template for ALD that does not reduce the mobility of the carriers in graphene. Recently, impressive results in mobility have been demonstrated through non-covalent bonding of polymers on graphene to serve as a thin *buffered* layer [12].

Finally, there is growing interest in bandgap engineering of graphene. Unlike conventional semiconductors such as silicon, which contain a bandgap, graphene is a zero-bandgap material and has ON/OFF ratios around 5-10, thus limiting its effectiveness for digital applications. Much work has been focused on generating a bandgap of up to 500 meV through 1-D quantum confinement of graphene nanoribbons (GNR) or through strain induced substrate interactions. So far, GNR have demonstrated moderate band gaps that have translated to much higher ON/OFF ratios [13], however the fabrication of these GNR transistors is very challenging. Electron-beam lithography is limited to feature sizes around 10-20 nm. However, to generate an appropriate sized band gap requires dimensions on the order of <10 nm. Furthermore, sidewall roughness also limits the mobility of these transistors due to edge state scattering. An alternative approach to open a bandgap is by applying vertical electric fields in bilayer graphene [14]. Although this method has been successful in opening optical bandgaps (100-200 meV), the electrical bandgap has been much smaller than expected (<20 meV) and more work is needed to understand the full potential of this technology.

LOW NOISE AMPLIFIERS

Graphene is uniquely suited for high frequency low noise amplifiers. Its extremely high mobility offers the potential of ultra low source-to-drain resistances, extremely high current densities, and high efficiency operation. In addition, the unprecedented carrier confinement allowed by its one-atom thickness minimizes short channel effects and opens the door to ultra high frequency operation.

The first graphene FET (GFET), reported in 2004, was fabricated on an HOPG graphene flake deposited on top of a SiO₂/Si substrate [1]. The 300 nm thick SiO₂ layer deposited between the Si wafer and the graphene layer serves two different functions. First, its thickness was optimized to maximize the optical contrast between the graphene flake and the substrate in order to see the flake. Second, the SiO₂ layer served as gate dielectric. However, due to the large thickness of the SiO₂ layer, the device transconductance was very low, severely degrading the device properties. Lemme et al. demonstrated in 2007 the first top-gated graphene transistor [15]. In this device, a thin SiO₂ layer was used as gate dielectric. Although the use of a top-gate allowed much higher gate capacitance and modulation capability, the SiO₂ gate dielectric used in this demonstration caused a seven-fold reduction in the electron and hole mobility of the graphene layer.

The last few years have seen a fast increase in the frequency performance of graphene transistors. For example, Moon $et\ al.$ from HRL reported on the fabrication of GFETs grown on SiC substrates with an $f_T=4.2$ GHz and an $f_{\rm max}$ of 14 GHz in self-aligned devices with a gate length of 1 µm [16]. A record power gain cut-off frequency ($f_{\rm max}$) value of 14 GHz was reported for these devices. Y.M Lin from IBM reported non-self aligned devices fabricated on graphene flakes with an intrinsic f_T of 100 GHz [17]. To reduce the access resistances in these non-self-aligned devices, a substrate voltage was applied to induce carriers in the access regions.

In spite of the significant recent progress, there are still several issues that need to be overcome in order to use graphene as a low noise amplifier. First, the field effect mobility of graphene top-gated transistors, typically below 2000 cm²/Vs, is still many orders of magnitude lower than the mobility measured in suspended graphene samples. Also, the different surface functionalization methods used to deposit the gate dielectric on top of graphene are not completely reproducible. In addition, the lack of a bandgap reduces the ON-OFF modulation to a factor of 10, in the best case. This low modulation significantly reduces the device efficiency. Finally, the lack of a bandgap and the ambipolar transport increases the output conductance of these devices, which typically do not show current saturation. This high output conductance severely limits their power gain performance.

To improve the ON-OFF ratio and to increase the efficiency of future graphene amplifiers, several groups are trying to induce a bandgap in graphene as discussed in the previous section. However, each of the existing methods have their limitations either in fabrication or due to edge roughness of nanoribbons.

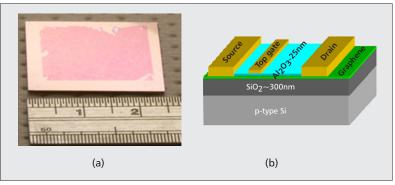


Figure 3. a) Optical micrograph of a CVD-grown graphene layer transferred to a Si substrate (courtesy of Jing Kong's lab at MIT); b) cross-sectional structure of a graphene field effect transistor. The p-type Si substrate is often used as a bottom gate to the device.

AMBIPOLAR NONLINEAR ELECTRONICS

One of the most intriguing properties of graphene is its ambipolar transport [4]. In graphene ambipolar transistors, the drain current is based on hole conduction for gate-to-source voltages below the minimum conduction point voltage ($V_{G,\min}$), while at higher voltages electron conduction dominates, as shown in Fig. 4a. Ambipolar transport in graphene together with its high mobility truly distinguishes graphene from other semiconductor materials and allows completely new nonlinear devices for radio frequency (RF) and mixed-signal applications, such as full wave rectifiers, frequency doublers, and mixers.

The V shaped current-voltage (I-V) transfer characteristic of graphene ambipolar transistors [4, 18] closely resembles that of an ideal full-wave rectifier (Figs. 4b and 4c). With a single graphene device it is therefore possible to realize full-wave rectification with zero-volt threshold voltage, something that would require a full bridge circuit with four diodes made of conventional semiconductors or an operational amplifier for zero-volt rectification.

Graphene ambipolar transistors can also be used for frequency doubling [18], by biasing the gate to the minimum conduction point and superimposing a sinusoidal input signal to the gate (Fig. 4d). Electrons and holes conduct in alternative half cycles to produce an output signal at the drain, whose fundamental frequency is twice that of the input. Figure 5a shows the experimental demonstration of this concept based on CVD grown graphene with an input frequency of 20 MHz and an output frequency of 40 MHz. This frequency doubler device shows high spectral purity in the output RF signal, where 93 percent of the output RF energy is at the fundamental frequency (40 MHz). Measurements at a lower input frequency (100 Hz) demonstrated similar spectral purity, confirming that the high spectral purity at the output is due to the sublinear I_{DS} - V_{GS} characteristics, not to parasitic capacitances. This is the first time frequency doubling is realized with just a single transistor device and with high spectral purity at the output without any filtering elements.

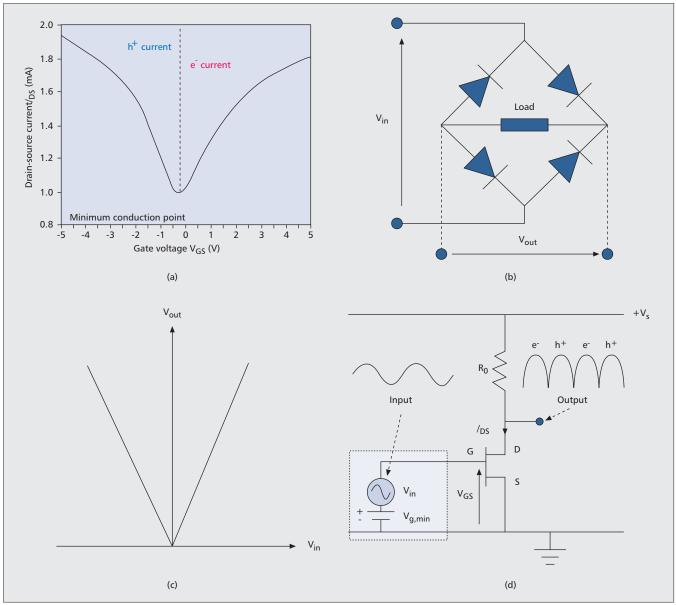


Figure 4. a) Transfer characteristic of a typical ambipolar G-FETs fabricated in the Palacios' lab at MIT; b) circuit diagram of a full-wave rectifier made with conventional diodes; c) transfer characteristics of the full-wave rectifier circuit shown in b). Diodes with zero threshold voltage are required to achieve this ideal behavior; d) graphene-based circuit for frequency multiplication of the input signal V_{in} . With the device biased at the minimum conduction point, electrons (e-), and holes (h+) conduct alternatively in neighboring half-cycles of the output signal.

GFETs can also act as a nonlinear component for frequency mixing. The symmetrical transfer characteristics of GFETs usually show a very significant quadratic component (Fig. 4a); hence, these devices can be used as excellent RF mixers. Assuming that the transfer characteristics of the GFET are completely symmetric, and infinitely differentiable, we can then describe the drain current as

$$I_D = a_0 + a_2(V_{GS} - V_{G,\min})^2 + a_4(V_{GS} - V_{G,\min})^4 + \dots,$$
 (1)

where $V_{G,\min}$ is gate voltage at the minimum conduction point. a_0, a_2, a_4, \ldots are constants. From this expression, for ideal GFETs with symmetric transfer characteristics and biased at the

minimum conduction point, no odd-order intermodulation distortions should appear at the output, and all the output power is coupled to the difference and sum frequency, and other evenorder terms. Therefore odd-order intermodulations, which are often present in conventional unipolar mixers and are harmful to circuit operations [19], can be significantly suppressed in GFET mixers.

Figure 5b shows the power spectrum at the output of a graphene mixer. If two signals, an RF input signal and a local oscillator (LO) signal with frequencies $f_{\rm RF}=10.5$ MHz and $f_{\rm LO}=10$ MHz, are introduced to the gate, the GFET mixes them to generate output signals with a frequency equal to the sum $(f_{\rm RF}+f_{\rm LO}=20.5$ MHz) and difference $(f_{\rm RF}-f_{\rm LO}=500~{\rm kHz})$ at

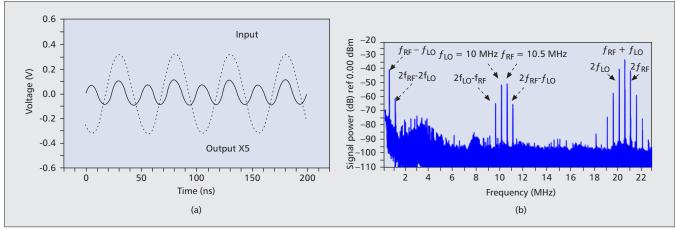


Figure 5. a) Experimental demonstration of a graphene frequency multiplier with input signal at 20 MHz and output signal at 40 MHz. Frequency doubling is clearly achieved. The output signal shows high spectral purity and low noise. b) Power spectra at the output of a graphene ambipolar mixer with input signals at 10 and 10.5 MHz. Due to the symmetric character of the transfer characteristic of a graphene ambipolar device, the odd-order intermodulation products are attenuated with respect to the even-order ones.

the same time that the odd-order intermodulation products are significantly suppressed. These new devices, a result of the unique transport properties of graphene, can potentially revolutionize the way many RF communication circuits are designed and can improve chip performance.

Compared to conventional Si and III-V electronics, ambipolar graphene electronics have many advantages. The higher mobility of graphene allows higher operating frequency for frequency doubling and mixer applications. In addition, ambipolar devices can significantly reduce the number of transistors needed in these applications. Simpler circuits mean less power consumption and smaller chip area. In addition, graphene is also an ideal material for flexible electronics. Graphene grown by CVD can be transferred to arbitrary substrates, including transparent and elastic substrates. Furthermore, the two-dimensional geometry, in combination with the excellent chemical and thermal stability of graphene make fabrication of graphene circuits fully compatible and integrable with silicon technology, which is the mainstream of the semiconductor industry.

To achieve the expected high frequency performance, the device geometries and technology need to be optimized. The current frequency performance of graphene mixers is limited to tens of megahertz in this experiment due to the parasitic capacitances and resistances. f_T can be calculated by using the expression

$$f_T = \frac{g_m}{2\pi C_C}.$$

In our device $g_m = 5.5$ mS/mm, as obtained from the slope of the I_{DS} - V_{GS} curve. Capacitance-voltage (CV) measurements show a gate capacitance of 4.5 pF/mm in this device. This leads to a calculated f_T of about 190 MHz for these devices. Higher frequency performance can be achieved by shrinking the gate length and gate oxide thickness in the device. As a first order estimation, using a $1/L_G^2$ dependence for f_T , the maximum frequency of these devices will be in the

gigahertz range for gate lengths less than 1 μ m, and exceeding 100 GHz for gate lengths of 60 nm. Much higher frequencies would be possible in devices with mobilities above 1000 cm²/Vs.

GRAPHENE RESONATORS AND RF SWITCHES

Numerous communication systems rely on electromechanical devices, such as filters, resonators, and RF switches. The miniaturization of these devices will strongly affect the development of future communication systems. The ultimate limit to this miniaturization is represented by graphene electromechanical devices, which are only one atom thick. In fact, its enormous stiffness and low density make graphene the ideal material for these kinds of devices.

The first electromechanical devices ever demonstrated in graphene were nanomechanical resonators. In 2009 Chen et al. fabricated monolayer graphene nanomechanical resonators with operating frequencies in the 50–80 MHz frequency range [20]. These devices showed quality factors of $\sim 1 \times 10^4$ at low temperatures (5 K). It has been predicted that graphene's ability to withstand ultrahigh strains, up to ~ 25 percent in nanoindentation experiments, will allow increasing the resonance frequency of these devices above the gigahertz range while maintaining a robust signal level.

Graphene electromechanical switches have also been demonstrated recently. Milaninia *et al.* [21] developed a switch comprising two polycrystalline graphene films grown by CVD. The top film is pulled into contact with the bottom one by applying a voltage of 5 V between the layers, and the contact is broken after removing the voltage due to restoring mechanical forces. In the ON state, more than 7 kA/cm² of current can flow through the switch. Although the device performance suffers from a relatively large contact resistance, it is expected that the graphene-graphene contact will be more robust than the traditional metal-metal contact, which will signif-

Advanced graphene devices could enable the introduction of advanced RF communication systems in a broad array of new applications. Graphene is in an excellent position to help RF communication systems to become even more ubiquitous and versatile than they are today.

icantly increase the reliability of future DC and RF switches.

CONCLUSIONS, CHALLENGES, AND **PROSPECTS**

In summary, graphene is both quantitatively and qualitatively different from any other material conventionally used in electronic applications. Not only does it have room temperature electron and hole mobilities more than 100 times higher than those of Si, as well as excellent mechanical properties, but also, its ambipolar transport properties, ultra thin and flexible structure, and electrostatic doping offer a new degree of freedom for the development of advanced electronic devices with many potential applications in communications and RF electronics.

From the preliminary device results currently available, graphene offers great potential to impact RF communication electronics in areas as diverse as low noise amplifiers, frequency multipliers, mixers and resonators. However, in order to take advantage of the full potential of graphene devices, more basic research needs to be combined with improved material growth and device technology. A better understanding of parameters such as breakdown voltage, electron velocity, and saturation current is needed to allow a complete benchmark of this material and an evaluation of its potential performance. In addition, these new applications will have to overcome the limitations of graphene that arise from the lack of bandgap.

Once the growth and fabrication technology of these new devices matures, their integration with conventional Si electronics, and/or flexible and transparent substrates has the potential to transform communications. Advanced graphene devices could enable the introduction of advanced RF communication systems in a broad array of new applications. Graphene, the ultimate nano-material, is therefore in an excellent position to help RF communication systems become even more ubiquitous and versatile than they are today.

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BIOGRAPHIES

TOMAS PALACIOS (tpalacios@mit.edu) is an associate professor in the Department of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology, where he leads the Advanced Semiconductor Materials and Devices Group. He received his Ph.D. in electrical engineering from the University of California — Santa Barbara, and a B.Sc. degree from the Polytechnical University of Madrid, Spain. His research focuses on the development of new electronic devices to advance the fields of information technology, biosensors, and energy conversion. He is especially interested in expanding the frequency performance of GaN transistors, and developing new devices and circuits with graphene. His work has been recognized with multiple awards including the 2009 NSF CAREER Award, the 2009 ONR Young Investigator Award, the 2008 DARPA Young Faculty Award, the 2006 UCSB Lancaster Award, the Young Researcher Award at the 6th International Conference on Nitride Semiconductors, the Best Student Paper Award at the 63rd IEEE Device Research Conference, and the European Prize Salva i Campillo. He has authored more than 100 contributions on advanced semiconductor devices in international journals and conferences (35 of them invited), three book chapters, and eight patents.

ALLEN HSU holds a Master's degree in electrical engineering from Massachusetts Institute of Technology in 2008, and a Bachelor's degree in electrical engineering from Princeton University in 2006. He is currently pursuing a Ph.D. in graphene electronics and optoelectronics at MIT.

HAN WANG received his B.A. and M.Eng. degrees in electrical and information science, both with highest honors, from Cambridge University, England, in 2006 and 2007. He is currently pursuing his Ph.D. degree in electrical engineering and computer science at MIT. He worked on modeling and simulation of power electronic devices from 2006 to 2007 in Cambridge University. At MIT since 2008, he has been working on graphene-based electronics and GaNbased devices. His current research interest focuses on the development of graphene-based transistors for millimeterwave applications and the search for novel graphene-based ambipolar devices for applications in nonlinear electronics. His work at MIT also includes GaN-based transistors for high frequency and high power applications.