Architectural Selection of A/D Converters

Martin Vogels
Katholieke Universiteit Leuven
ESAT-MICAS
Leuven, Belgium
mvogels@ieee.org

Georges Gielen
Katholieke Universiteit Leuven
ESAT-MICAS
Leuven, Belgium
georges.gielen@esat.kuleuven.ac.be

ABSTRACT

A method for the architectural selection of analog to digital (A/D) converters based on a generic figure of merit is described. First a figure of merit for the power consumption is introduced. This figure of merit includes both target specifications and technology data and has five generic parameters. The values of these generic parameters can be estimated by analyzing the different converter structures or by means of a fitting procedure using data from published designs. It is shown that the generic parameters have different values for different types of converters. Therefore the trade-off between speed, resolution, power dissipation and technology parameters depends on the type of converter. It is shown that the calculated figures of merit of the published designs, together with the calculated global trade-off comprise a surface in the (5 dimensional) design space. This surface makes it possible to accurately predict the power consumption and select the best converter solution for a certain target application. This can then serve as a first step in data converter synthesis or as a power estimator during high-level system design exploration.

Categories and Subject Descriptors

J.6 [**Computer-aided engineering**]: Computer-aided design (CAD)

General Terms

Theory

Keywords

A/D conversion, power estimation

1. INTRODUCTION

As a result of the trend of integrating more and more digital functionality on a single chip, VLSI technology has continued scaling in both feature size and power supply. As a result of this, analog and mixed-signal designers have to work in an ever increasingly challenging technological environment. On the other hand, designers of the crucial analog to digital converter in mixed signal design meet more and more stringent specifications on accuracy, bandwidth and power consumption. To overcome some of these difficulties several solutions for topological choices of converters have been proposed, based on simulation [3] or estimation from a model [5].

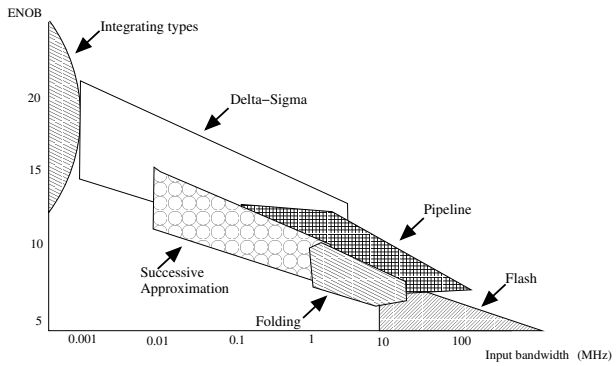

Figure 1: Areas of application for different converter types.

However, all these solutions deal with one type of converter, assuming that the choice for this type of converter has already been made. Chosing a certain converter usually is based on rules of thumb. A visual representation of these rules of thumb is shown in Fig. 1. A problem with this method is that it tends to be too conservative, as it does not take into account possible changes in this picture because of e.g. technology changes or new design ideas. A good example of this is the Delta-Sigma modulator, that was originally thought of to be limited to low frequencies, but that has recently been used even in the megaHertz domain [4].

This paper proposes a more quantitative method to the selection of A/D converter types, based on a figure of merit that has five generic parameters. This figure of merit is introduced in the next section.

2. THE FIGURE OF MERIT

To compare different architectural solutions for analog to digital conversion, first a figure of merit (*FOM*) must be agreed upon. One of the key insights here is that every design is the product of both designer knowledge and technological 'benefits'. This means that any figure of merit that is proposed should be normalized with respect to technological values such as supply voltage and minimal feature size. What remains is a figure of merit that quantifies how suitable the architectural choices of a designer for a certain application area are. This *FOM* is a power *FOM* (as opposed to for instance an *FOM* for the area). Here, the proposed *FOM* is:

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$$FOM = \frac{a_1^{ENOB} F_b^{a_2} V_{dd}^{a_3} L^{a_4}}{P} a_5 \quad (1)$$

Where F_b is the input signal bandwidth, V_{dd} is the supply voltage, L is the minimum feature size of the technology and P is the power consumption. The *ENOB* is the number of effective bits at F_b (i.e. $F_s/2$ for non-oversampling converters). a_1, a_2, a_3 and a_4 have to be extracted from design data. The factor a_5 is a scaling factor making the figure of merit 1 for the average[1], while the unit of a_5 will be chosen such that the total expression is dimensionless. Using this *FOM* a design can be said to be suited for a certain application area if its *FOM* is 1 or higher (and not suited if it is lower).

3. ESTIMATION OF PARAMETERS FOR DIFFERENT ARCHITECTURES

Numerous architectural solutions exist to perform analog to digital conversion. Three of the most used in todays designs are the flash ADC, the pipelined ADC and the Delta-Sigma modulator. For each of these ADC's now an estimation for the generic parameters a_1 to a_4 is derived. The technical analysis not only is useful to be able to estimate these parameters (and the trade-off between them) before fitting, it also helps to explain the results after the fitting procedure.

3.1 Flash converters

A popular architecture for high-speed, low-resolution A/D conversion is the flash structure. It consists of $2^N - 1$ comparators, that in most cases are preceded by a preamplifier. The power estimation formula for this structure can be found by realizing that the power of a single digital gate equals:

$$P_{dig} = V_{dd} I = V_{dd} F_s C_{gs} V_{sw} \propto V_{dd} V_{sw} F_s C_{ox} W L \propto V_{dd}^2 F_b L \quad (2)$$

where it is assumed that the W scales proportional to L (since it is a digital circuit) and C_{ox} scales inversily proportional to L (because of necessary scaling of t_{ox}). The power consumption of an analog preamplifier can be found by realizing that the gain-bandwidth product of this amplifier is proportional to the sampling frequency F_s [10]

$$F_s \sim \frac{g_m}{2\pi C_{gs}} \sim \frac{2I}{2\pi W L (2/3) C_{ox} (V_{gst})} \quad (3)$$

where it assumed that C_{gs} (the gate-source capacitance) of the input stage is the dominant capacitor. V_{gst} denotes the transistor overdrive voltage $V_{gs} - V_T$. For the power of the preamplifier this means:

$$P_{pamp} = V_{dd} I \propto V_{dd} F_b W L C_{ox} V_{gst} \quad (4)$$

Since V_{gst} (normally) does not scale with V_{dd} here the exponent of the voltage is 1 instead of two. However, the consumed power is dependent on the size of C_{gs}. From [10] it becomes clear that the size of the capacitor is mainly determined by matching considerations. Since V_t mismatch scales roughly with minimum feature size, the required capacitor size is also roughly proportional to the minimum feature size.

With this information the fitting parameters of the proposed figure of merit can be estimated. For the dependence on the supply voltage a_3, a figure between 1 and 2 is expected, the dependence on the minimum feature size a_4 will be close to one. The dependence of the digital power on the effective number of bits a_1 should be two since an extra bit means roughly two times more comparators and digital logic. For the analog circuitry, an extra bit means a factor four increase in power, again because of matching considerations (this is the speed-accuracy power trade-off [6]). The other dependencies are listed in table 1.

[1]Since the generic parameters will be fitted using data from the highest ranked design conference and journal, average means that it is can compete with the best designs.

3.2 Delta Sigma modulators

Another popular ADC architecture is the Delta-Sigma modulator, that consists of a loop filter and a low resolution quantizer that is oversampled ($F_s >> 2F_b$). Since the quantizer output is fedback to the loopfilter, the quantization noise is shaped such that the noise in the band of interest is attenuated. For oversampling ratios larger than two, the dynamic range of a Delta-Sigma modulator can be approximated by [1]:

$$DR = 12 \frac{(2O_l + 1) OSR^{2O_l+1}}{\pi^{2O_l}} \quad (5)$$

where OSR is the oversampling ratio defined by $\frac{F_s}{2F_b}$ and F_b is the input bandwidth, O_l is the order of the loopfilter. To estimate the different parameters, the gain-bandwidth product of the opamps is assumed to be proportional to the speed:

$$F_s \sim \frac{g_m}{2\pi C_{tot}} = \frac{2I}{2\pi V_{gst} C_{tot}} \quad (6)$$

where C_{tot} is the total integration capacitance. If it is assumed that the modulators performance is limited by thermal ($\frac{kT}{C}$) noise, it follows that the sampling capacitance of the first integrator should be [9]:

$$C_s = \frac{4kT(DR)}{OSR V_{sw}^2} \quad (7)$$

The power can then be expressed as:

$$P = V_{dd} I \propto \frac{V_{dd} F_s V_{gst} C_{tot} 4kT DR}{C_s OSR V_{sw}^2} \quad (8)$$

Note that (8) predicts that every extra bit of accuracy, takes about a factor 4 in power consumption if the same *FOM* is to be achieved (this is again the speed-accuracy-power tradeoff). Although this is true if the design is compared to some reference design that has a perfect scaled C_s, this seems never to be the case since designs that are compared with this figure of merit do not nearly reach the ideal [4]. However, when thermal noise is not the limiting factor in a design, one can state that when the same design is considered for two different values of the OSR, but for the same F_s, the power consumption will not change. Since *FOM* is supposed to be related to the design, it will not change either. This means that if all capacitances and voltages stay the same the following holds:

$$1 = \frac{FOM_2}{FOM_1} = \frac{f(DR_2) F_{b_2}}{f(DR_1) F_{b_1}} = \frac{\gamma_1^{\log_{10}(DR_2)} F_{b_2}}{\gamma_1^{\log_{10}(DR_1)} F_{b_1}} \quad (9)$$

Using (5) it becomes clear that even for a O_l of two γ_1 has a value of 1.59 which is much smaller than the factor 10 that is predicted by (8). This means that a_1 ranges from 1.3 to 4, depending of what noise source is dominant. For a good design it will be close to 2. For the dependence on V_{dd} a_3a factor of at least 1 is expected, while there will be very little influence of the scaling of L a_4.

3.3 Pipelined converters

Another very popular structure is the so called pipelined converter. This structure consists of a chain of flash converters and multibit digital to analog converters (MDACS), preceded by a sample and hold (S/H).

Although more detailed (bottom-up) analyses are available such as in [5], here it will be assumed that the main noise contribution of this type of converter is the first stage and the sample and hold circuit. The resulting size of the sample and hold capacitance is the same as stated in (7), leading to an expression similar to (8). However, as with the Delta-Sigma case, thermal noise is not the only parameter of consideration. Another important specification in pipelined converters is the matching between the capacitors used in the MDACS. If this is the limiting factor, increasing the resolution with one bit will in general cost less than a factor four since digital calibration techniques can be used, which can be very power efficient. However, thermal noise will be a problem for very high resolution (>14 bits) converters. As for the Delta-Sigma modulator the value of a_1 will probably be around 2. The value of a_3 will be in between 1 and 2. The digital part and flash converters will scale with a factor 2, while the analog opamps scale with 1. The other estimates can be found it table 1.

4. FITTING OF THE PARAMETERS

In the previous section it has been shown that different converters result in different estimates for the generic parameters. To be able to finetune the expression for the *FOM*, a fitting procedure will be used [7]. The parameters will be fitted using data from actual implementations of the three types of converters, published in recent years in both the IEEE Journal of Solid State Circuits and the proceedings of the ISSCC. For the Delta-Sigma modulator only the low-pass kind is considered. The fitting process is performed using a least mean squares error (LMS) criterion. One should be careful using this criterion, since the use of it assumes implicitly that the model is correct and that the underlying process has a random Gaussian distribution [8], both of which we cannot be certain in this case. Therefore it is first tested if the resulting error distribution after fitting is Gaussian using the chi-square test. If the test shows high probability that the resulting error is indeed Gaussian, this means that the probability that the model is correct is also high (if not it indicates that the model should be changed or another criterion should be used). Note that this does not mean that the standard deviation on the *FOM* is low since this depends on the actual designs. This can be resolved by using a two-step procedure. First of all a normal fit is done on all designs. Then, those design making up the bottom 25% of the *FOM*'s for a particular architecture are discarded. The remaining designs are then selected and a second fit is made. This procedure makes it possible to automatically filter out those designs where power was (apparently) not the primary goal and concentrate on the designs where it was.

The final results of this two-step fitting procedure for the different converter types are listed in table 1 and will now be discussed. The results of the fitted estimated power and the actual power for the three structures are depicted in Fig. 2. The straigth line indicates where the *FOM* equals 1.

4.1 Pipelined converters

Since the resulting error distribution when applying these fitted results is Gaussian with only 50% certainty, the minimax rather than the least mean squares criterion is used for the final fit. Using this criterion the resulting standard deviation is 1.72 From table 1 it is clear that the power scales with a factor that is much lower than two for an extra bit. This means thermal noise is not (yet) the limiting factor and that resolution is primarily dominated by mismatch, which can be efficiently diminished using digital calibration techniques. Power scales with the square of the supply voltage indicating that digital circuitry does consume a large portion of the power.

Table 1: Estimated and fitted values for the parameters a_1 to a_4, σ expresses the standard deviation on the power estimate

type	a_1	a_2	a_3	a_4	a_5	σ
flash estim.	2	1	1-2	1	-	-
flash fitted	1.6	1.045	1.3	1.1	0.0466	1.42
pipel. estim.	1-2	1	1-2	0	-	-
pipel. estim.	1.24	0.79	2	0.04	0.241	1.72
ΔΣ estim.	2	1	1	0	-	-
ΔΣ fitted	1.73	0.74	1.6	0.18	0.0048	1.78

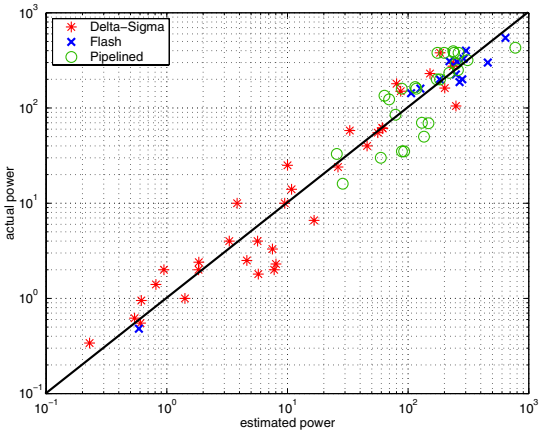

Figure 2: Results of power estimation after fitting for the different converters

4.2 Flash converters

The standard deviation for the flash converters is 1.42. The resulting error distribution was Gaussian with nearly 80% certainty, showing that the constraints for the LMS mentioned above were met. The fitted value of a_3 shows that the power consumed in the preamplifiers (4) has consideable impact on the total power. The fact that a_1 is smaller than the expected value of two can be explained by the fact that for a higher resolution converter a designer will try extra hard to minimize power consumption.

4.3 Delta-Sigma modulators

Although the data is more spread than for the other structures, the resulting error distribution is Gaussian with 78% certainty, showing that again the constraints for the LMS were met. This implies that the proposed model is suited to describe this particular problem. The standard deviation of the *FOM* is 1.78. The value of a_1 is close to the predicted value of 2, showing that the power consumption is indeed not limited by thermal noise (only).

5. USING THE FOM FOR A/D CONVERTER ARCHITECTURAL SELECTION.

It is clear that the found coefficients of the *FOM* provide a means to do an estimation of the power consumption for the different converters in a certain application area. The simplest way to accomplish this is to assume that the converter will have a *FOM* that equals one and use (1) to calculate the power. A problem with this method is that it does not take into account any local information i.e. if the target specifications are close to the specifications of a

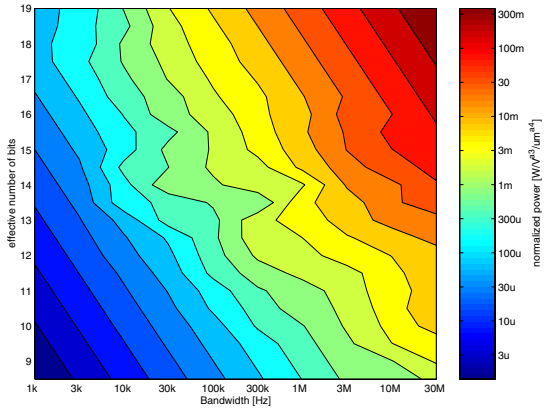

Figure 3: Contour plot for the power of ΔΣ converters.

realized design. A published design with a *FOM* greater than one provides actual proof that it is possible to realize the target specifications while consuming less power than predicted by (1). On the other hand, a design with a *FOM* lower than one provides evidence that the estimated power consumption may be too optimistic.

To include this local behavior, the following procedure is used. First note that the definition of (1) equalling 1 actually comprises a hyperplane in a 5 dimensional space. The actual *FOM's* of the realized designs are then spikes above and below this hyperplane. If now this surface is passed trough a low-pass filter, the spikes will be smeared out over the surface. This means that in the local (5-dimensional) area around a published design a value in between the actual *FOM* and a *FOM* will be the result. The definition of local is of course somewhat arbitrary, here it is defined as a maximum change in resolution of one bit and a maximum change in bandwidth of a factor two. The supply voltage and minimum feature size scale by less than an order of magnitude over the entire data set, so for these two parameters there is no difference between local and global behavior. This means that the actual filter only needs to be two-dimensional and the resulting *FOM* surface can be calculated using standard 2-dimensional convolution. Using the *FOM* surface the estimated power for different target specifications can be calculated. Figure 3 shows a contour plot of the power consumption (normalized with respect to minimum feature size and power supply) versus number of effective bits and bandwidth for the Delta-Sigma modulators (using the fitted values from table 1) The influence of the local variations in *FOM* can be clearly seen, since a global *FOM* of 1 would result in the contour lines being parallel straight lines. For the other converter types discussed in this paper a similar contour plot can be made. An additional benefit of using this local information is that a *FOM* differing from 1 indicates that there was already a design published in this application area, which can give valuable insight in topological choices. .

5.1 Architectural selection of an A/D converter for VDSL applications

Using the described procedure, selection of data converter architectures during design or synthesis can be performed. An interesting problem is the selection of an A/D converter for VDSL specifications. The required resolution for this A/D converter is 13 bits, while an input bandwidth of 8 MHz needs to be realized, the technology is 0.25um CMOS with a 2.5 Volt supply voltage. In this case only two of the three A/D converters architectures are considered, pipelined converters and Delta-Sigma modulators. Given the fitted values of table 1 for pipelined converters and Delta-Sigma modulators and an estimated *FOM* of 1, the estimated power consumption for a pipelined converter is 121mW while for the Delta-Sigma modulator this is 94mW. Using local information, the power consumption for Delta-Sigma remains unchanged (there are no already published local designs). For the pipelined converter, the local *FOM* equals 0.9 because of a design [2] close to it with a *FOM* of 0.69. This brings the estimate on 134mW. The conclusion is here that the best power choice for VDSL applicationsis a Delta-Sigma modulator under the condition that the digital decimation filter consumes less than 40 mW, otherwise a pipeline design would be better.

6. CONCLUSIONS

A selection strategy for analog to digital converter architectures based on a generic figure of merit was presented. The generic parameters where derived from theory and fine-tuned using a fitting procedure on published designs. The actual method is based on power estimation using both the global trade-off and the local variations. The suitability of this method was demonstrated with some examples. An additional advantage of this strategy is that not only the converter architecture is selected, but it is also detected whether there are already designs for this application area in the database.

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