Architecture and IC Implementation of a Digital VRM Controller

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***Abstract*—This paper develops the architecture of a digital PWM controller for application in multiphase voltage regulation modules (VRMs). In this context, passive current sharing and VRM transient response with nonzero controller delay are analyzed. A scheme for sensing a combination of the VRM output voltage and output current with a single low-resolution window analog-to-digital converter (ADC) is proposed. The architecture and IC implementation of a digital PWM (DPWM) generation module, using a ring-oscillator-multiplexer scheme, is discussed. Experimental results from a prototype VRM and a partial controller IC implementation are presented.**

***Index Terms*—Analog-digital conversion, current sharing, digital control, digital modulation, inductance, integrated circuits, power conversion, pulse-width modulation, ring oscillators, transient analysis, voltage control.**

I. Introduction

DIGITAL controllers are a strong candidate for use in voltage regulation modules (VRMs) due to their low quiescent power, immunity to analog component variations, ease of integration with other digital systems, ability to implement sophisticated control schemes, and potentially faster design process [1]–[12]. In particular, the ability of digital controllers to accurately match multiple pulse-width modulation (PWM) signals, may allow for the use of passive current sharing schemes in multiphase VRMs, thus reducing the units' cost and complexity. Further, the ease of interface between a digital controller and other digital hardware can be advantageous in microprocessor and communication systems. In addition, the low power dissipation of digital controllers makes them an attractive choice for portable applications.

In this paper we develop an architecture for a digital VRM controller and discuss aspects of its integrated circuit (IC) implementation. In Section II we start with a brief overview of the structure of a digitally controlled multiphase VRM. In Section III we analyze passive current sharing, and derive estimates for the possible phase current mismatch due to power train parameter variations. In Section IV we discuss the VRM transient response with nonzero controller delay, and introduce an implementation of optimal voltage positioning with a digital controller. We then propose a low resolution analog-to-digital converter (ADC) topology that can be used in the VRM. Results from a prototype VRM are presented. Section V addresses the architecture of digital PWM (DPWM) generation modules. We discuss the IC implementation of a ring-oscillator-MUX DPWM scheme, and present test chip data. Finally, in Section VI we overview the architecture of a complete IC implementation of a digital VRM controller.

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II. Overview of a Digitally Controlled Multiphase VRM

A block diagram of a digitally controlled 4-phase buck VRM is shown in Fig. 1. A controller with similar structure has been discussed in [2]. The controller consists of an ADC which converts the regulated quantity (typically a combination of the output voltage V_o and the output current I_o), a discrete-time control law which calculates the duty cycle command from the output of the ADC and a digital reference word [typically a voltage identification code (VID) supplied by a microprocessor], and a DPWM module which generates the gating signals for the power train switches. The four phases are switched $360°/4 = 90°$ out of phase which reduces the output voltage ripple and the input current ripple, and can improve the transient response of the converter.

III. Passive Current Sharing in a Digitally Controlled Multiphase VRM

In general, like analog controllers, digital controllers for multiphase VRMs can be used successfully with active current sharing schemes, typically involving individual current sensing of each phase. However, unlike their analog counterparts, digital controllers have the advantage of almost perfect matching of the duty cycles of the PWM signals among the different phases, potentially allowing for the use of *passive current sharing* schemes, which eliminates the need for individual sensing and control of the phase currents. The use of passive current sharing may reduce the cost of the VRM, as a result of the smaller number of current sensors needed, as well as the reduced pin count of the controller IC.

To study the dc current sharing among the different phases in a k-phase converter we model the latter with the circuit shown in Fig. 2. Resistors R_1, R_2, …, R_k model the dc resistance of each phase of the power train, and V_1, V_2, …, V_k model the average open-circuit voltage for each phase

$$V_i = V_{in} D(i), \qquad i = 1, 2, \ldots, k \tag{1}$$

where $D(i)$ is the duty cycle command for phase i, and V_{in} is the input voltage.

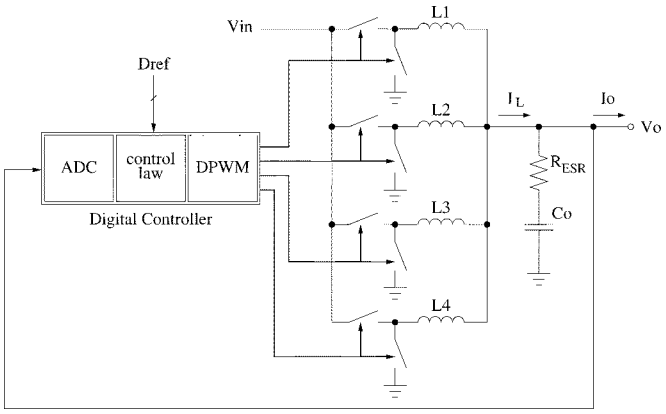

Fig. 1. Block diagram of a digitally controlled multiphase VRM.

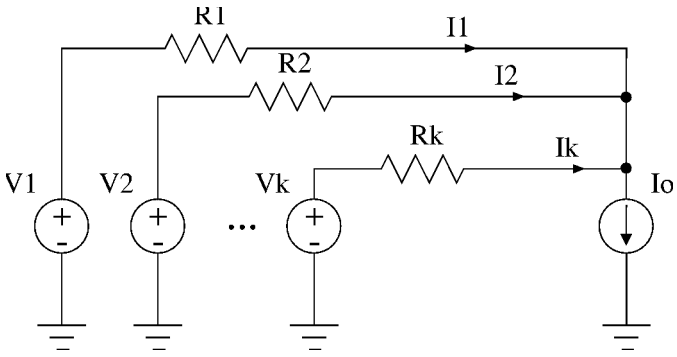

Fig. 2. DC current sharing model of a k-phase converter.

With $R_1, R_2, \ldots, R_k$ having arbitrary and possibly mismatched values, as a result of power train mismatches among the phases, total power dissipation of the system is minimized when $V_1 = V_2 = \cdots = V_k$. To see this, consider

$$\hat{P} = \sum_{i=1}^{k} R_i I_i^2 + \lambda \left(I_o - \sum_{i=1}^{k} I_i \right) \tag{2}$$

which is the total dc power loss in the power train with the constraint that, the sum of the individual phase currents must equal the total load current, appended with Lagrange multiplier λ. A necessary condition for a minimum of the total power loss subject to the constraint is that all first order partial derivatives of $\hat{P}$ in (2) are zero. This yields

$$2R_i I_i - \lambda = 0 \tag{3}$$

for each index i corresponding to each phase of the converter. The constraint (3) implies that the dc voltage drops $R_i I_i$ for all phases are equal, which is equivalent to the power optimality condition $V_1 = V_2 = \cdots = V_k$ stated above.

The above result implies that when the duty cycles applied to different phases are identical, the power loss is minimized regardless of the possible resistive mismatch among the phases. A digital controller can produce accurately matched PWM waveforms for the different phases, with possible timing mismatch resulting only from parameter variations of the power FETs and gate drives, which is discussed in Section III-B.

A. Phase Current Mismatch Due to Power Train Resistance Mismatch

As it was argued above, if the multiphase converter has matched duty cycles but mismatched power train resistances among the phases, the output current distributes itself among the phases so as to minimize the power dissipation in the power train. However, the actual current mismatch is still of interest since it may have undesirable consequences such as possible saturation of the inductors.

Assume matched duty cycles among the phases, $V_1 = V_2 = \cdots = V_k = V_{in}D$. Then, a power train resistance mismatch ΔR results in worst case current mismatch through a particular phase (let this be phase i) when all other phases have the same power train resistance equal to R, while that phase has mismatched resistance $R_i = R + \Delta R$. Since the power train resistances of the different phases form a current divider for the output current I_o, the current through phase i is

$$I_i = I_o \frac{R/(k-1)}{R_i + R/(k-1)}. \tag{4}$$

Then, the mismatch current flowing in phase i is the difference between current I_i and the nominal phase current I_o/k,

$$\Delta I_i = I_i - \frac{I_o}{k} = -I_i \frac{k-1}{k} \frac{\Delta R}{R}. \tag{5}$$

Hence, the worst case phase current variation due to a power train resistance mismatch ΔR, is

$$\left(\frac{\Delta I_i}{I_i} \right)_R = -\frac{k-1}{k} \frac{\Delta R}{R}. \tag{6}$$

Finally, the value of the effective power train resistance for each phase can be estimated from

$$R = DR_{DS(on),h} + (1-D)R_{DS(on),l} + R_L + R_{trace} \tag{7}$$

where D is the duty cycle; $R_{DS(on),h}$ and $R_{DS(on),l}$ are the on-resistances of the high- and low-side MOSFET switches, respectively; R_L is the inductor dc resistance; and R_{trace} is the resistance of the printed circuit board traces in the power train for each phase. The relative variations of these parameters can be obtained from the data sheet for a particular process, and (7) can be used in conjunction with (6) to estimate the total current mismatch due to power train resistance mismatch.

B. Phase Current Mismatch Due to Duty Cycle Mismatch

Consider again Fig. 2 and let $R_1 = R_2 = \cdots = R_k = R$. However, assume that $V_1, V_2, \ldots, V_k$ are not equal as a result of duty cycle mismatch among the phases. A duty cycle mismatch ΔD results in worst case current mismatch through a particular phase (let this be phase i) when all other phases are switched with the same duty cycle D, while that phase is switched with a mismatched duty cycle $D + \Delta D$, i.e., $V_i = V_{in}(D + \Delta D)$. The mismatch current through phase i, $\Delta I_i = I_i - I_o/k$, is then

$$\Delta I_i = \frac{V_i - V_{in}D}{R + R/(k-1)} = \frac{k-1}{k} \frac{V_{in}}{R} \Delta D. \tag{8}$$

The dc conduction power loss in the multiphase part of the power train is $P_{loss,\,mp} = I_o^2 R/k$, and the converter input power is $P_{in} \approx DV_{in}I_o$. Then the dc conduction efficiency of the multiphase part of the converter power train is

$$\eta_{mp} = 1 - \frac{P_{loss,\,mp}}{P_{in}} \approx 1 - \frac{I_o^2 R/k}{DV_{in}I_o}. \tag{9}$$

Solving (9) for R and substituting in (8), we obtain an expression for the worst case phase current variation, $\Delta I_i/I_i$ due to a duty cycle mismatch ΔD

$$\left(\frac{\Delta I_i}{I_i}\right)_D \approx \frac{k-1}{k}\,\frac{1}{1-\eta_{mp}}\,\frac{\Delta D}{D}. \tag{10}$$

One immediate observation from (10) is that the current mismatch sensitivity becomes worse if the efficiency of the converter improves, or if the duty cycle decreases.

C. Duty Cycle Mismatch due to MOSFET Switching Parameter Variations

A digital PWM controller can provide very accurate matching among the duty cycles for the different phases, thus the main source of duty cycle mismatch are the analog gate drives and power switches. Fig. 3 shows a simplified model of the switching characteristic of a MOSFET which determines the relation between the duty cycle output by the controller (D) and the effective duty cycle seen at the switching node of the power train (D_{eff}). The gate drive of the MOSFET is modeled as a current source with output current $\pm I_G$ and maximum output voltage V_{GG}. Let C_{gs} and C_{gd} denote respectively the transistor gate–source and gate–drain capacitances, and let subscripts sat and lin refer respectively to the saturation and linear regions of operation of the MOSFET.

In the beginning of the switching period ($T = 1/f_{sw}$) the gate drive sources current I_G into the high-side MOSFET gate, making its gate-source voltage V_{gs} ramp up at a rate of approximately $s_{g1} = I_G/(C_{gs} + C_{gd})_{sat}$. Drain-source voltage V_{ds} remains at the supply voltage V_{DD} until the drain current I_d reaches the value of the output current I_o. Then V_{gs} plateaus at

$$V_{pl} \approx V_{TH} + \sqrt{2I_o/k_m} \tag{11}$$

where k_m is the device gain factor and we assume that $I_o \gg I_G$. While $V_{gs} = V_{pl}$, V_{ds} moves down at a rate of $s_{d1} = -I_G/C_{gd(sat)}$ until the transistor goes into the linear region. Then V_{gs} continues to increase at a rate $s_{g2} = I_G/(C_{gs} + C_{gd})_{lin}$ until it reaches V_{GG}. In the linear region V_{ds} is about $I_o R_{DS(on)}$. The MOSFET turn-off is analogous.

From Fig. 3 it can be seen that the effective duty cycle, measured between the midpoints in the swing of V_{ds}, is

$$D_{eff} \approx D + (V_{GG} - 2V_{pl}) f_{sw}/s_g \tag{12}$$

where, for simplicity, we have set $s_g = s_{g1} = s_{g2}$. Then the variation of D_{eff} due to perturbations of V_{TH} and s_g is

$$(\Delta D_{eff})_{V_{TH}} \approx -2 f_{sw}/s_g \cdot \Delta V_{TH} \tag{13}$$

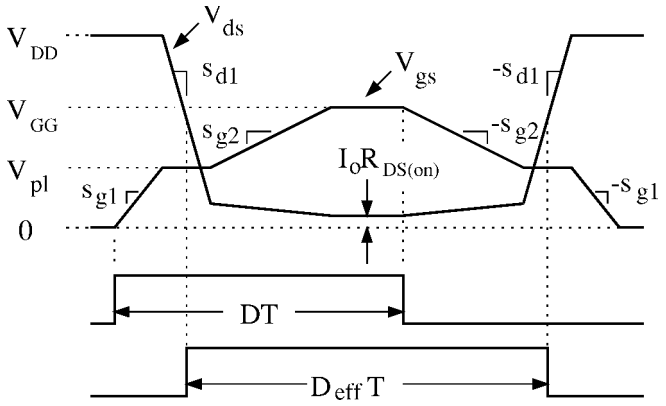

Fig. 3. Duty cycle variation due to the MOSFET switching characteristic in continuous conduction mode.

and

$$(\Delta D_{eff})_{s_g} \approx -(V_{GG} - 2V_{pl}) f_{sw}/s_g^2 \cdot \Delta s_g. \tag{14}$$

Since typically $2V_{pl}$ is close to V_{GG}, (14) has small contribution to the overall D_{eff} variation relative to (13), and its effect may be neglected. Then, (13) can be used in conjunction with (10) to estimate current variation among phases due to duty cycle mismatch.

D. A Passive Current Sharing Calculation Example

Given a certain specification on the maximum tolerable current mismatch among the phases of a multiphase converter ($\Delta I_i/I_i$), the equations developed above can be used to estimate converter parameters such as the maximum allowable power MOSFET gate rise/fall time ($t_g = V_{GG}/s_g$), and total power train resistive mismatch among the phases ($\Delta R/R$). Equations (6), (10), and (13) were used to derive the constraints in Table I based on a sample converter design. Finally, it should be noted again that, while the possible 20% phase current mismatch due to duty cycle mismatch may result in nonoptimal power dissipation, the 20% current mismatch due to resistive mismatch will not degrade the converter efficiency. In this example, it is seen that a modest gate drive rise/fall time of $<$13 ns leads to quite acceptable current-sharing behavior. Experimental results supporting the feasibility of open-loop current sharing are presented in Section IV-C, as well as in [13].

IV. Output Sensing and Analog-to-Digital Conversion

The precision with which a digital controller positions the output voltage V_o is determined by the resolution of the ADC. In particular, V_o can be regulated with a precision of one LSB of the ADC. Applications such as modern microprocessor VRMs require regulation precision of about 10 mV [14], demanding ADC modules with very high resolution. For example, regulation resolution of 10 mV at $V_{in} = 12$ V corresponds to ADC resolution of $N_{ADC} = \log_2(12\ \text{V}/10\ \text{mV}) \approx 10$ b. Further, microprocessor VRM designs target switching frequencies in the megahertz range, implying ADC conversion times of less than a microsecond. The need for high resolution and fast conversion time may result in expensive and high-power ADC de-

TABLE I
A PASSIVE CURRENT SHARING EXAMPLE

	Specifications	
$\Delta I_i/I_i$	phase current mismatch	40%
$(\Delta I_i/I_i)_R$	– due to resistive mismatch	20%
$(\Delta I_i/I_i)_D$	– due to duty cycle mismatch	20%
	Some Converter Parameters	
k	number of phases	4
f_{sw}	switching frequency	1 MHz
D	duty cycle	1/5
η_{mp}	multi-phase power train efficiency	90%
V_{GG}	gate drive voltage	5 V
ΔV_{TH}	threshold voltage variation	1 V
	Resulting Constraints	
s_g	power MOSFET gate rate	$>$ 0.38 V/ns
t_g	power MOSFET gate rise/fall time	$<$ 13 ns
$\Delta R/R$	power train resistive mismatch	$<$ 26%

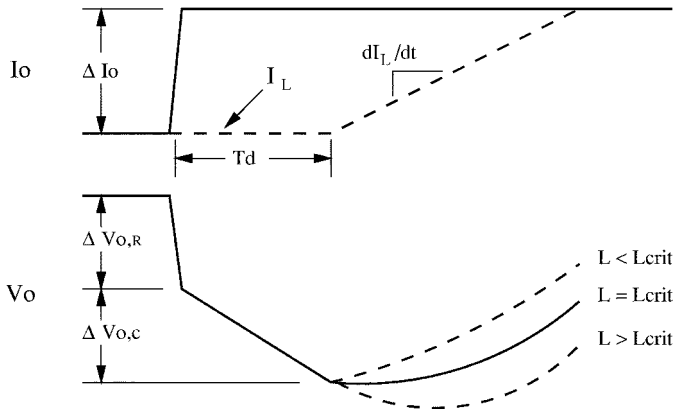

Fig. 4. Transient response of a buck VRM due to load current step.

signs. Therefore, it is advantageous to look for low-resolution ADC topologies that meet the tight regulation specification.

A. VRM Transient Response

An output voltage transient of a buck VRM due to an increase in the load current I_o by ΔI_o is illustrated in Fig. 4. The load current step will first cause output voltage drop of magnitude $\Delta V_{o,R} = \Delta I_o R_{ESR}$ due to the effective series resistance (R_{ESR}) of the output capacitor.[1] Since the controller has nonzero response delay, V_o will continue to drop due to discharge of the output capacitor C_o. Let T_d be the delay of the controller response, i.e., the time between the instant a load current step has occurred and the resulting update of the duty cycle. Then the V_o drop due to the capacitive discharge will be $\Delta V_{o,C} = \Delta I_o T_d / C_o$. After time T_d, the controller responds to load step by increasing the duty cycle, resulting in total inductor

[1]Here, for clarity, we are omitting the initial V_o drop due to the series inductance of the output capacitor. See [15] for capacitor inductance modeling.

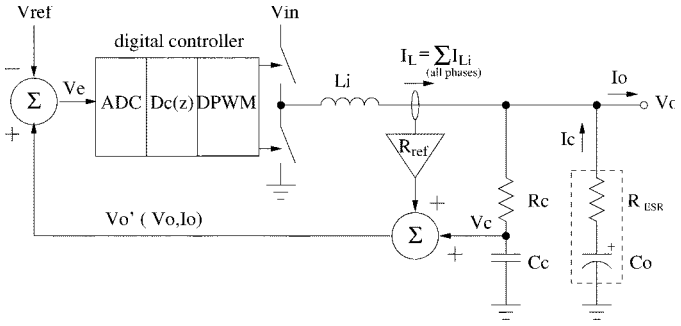

Fig. 5. Implementation of optimal voltage positioning with a digital controller.

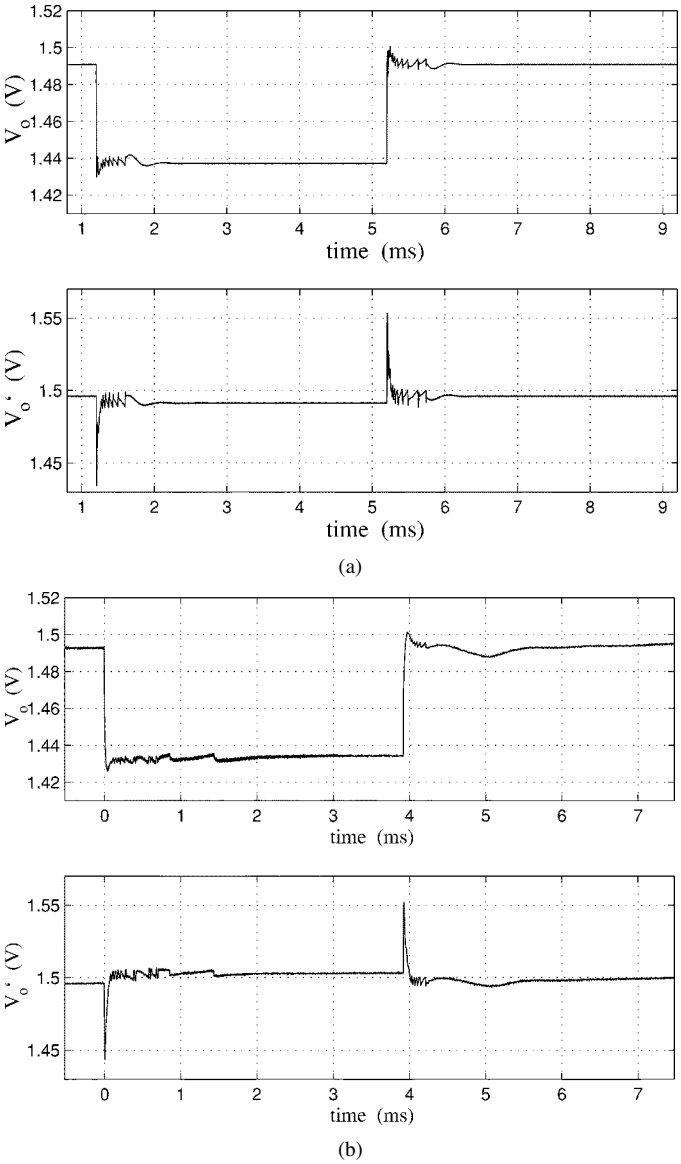

Fig. 6. Transient response of a prototype digitally controlled multiphase buck converter with parameters from Table II, resulting from a 10 A load current step: (a) simulation and (b) experimental results. V_o is the output voltage, and V_o' is the quantity compared to V_{ref} to form the error signal.

current (I_L) increase at a rate of $dI_L/dt = V_L/L$, where L is the combined inductance of all phase inductors in parallel, and, assuming saturated controller response, $V_L = V_{in} - V_o$. Consequently, V_o exhibits second-order behavior which depends on the value of L, and eventually starts to increase. If $L \leq L_{crit}$,

TABLE II
PROTOTYPE VRM PARAMETERS

V_{ref}	reference voltage	1.5 V
V_{in}	input voltage	5 V
k	number of phases	4
f_{sw}	switching frequency	250 kHz
L_i	phase inductors	4.4 μH
C_o	output capacitance	4 mF (tantalum)
R_{ESR}	output capacitor ESR	4 $m\Omega$
R_{ref}	closed-loop output impedance	$5m\Omega$
N_{adc}	effective ADC resolution	9 bit
N_{dpwm}	effective DPWM resolution	7 bit (hardware) + 3 bit (dither)
K_p	proportional gain	10
K_d	derivative gain	14
K_i	integral gain	0.25
τ_c	$R_c - C_c$ estimator time const.	10 ns
T_d	controller delay	5 μs

V_o starts to increase immediately after I_L begins to ramp up. The critical inductance value is (see the Appendix)

$$L_{crit} = \frac{\tau_o V_L}{\Delta I_o} \tag{15}$$

where the output capacitor time constant $\tau_o = R_{ESR}C_o$ is approximately constant for a particular capacitor technology. On the other hand, when $L > L_{crit}$, even if the controller saturates the duty cycle, V_o first starts to decrease reaching a minimum which is a nonlinear function of ΔI_o, and only then increases.

The unloading transient (a decrease of I_o by ΔI_o) is analogous with $V_L = -V_o$.

B. Implementation of Optimal Voltage Positioning

The concept of optimal voltage positioning has been widely used in recent voltage regulator designs. The idea is to always position V_o at $V_{ref} - R_{ESR}I_o$, where V_{ref} is the reference voltage, instead of driving it to V_{ref} [16]. In that case, the converter behaves as a voltage source with value V_{ref} and output impedance that is always real and equal to R_{ESR}. If optimal voltage positioning is used, ideally C_o can be made half the size required for a stiff voltage regulator design, which can save on cost and circuit area and volume.

The optimal voltage positioning technique can be extended to include nonzero controller delays. From Fig. 4 it can be seen that, assuming $L \leq L_{crit}$, the V_o excursion due to a load current step ΔI_o is

$$\begin{aligned}\Delta V_o &= \Delta V_{o,R} + \Delta V_{o,C} = \Delta I_o R_{ESR} + \Delta I_o T_d / C_o \\ &= \Delta I_o R_{ESR}(1 + T_d/\tau_o).\end{aligned} \tag{16}$$

Equation (16) shows that the output voltage step is directly proportional to the output current step, with proportionality constant which is a linear combination of the output capacitor ESR and the delay of the controller. Thus, using the reasoning behind the optimal voltage positioning technique, we can design the controller to always position V_o at

$$V_o \rightarrow V_{ref} - R_{ref}I_o \tag{17}$$

where

$$R_{ref} = R_{ESR}\left(1 + \frac{T_d}{\tau_o}\right). \tag{18}$$

This extension is particularly important for capacitor technologies with small τ_o, such as ceramic capacitors, where the term corresponding to controller delay may dominate.

If $L > L_{crit}$, ΔV_o becomes a nonlinear function of ΔI_o and the optimal voltage positioning technique is not applicable.

A scheme for implementing optimal voltage positioning with a digital controller is shown in Fig. 5. The idea is to reconstruct the output current I_o by sensing the total inductor current through all phases, $I_L = \sum_{i=1}^{4} I_{Li}$, and estimating the current flowing out of the output capacitor, I_C. If the time constant τ_c of the estimator $R_c - C_c$ is equal to τ_o, the output of the estimator is the voltage across C_o

$$V_c = V_o + R_{ESR}I_C. \tag{19}$$

By adding the output of the estimator to the inductor current I_L multiplied by a transresistance gain of R_{ref}, we obtain the quantity

$$\begin{aligned}V_o' &= V_o + R_{ESR}I_C + R_{ref}I_L \\ &\approx V_o + R_{ref}I_o, \qquad \text{if } R_{ref} \approx R_{ESR}.\end{aligned} \tag{20}$$

Subtracting V_{ref} from V_o' we form the error signal V_e. Thus, if the controller has high gain, and the system is stable, V_o will follow (17).

The controller implements a digital PID control law $D_c(z)$ which represented in the discrete-time domain has the form

$$\begin{aligned}D_c(n+1) = &-K_p D_e(n) - K_d[D_e(n) - D_e(n-1)] \\ &- K_i D_i(n) + D_{ref}(n)\end{aligned} \tag{21}$$

where $D_c(n)$ is the duty cycle command at discrete time n, $D_e(n)$ is the quantized error signal V_e, and $D_i(n)$ is the state of an integrator

$$D_i(n+1) = D_i(n) + D_e(n). \tag{22}$$

Further, K_p is the proportional gain, K_d is the derivative gain, and K_i is the integral gain. All variables are normalized to the input voltage, V_{in}. Variable $D_{ref}(n)$ is the digital representation of V_{ref}, and is used as a feedforward term in (21). Design of digital PID control law is discussed in [17]–[19].

Finally, observe that the sensing approach introduced above uses only one ADC to obtain information about both V_o and I_o, and that all current sensing is done before the output capacitor to ensure low output impedance.

C. Experimental Results

A prototype digitally controlled VRM using a four-phase buck topology with passive current sharing was simulated and built with the parameters shown in Table II. The simulation was done in MATLAB, while the actual controller was implemented

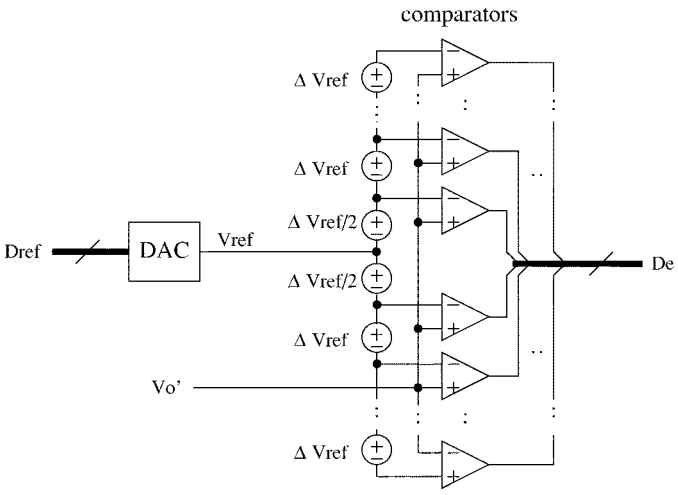

Fig. 7. Block diagram of a window ADC. It implements both an ADC and an error amplifier.

using a DSP board connected to a PC, and an FPGA to produce the overall timing and the multiphase DPWM signals. The controller has 9 b of effective ADC resolution, and effective 10 b of DPWM resolution (7 b of hardware resolution plus 3 b of digital dither [5]). Optimal voltage positioning was implemented using the scheme discussed in Section IV-B. The estimator time constant was adjusted so that $\tau_c \ll \tau_o$ to achieve good performance with moderate controller gain. Fig. 6(a)[2] and (b) show, respectively, the simulated and experimental response of the converter to a load current change from 1 A to 11 A and back to 1 A ($\Delta I_o = 10$ A). Finally, current matching among the four phases was observed to be very good ($|\Delta I_i/I_i| < 10\%$).

D. ADC Topology

Modern microprocessors VRMs have to handle load current slew rates of more than 50 A/μs [14] demanding controllers with extremely fast responses. Further, topologies with low ADC latency are desirable in the cases when the ADC is inside a feedback loop, since delays in the ADC correspond to phase shift that may degrade the loop response. Consequently the ADCs used in digital VRM controllers should have very low latency. While multistage ADC topologies may have high throughput (high sampling rate), they have larger latency due to either multiple comparisons (pipeline ADCs), or digital filtering ($\Sigma\Delta$ ADCs). Thus a single stage (flash) topology is preferable in applications such as VRMs where the speed of response is of paramount importance. From Fig. 6 it can be seen that the controlled quantity V_o' does not have large excursions beyond V_{ref} in normal operation. Thus, using a high resolution flash ADC that covers the full range between ground and V_{in} will demand excessive power and silicon area. Rather, an ADC topology can be conceived of, which has high resolution only in a small window around V_{ref}.

A block-diagram of such a "window" ADC is presented in Fig. 7. A digital-to-analog converter (DAC) converts the digital reference word D_{ref} to an analog voltage V_{ref}. Note that this DAC can be slow compared to the response time of the regulator, since D_{ref} does not change very fast, if at all. Then, a number of comparators are connected to V_{ref} through an offset network with steps ΔV_{ref}, creating a few quantization bins around V_{ref}. The controlled quantity V_o' is fed in the other input of the comparators. Note that, since V_o' is compared against V_{ref}, the resulting digital signal (D_e) is the difference between the two, which is a digital representation of the error signal V_e. Hence, this is a differential architecture implementing both an ADC and an error amplifier.

For example, if the converter is designed for regulation range of 50 mV, V_o' will not exceed $\pm$50 mV about V_{ref} under normal operation. In this case ADC resolution of $\Delta V_{ref} = 10$ mV seems reasonable to provide good control of V_o within the regulation range. Then only 2×50 mV/10 mV $= 10$ ADC bins are required to cover the range of V_o', which corresponds to ADC resolution between 3 and 4 b. In fact, the ADC in the prototype VRM from Section IV-C used a window structure. The window ADC concept was used in a delay-line ADC [12].

Some VRM control schemes saturate the duty cycle if the error signal exceeds a certain magnitude in order to improve converter transient response [13], [20], [21]. This function can be easily implemented with window ADC by enabling the comparators at the ends of the quantization window to turn all converter phases on or off (depending on direction of the transient).

[2]In this simulation the data is sampled at the switching frequency, therefore the switching ripple on V_o and V_o' cannot be seen. For this discussion the switching ripple is not of interest and its omission makes the plots clearer.

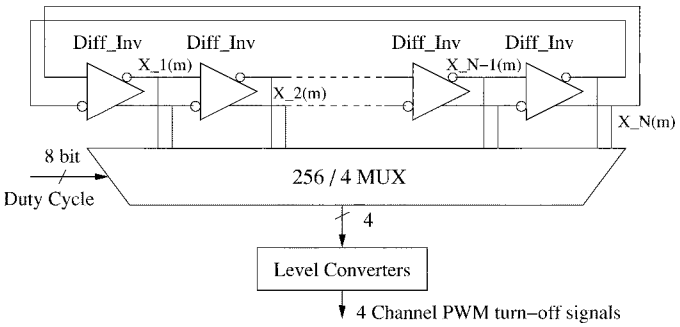

Fig. 8. Ring-oscillator-MUX 8-b PWM generation block diagram.

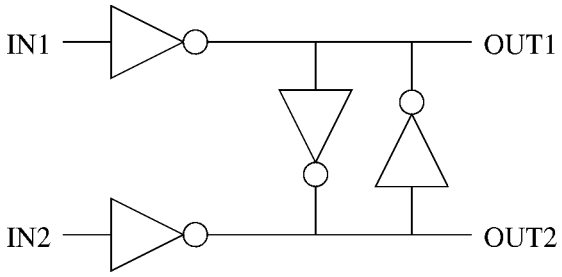

Fig. 9. Ring oscillator delay cell.

V. Digital PWM Generation Circuits

A. Overview of Digital PWM Generation Schemes

One method to digitally create PWM signals is a fast-clocked counter-comparator scheme [8]. This design takes reasonable die area but the power consumption reported is on the order of mWs. The main reason is that in this scheme, a high frequency clock and other related fast logic circuits are needed to achieve

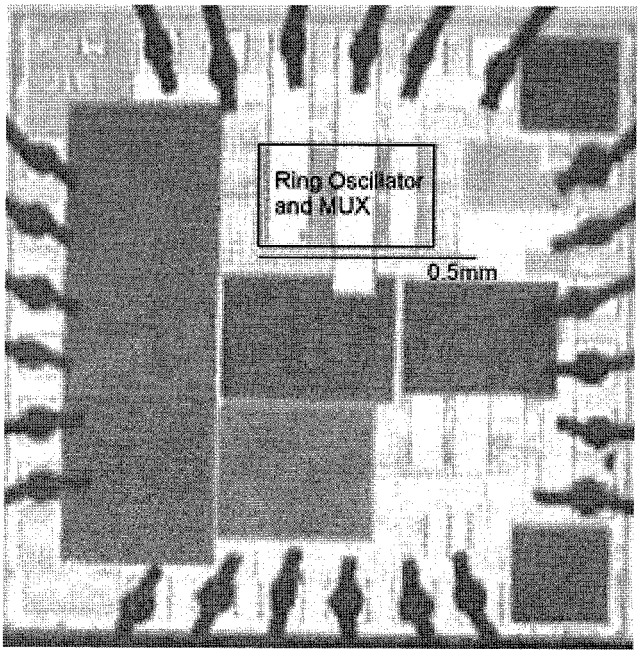

Fig. 10. Die photo of ring-oscillator-MUX test chip in 0.25 μm CMOS process.

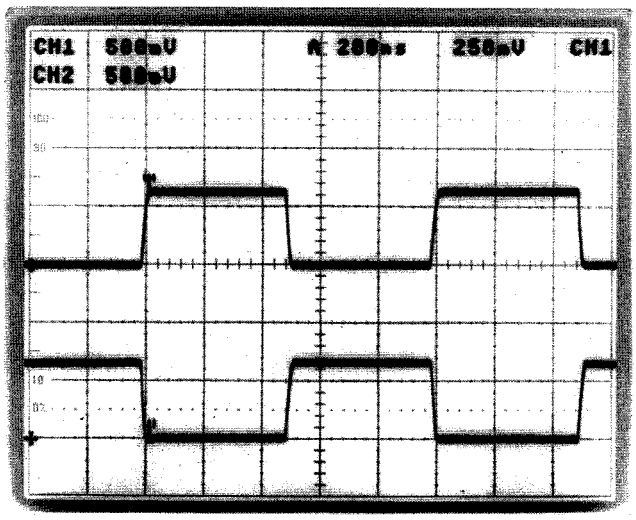

Fig. 11. Differential output of one ring oscillator delay stage. The upper waveform is taken from one tap on one stage of the ring, and the lower waveform is taken from the symmetric tap from the same stage. The vertical scale is 500 mV/div, and horizontal scale is 200 ns/div.

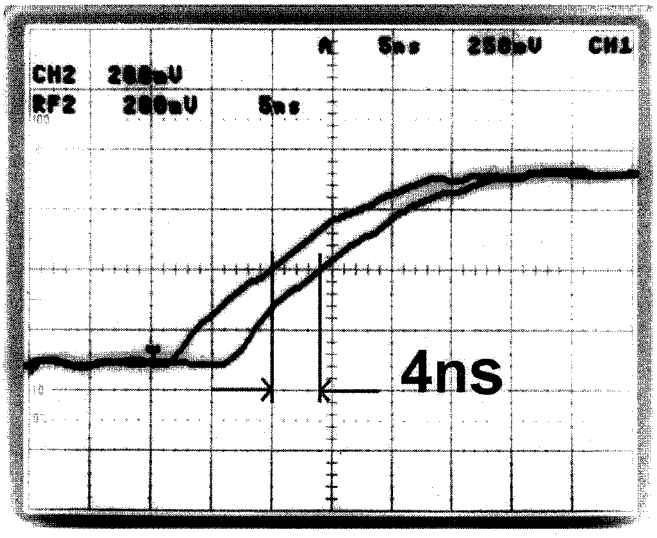

Fig. 12. 8-b resolution is achieved between two adjacent outputs of a ring oscillator delay cell. At 1 MHz oscillation frequency, the resolution is 4 ns.

a high control resolution based on a reasonable switching frequency. Even worse, in a multiphase application, PWM generation circuitry cannot easily be shared among phases, so an independent counter-comparator pair must be implemented for each phase, leading to increased die area and power.

A tapped delay line scheme is proposed in [7]. Power is significantly reduced with respect to the fast-counter-comparator scheme since the fast clock is replaced by a delay line which runs at the switching frequency of the converter. One drawback of this design is that the delay line is not well suited for multiphase application. In a multiphase controller, precise delay matching among the phases places a stringent symmetry requirement on the delay line. Also, area is a limiting factor for this scheme since the size of the MUX grows exponentially with the number of resolution bits N.

A combined delay line-counter structure is reported in [6], aiming to make a compromise between area and power. However, the asymmetry of the delay line remains a problem for multiphase applications.

B. Ring-Oscillator-MUX Scheme

A ring-oscillator-MUX implementation of a DPWM module, as illustrated in Fig. 8, has area and power considerations similar to those of the delay line approach. However, this scheme has the advantage of a symmetric structure.

Main components of the ring-MUX scheme are a 128-stage differential ring oscillator, which yields 256 symmetrically oriented taps, and a 256-to-4 MUX that can select appropriate signals from the ring. MUX allows control of PWM timing for each of four phases, as would be used in a four-phase VRM.

A square wave propagates along the ring. When the rising edge reaches tap zero in the ring, the rising edge of the PWM signal for phase one is generated. The falling edge of this PWM signal is generated when the rising edge of the propagating square wave reaches a specified tap in the ring. MUX is used to specify the tap for phase one, in accord with the commanded duty cycle. The PWM signals for each of phases two through four are generated in an analogous manner, but using taps on the ring offset by 64 positions for each subsequent phase.

A fully differential inverter is used as the basic cell of the ring oscillator, as shown in Fig. 9, allowing a ring with an even number of stages to support a stable oscillation. This makes the ring oscillator scheme especially suited for multiphase PWM generation since the different phases can be tapped out from symmetric positions on the ring.

The ring oscillator provides the clock for the digital controller. The frequency of the ring oscillator can be controlled

by adjusting the supply current to the entire ring. The ring frequency obeys the relationship

$$f = \alpha \cdot I_{avg}/C_{load} \cdot V_{swing} \tag{23}$$

where I_{avg} is the current supplied to ring oscillator, V_{swing} is voltage swing seen in the ring, and α is a constant. It is straightforward to control frequency by adjusting oscillator current.

In principle, a ring oscillator can support more than one frequency mode, depending upon initial condition. Only the quasisquare wave at the fundamental frequency is desirable. As shown in [4], the dynamics are such that only the fundamental mode is stable. This result is shown experimentally as well.

C. Experimental Results

A test chip to generate an 8-b resolution PWM signal has been fabricated on a 0.25 μm CMOS process, the die photo of which is shown in Fig. 10. Instead of using a flat MUX, a binary-tree MUX is used because of its smaller transistor count and smaller area. The oscillator runs in current-starved mode and the voltage swing is reduced to the range of 0.4 V to 1 V depending on the frequency. The target dc–dc buck converter applications require switching in the frequency range of 100 kHz to 5 MHz. The corresponding current drawn by the entire chip comprising the ring oscillator and one MUX is 80 μA at 5 MHz and less than 1 μA at 100 kHz. The waveforms of the complementary outputs of one of the stages for operation at 1 MHz are shown in Fig. 11. Fig. 12 shows the LSB resolution of 4 ns for 1 MHz operation. Level converters convert the reduced voltage swing back to rail to rail, and each level converter takes 2 μA at 1 MHz. In the test chip, only the fundamental oscillation mode has ever been observed.

VI. Digital Controller IC Architecture

A summarizing block diagram of a digital controller IC for a four-phase VRM and the associated timing diagram are shown in Fig. 13. The window ADC samples $V_o' = V_o + R_{ref} I_o$ (see Section IV-B) at the switching frequency, producing the error signal D_e.[3] The duty cycle calculation block implements a PID control law (21) using twos complement arithmetic to calculate the duty cycle command D_c based on D_e. Digital dither is used to modulate the least significant bits (LSBs) of D_c in order to achieve high DPWM resolution with a DPWM module with moderate hardware resolution [5]. Subsequently, two MUXs are used in an interleaved manner, in conjunction with a differential ring oscillator, to generate the PWM turning-off signals for the four phases (PWM1OFF, $\cdots$, PWM4OFF). During every switching period, the new duty cycle command $D_c(n)$ is applied to one of the MUXs while the other one is holding the previous value $D_c(n-1)$ to ensure correct PWM signal generation for all phases. In general, two MUXs are sufficient for updating D_c in a multiphase application.

Test ICs, implementing the duty cycle calculation module and the DPWM module, were successfully fabricated and tested.

[3]In VRM applications requiring controller delay of less than one switching period, tha ADC can be sampled at a frequency higher than the switching frequency [21].

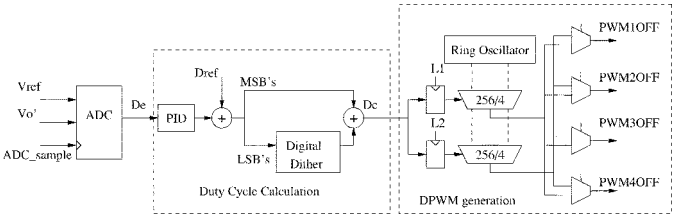

Fig. 13. Block diagram and timing of proposed digital controller IC.

VII. Conclusion

This paper developed the architecture of a digital PWM controller for application in multiphase VRMs. Passive current sharing was investigated, and estimates of the phase current mismatch due to power train parameter variations were derived. The VRM transient response was analyzed, considering nonzero controller delay, and a scheme for sensing a combination of the VRM output voltage and output current with a single low-resolution window ADC was proposed. The architecture and IC implementation of a DPWM generation module, using a ring-oscillator-MUX scheme, was discussed. Experimental results from a prototype VRM and an IC implementation of the DPWM module were presented.

Appendix
Critical Inductance Derivation

For the converter of Fig. 1, an output voltage V_o transient resulting from a change of the load current by ΔI_o was discussed in Section IV-A and Fig. 4. If the load current step occurs at time $t = 0$, then, assuming saturated controller response, the resulting output voltage change follows:

$$\Delta V_o = -\Delta I_o R_{ESR} - \frac{\Delta I_o}{C_o} t \tag{24}$$

for $0 \le t < T_d$, and

$$\Delta V_o = -\Delta I_o R_{ESR} - \frac{\Delta I_o}{C_o} t + (t - T_d) R_{ESR} \frac{V_L}{L} + \frac{(t-T_d)^2}{2C_o} \frac{V_L}{L} \tag{25}$$

for $t \ge T_d$. If $L \le L_{crit}$ the magnitude of ΔV_o reaches a maximum at $t = T_d$ and then starts decreasing, while if $L > L_{crit}$ it continues to increase for a while after $t = T_d$. Thus L_{crit} corresponds to the value of L for which the first derivative of (25) is zero at $t = T_d$,

$$\left.\frac{dV_o}{dt}\right|_{t=T_d} = -\frac{\Delta I_o}{C_o} + R_{ESR} \frac{V_L}{L_{crit}} = 0 \tag{26}$$

hence

$$L_{crit} = \frac{R_{ESR} C_o V_L}{\Delta I_o}. \tag{27}$$

Since the capacitor time constant $\tau_o = R_{ESR} C_o$ is approximately constant for a particular capacitor technology (e.g., about 10 μs for electrolytic, and 0.8 μs for ceramic), (27) can be

$$L_{crit} = \frac{\tau_o V_L}{\Delta I_o}. \tag{28}$$

Note that L_{crit} is a function only of power train parameters. Further, it depends on the choice of capacitor technology for C_o, and not on the actual value of C_o.

Similar analysis is done in [16] deriving a critical capacitance value as a function of R_{ESR} and L, however since C_o and R_{ESR} are related, L_{crit} appears to be a more relevant design parameter. Other authors [22] have used frequency domain analysis to derive a result similar to (28).

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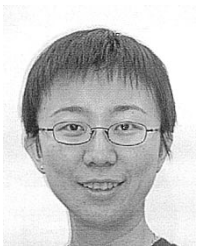

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Dr. Sanders received the NSF Young Investigator Award in 1993 and Best Paper Awards from the IEEE Power Electronics Society and the IEEE Industry Applications Society. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom.