Hindawi
Active and Passive Electronic Components
Volume 2018, Article ID 9343241, 8 pages
https://doi.org/10.1155/2018/9343241

Review Article

Architecture Characteristics and Technical Trends of UHF RFID Temperature Sensor Chip

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Received 29 May 2018; Revised 21 August 2018; Accepted 3 September 2018; Published 1 October 2018

Academic Editor: Wen-Ming Zhang

The integration of temperature sensor (TS) and UHF RFID technology has attracted wide attention theoretically and experimentally. The architecture, power consumption, temperature measurement range, accuracy, and communication distance are key indicators of the performance of UHF RFID temperature sensor chip (RID-TSC). This work aims to provide a clearer view of the development of UHF RFID-TSC integration technology. After a systematic analysis of the characteristics of ADC, TDC, and FDC used in an integrated TS, the key low-power technologies under different architectures are summarized. Through the observation of the latest researches and commercial products, the development trend of UHF RFID-TSC technology is obtained, including on-chip and off-chip coordination, multiprotocol and multifrequency support, passive wireless sensor intelligence, miniaturization, and concealment.

1. Introduction

In recent years, the development of Internet of Things (IoT) technology has greatly expanded the function of RFID. The new sensor integrated with RFID chip is the bridge of integrating RFID technology into wireless sensor network [1] and IoT applications [2]. In the IoT systems, temperature is an important indicator of environment, goods, and vital signs. In 1988, MIDDelHek first proposed integrating temperature sensor (TS) with RFID [3]. At present, the progress of microelectronics and RF/microwave circuit integration technology makes new RFID applications possible [4], such as human health monitoring [5], food monitoring [6–8], and environmental monitoring [9].

There are many different ways to transform RFID tags into RFID sensor tags. For example, the traditional tag antenna is replaced by a sensitive material, which is sensitive to the physical characteristics of its surrounding environment [10–13]. In addition, the sensor unit can also be directly integrated into the RFID chip circuit [6–8, 14]. Some RFID sensing tags have been implemented, such as temperature, light, and pressure sensors [15, 16]. This paper focuses on the RFID temperature sensor chip (RID-TSC), which is the integration technology of temperature sensor (TS) and RFID. Obviously, in order to realize the integration of these two functions, there are still many problems to be addressed, such as power consumption, temperature measurement range and accuracy, and communication distance.

Due to the lack of clear information, it is difficult for chip designers to make correct choices in different architectures and key technologies. Therefore, in this paper, the existing scientific research achievements and commercial products are analyzed. Furthermore, the typical technical architectures and key technologies are summarized. At last, the technical development trend of RFID-TSC is prospected.

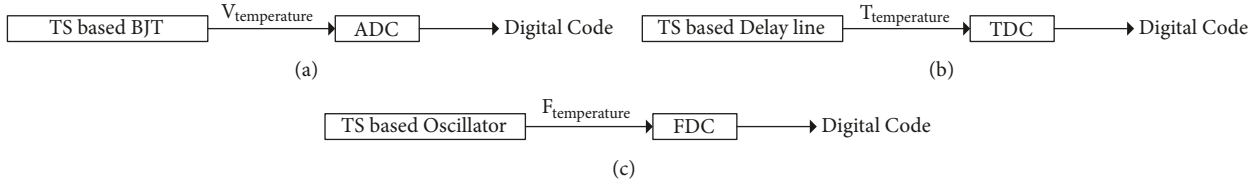

Figure 1: Typical technology architectures for CMOS-based RFID TS. (a) ADC architecture. (b) TDC architecture. (c) FDC architecture.

The organization of this paper is as follows. In Section 2, the technical architecture and characteristics of RFID-TSC are systematically analyzed. In Section 3, the low-power technology of RFID-TSC is summarized. In Section 4, the performance indicators of the latest scientific research results and the commercial products are discussed. In Section 5, a research conclusion and the prospect of RFID-TSC technology are given.

2. Architecture and Characteristics

2.1. Architecture of TS. The integrated TS architecture based on CMOS process can be divided into three categories [8]: TS based on bipolar junction transistor (BJT) and analog-to-digital converter (ADC) [17–19], TS based on propagation delay line and time-to-digital converter (TDC) [6, 14], and TS based on ring oscillator and frequency-to-digital converter (FDC) [7, 20–22], as shown in Figure 1. CMOS process has the advantages of high integration, low cost, low-power consumption, compatibility with standard digital process, and small chip area. It has become the mainstream technology of intelligent sensor to integrate more signal sensing [23].

The ADC architecture includes sigma-delta ADC, successive approximation ADC (SAR ADC), and zoom ADC composed of SAR ADC and sigma-delta ADC. This architecture has the advantages of high measurement accuracy and wide measurement range, but it also has the disadvantages of complex structure, high power consumption [43], and low conversion rate, such that the ADC module will cost the total power of 80% [8].

The TDC architecture usually produces two voltage signals: proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) [6, 8, 14, 17–19]. The PTAT and CTAT delays are used to form a differential structure, and by eliminating the pulse signal offset a good pulse signal can be obtained and converted into temperature digital code [6]. Due to the nonlinearity of the delay unit, the unequal slope caused by the process variation, and the supply voltage fluctuation [22], therefore, the accuracy based on the TDC architecture is poor. To achieve acceptable temperature measurement accuracy, hundreds of inverters are required [44, 45]. To obtain a sufficient range of operating delays, a delay-locked loop (DLL) is employed [46], but it occupies a large chip area and consumes a large amount of power.

The FDC architecture converts the temperature-dependent signal into a frequency through a ring oscillator, which converts the frequency into a temperature-dependent digital signal by the FDC [8, 22]. The linearity of the temperature sensing signal can be improved by adjusting the linear frequency difference slope [8], and the accuracy can be improved by single or multipoint calibration.

Generally speaking, although the ADC architecture has high precision, it is not suitable for RFID applications because of its high power consumption and large chip area [14]. However, TS based on FDC and TDC are often used due to low chip area and power consumption [6–8, 47], while TDC has lower power consumption and higher accuracy than FDC [8].

2.2. Architecture of RFID-TSC. Regarding the integration technology of RFID and TS, many works have proposed different technical architectures [7, 9, 28, 48]. In general, RFID-TSC mainly consists of two parts: antenna and chip. According to the function, the chip is divided into four parts: RF analog front-end, nonvolatile memory (NVM), temperature sensing (TS) unit, and digital baseband. Among them, the temperature sensing (TS) unit can be divided into on-chip and off-chip implementations. A typical RFID-TSC technology architecture is shown in Figure 2.

The antenna has an important influence on the performance of the RFID-TSC. According to the material and production process, antennas include two types:

(1) The on-chip antenna (OCA) or in-chip antenna, which is on the same silicon substrate as the circuit chip

(2) The packaged antennas are not used as circuit chips on the same silicon substrate, but it is encapsulated in the same shell

OCA performance is affected by area, CMOS process and materials, signal interference, silicon interconnect metal size, high dielectric constant, and low resistance silicon substrate. A multiport microstrip patch antenna was proposed [16], one of which has a stack of thin-film solar cells for energy harvesting and the other port is assigned to the patch antenna to replenish the RF signal transmitted from the reader. Two antennas [49–51] were studied, one connected to the RFID chip to receive/transmit data from the reader and the other for RF energy harvesting, to power the digital circuits of sensors and microcontroller units (MCUs). In order to eliminate the need of two antennas, a circularly polarized patch antenna (CPPA) [52] was proposed, which utilizes the circular polarization (CP) generated by the new antenna shape to match the two chips with an asymmetric star-shaped slot microstrip patch antenna; one is as a reference node and the other can be connected to the sensor.

The RF analog front-end realizes the RF carrier into DC power and generates reference voltages and signals for other modules. It consists of several rectifier circuits, demodulation circuits, backscatter modulation circuits, reference circuits,

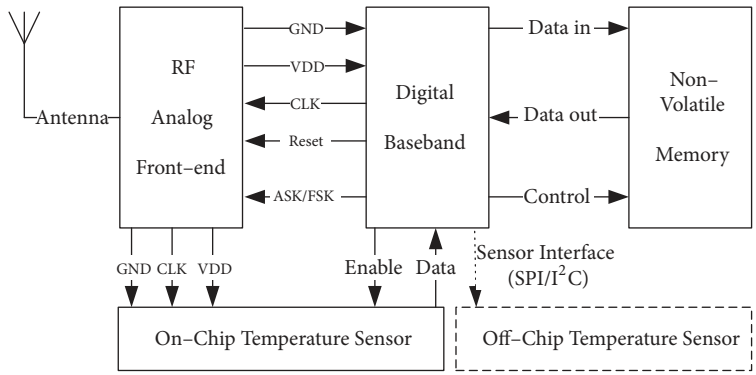

Figure 2: RFID-TSC typical architecture.

regulator circuits, clock circuits, and reset circuits [9, 48]. It is also responsible for communication interfaces and interactions with readers through electromagnetic fields.

The digital baseband mainly implements communication protocols, encryption and decryption, encoding, decoding, anticollision algorithms, and operation control [53]. The digital demodulator detects and demodulates the signal from the RF analog front-end [7, 9]. The operation instructions and parameters can be captured and processed through the finite state machine (FSM), and the communication flow with the reader is controlled according to the communication protocol. Compared with RFID, the RFID-TSC digital baseband needs to increase the management of TS and realize the reading of the temperature by the enable signal. Finally, the transmitter modulates the tag ID and the temperature value to the reader.

Usually, the NVM for UHF RFID includes E^2PROM [54, 55], ferroelectric RAM(FeRAM) [56], and improved planar E^2PROM [57] for storing tag information and temperature data. FeRAM has an advantage in writing speed and power consumption [56], but it has the disadvantage of data loss. More importantly, it requires special processes, resulting in more expensive than others [57]. The improved planar E^2PROM operates at a lower voltage, thus reducing write power consumption, but the area is twice the conventional E^2PROM. At the same time, the design risk is unpredictable because of the fewer foundries supported. Therefore, E^2PROM is the most mainstream technology in UHF RFID design with its low cost, mature technology, and support from many foundries [58].

2.3. Sensing Interface. The RFID chip is mainly extended by the sensor interface and can integrate various sensors such as temperature, humidity, pressure, and acceleration [59]. Therefore, RFID can be more easily integrated into sensor networks and other IoT applications. As shown in Figure 2, the serial peripheral interface (SPI) [33] bus and the interintegrated circuit (I^2C) bus [28, 51, 60, 61] are common interfaces. Because the SPI bus occupies more pins than the I^2C bus, it limits the expansion of the RFID-TSC function. In contrast, the I^2C bus is a better choice for multisensor integration.

3. Low-Power Technology of RFID-TSC

For UHF passive RFID tags, the power of the reader determines the communication distance, but it is strictly limited in different countries and regions. For example, the United States stipulates that the effective isotropic radiated power (EIRP) of UHF RFID reader cannot exceed 4W (36dBm), the European standard is 500 mW (27dBm), and China standard is 2W (33dBm). Because the integrated TS adds additional power consumption, which will further shorten the communication distance of the RFID tag, so low-power consumption is also a key technology in the RFID-TSC. The technical architecture and low-power technology used by TS together determine the overall power consumption of the RFID-TSC.

3.1. State of RFID-TSC Based on ADC. Second-order sigma-delta ADC or zoom ADC, dynamic element match (DEM), and bias current are commonly used in low-power design. Dynamic threshold technique and second-order zoom ADC are used to realize temperature detection [18], which corresponds to the minimum energy consumption of 2nJ for each conversion. Using the second-order sigma-delta ADC, the power consumption is 13.2μW [28] and 26μA [29], respectively. Two parasitic substrate PNP transistors with different current densities and ultralow power 12 bit SAR ADC are used to detect the temperature; the average current is 17.5μA (31.5μW) [1] at 1.8V working voltage.

3.2. State of RFID-TSC Based on TDC. Usually, MOS elements, MOSFET and substrate parasitic NPN bipolar subthreshold are used as temperature sensing units. Clock or circuit reuse, module time-sharing, PSRR cascode current source mirror bias circuit, and subthreshold technology bias transistors can further reduce power consumption.

The subthreshold and clock multiplexing of MOS elements are adopted, and the power consumption is 119nW [6]. The power consumption of 38 nW is achieved by using MOSFET, module time division, and transistors biased in subthreshold region. The reference voltage deviation of band gap is avoided by time domain comparison, and the designed TS achieves 0.9nW power consumption [24]. The substrate

Table 1: Comparison of TS.

Work/ Architecture	Power Consumption (μW)	Chip Area (mm^2)	Work voltage (V)	Temperature Range/error (°C)	Accuracy (°C)
[6]TDC	0.119	0.0416	0.50~1.00	-10~30/-0.80~1.00	- -
[8]TDC	0.112	0.0125	0.50	-10~20/-0.10~0.30	0.049
[14]TDC	0.68	- -	0.60~1.00	-20~30/-0.80~0.80	- -
[24]TDC	0.90	0.20	- -	+27~47/-1.00~1.00	- -
[25]TDC	0.35	0.14	1.00	-30~60/-1.50~1.50	0.30
[26]TDC	- -	- -	1.80	-10~100/- -	0.50
[27]TDC	0.10	- -	1.50	-20~80/- -	0.403
[1]ADC	31.5	- -	1.80	-37~91/-0.10~0.43	- -
[17]ADC	7.4	0.12	1.60~2.00	-30~125/-0.20~0.20	- -
[18]ADC	- -	0.08	1.50~2.00	-55~125/-0.15~0.15	0.25
[28]ADC	13.20	1.44	1.20	-20~50/-1.00~0.80	0.02
[29]ADC	- -	- -	1.80	-20~120/-0.65~0.65	- -
[9]FDC	0.60	0.731	1.00	-40~85/-1.50~1.50	0.50
[20]FDC	0.22	0.05	1.00	0~100/-1.60~3.00	0.30
[22]FDC	- -	0.008	1.00	0~110/-1.50~1.50	0.18
[30]FDC	0.125	0.062	0.50	-40~80/-0.70~1.20	- -
[31]FDC	0.095	0.04	- -	+8~85/- -	0.40
[32]FDC	0.20	0.585	1.50	-75~125/- -	0.45

parasitic NPN bipolar is used to generate temperature-dependent current signal to realize temperature detection; the power consumption is 0.35 μW [25]. The current source mirror bias circuit with PSRR cascode structure generates two currents which are opposite to the temperature, and the power consumption is only 1.39 μW [26]. The analog front-end circuit is used repeatedly as the bias current of the temperature conversion module to reduce power consumption, which is only 100nW [27]. The multiplexed internal circuit acts as a bias current, and the internal oscillator is multiplied to produce a signal multiplication with a power consumption of only 0.1 μW [62].

3.3. State of RFID-TSC Based on FDC. A ring oscillator is used to design the TS, and the power [30] of 0.125μW is achieved at 0.5V voltage. A voltage controlled oscillator is used to make the MOSFET work in the subthreshold region, and the power consumption is 0.101 μW [63] and is realized by using the dynamic threshold technique. The threshold voltage and carrier mobility of MOS transistors are dependent on the frequency and temperature of the ring oscillator. In order to satisfy different temperature conditions, the subthreshold operating voltage is 0.3V, the other operating voltage is 0.4V, and the power consumption is 95nW [31] at the sampling frequency of 10Hz. By adding the control transistor to the circuit, when the voltage regulator is not needed, the voltage stabilizing circuit can further reduce the power consumption and improve the energy utilization ratio [34].

3.4. Summary. Through low-power research and analysis of the three architectures, subthreshold MOS elements, bias current, circuit multiplexing, time division technology, etc. commonly used low-power key technologies, which can achieve ultra-low-power consumption of only 0.1μW, which can be integrated with UHF RFID technology to meet the needs of RFID-TSC applications very well.

4. Comparison and Analysis of RFID-TSC

4.1. Comparison and Analysis of TS. Power consumption, chip area, temperature range, and accuracy are important indicators that affect TS performance. Table 1 compares the performance indicators of the current research results. The results show that the ADC architecture requires a large chip area and a large amount of power consumption and also has the advantages of wide temperature range and high precision. So, it is suitable for application scenarios that are not sensitive to power consumption. The TDC and FDC architectures have relatively low power consumption, but the temperature range is small, so they are more suitable for specific applications sensitive to a certain temperature range, such as animal temperature measurement and cold chain logistics.

4.2. Comparison and Analysis of UHF RFID-TSC. In commercial applications, RFID-TSC products not only pursue performance indicators but also are compatible with mainstream protocols and standards, communication distances, working modes, etc., which together determine their market share and potential. Because different brands of UHF RFID-TSC products adopt different protocols and standards, Table 2 compares and analyzes the UHF RFID-TSC products on the market from the aspects of RF working frequency band, working mode, air interface protocol, temperature range/error, and communication distance.

Table 2: Comparison of UHF RFID-TSC.

Work / product	RF Band(MHz)	Working Mode (active / passive / semi-passive)	Air Interface Protocol	Temperature Range/error(°C)	Communication distance(m)
[9]Xidian University	860~960	passive	- -	-40.00~85.00/ -1.50~1.50	6.00(read)/ 2.50(write)
[28]CAS/IOS	- -	passive/ semi-passive	EPC C1G2	-20.00~50.00/ -1.00~0.80	9.50(read)/ 6.00(write 4W EIRP)
[33]PE3001	860~960	passive	EPC C1G2	-20.00~30.00/ -1.00~1.00 30.00~50.00/ -1.75~1.75	- -
[34]Tianjin University	915	passive	- -	-40.00~55.00/ -2.00~2.00	7.50
[35]Ams/SL900A	860~960	passive/ semi-passive	EPC C1/ C3 G2	-20.00~60.00/ -1.00~1.00	5.00~6.00
[36]farsens/Fenix-Vortex-P25H	860~960	passive	EPC C1G2/ ISO18000-6C	-30.00~85.00/ -2.00~2.00	2.00
[37]CAENRFID/A927ZET/A927Z	860~928	semi-passive	EPC C1G2/ ISO18000-6C	-40.00~85.00/ -0.10~0.10	10.00(in air)/ 2.50(in metal)
[38]CAENRFID/RT0005	860~928	semi-passive	EPC C1G2/ ISO18000-6C	-20.00~70.00/ -0.50~0.50	10.00(in air)
[39]Infratab/Infratab Freshtime™	- -(UHF)	semi-passive	EPC C1G2	-25.00~-20.00/ -1.00~1.00 -20.00~50.00/- 0.50~0.50 50.00~70.00/ -1.00~1.00 -25.00~-20.00/ -1.00~1.00	- -
[40]SMARTRAC/SENSOR DOGBONE	860~960	passive/	EPC C1G2/ ISO 18000-6C	-40.00~85.00/ - -	- -
[41]gaorfid/Sensing RFID Tag	860~928	semi-passive	EPC C1G2/ ISO 18000-6C	-30.00~70.00/ -0.10~0.10	10.00
[42]TELID 412	860~960	passive	ISO18000-6C	-10.00~20.00/ -0.50~0.50 -40.00~65.00/ -1.00~1.00	0.50

As shown in Table 2, the maximum communication distance of the products in the air is 10m [37], the maximum write distance under 4W(EIRP) is 6m [28], the temperature range is - 40~85°C [9, 37], and the minimum error is 0.1°C[37]. It can be seen that the existing products can basically meet the needs of different application scenarios, such as food quality control temperature measurement range requirements -10~30°C[6, 8] and animal or human body temperature monitoring requirements at about 37°C [7].

5. Conclusion

In this paper, the integration technology of RFID and sensor is summarized and analyzed. Three typical architectures and key technologies of ADC, TDC, and FDC for TS are discussed. On this basis, the overall architecture of UHF RFID-TSC is given. Then the existing research results and commercial products were compared and analyzed from the aspects of technical architectures, power consumption, temperature measurement range and accuracy, communication distance, protocol standards, and other dimensions. It is believed that the extended sensor interface can realize the automatic perception of temperature, humidity, pressure, and other environmental information by RFID, which greatly expands the traditional RFID application scenarios. Based on the above analysis, the development trend and prospect of UHF RFID-TSC are listed as follows.

5.1. On-Chip and Off-Chip Coordination. SPI and I^2C bus as the sensor interface of RFID chip can greatly expand the function of RFID and have achieved success, and some products have been successfully applied. For example, the AMS/SL900A provides an easy-to-use interface for access to external sensors [35], the FEIX-VROTEX-P25H supports external access temperature and pressure sensors [36], and the A927 ZET has both on-chip and off-chip temperature

sensing unit and supports setting threshold to achieve precise control [37].

5.2. Multiprotocol and Multifrequency Support. The current mainstream air interface protocol of is EPC Global C1 G2/ISO 18000-6C, and most products are fully compatible. In addition, HF and UHF work frequencies have different advantages. For better commercial applications, multiprotocol and multifrequency fusion innovation are a good way to develop. For example, a sensor chip [64] compatible with HF and UHF work frequencies can operate at frequencies from 13MHz to 2.45GHz, making full use of HF low-power and UHF long-distance communication, which significantly improves the flexibility of RFID as a sensor node.

5.3. Passive Wireless Sensor Intelligence. In the IoT systems, RFID is no longer a simple individual identification function. It has evolved into a feature-rich intelligent wireless sensor node. Most importantly, RF technology solves the problem of relying on power in traditional sensor technology. For example, the sensing unit and the off-chip sensing interface make RFID a wireless sensor node [16, 64], PE3001 can be integrated with other MCUs [33], and SAR ADC can be well integrated into the sensing interfaces of passive and semipassive RFID tag [65].

5.4. Miniaturization and Concealment. Although some achievements have been made in UHF RFID-TSC research, the overall size of the product is too large, it is still mainly attached to the surface of the object, and the concealment of the tag cannot be achieved. Therefore, on the basis of keeping distance and realizing temperature sensing function, how to realize miniaturization and miniaturization of products, how to implant them into the object to realize invisibility, and how to sense the temperature and other information inside the object are still a hot and difficult point worth researching.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

Acknowledgments

This work was supported by the Project of Scientific Operating Expenses from Ministry of Education of China (Grant no. 2017PT19) and Open Research Fund of Beijing Key Laboratory of Big Data Technology for Food Safety, Beijing Technology and Business University.

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