Architectures for High Dynamic Range, High Speed Image Sensor Readout Circuits

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***Abstract*— The stringent performance requirements of many infrared imaging applications warrant the development of precision high dynamic range, high speed focal plane arrays. In addition to achieving high dynamic range, the readout circuits for these image sensors must achieve high linearity and SNR at low power consumption. We first review two high dynamic range image sensor schemes that have been developed for visible range imaging and discuss why they cannot meet the stringent performance demands of infrared imaging. We then describe a new dynamic range extension scheme, Folded Multiple Capture, that can meet these performance requirements. Dynamic range is extended using synchronous self-reset while high SNR is maintained using few non-uniformly spaced captures and least-squares fit to estimate pixel photocurrent. We conclude with a description of a prototype of this architecture targeted for 3D-IC IR focal plane arrays.**

I. INTRODUCTION

Precision high dynamic range (HDR), high speed imaging is finding growing applications in the automotive, surveillance, tactical, industrial, and medical and diagnostic instrumentation (e.g., fluorescence detection and spectroscopy) arenas. These applications can be broadly segmented into those operating in the visible range (typically $400\text{nm} < \lambda < 800\text{nm}$) and those operating in the infrared (IR) range (typically $4\mu\text{m} < \lambda < 12\mu\text{m}$). Precision HDR, high speed IR imaging applications, specifically, are fraught with challenges. In addition to the ability to capture scenes with large variations in irradiance due to object temperatures, the imaging system must be able to deal with undesirable scene disturbances, due to, for example, sun reflection or laser jamming. The imaging system must also have highly linear, shot noise limited readout in order to achieve the stringent sensitivity requirements. In [1], it is argued that low power IR focal plane arrays (FPAs) with $>$ 120dB dynamic range operating at 1000 frames/sec are needed for such applications. These performance requirements are far more aggressive than is achievable with present-day IR FPAs.

Several HDR extension schemes have been developed in recent years mainly for visible range imaging applications, e.g., [2]–[8]. While these schemes require pixels that are too large to be practical for such applications, they are better suited to IR FPAs where pixel sizes are inherently larger due to the longer wavelengths and the use of bump-bonded detectors, e.g., [9]. Moreover, with the advent of 3D-IC technology whereby multiple wafers can be stacked and vertically interconnected, the effective pixel area available to implement these schemes is increased [1]. However, as discussed in [10], [11], none of the existing HDR schemes can meet the aforementioned IR FPA performance requirements. In [12], a HDR extension scheme denoted by Folded Multiple Capture (FMC) that can achieve all the requirements stated in [1] is presented. Low power consumption is achieved while maintaining high SNR by using digital signal processing to relax the demands on the analog front-end (AFE). FMC also provides tolerance to disturbances in the scene that generate large transient spikes of photocurrent. A proof-of-concept of the FMC architecture has been fabricated and is readily extendable to a fully integrated imaging system using 3D-IC technology [13].

The rest of the paper is organized as follows. In Section II, we begin by reviewing the fundamentals of image sensors and introduce needed terminology. We then discuss the stringent fidelity requirements in IR imaging applications and review two dynamic range extension schemes that have been developed for visible range imaging. In Section III, we discuss the architecture and operation of FMC, implementation of a prototype, and experimental results obtained.

II. BACKGROUND

An image sensor consists of an array of photodetectors followed by circuits for readout. Sensor performance is therefore a function of both the photodetector used and the readout circuits. Each photodetector in a conventional image sensor, e.g., CCD, CMOS APS, or IR FPA, converts incident photon flux into photocurrent i_{ph}. In visible range imaging, the incident photon flux corresponds to light reflected off of objects in the scene, while in IR imaging, the incident photon flux corresponds to object thermal radiation. A simplified Signal-to-Noise ratio (SNR) of the integrated photocurrent is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{qi_{ph}t_{\text{int}} + q^2\sigma^2_{\text{Readout}}}, \quad \text{for } i_{ph} \leq \frac{qQ_{\max}}{t_{\text{int}}},$$

where t_{int} is the integration time, q is the charge of an electron, $Q_{\max}$ is the saturation charge or well capacity, and σ_{Readout} is the readout noise. Note that this simplified SNR only considers integrated shot noise and readout noise and assumes that correlated-double-sampling (CDS) is performed,

thus eliminating the reset noise and offset contributions. We also assume that gain FPN and dark current are either negligible or calibrated for, as is usually the case for state-of-the-art visible and IR sensors.

Image sensor dynamic range (DR) is defined as the ratio of the largest nonsaturating photocurrent to the minimum detectable photocurrent, typically defined as the standard deviation of the noise under dark conditions. In visible range imaging, this corresponds to the range of intrascene illumination levels that can be imaged, while in IR imaging, this corresponds to the range of intrascene temperatures that can be imaged. Assuming the above sensor model, $i_{\max} = qQ_{\max}/t_{\text{int}}$ and $i_{\min} = q\sigma_{\text{Readout}}/t_{\text{int}}$ and dynamic range is given by

$$\text{DR} = \frac{i_{\max}}{i_{\min}} = \frac{Q_{\max}}{\sigma_{\text{Readout}}}.$$

Since the dynamic range of image sensors is generally limited by the readout circuitry, HDR extension schemes modify a conventional sensor's readout circuits to improve its DR. Extending DR at the low end requires reducing $i_{\min}$, which can be achieved by either reducing σ_{Readout} or increasing t_{int}. DR extension at the low end obtained by decreasing the diode or sense node capacitance to reduce σ_{Readout}, as is usually done in visible range image sensors, reduces $Q_{\max}$ which is not desirable for IR imaging. Extending dynamic range at the high end requires increasing $i_{\max}$, which can be achieved by adapting the integration times to photocurrent or increasing the effective well capacity.

A. Infrared imaging

Using Planck's Blackbody law, typical parameters for a given detector and optics, and assuming that the object distance is much longer than the focal length of the lens, the relationship between temperature and resulting photocurrent is given by

$$i_{ph}(T) = \int_{\lambda} R_d(\lambda) A_d \tau_{\text{optics}} T_{\text{atmsphr}} \frac{c_2}{4F\sharp^2 \lambda^4 (e^{c_1/\lambda T} - 1)} d\lambda,$$

where $R_d(\lambda)$ is the detector responsivity, A_d is the detector area, τ_{optics} and T_{atmsphr} are the transmittances of the optics and atmosphere, respectively, $F\sharp$ is the f-number of the imaging lens, λ is the wavelength, T is the temperature, and c_1 and c_2 are constants. An example of photocurrent as a function of temperature is plotted in Figure 1 for Medium Wavelength IR (MWIR), $4\mu\text{m} < \lambda < 5\mu\text{m}$. The nonlinear relationship between temperature and photocurrent, coupled with the fact that in general the background temperature produces a large photocurrent, serve to explain why high DR image sensors are required for IR imaging applications.

A demanding imaging scenario that elucidates the need for precision imaging in IR is one that involves scenes having very small variations in temperature around a much larger background temperature. For example, for imaging the human body the target temperature range is within only ± 2K around a nominal background of about 310K. Thus sensitivity is critical,

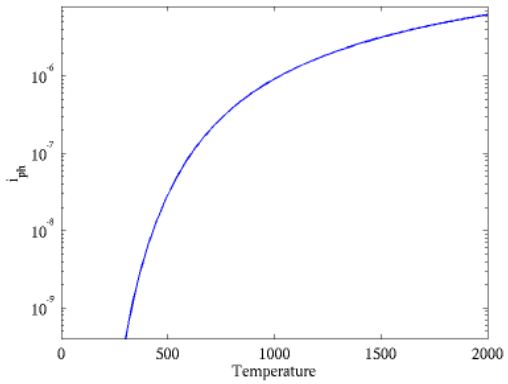


Fig. 1. i_{ph} vs. temperature for a typical MWIR pixel with $F\sharp = 2.5$, $A_d = 30 \times 30\ \mu\text{m}^2$.

necessitating shot noise limited readout with high SNR. Such sensitivity is typically quantified in the temperature domain as Noise Equivalent Temperature Difference (NETD) [14]. Assuming shot noise limited operation for a given integration time, NETD can be derived as

$$\text{NETD}(T) = \sqrt{\frac{q i_{ph}(T)}{t_{\text{int}}}} \Bigg/ \frac{d}{dT} i_{ph}(T). \tag{1}$$

In general,

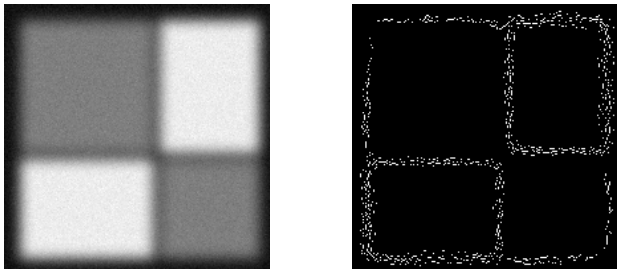
$$\text{NETD}(T) = \frac{i_{ph}(T)}{\sqrt{\text{SNR}}} \Bigg/ \frac{d}{dT} i_{ph}(T).$$

The numerator corresponds to the minimum detectable photocurrent and the denominator translates it into the temperature domain. Note that achieving NETD in the order of 10mK, as is often the case in medical imaging applications, requires detection of photocurrents within the range of a few femtoamps in the presence of a nanoamp offset. This accuracy can be achieved with $t_{\text{int}} = 1$msec using a long wavelength IR FPA if equation 1 holds. In practice the charge-handling capacity of the pixel, constrained by its area, limits the achievable SNR and thus frame averaging is typically performed.

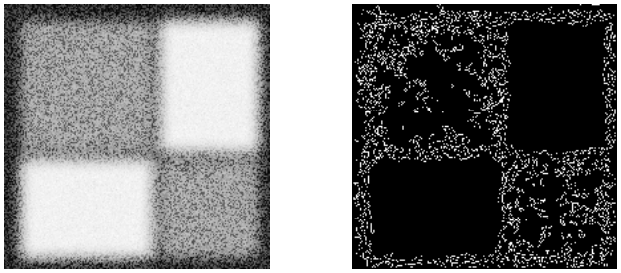
Since calibration is typically performed in IR FPAs to compensate for large variations in detector parameters, such as dark current and gain mismatch, linearity of the readout is essential. Further, the frame averaging alluded to above relies on linear readout. Averaging is only effective in minimizing NETD if the additive noise is zero mean and uncorrelated, such as for temporal noise. This is illustrated in Figure 2 where simulation results are shown for two different readouts imaging a scene with four temperature patches. For the linear, shot noise limited readout, the NETD achieved after averaging 100 frames is 5mK and the output after applying an edge-detection algorithm is satisfactory. For the readout with nonlinearity, however, the NETD achieved is 40mK and the resulting output after applying the same edge-detection algorithm is clearly unsatisfactory.

B. Dynamic range extension

Schemes that extend dynamic range at the high end can either to do so by adapting the integration time to pixel



(a) Linear, shot noise limited readout.



(b) Readout with 0.3% nonlinearity.

Fig. 2. Simulation of effect of readout nonlinearity on multiple frame averaging. For each readout, output images are obtained after averaging 100 frames and calibrating for the pixel gain/offset nonuniformity (left), followed by Canny edge-detection (right).

photocurrent, providing long integration times for pixels with small photocurrents and short integration times for pixels with high photocurrents [2], [4], [6], or by recycling the integrator and therefore extending dynamic range using self-reset or charge subtraction [5], [7], [16]. We briefly review two such schemes below.

Multiple-Capture

The multiple-capture scheme [2] can achieve high DR with high SNR but at moderate speed. This scheme increases dynamic range by sampling the signal nondestructively multiple times during integration. The HDR image can be constructed using the last-sample-before-saturation algorithm [17] as illustrated in Figure 3.

To define DR and SNR, we assume uniform sampling time $t_{\rm capt}$ and that the filter only performs last-sample-before-saturation and digital CDS. The maximum nonsaturating signal is given by $i_{\max} = qQ_{\max}/t_{\rm capt}$ and the minimum detectable signal is given by $i_{\min} = q\sigma_{\rm Readout}/t_{\rm int}$. Thus

$$\text{DR} = \frac{Q_{\max} t_{\rm int}}{\sigma_{\rm Readout} t_{\rm capt}}.$$

It can be shown that for $i_{ph} > Q_{\max}/t_{\rm int}$, SNR$> Q_{\max}/2$ [10]. Note that this scheme provides high SNR at both the high and low ends. The accurate timing of the capture times and cancelation of the reset noise and offsets via digital CDS guarantee the high SNR of this readout architecture.

DR at the high end is directly related to $t_{\rm capt}$. The general implementation of the multiple-capture scheme requires per-pixel ADC [17], and as discussed in [10], multiple-capture achieves only high dynamic range at moderate speeds due to the limitation in the per-pixel ADC speed/resolution performance. Increasing $i_{\max}$ requires decreasing $t_{\rm capt}$. Generally

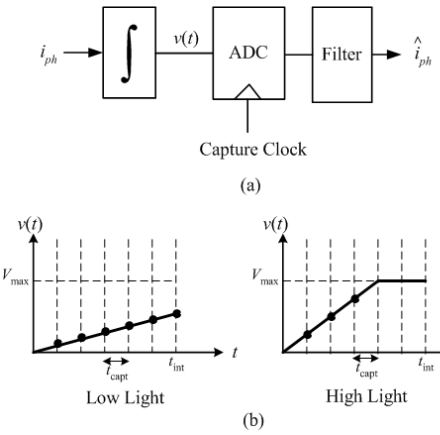


Fig. 3. Multiple Capture scheme (a) block diagram (b) sample waveforms.

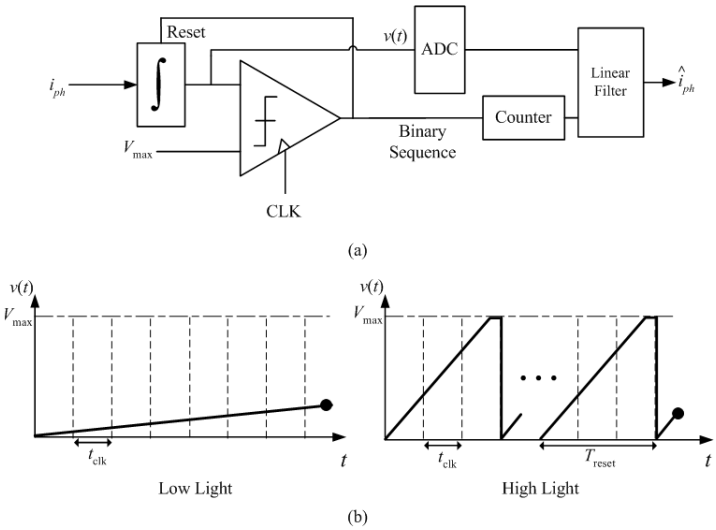


Fig. 4. Synchronous self-reset scheme (a) block diagram (b) sample waveforms.

for a given pixel area, the ADC speed can only be increased by reducing resolution, which results in SNR reduction.

Synchronous Self-reset with Residue Readout

The synchronous self-reset with residue readout scheme proposed in [16] promises high dynamic range at high speed with low power consumption, but cannot achieve high SNR. The scheme is described in Figure 4. The photocurrent is integrated and converted into voltage $v(t)$, which is periodically compared to a reference voltage $V_{\max}$. If $v(t) \geq V_{\max}$, the comparator switches, the integrator is reset, and the counter is incremented. At the end of integration, the digitized value of $v(t_{\rm int})$ and the reset count are combined to estimate the photocurrent. Let $n_{\rm Reset}$ be the number of resets, then

$$\hat{i}_{ph} = \frac{qQ_{\max}}{t_{\rm int}} \left(n_{\rm Reset} + \frac{v(t_{\rm int})}{V_{\max}} \right).$$

To compute DR and SNR, we first compute the distortion due to the underestimation of charge resulting from saturation before synchronous resetting takes place (see the waveform in Figure 4(b)). At the high end, assuming no noise $T_{\rm reset} = \lceil qQ_{\max}/(i_{ph} t_{\rm clk}) \rceil \, t_{\rm clk}$, and the counter output is given by $n_{\rm Reset} = \lfloor t_{\rm int}/T_{\rm reset} \rfloor$.

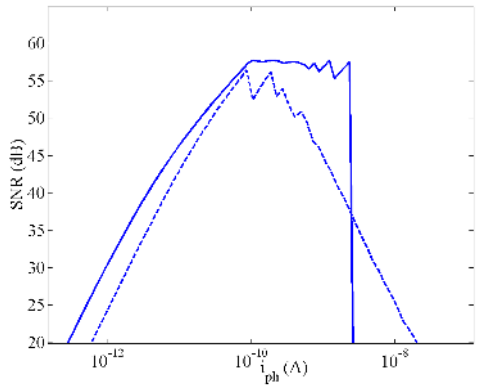


Fig. 5. Simulated SNR vs. i_{ph} for multiple capture (solid) and synchronous self-reset (dashed) with $t_{\rm int} = 1$msec and 100fF integrating capacitor.

It can be shown that,

$$\mathrm{DR} = \frac{\sqrt{3} Q_{\max} t_{\rm int}}{\sqrt{\sigma^2_{\rm Readout} + \sigma^2_{\rm Reset}} t_{\rm clk}}.$$

SNR is also given by

$$\mathrm{SNR}(i_{ph}) = \frac{(i_{ph} t_{\rm int})^2}{\sigma_i^2}.$$

where,

$$\sigma_i^2 = \sigma^2_{\rm Distortion} + \frac{q i_{ph}}{t_{\rm int}} + (n_{\rm Reset} + 1)\left(\frac{q\sigma_{\rm Reset}}{t_{\rm int}}\right)^2 + \left(\frac{q\sigma_{\rm Readout}}{t_{\rm int}}\right)^2 + \left(\frac{q\sigma_{\rm Offset} n_{\rm Reset}}{t_{\rm int}}\right)^2 + (\sigma_H i_{ph})^2$$

and

$$\sigma^2_{\rm Distortion} = \frac{1}{3}\left(\frac{i_{ph} t_{\rm clk}}{t_{\rm int}} \times \left\lfloor \frac{t_{\rm int}}{\lceil q Q_{\max}/(i_{ph} t_{\rm clk})\rceil\, t_{\rm clk}} \right\rfloor\right)^2.$$

DR at the high end increases as $t_{\rm clk}$ is decreased, which is possible if a simple, low power regenerative comparator is used. However, as discussed in [10], synchronous self-reset suffers from low SNR at both the high and low ends. At the high end, it suffers from the underestimation of charge and large gain FPN due to comparator and self-reset offsets. It suffers at the low end since CDS is not performed.

As discussed, multiple capture achieves high SNR over the extended range, but cannot achieve the required 120dB of dynamic range at 1000 frames/sec. On the other hand, synchronous self-reset can achieve very high DR at high frame rates, but suffers from poor SNR at both the low and the extended ends. Figure 5 plots SNR versus photocurrent for the two schemes. Note the drop in SNR for synchronous self-reset in the extended range.

In the following section, we discuss the new Folded Multiple Capture HDR scheme [13], which by combining features of the synchronous self-reset and multiple capture schemes discussed above, can satisfy the precision imaging requirements in IR with low power consumption and robust circuits. We first discuss the architecture and operation of FMC. We then describe a prototype of the architecture and experimental results obtained.

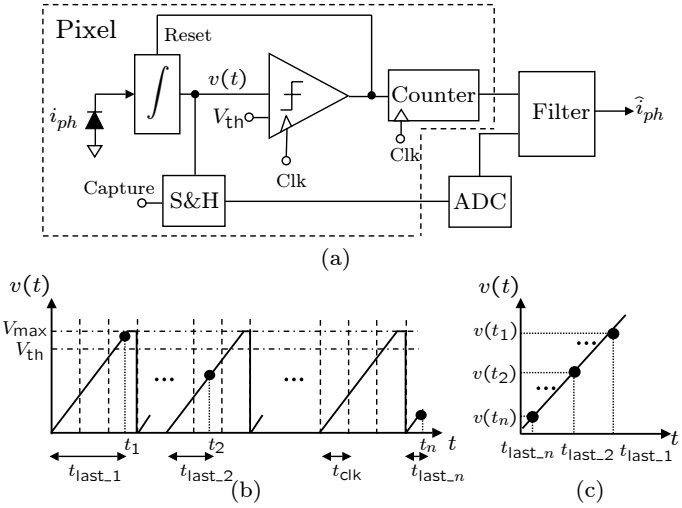


Fig. 6. Above: FMC architecture. Below: FMC operation.

III. Folded Multiple Capture

A block diagram of the FMC architecture is shown in Fig. 6(a). Each pixel consists of an integrator, with reset that is controlled by a comparator, a counter, and a sample-and-hold (S&H). The S&H output is digitized by a fine ADC, whose output along with the counter values are fed to a filter that generates the photocurrent estimate. At each clock cycle, the integrated photocurrent, $v(t)$, is compared to a threshold voltage $V_{\rm th}$. The integrator is reset when the comparator output flips creating the folded waveform shown in Fig. 6(b). Meanwhile, the integrator output is sampled and digitized at predefined sampling or capture times $t_1, t_2, \ldots, t_n$. The capture times are synchronized with Clk, shifted by $t_{\rm Clk}/2$ to avoid simultaneous reset and capture. The counter is incremented by the clock and reset by the comparator output signal. Its value, which corresponds to the *effective integration time* $t_{\rm last\_i}$ (the time from the last reset), is read out at each capture time. The slope of the linear least-squares fit of the digitized capture values and their corresponding integration times is used to estimate the photocurrent (see Fig. 6(c)). In effect, FMC performs n regular captures during an exposure time and combines them to achieve a high fidelity estimate of the photocurrent. Dynamic range is extended by $2t_{\rm int}/t_{\rm Clk}$ over the integrating capacitor dynamic range. For example, for $t_{\rm int}/t_{\rm Clk} = 1000$, DR increases by 66dB. Fig. 7 shows example waveforms for $t_{\rm int}/t_{\rm Clk} = 8$ and four capture times. A low input photocurrent (see Fig. 7(a)) results in no reset and the scheme reduces to a conventional FPA with Fowler readout [15]. A high photocurrent (see Fig. 7(c, d)) results in periodic reset. Unlike other self-reset schemes discussed earlier, however, the number of resets is not used to estimate the signal.

For low power, the number of captures used in achieving the high fidelity estimate of the photocurrent must be small. A surprising fact about FMC is that only 3 to 4 scene-independent globally set captures are needed to achieve uniformly high SNR. We wish to select capture times to guarantee a minimum SNR of $Q_{\max}/2$, for photocurrents $\geq q Q_{\max}/t_{\rm int}$. Note that

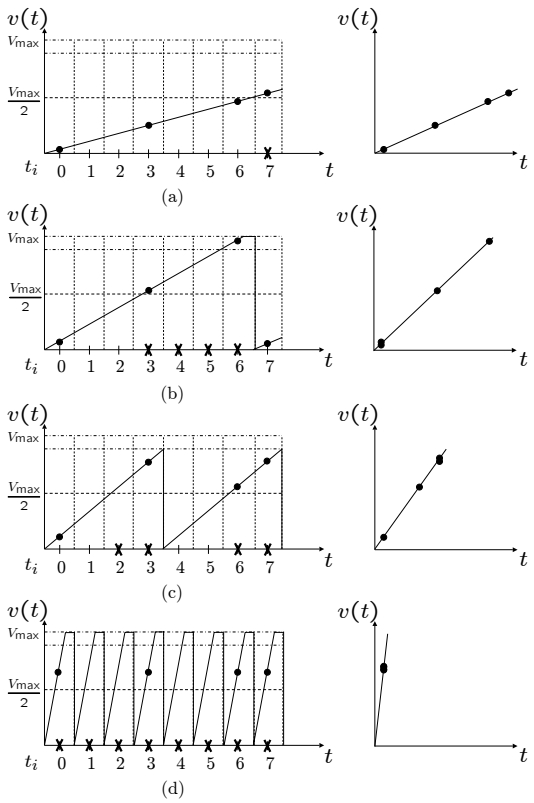


Fig. 7. Integrator output (left) and corresponding least-squares estimate (right) for four photocurrent values with capture times, $(t_1, t_2, t_3, t_4) = (0, 3, 6, 7)t_{\rm Clk}$. The $\times$ indicate capture times that satisfy $Q_{\rm int} > Q_{\rm max}/2$.

a single capture only guarantees this requirement for a certain range of photocurrents. To illustrate this point, consider the example in Fig. 7 again. A capture at $t_4 = 7t_{\rm Clk}$ satisfies the above SNR condition for the examples in Fig. 7(a),(c),(d). However, using only this capture results in SNR ≈ 0 for example (b). The problem is solved by using another capture, e.g., between $3t_{\rm Clk} \leq t_3 \leq 6t_{\rm Clk}$. It can be shown that capture times $(t_2, t_3, t_4) = (3, 6, 7)t_{\rm Clk}$ for $t_{\rm int}/t_{\rm Clk} = 8$ ensure that for all photocurrent values, at least one of the capture values has a value higher than $Q_{\rm max}/2$. To perform offset cancelation, a low value capture, e.g., at $t_1 = 0$, is also required.

While the above algorithm guarantees minimum SNR of $Q_{\rm max}/2$, least-squares fit of the captures and corresponding effective integration times to estimate photocurrent further improves SNR by canceling offsets, e.g., due to integrator and readout, and reducing the read, shot, and 1/f noise (see [15]). Note that since all signals in FMC are synchronized with a low jitter clock, SNR is not affected by timing inaccuracies. Further area and power reductions are achieved by relaxing the comparator specifications. As discussed earlier, the variation of the reset period with comparator offsets results in fixed pattern noise (FPN) that typically degrades SNR of HDR schemes. Since in FMC reset periods are not used to estimate photocurrent, the associated FPN is avoided and a simple regenerative architecture can be used for the comparator, obviating the need for a larger, power consuming gain stage. A relaxed comparator design also means that the highest clock frequency is not limited by the comparator speed, but by the settling time of the S&H circuit.

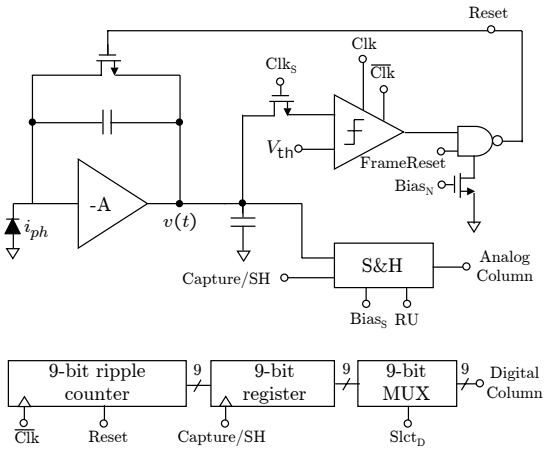


Fig. 8. Pixel block diagram.

A. Implementation

A prototype of the FMC architecture has been implemented in a 0.18μm CMOS double-poly, five metal-layer process. A block diagram of the pixel readout circuit is depicted in Fig. 8. To maintain compatibility with IR detectors, we use a Capacitive Trans-impedance Amplifier (CTIA) as an integrator. The comparator is implemented using a regenerative architecture. A slow fall NAND gate is used to reduce the random charge injection on the feedback capacitor. The S&H block consists of a source follower with dynamic bias control followed by the sampling circuit which is followed by column readout circuitry. All analog circuits operate at 3.3V. The digital portion of the pixel consists of a 9-bit ripple counter with an output register. All digital circuits operate at 1.8V and a level shifter is used to drive counter reset. After each capture, the analog capture values and the latched counter values are readout serially from each column off-chip.

The chip micrograph is shown in Fig. 9. Four columns have pixels with NWELL/PSUB diodes and the fifth has pixels driven by external current sources. Provisions have been made for bump-bonding IR detectors adjacent to the diodes. The analog and digital periphery circuits are placed at opposite ends of the pixel array. The Timing Control block generates all control signals. The clock rate (and thus dynamic range) and capture times are programmable via a scan chain. Each pixel occupies an area of $30\mu{\rm m} \times 150\mu{\rm m}$ (40% analog, 60% digital). The digital section is implemented using standard cells and is readily miniaturized with custom design. Analog area is dominated by the CTIA and S&H to meet the linearity requirement. In a 3D-IC implementation of the fully integrated imaging system [1], each pixel is estimated to be $30\mu{\rm m} \times 30\mu{\rm m}$ with 2 analog and 1 digital circuit layers.

B. Experimental Results

A uniform LED illuminator is used as the light source for characterization. The chip analog column outputs, digitized using an on-board ADC, and the chip digital column outputs are transferred to a PC via an FPGA-based data acquisition

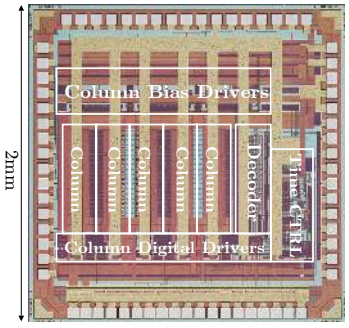


Fig. 9. FMC chip micrograph.

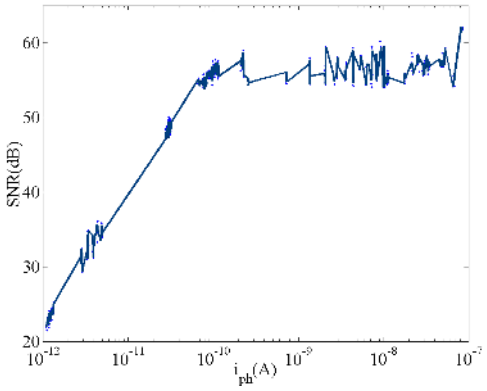


Fig. 10. Experimental scatter plot of SNR vs. i_{ph} for FMC.

board. Least-squares fit of the digitized capture values and corresponding effective integration times to estimate photocurrent is then performed in software.

The linearity and SNR are characterized locally at multiple random intervals. Experimental SNR versus i_{ph} results are shown in Figure 10. Read noise is expected to be lower with test setup improvements. Table I summarizes the chip characterization results.

The power consumption per pixel is 25.5μW and dominated by the CTIA. This corresponds to energy consumption of 25.5nJ for each pixel readout with DR = 138dB and SNR = 60dB. Note that the CTIA power consumption can be significantly reduced, e.g., using switched biasing, with knowledge of the detector parameters.

TABLE I

PERFORMANCE CHARACTERISTICS

$t_{\rm int}$, $t_{\rm Clk}$	1msec, 1μsec
Capture times used (t_1, t_2, t_3, t_4)	$0, 143, 334, 818\mu$sec
Integrator capacitance	100fF
Integrator voltage swing	1.5V
Frame rate	1000 frames/sec
Dynamic range	138dB
Maximum input current	200nA
System read noise	240μV
Peak SNR	62dB
Linearity	$< 0.15\%$
NETD (estimated for MWIR, F# 2.5)	20mK
Pixel power consumption	25.5μW

IV. Conclusion

This paper discusses the need for precision high dynamic range, high speed focal plane arrays for IR imaging applications. High dynamic range schemes targeted for visible range imaging are reviewed. A new HDR scheme, Folded Multiple Capture, that meets the stringent performance requirements of IR imaging applications is discussed. A prototype of the architecture targeted towards 3D-IC IR FPAs is described.

Acknowledgment

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