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ARCHITECTURES FOR RF FREQUENCY SYNTHESIZERS

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To Viviane

Foreword

The progress in the semiconductor industry has brought us advanced electronic systems available for large groups of people. By putting more and more functionality on an integrated circuit (IC) these systems could become cheap in mass production. This is the reason why scientists and engineers put constant effort in integrating more functions into ICs.

Many of these electronic systems need internal signals with a tunable, stable and accurate frequency. An example of this is a radio-frequency receiver, where a signal with a stable frequency is used to tune to a radio-station of interest. In the past this frequency was generated with the help of bulky passive mechanically tunable components. But if one wishes to integrate such a receiver on a chip, other components are needed to generate the tunable frequency. In this case, one needs to integrate a so-called frequency synthesizer, which relies on a clean fixed reference frequency, usually derived from a crystal, to create a variety of other frequencies.

A frequency synthesizer is usually realized with a phase-locked loop (PLL) which in turn can be implemented with on-chip components like transistors, resistors and capacitors. Such a synthesizer is far more complex than the old-days mechanically tuned resonators and can contain thousands of components. But still they are cheaper, more reliable, and easier in use: everybody wants a "digitally tunable" radio.

The application of synthesizers has gone through an enormous growth in the past years. Today they are widely used in wireless telecommunication systems like mobile phones but also in optical communication systems and cable modems. PLL circuits are also widely used as clock generators for microprocessors. PLL frequency synthesizers, and in particular radio-frequency (RF)

synthesizers, are therefore important components of modern electronic systems.

A PLL frequency synthesizer may be cheap in mass production, but it is certainly not a simple circuit to design. Phase-locked loops are non-linear systems with very complex behaviour. Furthermore, PLLs are hard to simulate because time-constants are involved which may differ by many orders of magnitude. The output of a synthesizer has inaccuracies which are characterised as jitter and phase noise. These effects are very difficult to understand and to simulate. Finally, PLL design requires deep insight in system level design as well as transistor level design. So it is no surprise that there is a large need for design know-how on frequency synthesizers.

This book deals with the design of RF frequency synthesizers. It contains basic information for the beginner as well as in-depth knowledge for the experienced designer. Since frequency synthesizers are used in many different applications, different performance aspects are important in every case. Sometimes settling-time is important, sometimes residual phase deviation is important and sometimes residual frequency deviation is important. In all cases the design must be optimized in a completely different way. This book describes a conceptual framework for the different optimisations. It is, furthermore, widely illustrated with practical design examples used in industrial products.

The book was originally the Ph.D. thesis of Cicero Vaucher, who wrote it after 10 years of experience in RF frequency synthesizers at Philips Research Laboratories. I really enjoyed working with Cicero during the preparation of his thesis and now I feel very happy that it has been published as a book. Cicero has a natural talent in clear writing and therefore I believe this book is really worth reading for a broad group of scientists and engineers.

BRAM NAUTA
Professor IC Design
University of Twente, The Netherlands

Preface

Frequency synthesizers are an essential building block of RF communication products. Digital tuning has become commonplace in traditional market segments, such as TVs and AM/FM radios, and is fundamental to the operation of personal cellular communication systems, in which the RF channels are dynamically allocated as the users move within the network, and the mobile hand-sets have to automatically and transparently re-tune to different RF carrier frequencies.

The design of high-performance frequency synthesizers involves familiarity with system optimization techniques and knowledge of state-of-the-art system and building block architectures. Common technical requirements which need to be considered during the design phase include high spectral purity, fast settling time and low power dissipation. These are the main aspects treated in this book.

The main body of the text presents a theoretical analysis of different PLL properties, followed by descriptions of innovative architectures, circuit implementations and measurement results. The analysis of the PLL properties is performed with the use of the open-loop bandwidth and phase margin concepts, to enable the influence of higher-order poles to be taken into account from the beginning of the design process. The common concepts of undamped natural frequency and damping factor, originated in the analysis of second-order systems, are therefore not used in the text.

Chapters 1, 2 and 3 are of a tutorial nature. Chapters 1 and 2 review basic communication techniques and the main specification points of frequency synthesizers for tuning system applications. Chapter 3 focuses on single-loop architectures, with a discussion of the properties of PLL building blocks on the

system level and a review of single-loop architectures in which the minimum step size is not equal to the reference frequency.

When organising this book I had the option to place the system-level analysis of different performance aspects in different chapters, that is, separated from more practical considerations such as the description of the application requirements and the implementation of the building blocks. Instead, I have chosen to "frame" the theoretical analysis within a few chapters which also describe the requirements of the intended applications. In this way, I hope that the reader will have a better understanding of the background and of the need for the theoretical system analysis being presented. Chapter 4, for example, focuses on tuning systems for phase-modulation communication systems, having as a practical application an L-band tuner for digital satellite reception. Here, a crucial specification point is the residual phase deviation of the oscillator signal; as such, Chapter 4 includes an in-depth analysis of the residual phase deviation of PLL frequency synthesizers.

Chapter 5 is the result of a frequency-modulation receiver project for car-radio applications, where the challenge was the combination of fast settling time with low residual frequency deviation. An analysis of the settling time performance as a function of the open-loop bandwidth and phase margin is presented, followed by an analysis of the residual frequency deviation performance. This analysis led to the perception that the design procedure which optimises the residual phase deviation performance, described in Chapter 4, must be avoided in frequency-modulation applications, as it always results in a sub-optimal residual frequency deviation performance. In other words, it is necessary to consider, during the optimization of the PLL frequency synthesizer parameters, whether it will be used in a phase-modulation or in a frequency-modulation communication system.

Chapter 6 focuses on programmable frequency dividers, having as practical application a low-power paging receiver. Among others, a truly-modular and an adaptive-power architecture for low-power multi-band applications are presented. Chapter 7 presents a summary of conclusions. Appendix A looks at the stability limits of PLLs using a PFD/CP combination, and Appendix B links the design of clock-conversion PLLs for optical networks to the wide-band loop design techniques developed in Chapter 4.

The circuit design of VCOs and crystal oscillators is not treated in this work. However, extensive reference lists to literature on VCO design have been included at the end of Chapters 1 and 3.

Acknowledgements

Many persons contributed to the development of this book. I would especially like to thank Dieter Kasperkovitz for his support and motivation during the execution of the projects described in the text. Dieter is also acknowledged for his valuable inputs to the circuits and architectures presented in Chapters 4, 5 and 6. I would also like to thank Prof. Bram Nauta for his continuous assistance and constructive remarks during the preparation of the manuscript. The circuits described in the text were realised in close cooperation with many colleagues, mainly from Philips Semiconductors. In particular, I want to acknowledge the following persons: Jon Stanley, Onno Kuijken, Philippe Gorisse, Alain Vigne, Pascal Walbrou and Johan van der Tang for contributions to the work described in Chapter 4. For contributions to Chapter 5, I would like to thank Kave Kianush, Huub Vereijken, Bert Egelmeers, Jan Meeuwis and Gerrit van Werven. I am also grateful to Zhenhua Wang and Gerrit van Veenendaal for contributions to Chapter 6. Pieter Hooijmans is gratefully acknowledged for the support provided for this work. Finally, I would like to thank everyone who proposed improvements to earlier versions of the text.

CICERO S. VAUCHER
Eindhoven, The Netherlands
April 2002

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List of Acronyms

ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Control
AM	Amplitude Modulation
BER	Bit Error Rate
CP	Charge-Pump
DAC	Digital-to-Analog Converter
dBc	dB with respect to the Carrier
DDS	Direct Digital Synthesizer
D-FF	D-type Flip-flop
dg	Degree
DSB	Double Sideband
EMC	Electromagnetic Compatibility
EXOR	Exclusive-OR
FM	Frequency Modulation
FSW	Frequency Setting Word
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
IF	Intermediate Frequency
J	Joule
K	Kelvin
LO	Local Oscillator
LPF	Low-Pass Filter
MASH	Multi-Stage Noise Shaping Modulator
PC	Personal Computer
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop

PM	Phase Modulation
QPSK	Quadrature Phase Shift Keying
RDS	Radio Data System
RF	Radio Frequency
rms	Root-Mean-Square
ROM	Read Only Memory
S-H	Sample-and-Hold
SNR	Signal-to-Noise Ratio
SSB	Single Sideband
VCO	Voltage-Controlled Oscillator
VHF	Very High Frequency
VLSI	Very Large Scale Integration

List of Symbols

Symbol	Meaning	Page
acc	Output of a digital accumulator	79
A_{LO}	Amplitude of the carrier signal (V)	15
A_{sp}	Amplitude of a spurious signal (V)	16
a_{sp}	Relative amplitude of a spurious signal with respect to the carrier (dBc)	16
b	Ratio of the time constants of the loop filter τ_2/τ_3	39
C_1, C_2	Capacitances of the loop filter (F)	40
F	Fractional (decimal) part of division ratio	75
F_{out}	Output frequency of a PLL (Hz)	28
f_c	Open-loop bandwidth, 0 dB cross-over frequency (Hz)	44
f_{center}	Output frequency of a VCO when $V_{tune} = 0$ V (Hz)	28
$f_{c,min}$	Minimum value of the open-loop bandwidth (Hz)	124
f_{clock}	Clock frequency of a DDS synthesizer (Hz)	88
f_{div}	Frequency of the signal at the output of a frequency divider (Hz)	28
$f_{eq,r}$	Reference frequency at which the equivalent phase noise floor is specified (Hz)	58
f_{error}	Maximum frequency error with respect to f_{lock} (Hz)	13
f_h	Higher offset frequency for integration of noise power density (Hz)	103
f_{in}	Input frequency to a frequency divider or PFD/CP (Hz)	30

f_{LO}	Output frequency of the tuning system (Hz)	4
f_l	Lower offset frequency for integration of noise power density (Hz)	103
f_{lock}	Target frequency after a frequency step (Hz)	13
f_m	Fourier frequency (offset, modulation or baseband frequency) (Hz)	15
f_{max}	Frequency of maximum phase advance of the open-loop transfer function (Hz)	45
f_{min}	Minimum step size of the tuning system (Hz)	12
f_r	Offset frequency at which the free-running VCO phase noise power density is specified (Hz)	104
f_{ref}	Operation frequency of the PFD (Hz)	28
$f_{ref,max}$	Maximum PFD operation frequency at which frequency discrimination can be realized (Hz)	36
$f_{ref,min}$	Minimum value of the reference frequency in a wide-band loop (Hz)	131
f_S	Symbol rate in a digital communication system (Hz)	103
f_{shift}	Mixing frequency in a translation loop (Hz)	86
f_{start}	Operation frequency before a frequency step (Hz)	13
f_{step}	Magnitude of a frequency step (Hz)	162
f_{xtal}	Frequency of crystal oscillator (Hz)	28
f_{xover}	Phase noise cross-over frequency (Hz)	106
$G(s)$	Open-loop transfer function of a PLL	43
$H(s)$	Closed-loop transfer function of a PLL	43
$H_d(j2\pi f_m)$	Low-pass transfer function (de-emphasis network)	169
I_{cp}	Amplitude of the output current of a charge pump (A)	33
I_{leak}	Leakage current in the tuning line of the VCO (A)	50
I_{out}	Instantaneous output current of a charge pump (A)	34
i	An integer	
$i_{np}(f_m)$	rms current noise density originated in the charge pump $(\mathrm{A}/\sqrt{\mathrm{Hz}})$	54
K	Binary input to a digital accumulator	75
K_{pd}	Gain of PFD/CP combination (A/rad)	35
K_{vco}	VCO gain factor (Hz/V)	28
k	Gain factor which depends on the configuration of the loop filter	39

k_B	Boltzmann constant; 1.37×10^{-23} J/K	59
$\mathcal{L}(f_m)$	SSB phase noise power density in a 1 Hz bandwidth to total signal power, at offset frequency f_m (dBc/Hz)	20
$\mathcal{L}_{eq}$	SSB equivalent synthesizer phase noise floor at the input of the phase detector (dBc/Hz)	58
$\mathcal{L}_{\Sigma\Delta}(f_m)$	SSB phase noise power density due to quantization noise from a $\Sigma\Delta$ modulator (dBc/Hz)	83
$\mathcal{L}_{vco}(f_m)$	SSB free-running phase noise power density of the VCO (dBc/Hz)	109
l	An integer	
loopnoise	Upper limit to the sum of the noise specification of the building blocks (dB)	118
M	Integer denoting frequency division	71
m	Number of bits, word-width of a digital accumulator	75
maxspurious	Maximum (specified) magnitude of spurious signals (dBc)	63
N	Main divider division ratio, integer	28
N_{max}	Maximum value of N which leads to compliance to $\Phi_{spec,wb}$	123
n	An integer	
n'	Effective length of a programmable divider chain	209
P_{comp}	Proportionality factor	79
p	Order of a $\Sigma\Delta$ modulator	81
p_i	Binary number	138
R	Reference divider division ratio, integer	28
R_1	Resistor used in the loop filter (Ω)	40
R_p	Ratio of the limiting values of the residual frequency deviation	173
$s = \sigma + j\omega$	Laplace transform complex variable	
T	Absolute temperature (K)	64
$T_{hp}(s)$	High-pass transfer function	60
T_{in}	Period of the input signal to a frequency divider (s)	206
T_{out}	Period of the output signal of a frequency divider (s)	206
T_{ref}	Period of the input signal to the PFD, $= 1/f_{ref}$ (s)	
t	Time (s)	
t_{lock}	Locking time after a frequency step (s)	13

$V_{mismatch}$	Magnitude of the ripple voltage due to mismatch in the CP current sources (V)	53
V_{ripple}	Magnitude of the ripple voltage at the VCO tuning line (V)	51
V_{tune}	Voltage at the tuning input of a VCO (V)	28
$v_{nf}(f_m)$	rms voltage noise density originated in the loop filter $(V/\sqrt{Hz})$	54
$Z_f(s)$	Transimpedance of the loop filter (Ω)	39
x	A positive number, expresses the dependency of the equivalent phase noise floor on the reference frequency	58
$\alpha_{lf}(f_m)$	Relative magnitude of the phase noise due to loop filter elements	64
$\gamma(\phi_m)$	Excess noise factor	109
$\Delta f_e(t)$	Remaining frequency error with respect to final value (Hz)	162
Δf	Peak frequency deviation (Hz)	51
Δf_{res}^2	Residual frequency deviation power (Hz^2)	169
$\Delta f_{vco,fr}^2$	VCO free-running frequency deviation power (Hz^2)	172
$\Delta loopnoise$	Expresses the influence of the phase margin on *loopnoise* (dB)	120
ΔR	Reset time of the D-FFs when the loop is phase-locked (s)	36
$\Delta\theta$	Phase difference at the input of a phase frequency detector (rad)	35
$\Delta\theta_{hf}$	Maximum phase difference that can be detected before PFD/CP switches polarity of the output pulses (rad)	37
δ_{cp}	Duty-cycle of the output pulse of a charge-pump	38
$\delta f_o^2(f_m)$	Frequency deviation power spectral density (Hz^2/Hz)	169
$\delta f_{vco,fr}^2$	Free-running VCO frequency deviation power density (Hz^2/Hz)	174
ζ_e	Effective damping coefficient	164
$\theta(t)$	Excess phase of a sinusoidal signal (rad)	15
θ_{div}	Phase of the output signal of a frequency divider (rad)	30

θ_{error}	Phase error at the input of PFD/CP (rad)	78
θ_{in}	Phase of the input signal to a frequency divider (rad)	30
θ_{max}	Maximum value of θ_{error} during a settling transient (rad)	166
θ_p	Peak phase deviation of phase modulation (rad)	15
θ_{ref}	Phase of the output signal of the reference divider (rad)	35
$\theta_{rms,i}$	rms phase deviation associated with a pair of PM spurious signals (rad)	17
$\theta_{rms,total}$	rms phase deviation due to several pairs of PM spurious signals (rad)	17
$\theta_{rms,single}$	rms phase deviation associated with a single spurious signal (rad)	18
τ	Active time of the charge pump output signal (s)	38
τ_2, τ_3	Time constants of the loop filter (s)	39
$\tau_{3,sp}$	Time constant determined from spectral purity considerations (s)	68
τ_{dz}	Single-sided magnitude of the dead-zone (s)	187
Φ^2_{min}	Minimum residual phase deviation power (rad^2)	109
$\Phi^2_{min,app}$	Minimum approximated residual phase deviation power (rad^2)	108
Φ^2_{res}	Residual phase deviation power (rad^2)	103
$\Phi^2_{res,app}$	Approximated residual phase deviation power (rad^2)	105
$\Phi^2_{res,ml}$	Residual phase deviation power of a multi-loop tuning system (rad^2)	125
$\Phi_{spec,max}$	Specification for the maximum residual phase deviation of the LO (rad rms)	116
Φ_{spec}	Specification for the residual phase deviation due to stochastic phase noise sources (rad rms)	116
$\Phi_{spec,spur}$	Specification for the residual phase deviation due to spurious signals (rad rms)	116
$\Phi_{spec,wb}$	Residual phase deviation specification for a wideband loop (rad rms)	122
$\Phi^2_{tr,i}$	Residual phase deviation power transferred to the output of a multi-loop tuning system (rad^2)	125
$\phi_d(f_m)$	rms phase noise power density of main divider $(\text{rad}/\sqrt{\text{Hz}})$	54

$\phi_{div}^2(f_m)$	Phase noise power density at the output of a frequency divider (rad^2/Hz)	71
$\phi_{eq}^2(f_m)$	Equivalent synthesizer phase noise floor at the input of the phase detector (rad^2/Hz)	55
$\phi_{lf}^2(f_m)$	Open-loop phase noise power density generated by the loop filter elements (rad^2/Hz)	60
ϕ_m	Phase margin (radians in equations, degrees in figures)	44
ϕ_{max}	Maximum phase advance of function $\Psi(j\omega)$ (rad)	45
$\phi_o^2(f_m)$	Phase noise power density of the PLL output signal (rad^2/Hz)	54
$\phi_{olp}^2(f_m)$	"Low-pass" phase noise power component of $\phi_o^2(f_m)$ (rad^2/Hz)	55
$\phi_{ohp}^2(f_m)$	"High-pass" phase noise power component of $\phi_o^2(f_m)$ (rad^2/Hz)	60
$\phi_{pd}(f_m)$	rms phase noise power density of phase frequency detector ($rad/\sqrt{Hz}$)	54
$\phi_{ref}(f_m)$	rms phase noise power density of reference divider ($rad/\sqrt{Hz}$)	54
$\phi_{vco}(f_m)$	rms phase noise power density of free-running VCO ($rad/\sqrt{Hz}$)	54
$\phi_x(f_m)$	rms phase noise power density of crystal oscillator ($rad/\sqrt{Hz}$)	54
χ	Ratio of f_{xover} and the effective noise bandwidth f_h	173
$\Psi(j\omega)$	Phase of the open-loop transfer function $G(j\omega)$ (rad)	45
$\psi_p(f_m)$	DSB peak phase noise power density ($rad/\sqrt{Hz}$)	20
$\omega = 2\pi f_m$	Angular frequency (rad/s)	
$\omega_c = 2\pi f_c$	Open-loop bandwidth (rad/s)	44
ω_{max}	Frequency of maximum phase advance of the open-loop transfer function (rad/s)	45