Arrays of Optoelectronic Switching Nodes Comprised of Flip-Chip-Bonded MQW Modulators and Detectors on Silicon CMOS Circuitry

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***Abstract*— We describe 8 × 8 arrays of smart pixels, designed and fabricated using MQW modulators and detectors flip-chip-solder-bonded to silicon CMOS circuits. The individual circuits implement 2 input, 1 output embedded control switching nodes. Four arrays from two different designs were fabricated and tested. For the array with the highest yield, 60 of 64 nodes functioned correctly at low speeds and were tested up to 250 Mb/s without re-adjusting individual bias voltages with the maximum speed of an individual node of 375 Mb/s. For the second-generation array, the center 4 × 8 section of the array was tested at data rates beyond 700 Mb/s with individual nodes having short term bit error rates below 10^{-11}.**

ONE APPROACH to improving the performance of large processing or telecommunications switching systems is to interconnect integrated circuits using optics. Smart pixels, with integrated optical detectors, modulators, and electronic logic, could potentially be used in these systems. The FET-SEED, consisting of the monolithic integration of multiple quantum well (MQW) optical modulators and detectors with GaAs field effect transistors, is one design platform for these smart pixels [1], [2]. Another potential design platform uses the hybrid integration of MQW modulators and detectors with commercial electronic circuits [3]–[6]. This latter approach allows one to design circuits with greater complexity and circuit yield, because it uses available established VLSI processes.

We describe 8 × 8 arrays of smart pixels, designed and fabricated using MQW modulators and detectors flip-chip-solder-bonded to silicon CMOS circuits. The modulators were designed for 850 nm operation and the substrate was removed to avoid excess absorption in the substrate [5]. The individual circuits implement 2 input–1 output embedded control switching nodes.

The CMOS circuit shown in Fig. 1 is functionally similar to switching nodes previously made using the monolithic FET-SEED technology [7]. Each node contains a single optical receiver. The first-generation arrays have two different receiver designs in alternating columns of the array, one with and one without voltage clamps on the receiver inputs. The second-generation arrays had four different transimpedence receiver designs with feedback elements shown in Fig. 1(b). The transimpedance receivers operated at lower optical powers and higher data rates. In both designs, the electrical output from a given receiver is connected to the data input of a first 2 × 1 multiplexer physically located within the same node as the receiver and a second 2 × 1 multiplexer physically located in a second node next to the first node. Each multiplexer has a pair of complementary electrical inputs, known as the control bit, that determines which input is regenerated as the optical output. In each node, a control memory (set-reset latch) stores this control bit. In the embedded control architecture, the format of the input optical signals consists of the control bits followed in time by the data bits. An electrical control load signal, common to all the nodes within the array, is held high to enable the writing of the control memories with the control bits. Once the control bits are loaded, the control load signal is held low to disable the writing of the memory, and the correct input data bits are regenerated at the output based upon the state of the memory. The output modulators are driven by an electrical inverter following the multiplexers. Other than the receivers, the circuit schematics were the same for the two designs, except that the FET's were wider in the second-generation design to provide increased current for operation at higher data rates.

The first- and second-generation circuits were designed using 1.2 μm and 1.0 μm CMOS. The center to center spacing of the nodes was 135 μm × 120 μm, so each node occupies an area equal to ∼28% of that of the comparable monolithic circuit [7]. The bump-bond pad sizes and optical window sizes were 15 μm × 15 μm with a minimum space between two bump-bonds of 15 μm. Transistors were located greater than 2 μm from the bond pads, but recently circuits have been made with FET's directly under the pads [8]. The detector and modulator window spacings were 60 μm and the spacings between detectors and modulators within a node were 75 μm.

The MQW modulators were made using processes similar to the monolithic FET-SEED [2]. The layer structure consisted of 95 periods of 9 nm GaAs quantum wells with 3.5 nm $Al_{0.3}Ga_{0.7}As$ barriers. Additional steps to the process included

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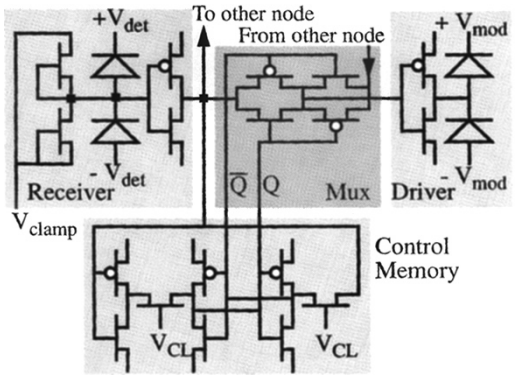

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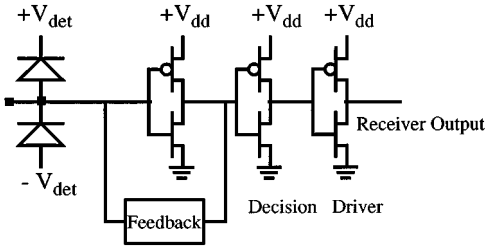

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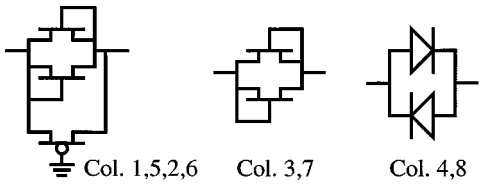


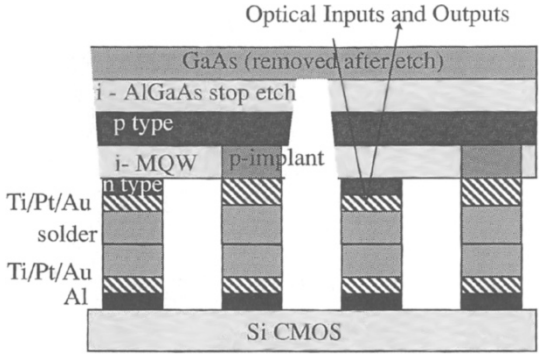
(c)

Fig. 1. (a) Schematic diagram of embedded control 2×1 nodes of the first-generation design. T's are connected, and crosses are open unless indicated. n-fets are connected to GND, and p-fets are connected to $V_{\rm dd}$. Clamping transistors are present on alternate columns. (b) Receiver section for second-generation design (c) feedback elements for receivers in (b) for the different columns in the array.

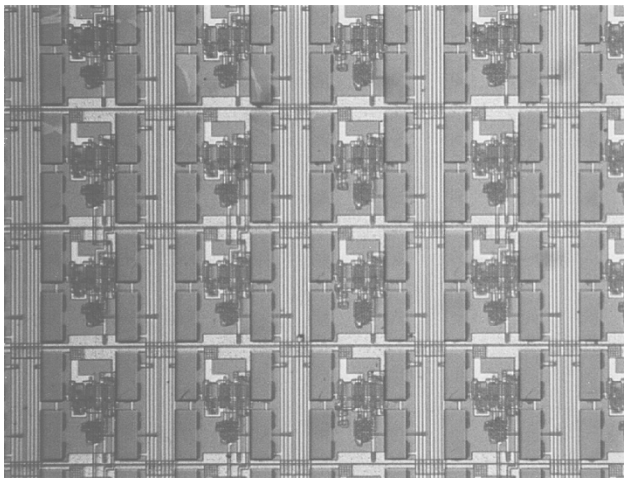
a deep mesa etch between diodes and the deposition of solder on the pads. After receiving the fabricated CMOS chips, additional metal layers (Ti, Ni, Au) and solder were deposited on the solder bump pads. After the GaAs chip was bonded to it, the GaAs substrate was removed, and the device was packaged and antirefletion coated. A more detailed description of the process is given in [5]. A cross sectional schematic and photograph of a section of a bonded chip is shown in Fig. 2. The total height of the front of the modulator from the surface of the CMOS chip is $\sim$10 μm.

Three arrays of the first design and one of the second were fabricated and tested. During substrate removal, the etchent attacked some of the modulators on the end columns of the array. For one array (of the first design), all but 1 detector and 3 modulators out of 256 quantum well diodes were operational after substrate removal.

Reflectivity and responsivity were measured for this array as a function of voltage for the bonded MQW diodes. The peak responsivities varied between $\sim$0.4 and $\sim$0.45 A/W, the high and low state reflectivities varied from $\sim$0.3–$\sim$0.4 and from $\sim$0.06–$\sim$0.15 respectively at a fixed wavelength of $\sim$850



(a)



(b)

Fig. 2. Cross sectional schematic (a) and photograph (b) of a section of the array. Rectangles are the individual MQW diode mesas, which measure $\sim$20 μm $\times$ 50 μm.

nm, and the contrast ratios varied from $\sim$1.8:1 to $\sim$2.9:1 for a 5 V swing.

High-speed testing was done on the arrays by current modulating the two input laser diodes with complementary sets of nonreturn to zero (NRZ) data from a digital word generator and supplying these optical inputs to one receiver at a time in the array. The center 4×5, 6×6, and 6×8 sections of the first design operated above 250 Mb/s and individual nodes were tested to 375 Mb/s. Fig. 3 shows the one of the outputs from each node from the center 4×8 section of the second-generation array at 700 Mb/s, with the control set so that each 2×1 node selected its own receiver. However, in all four arrays, we observed the same performance when either input of a given node was selected. At 700 Mb/s, the feedback resistors in columns 5 and 6 had too high of an impedance to affect the circuit, so the response was similar to column 3 that has FET clamps only. The nodes in column 4 with diode clamps required very asymmetric input powers, and the cause of this is unknown.

Fig. 4 shows one of the optical outputs from a node where the optical inputs to the receiver were modulated with a 10^{-23} pseudorandom pattern at 700 Mb/s. There is noticeable pulse-pattern dependency as evidenced by the separation of traces on the falling edges. This was likely caused by the nonlinear feedback resistor. With proper adjustment of the circuit supply

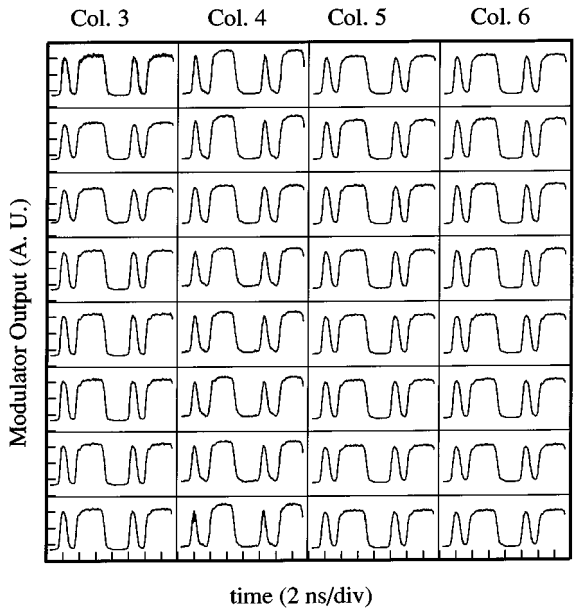


Fig. 3. Detected oscilloscope outputs from one modulator from each 2×1 switching node from the center 4×8 section of the second-generation array at a data rate of 700 Mb/s. The 8 bit repetitive data pattern incident on the smart pixel receivers was "0 0 0 1 0 1 1 1." The optical powers were equal to 800 μW per beam (2.8 pJ) for columns 3, 5, and 6, but column 4 required asymmetric powers of 800 μW and 0 μW.

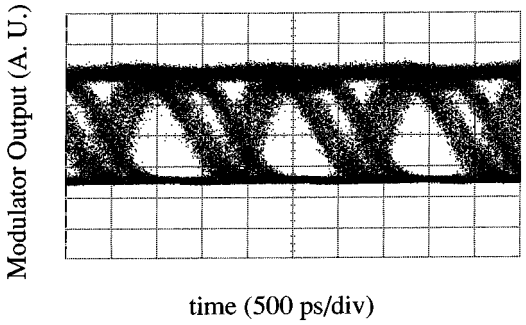


Fig. 4. Eye diagram of a particular node operating at 700 Mb/s. Individual nodes operated with short term bit-error rates below 10^{-11}.

voltages and BER detector sampling point (in time), these nodes exhibited a short term bit error rate (BER) below 10^{-11}. Laser mode-hopping prevented a long term BER measurement.

The third column of the second-generation array was particularly interesting in that it contained only feedback limiting transistors. This circuit could operate at optical powers well below 1 μW (although slowly) and could dynamically hold its state in the absence of light. We have previously described how the diode-clamped receiver can make use of this fact to operate more efficiently with optical inputs of short duration [9], [10]. Our measurements on this receiver show the same trend.

In Fig. 5, we show the supplied input optical energy for that receiver as a function of bit-rate for both nonreturn to zero (NRZ) and short pulsed inputs. The NRZ data is based on a BER for pseudorandom signals below 10^{-11}. For the pulsed data, we were unable to supply pseudorandom data, so the optical energies are based on visual inspection of the bit-pattern. We obtained clean patterns to 800 Mb/s and sightly

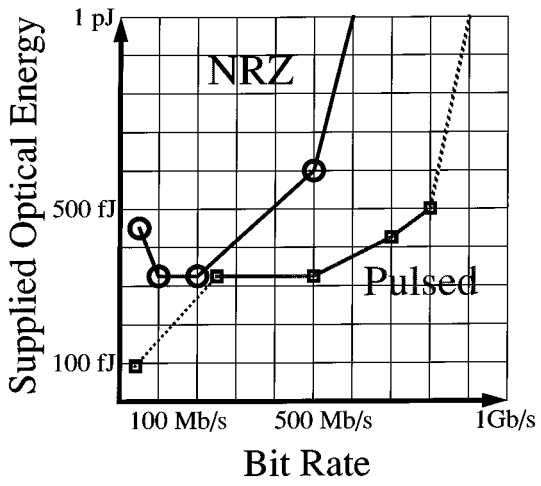


Fig. 5. Optical energy versus bit-rate for the nodes in the third column of the array for nonreturn to zero (NRZ) and return to zero (pulsed) data inputs. $V_{\rm dd}$ was lowered to 3 V for data at 25 Mb/s.

degraded patterns to 1 Gb/s. We believe the speed in both chips was limited by the driver and multiplexer circuitry.

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