Artificial Neural Network Model of SOS-MOSFETs Based on Dynamic Large-Signal Measurements

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***Abstract*—A measurement-based quasi-static nonlinear field-effect transistor (FET) model relying on an artificial neural network (ANN) approach and using real-time active load–pull (RTALP) measurement data for the model extraction is presented for an SOS-MOSFET. The efficient phase sweeping of the RTALP drastically reduces the number of large-signal measurements needed for the model development and verification while maintaining the same intrinsic voltage coverage as in conventional passive or active load–pull systems. Memory effects associated with the parasitic bipolar junction transistor (BJT) in the SOS-MOSFET are accounted for by using a physical circuit topology together with the simultaneous ANN extraction of: 1) the intrinsic FET current–voltage characteristics; 2) the intrinsic charges of the FET; and 3) the BJT dc characteristics, all from the same modulated large-signal RF data. The verification of the model using load-lines, output power, power efficiency, and load–pull, which is performed using two additional independent RTALP measurements, demonstrates that a reasonably accurate large-signal RF device model accounting for memory effects can be extracted from a single 10.5-ms RTALP measurement with a physically based ANN model.**

***Index Terms*—Artificial neural network (ANN), large-signal network analyzer (LSNA), memory effects, MOSFET, parasitic bipolar junction transistor (P-BJT), real-time active load–pull (RTALP).**

I. Introduction

VARIOUS semiconductor materials (Si, GaAs, GaN, InP, etc) and device structures (SOS-MOSFETs, MESFETs, LDMOSs, HEMTs, etc.) have been introduced and rapidly deployed in order to meet the high-power and high-efficiency requirements of modern high-frequency wireless communication[1], [2]. Under such circumstances, conventional modeling approaches (e.g., physically based or analytical closed-form empirical models) cannot keep up with the fast pace of technology development [3]. Measurement-based models, which bypass this technology dependence in the model equations, first took the form of: 1) measured S-parameter data for linear device operation; later on of 2) table-based device models like the Root model [4]; and more recently, 3) nonlinear behavioral models like X-parameters [5] for nonlinear device operation. In all these models, the functional bias or power dependence is typically implemented using spline functions. These measurement-based modeling approaches facilitate the development of large-signal models, and thus accelerate the design cycle for power amplifiers [4]–[7]. However, the main limitation in the use of spline function is: 1) their poor extrapolation outside of the range of the data available and 2) their possible oscillation between data points. The recently introduced artificial neural network (ANN) method provides very smooth functions and nonvanishing derivatives of infinite order while guaranteeing the capability to fit any nonlinear bias/power dependence in devices [8]–[10].

However, the model development cycle is still restricted due to the large number of S-parameters or nonlinear measurements needed for the model extraction. Indeed, the measurement time rapidly increases as a dense grid on the intrinsic voltage planes is required for an accurate extraction of the model. The advent and successful deployment of nonlinear vector measurement systems have created an incentive for using large-signal characterization instead of conventional small-signal characterization for device modeling [7]–[10]. The main advantage of using large-signal measurements for device modeling is that the model parameters are extracted under realistic device operating conditions and that the number of needed measurements can be reduced dramatically. The first trial using large-signal measurements was conducted for the extraction of the nonlinear charges of a field-effect transistor (FET) [11]. In [7] and [11], the gate and drain currents and charges extracted from large-signal measurements were compared to the ones obtained from small-signal measurements using an ideal analytical model to show the validity of the large-signal approach. In addition to the excellent agreement obtained with the small-signal results, the needed number of measurements was found to be reduced from N^2 to N times while obtaining the same intrinsic voltage coverage. However, the time-consuming tuner characterization and Smith chart sweeping required in passive load–pull or the large number of amplitude and phase sweep measurements in the active load–pull system still strongly impacts the model development cycle. Note that an even larger number of measurements is required for more advanced models [9] that model the dynamics of traps and thermal effects.

Manuscript received August 14, 2013; revised December 05, 2013; accepted December 09, 2013. Date of publication January 15, 2014; date of current version March 03, 2014. This work was supported in part by the National Science Foundation (NSF) under Grant ECS 1129013.

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Digital Object Identifier 10.1109/TMTT.2014.2298372

In this paper, we present a measurement-based quasi-static nonlinear model for an SOS-MOSFET whose intrinsic nonlinear charges and current sources are extracted and verified from large-signal measurements performed using the real-time active load–pull technique (RTALP) [12], [13]. Since RTALP data typically covers a wide range of device operating points, the nonlinear charge and current sources of the model can be extracted from only a single 10.5-ms modulation large-signal measurement with an LSNA. Further, by directly comparing the measured and modeled load-lines, the proposed methodology will allow for both fast model extraction and verification procedures.

This paper is organized as follows. In Section II and the Appendix, the supportive theory for the ANN modeling and the RTALP measurements are presented. In Section III, the extrinsic parameters of the device are extracted using dummy devices and a modified cold FET technique. In Section IV-A, the ANN modeling is applied to the RTALP large-signal RF measurements. The performance of the ANN model when the FET *IV* and charges are extracted separately and simultaneously will then be presented. In Section IV-B, the FET model is extended to explicitly include the parasitic bipolar junction transistor (P-BJT) of the SOS-MOSFET so as to better account for the associated low-frequency memory effects and yield a model with improved accuracy. Both linear and nonlinear bipolar junction transistor (BJT) models based on different model assumptions are extracted and compared. The extrapolation capability of the model for different loads and power levels are also investigated. Finally, this paper concludes with a summary of the achievements reported in Section V.

II. Supportive Theory

A. ANN for Displacement Current

The ANN will be used in this work for representing the voltage dependence of the charges and current sources associated with the gate and drain of the SOS-MOSFET. ANN models are trained for the desired output (e.g., drain current) from various inputs (e.g., gate, drain voltages, and time derivative of voltages) by minimizing an error of cost function [14], [15]. A detailed explanation on the general ANN algorithm and cost function is presented in the Appendix.

Let us consider the intrinsic gate current. In the general case, the intrinsic gate current includes both conduction and displacement currents

$$i_G(t) = I_G\left(v_{\rm GS}(t), v_{\rm DS}(t)\right) + i_{G,\rm disp}(t) \tag{1}$$

where I_G is the dc gate current and $i_{G,\rm disp}$ is the displacement current defined as

$$i_{G,\rm disp}(t) = \frac{dQ_G\left(v_{\rm GS}(t), v_{\rm DS}(t)\right)}{dt} = C_{gg}\frac{dv_{\rm GS}}{dt} + C_{gd}\frac{dv_{\rm DS}}{dt}. \tag{2}$$

If the dc gate current I_G has been characterized separately, the instantaneous displacement current can be obtained using $i_{G,\rm disp}(t) = i_G(t) - I_G(v_{\rm GS}(t), v_{\rm DS}(t))$.

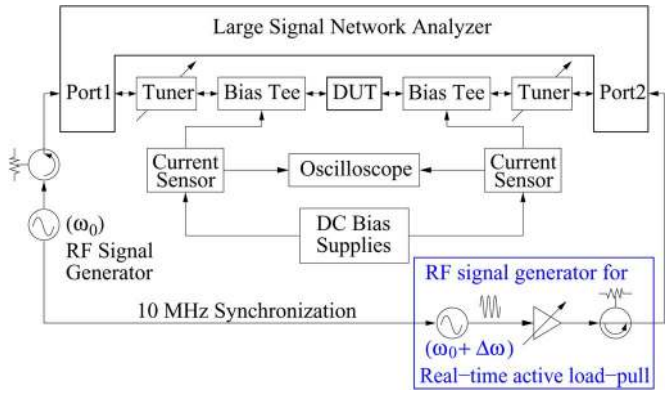


Fig. 1. Real-time active load–pull system testbed.

To integrate the displacement current $i_{G,\rm disp}$ and obtain the gate charge Q_G, we need to minimize the following cost function (see the Appendix):

$$\begin{aligned} E_G &= \left(i_{G,\rm disp} - i_{G,\rm disp,ANN}\right)^2 \\ &= \left(i_{G,\rm disp} - \left[\frac{dv_{\rm GS}}{dt}\cdot\Delta b_{31} + \frac{dv_{\rm DS}}{dt}\cdot\Delta b_{32}\right]\right)^2. \end{aligned} \tag{3}$$

In (3), Δb_{31} and Δb_{32} are the first derivatives of the ANN output $b_3 = Q_G$ (third layer) with respect to the network $v_{\rm GS}$ and $v_{\rm DS}$, inputs (1) and (2), respectively. The ANN Jacobian, which is required for the resilient back propagation (RPROP) [16] used for the extraction of the ANN of the charge from the displacement current, is presented in the Appendix for a three-layer ANN. The cost function for the general case where the drain charge is extracted simultaneously with the drain conduction current is also presented in the Appendix.

B. Time-Domain Reconstruction for Real-Time ALP

The RTALP testbed used to characterize the device is shown in Fig. 1. The RF voltage and current waveforms at port i are given by

$$v_i(t) = a_{i,\rm total}(t) + b_{i,\rm total}(t) \tag{4}$$

$$i_i(t) = \frac{\left[a_{i,\rm total}(t) - b_{i,\rm total}(t)\right]}{50} \tag{5}$$

where the time-domain incident $a_{i,\rm total}(t)$ and reflected $b_{i,\rm total}(t)$ waveforms can be reconstructed from the measured frequency domain complex waves $a_i(n\omega_0 + p\Delta\omega)$ and $b_i(n\omega_0 + p\Delta\omega)$ measured by the LSNA using

$$a_{i,\rm total}(t) = \sum_{n=1}^{N}\sum_{p=-\rm SSB}^{\rm SSB} \mathrm{Re}\left[a_i(n\omega_0 + p\Delta\omega)e^{j(n\omega_0+p\Delta\omega)t}\right] \tag{6}$$

$$b_{i,\rm total}(t) = \sum_{n=1}^{N}\sum_{p=-\rm SSB}^{\rm SSB} \mathrm{Re}\left[b_i(n\omega_0 + p\Delta\omega)e^{j(n\omega_0+p\Delta\omega)t}\right]. \tag{7}$$

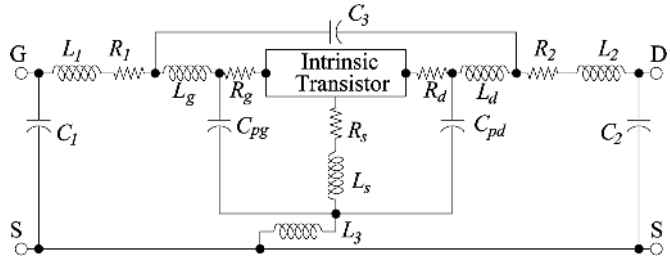


Fig. 2. Circuit schematic of a common-source FET and it parasitic networks for on-wafer measurement.

The time-varying reflection coefficients at the nth harmonic can then be extracted using

$$\Gamma_L(n\omega_0,t)=\frac{\sum_{p=-\mathrm{SSB}}^{\mathrm{SSB}} a_2(n\omega_0+p\Delta\omega)e^{jp\Delta\omega t}}{\sum_{p=-\mathrm{SSB}}^{\mathrm{SSB}} b_2(n\omega_0+p\Delta\omega)e^{jp\Delta\omega t}} \tag{8}$$

The fundamental RF output power at the output is also calculated by

$$P_{\mathrm{out}}(\omega_0,t)=-\frac{1}{2}\sum_{p=-\mathrm{SSB}}^{\mathrm{SSB}}\sum_{-\mathrm{SSB}}^{\mathrm{SSB}}\Big(v_2(\omega_0+p\Delta\omega) \times i_2^*(\omega_0+q\Delta\omega)e^{j(p-q)\Delta\omega t}\Big). \tag{9}$$

III. Extrinsic Parasitics Extraction

Fig. 2 shows the device structure including the intrinsic transistor, parasitics, and parasitic network for on-wafer measurements. To get access to the reference plane of the intrinsic transistor, all the parasitics shown in Fig. 2 were extracted in two separate steps, as described below. In the first step, the parasitics in the outer most layer $C_{1,2,3}$, $L_{1,2,3}$, and $R_{1,2}$ are extracted by measuring the S-parameters of dummy structures that were fabricated on the same wafer as the tested devices. Next, in the second step, using the extracted parasitics obtained in the first step, the remaining device parasitics $C_{pg,pd}$, $L_{g,s,d}$, and $R_{g,s,d}$ are extracted using a nonlinear least square method starting from physical estimated values.

The method used for this second extrinsic element extraction is the cold-FET [17], [18]. First, the device is biased with $V_{\mathrm{DS}}=0$ V so that there be no dc current in the channel. The gate voltage V_{GS} is then biased below and above the threshold voltage V_T and small-signal S-parameter measurements are performed for both conditions. Typically the small-signal equivalent circuit can be simplified sufficiently to enable one to unambiguously identify the various elements. In our particular case, we use the more rigorous circuit model provided by the FET wave-equation theory [19] for $V_{\mathrm{DS}}=0$ and $V_{\mathrm{GS}}>V_T$. Fig. 3 shows the fitted and measured S-parameter results. The extracted data are summarized in Table I.

Once all the parasitics are extracted, the intrinsic transistor model can be developed from the de-embedded large-signal measured data.

IV. Modeling the Intrinsic Transistor

The voltage-controlled gate charge and current sources and the voltage-controlled drain charge and current sources used for the intrinsic transistor are shown in Fig. 4. These charge and current sources are controlled by the instantaneous voltages v_{GS} and v_{DS}. Therefore, the total currents in the gate and drain sides are

$$i_G(t)=I_G\left(v_{\mathrm{GS}}(t),v_{\mathrm{DS}}(t)\right)+\frac{d}{dt}Q_G\left(v_{\mathrm{GS}}(t),v_{\mathrm{DS}}(t)\right) \tag{10}$$

$$i_D(t)=I_D\left(v_{\mathrm{GS}}(t),v_{\mathrm{DS}}(t)\right)+\frac{d}{dt}Q_D\left(v_{\mathrm{GS}}(t),v_{\mathrm{DS}}(t)\right). \tag{11}$$

Typically, the conduction current on the gate side is negligible and ignored due to insulating oxide between the gate and channel in SOS-MOSFETs. Therefore, only Q_G, Q_D, and I_D will be investigated for the intrinsic transistor such that (10) reduces to

$$i_G(t)=\frac{d}{dt}Q_G\left(v_{\mathrm{GS}}(t),v_{\mathrm{DS}}(t)\right). \tag{12}$$

It is to be noted that for the low gate voltages (≤ 0.8 V) to be considered in the rest of this paper, the dc IV and pulsed IV char-

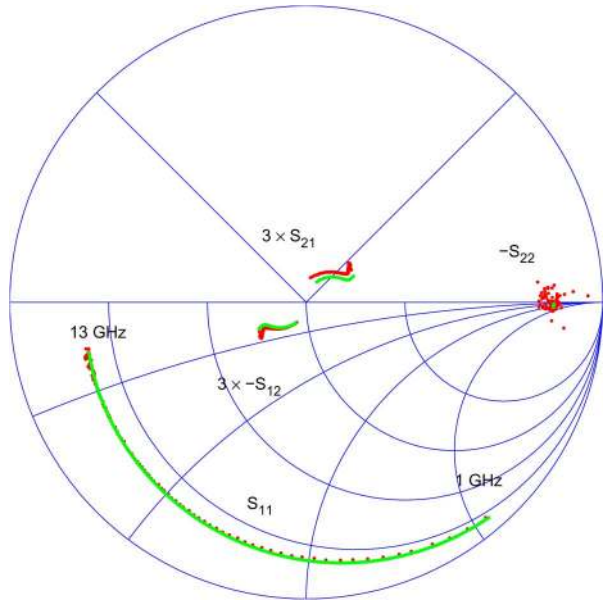


Fig. 3. Measured (red dots in online version) and fitted (green lines in online version) S-parameters for one conduction dc-bias point.

TABLE I
Extracted Parasitics From Dummy Structure and Using Cold-FET Approach

C_1 (fF)	19.0	C_2 (fF)	18.7
C_3 (fF)	3.22	C_{pg} (fF)	66.7
C_{pd} (fF)	175.0	R_1, R_g (Ω)	0.06, 6.5
R_2,R_d (Ω)	0.32, 1.10	R_s (Ω)	0
L_1, L_g (pH)	61.1, 30.0	L_2,L_d (pH)	50.5, 1.35
L_3, L_s (pH)	2.94, 13.1		

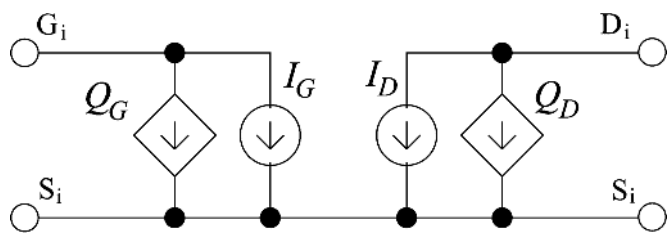


Fig. 4. Quasi-static large-signal intrinsic model with no memory effects.

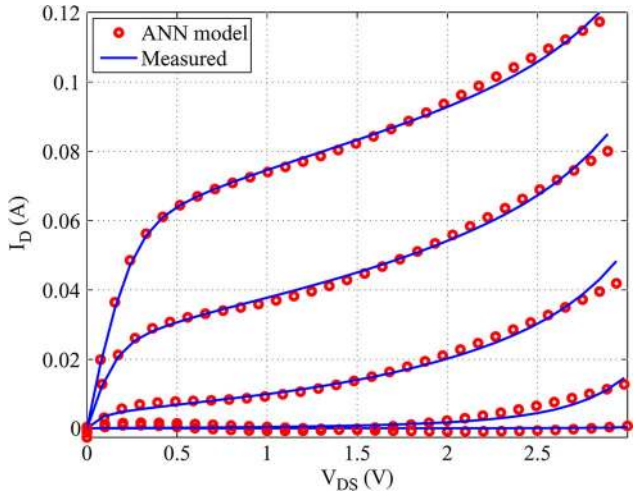


Fig. 5. Comparison of measured (lines) and ANN results (circles) for I_D.

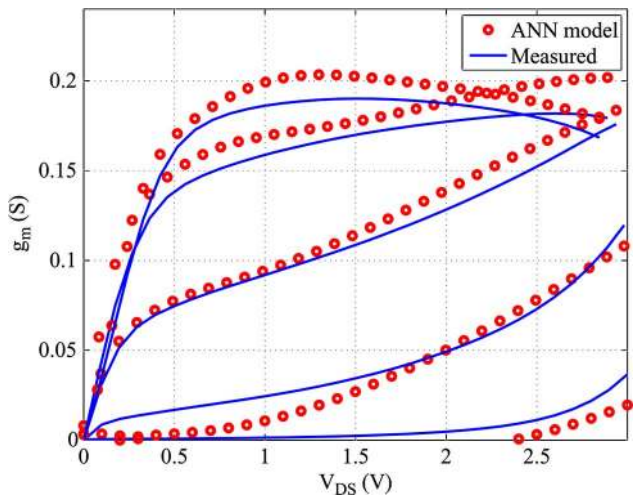


Fig. 6. Comparison of measured (lines) and ANN results (circles) for g_m.

acteristics are similar for the same substrate temperature, as self heating was found to be negligible at low gate voltage drives. The parasitic bipolar in the SOS-MOSFET was then verified to be relatively fast (around 100-MHz cutoff response). Therefore, in the next section, the less noisy dc *IV* characteristics will first be used instead of pulsed-*IV* characteristics for the conduction current model extraction.

A. Quasi-Static Model Extraction

To acquire the drain conduction current source I_D, dc *IV* measurements were performed using a Keithley 4200 in the range of 0–2 V with a 0.1-V step for $V_{\rm gs}$ and 0–3.5 V with a 0.1-V step for $V_{\rm ds}$. The three-layer ANN structure is selected for all state functions and consists of two inputs, 20 nonlinear neurons in the hidden layer, and one linear neuron at the output.

Figs. 5–7 show a comparison of the intrinsic drain current I_D, transconductance g_m, and drain conductance g_d, between the measurement (lines) and ANN model results (circles). As shown in these figures, the drain current as well as its first derivatives g_m and $g_{\rm ds}$ with respect to $V_{\rm GS}$ and $V_{\rm DS}$ compare

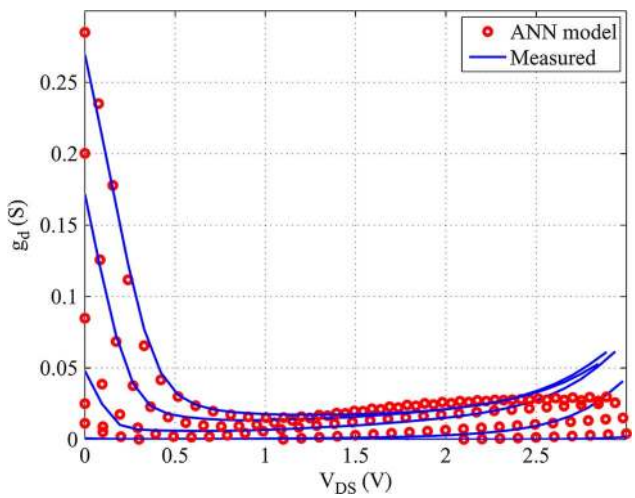


Fig. 7. Comparison of measured (lines) and ANN results (circles) for $g_{\rm ds}$.

well with the measured data. This is achieved by using the same weights for the *IV* and its first derivatives in the ANN error cost function for the accurate prediction of harmonics and intermodulation [14].

The next step is to develop the ANN model for the gate and drain charges. The dynamic load-lines measured by the LSNA in $(v_{\rm GS}, v_{\rm DS})$ space are given in Fig. 8(b). As the swept RF power on the drain side increases, a wider voltage coverage is obtained in RTALP due to larger amplitudes of the load reflection coefficients. One of the advantages of the large-signal RF characterization approach is that its measurement region can extend far beyond the conventional dc operating range of the device such that extreme regions (e.g., breakdown) can be characterized without any device degradation. This holds because the frequency of the excited RF signal is typically above 1 GHz and the instantaneous voltage spends a relatively short time (ns scale) in the high-voltage region. Furthermore, the dynamic large-signal data used for the model extraction shown in Fig. 8 is measured from only a single 10.5 ms (2^{18} IF data sampled at 25 MHz) LSNA modulation measurement thanks to the real-time tuning of RTALP. In previously reported large-signal approaches, such as passive load–pull or active load–pull systems, many different measurements from various load impedances, and RF power, and dc-bias conditions were necessary to obtain the same coverage. In this paper, the 12-dBm (magenta in online version) data is used for the model extraction in order to avoid the potentially unstable region where $|\Gamma_{\rm IN}| > 1$.

Fig. 9 compares the LSNA and model simulation results for the drain load-lines obtained at six different complex load impedances. The results shown provide a visual evaluation of the extraction accuracy. It is seen that the fit of the load-line is not optimal, motivating the need for further improvements.

Note that in this preliminary approach, the conduction and displacement current sources were extracted separately. First the ANN for the measured dc current and intrinsic voltages was extracted and next the ANN for the drain charge was extracted from the displacement current $i_D(t) - I_D(v_{\rm GS}(t), v_{\rm DS}(t))$ obtained from the 12-dBm RTALP large-signal RF measurement.

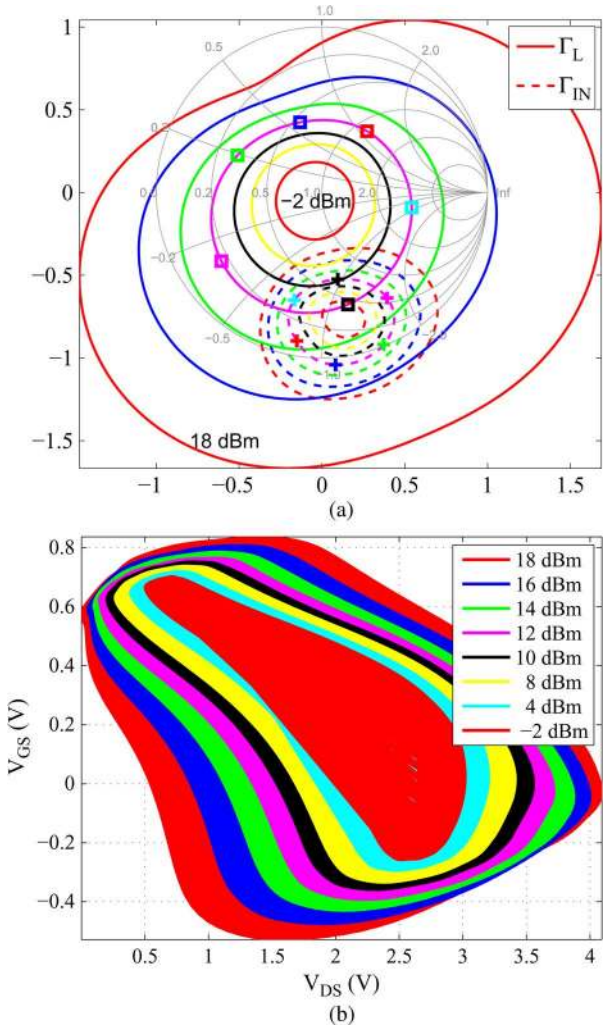


Fig. 8. (a) Loci of the swept Γ_L (solid line) in RTALP for eight different RF power levels injected on the drain side. Also shown is the device stability Γ_{IN} (dashed line). (b) Corresponding dynamic load-lines of $v_{GS}(t)$ versus $v_{DS}(t)$ for the eight RTALP measurements running from −2 to 18 dBm.

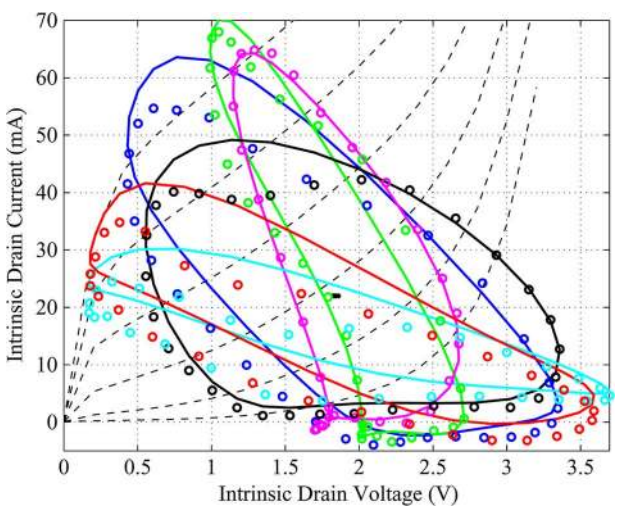


Fig. 9. Dynamic load-lines at six different load impedances obtained from the measurement (lines) and the model (circles). The intrinsic *IV*s (dashed lines) are extracted from the dc *IV* measurement. The associated loads $\Gamma_L(\omega)$ (squares) and $\Gamma_{IN}(\omega)$ (crosses) are shown in Fig. 8(a).

Alternatively, the ANN networks for the *IV* characteristics and the drain charges can be simultaneously extracted from the same 12-dBm RTALP large-signal RF data without using the dc *IV* data. In that case, the model used for the drain current reduces to

$$i_D(t) = I_{D,\text{trans}}(v_{GS}, v_{DS}, V_{GS}, V_{DS}) + \frac{d}{dt}Q_D(v_{GS}, v_{DS}) \tag{13}$$

where $I_{D,\text{trans}}(v_{GS}, v_{DS}, V_{GS}, V_{DS})$ is the transient *IV* characteristics holding for the dc bias (V_{GS}, V_{DS}). This is achieved by using an ANN error cost functions combining the conduction and displacement parts, as shown in the Appendix.

TABLE II
RMS COMPARISON

	Extraction 12 dBm	Prediction Case 1 10 dBm	Prediction Case 2 14 dBm
Separate extraction of FET charge and DC IV	6.55	5.25	9.18
Simultaneous extraction of FET charge and RF IV	3.08	3.69	5.65
Simultaneous extraction of FET and linearized BJT	2.77	3.65	5.44
Simultaneous extraction of FET and non-linear BJT IV	3.53	3.48	6.03

Using this simultaneous ANN extraction of the *IV* and charges from the same RF large-signal data, an improved fitting can be obtained. To quantitatively verify it, Table II compares the root mean square error (rms) values calculated from 100 different drain load-lines when the *IV* and charge ANNs are extracted separately and simultaneously. Note that different drain load-lines were also used in the evaluation of the rms for the extraction case. As is shown in Table II, the rms is decreased by a factor of 2 in the 12-dBm verification case, as well as exhibits a substantial improvement for both the 10-dBm (Case 1) and 14-dBm (Case 2) prediction cases. The improvement is due to the fact that the dc *IV* characteristics used for the simultaneously ANN extraction implicitly accounts for the memory effects associated with the P-BJT present in the SOS-MOSFET. This improvement further suggests modifications of the model, which are explored in the next section.

B. Quasi-Static Model Extraction Including Memory Effect

In the previous section, a quasi-static model with no explicit memory effects was developed and compared between different extraction approaches. Even though SOS-MOSFET devices used in this study exhibit less thermal effects than GaN HEMTs and negligible trapping effects, they feature a different memory effect mechanism associated with their P-BJTs. This parasitic bipolar transistor is activated by the hole component of the drain current generated by impact ionization at high drain voltages. However, the P-BJT is a large device that does not respond at GHz frequencies and is thus only activated by the slower varying baseband component $i_{D,\text{RF}}(BB)$ and V_{DS} of the FET drain current $i_{D,\text{RF}}$ (RF-*IV*) and the drain voltage v_{DS}, respectively. Note that memory effects were thus implicitly accounted for when simultaneously extracting the RF *IV* and the FET charge instead of using the dc *IV*. However, the variation in time at baseband of the bias $(V_{GS}(t), V_{DS}(t))$ during RTALP

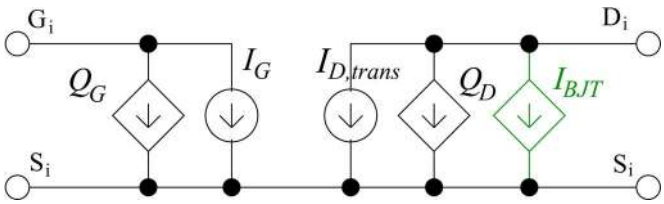


Fig. 10. Quasi-static large-signal intrinsic model with the parasitic BJT.

was not accounted for. To account for this effect and better include this unwanted P-BJT into the model, the drain current is modified, as indicated in Fig. 10, leading to the equation

$$I_{D,\mathrm{trans}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}, V_{\mathrm{GS}}, V_{\mathrm{DS}}) = I_{D,\mathrm{RF}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) + I_{\mathrm{BJT}}\left(I_{D,\mathrm{RF}}(\mathrm{BB}), V_{\mathrm{DS}}\right) \quad (14)$$

where $I_{\mathrm{BJT}}(I_{D,\mathrm{RF}}(\mathrm{BB}), V_{\mathrm{DS}})$ is the baseband BJT current and $I_{D,\mathrm{RF}}(v_{\mathrm{GS}}, v_{\mathrm{DS}})$ is the RF *IV*, which is assumed for simplicity not to be a function of the dc bias $(V_{\mathrm{GS}}, V_{\mathrm{DS}})$.

Note that since the baseband current $I_{D,\mathrm{RF}}(\mathrm{BB})$ of the RF FET *IV* $I_{D,\mathrm{RF}}$ is not available from the measurement, the baseband current $I_D(\mathrm{BB})$ of the total intrinsic drain current i_D measured during RTALP is used instead. Once the model extraction has been completed, the mapping between $I_D(\mathrm{BB})$ and $I_{D,\mathrm{RF},BB}$ is available and one can return to the original $I_{D,\mathrm{RF},BB}$ formulation if desired.

Two approaches are used to model the P-BJT current. In the first method, the P-BJT is assumed to be a linear function of the slowly varying baseband drain current and drain voltage induced by the real-time tuning of RTALP,

$$I_{\mathrm{BJT}}(t) = I_{\mathrm{BJT},0} \quad (15)$$

$$+\beta_{m,\mathrm{BJT}} I_{D,\mathrm{RF}}(\mathrm{BB})(t) + G_{d,\mathrm{BJT}}\left[V_{\mathrm{DS}}(t) - V_{\mathrm{DS}}(\mathrm{DC})\right] \quad (16)$$

This linear expansion is well justified by the fact that the bias point varies little during RTALP, as is demonstrated by its locus in Fig. 12(a) (black dots around 1.7 V and 22 mA). A single-layer ANN structure with a linear function is thus implemented and then added to the error cost function.

In the second approach, the full nonlinear characteristics of the P-JBT is represented by a separate ANN with $c_3 = I_{\mathrm{BJT}}$ (in the Appendix) and extracted by including the measured SOS-MOSFET dc *IV* beside the RF load-line data used for the ANN extraction. Indeed at dc or at low frequencies (<100 MHz), the dc *IV* of the SOS-MOSFET drain current includes contributions from both the FET and BJT dc characteristics

$$I_D(V_{\mathrm{GS}}, V_{\mathrm{DS}}) = I_{D,\mathrm{RF}}(V_{\mathrm{GS}}, V_{\mathrm{DS}}) + I_{\mathrm{BJT}}(I_{D,\mathrm{RF}}, V_{\mathrm{DS}}). \quad (17)$$

The necessary update of the ANN cost function to include the BJT contribution $(c_3 = I_{\mathrm{BJT}})$ is discussed in the Appendix. The calculation of the ANN Jacobian for the BJT is similar to that of the dc drain current.

Fig. 11 shows the measured (red circles in online version) and simulated (black lines) dc *IV* together with the RF *IV* (blue lines in online version) contributing to the RF and baseband drain conduction currents and the nonlinear P-BJT *IV* characteristic (purple lines in online version) contributing solely

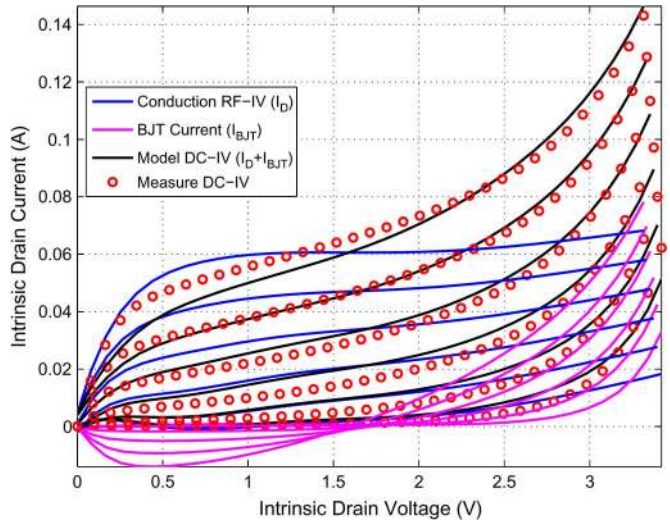
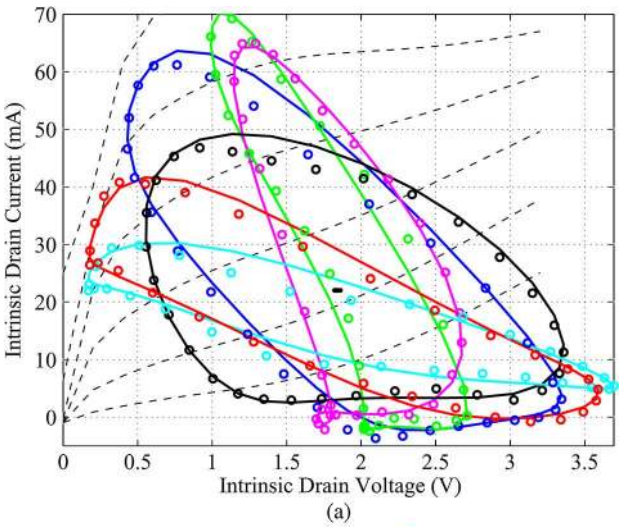
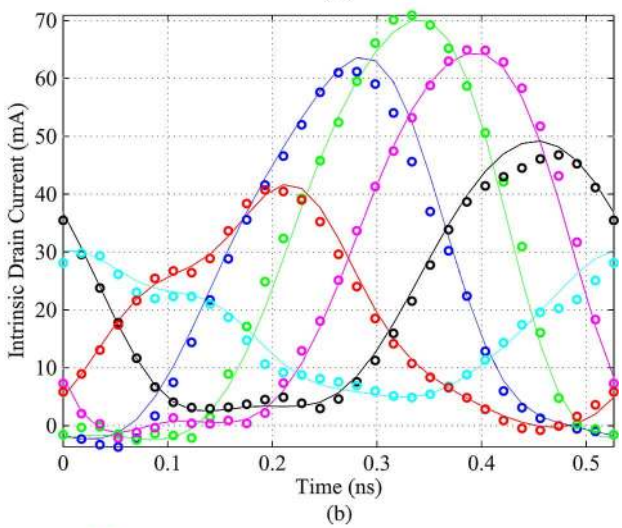


Fig. 11. Measured (red circles in online version) and reconstructed (black lines) dc *IV* together with the RF *IV* (blue lines in online version) and nonlinear P-BJT *IV* characteristic (purple lines in online version) contributing, respectively, to the RF and baseband drain conduction currents.

to the baseband drain conduction current. In the high drain voltage region, impact ionization brings about a substantial drain current increase due to the high electric field in the channel. In this model, breakdown is controlled by the slow P-BJT that accounts for the fact that breakdown occurs at lower V_{DS} (2.5–3 V) in the dc *IV*s (black line) compared to the RF *IV*s (blue line in online version) where no breakdown is detected up to 3.5 V. To account for this feature, the extracted P-BJT is shown to exhibit an exponentially increase in the current at high V_{DS} such that the total dc *IV* from the model exhibits a reasonably good agreement with the measured dc *IV*. However, the negative P-BJT currents at low V_{DS} voltages gives a measure of the range of validity of this model. Presumably, the charge distribution in the SOS-MOSFET is also affected by the impact ionization under high bias such that the assumption of RF *IV* characteristics $I_{D,\mathrm{RF}}(v_{\mathrm{GS}}, v_{\mathrm{DS}})$ that are independent of the bias points $(V_{\mathrm{GS}}, V_{\mathrm{DS}})$ might not be applicable to lower values of V_{DS}. Indeed, as we shall see, the less ambitious perturbative model that only models the BJT for the small variations in the dc-bias points $(V_{\mathrm{GS}}(t), V_{\mathrm{DS}}(t))$ during RTALP (instead of the full *IV*s) will noticeably outperform the nonlinear BJT model in terms of accuracy for the bias-considered. Nonetheless, the partitioning of the SOS-MOSFET in a fast RF-MOSFET and a slow nonlinear BJT subcomponents brings about some valuable insights in the complexity of memory effects in SOS-MOSFETs.

Table II compares the rms obtained over 100 different drain load-lines for the linear and nonlinear P-BJT models with the rms for the two extraction models reported in the previous section. The rms exhibits a noticeable improvement for both the verification and prediction cases for the linearized BJT model. A mixed results of small improvement and small degradation is, however, observed in both verification and prediction when using the nonlinear BJT model. The degradation in prediction for Case 2 may be due to the fact that the BJT model slightly exaggerates the impact of the drain baseband currents at higher power (14 dBm).





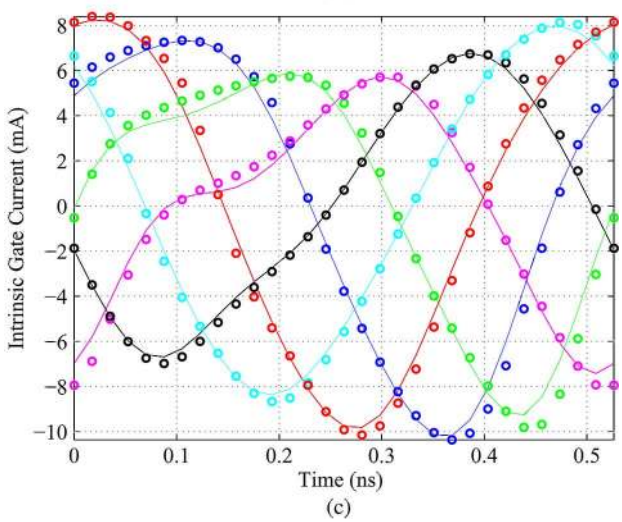
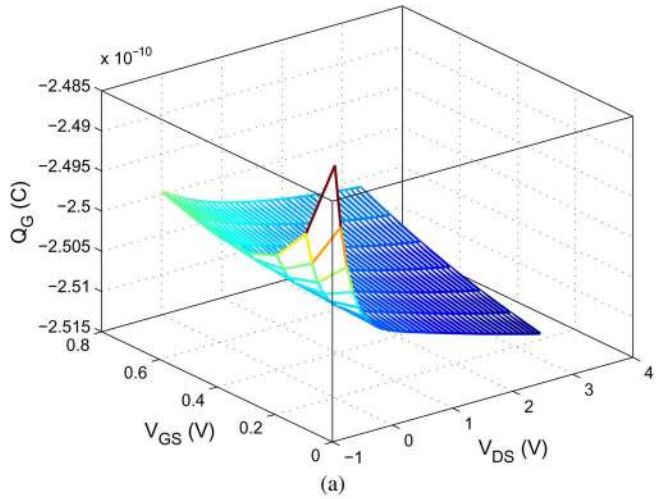


Fig. 12. (a) Dynamic load-lines at six different load impedances obtained from the measurement (lines) and the model (circles). The intrinsic RF-*IV*s (dashed lines) and the linear P-BJT response are extracted simultaneously from a single RTALP measurement. (b) and (c) Associated gate and drain current waveforms for these six load-lines. The associated loads $\Gamma_L(\omega)$ (square) and $\Gamma_{\rm IN}(\omega)$ (crosses) are shown on Fig. 8(a).

Fig. 12(a) compares the LSNA load-line measurement and model simulation results with the linear P-BJT implementation drain currents waveforms for the same six different complex load impedances used in Fig. 9. When comparing Fig. 9 and 12(a), a noticeable improvement is observed in all of the six different load-lines as predicted by the improvement in the rms figure-of-merit. The associated waveforms for the gate and drain currents are also shown in Fig. 12(b) and (c) for completeness.



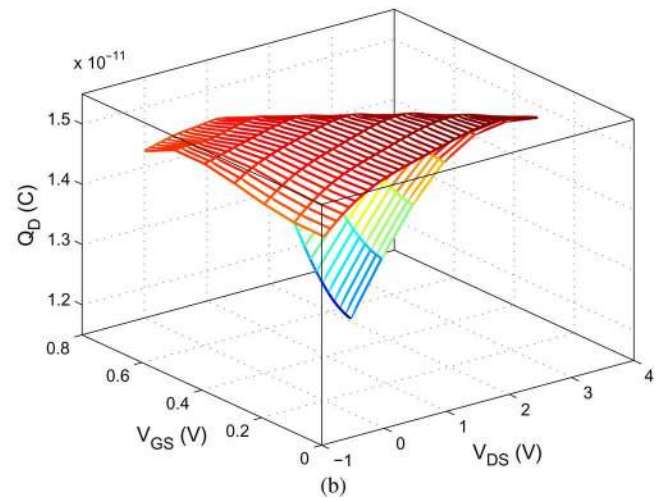


Fig. 13. Extracted: (a) Q_G and (b) Q_D from a single large-signal modulated RF measurement.

The charges Q_G and Q_D that are simultaneously extracted from the same measurement are presented in Fig. 13. As mentioned earlier, a graceful prediction of the gate and drain charges outside the data extraction region is observed thanks to the good ANN extrapolation capability compared to B-spline fitting (not reported here).

To further test the capability of this model, Figs. 14–16 present a comparison of the modeled and measured results for the input power $P_{\rm in}$, output power $P_{\rm out}$, dc dissipated power $P_{\rm dc}$, and power-added efficiency (PAE) at 20 different complex load impedances. Note that the 20 different points were selected from the same single (12 dBm) RTALP measurement, but these RTALP measurement data were not used in the ANN training. As shown in these figures, all the modeled results and most of the measured results are approximately following a sinusoidal shape, as the phase of the reflection coefficient $\Gamma_L(\omega)$ is swept by the real-time tuning along its closed contour.

Finally, a comparison of the model large-signal prediction with respect to measured output power and PAE on the Smith

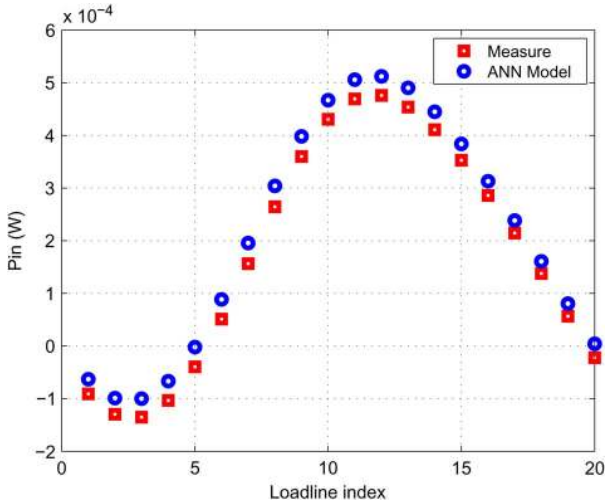


Fig. 14. Measured (red squares in online version) and modeled (blue circles in online version) input power comparison at 20 different complex load impedances.

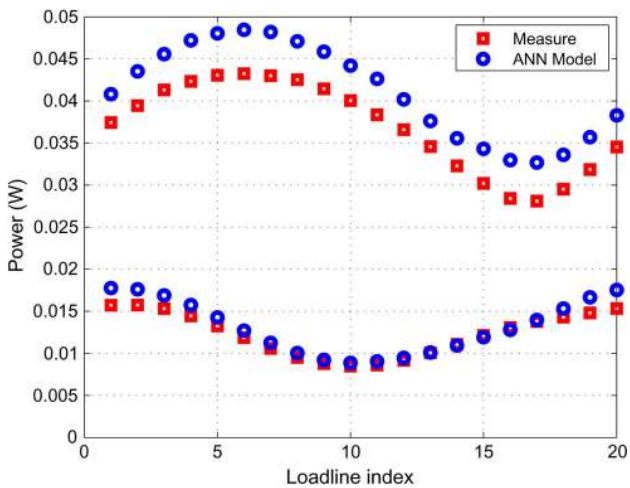


Fig. 15. Measured (red squares in online version) and modeled (blue circles in online version) $P_{\rm dc}$ and $P_{\rm out}$ comparison at 20 different complex load impedances.

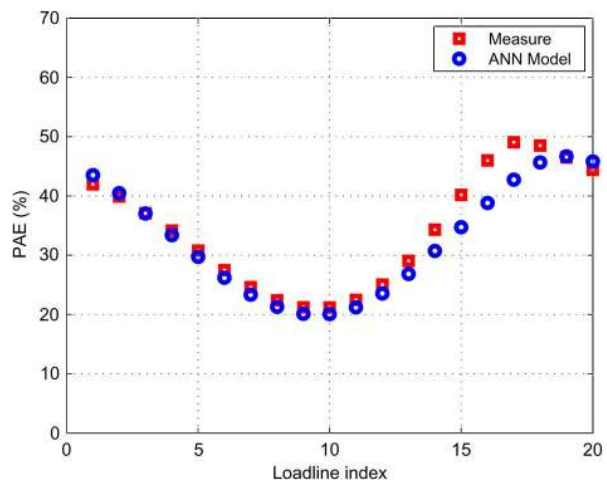


Fig. 16. Measured (red squares in online version) and modeled (blue circles in online version) PAE comparison at 20 different complex load impedances.

chart is presented in Figs. 17 and 18. The model agrees reasonably well with the measured output power and PAE. Note that the ANN model was only extracted using the 12-dBm

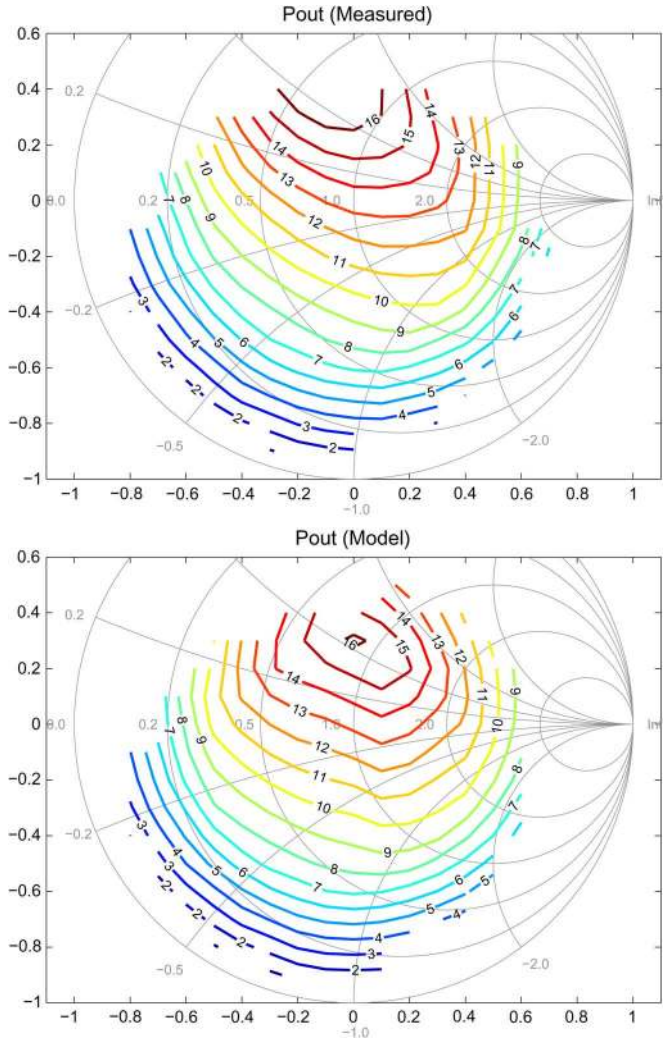


Fig. 17. Measured (*top*) and simulated (*bottom*) output power contours.

$\Gamma_L contour$, whereas the verification contour plots are generated using 10, 12, and 14 dBm of the Smith chart [see Fig. 8(a)]. The optimum load impedance points for output powers and PAEs located at different load points under this modulated RF measurement are reasonably well predicted. This indicates that the proposed model reflects well on the device behavior at both RF and low frequencies.

V. Conclusion

A measurement-based quasi-static nonlinear model relying on ANN modeling has been presented for an SOS-MOSFET exhibiting strong parasitic bipolar transistor memory effects. A rapid and convenient *IV* and charge extraction based on a single (10.5 ms) large-signal modulated RF measurement has been demonstrated. The extraction makes use of the unique characteristics of real-time active load–pull, which maps a wide range of gate and drain voltages in a single-modulation LSNA measurement. A new ANN error cost function was also introduced and implemented for the simultaneous ANN model extraction of the conduction current, charge sources, and parasitic bipolar transistor current from the RTALP large-signal RF measurements. Improved results were achieved when simultaneous extracting the FET *IV* and charge from the same large-signal RF

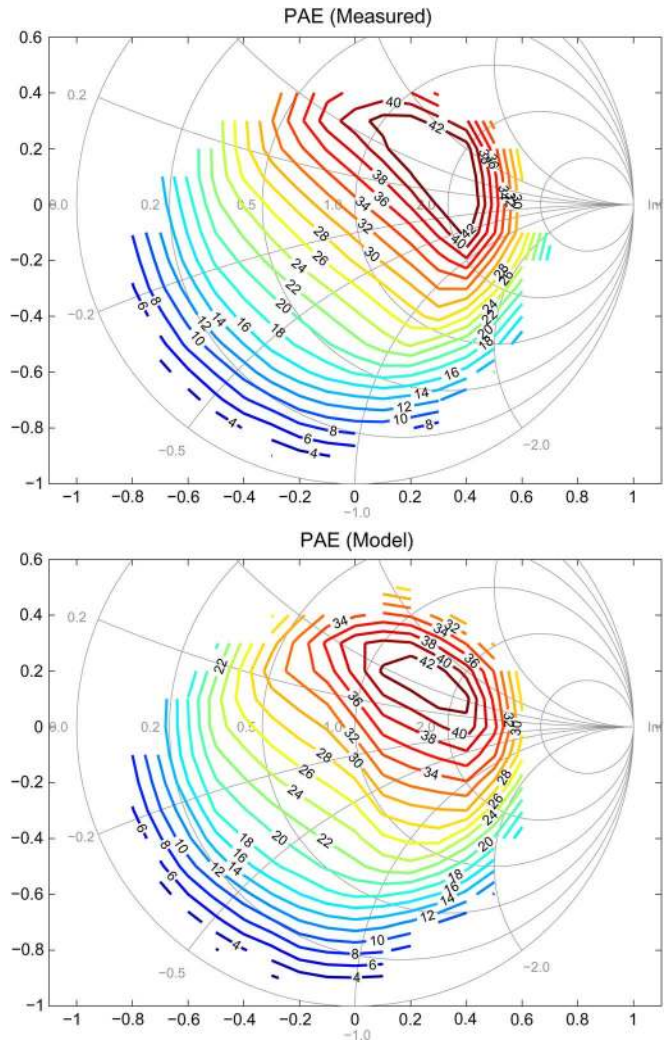


Fig. 18. Measured (*top*) and simulated (*bottom*) PAE contours.

data without using the dc *IV* characteristics. Reasonable parasitics bipolar transistor characteristics were also extracted at high bias, which explained the lower $V_{\rm DS}$ breakdown at dc compared to RF. The ANN model was also implemented in ADS and verified to yield the same results as in the MATLAB simulations.

To validate the proposed methodology, the load-line at different complex load impedances were compared and rms as low as 2.77% in extraction and 3.65% in prediction were obtained verifying the reasonable accuracy achieved by the proposed model topology and extraction methodology.

Furthermore, the similar sinusoidal trend obtained in the comparison of the variation of the PAE, dc power, and output RF power with the RTALP phase sweeping for the measured and modeled results demonstrated the ability of the proposed model to incorporate the low-frequency dispersions exhibited by the device into the RF large-signal model.

The model presented in this paper focused on presenting an RF large-signal model for SOS MOSFETs accounting for the quasi-static response of its relatively fast parasitics bipolar transistor. Further work is still needed to characterize the dynamics of the parasitics bipolar transistor at very high modulation frequencies. For this purpose, RTALP measurements with different sweeping/offset frequencies could be used as a probe of the P-BJT frequency response. Pulsed-RTALP [20], which is immune from low-frequency memory effects, could then provide a reference measurement for studying such dynamic effects.

APPENDIX
GENERAL DESCRIPTION FOR MODIFIED ERROR COST FUNCTION

ANNs are known to be a useful tool for various simulation fields such as electromagnetic (EM), signal integrity, transistor electrical parameter, and more [15]. If an analytical model, which is typically computationally expensive, is not available, the ANN approach especially provides an alternative solution with less computational price.

The ANN structure used in this paper consists of three different layers: the input, hidden, and output layers, which are interconnected by the two different weights $\mathbf{w}_1$ and $\mathbf{w}_2$, as shown in Fig. 19. The two different weights, therefore, need to be updated during the iterative extraction (back propagation) by comparing the past and present value of the output (drain current or P-BJT current). This is done with the help of the Jacobians of the cost function, which are defined as the derivative of the ANN cost function with respect to the weights vectors $\mathbf{w}_1$ and $\mathbf{w}_2$, respectively.

The most general cost function used in this work is of the form

$$E_D = \frac{1}{P}\sum_{i=1}^{P} e_D^2(i)$$

with

$$e_D(i) = i_D(i) - i_{D,\rm ANN}$$

and

$$i_{D,\rm ANN} = \left\{ a_3(i) + \left[\frac{dv_{\rm GS}(i)}{dt} \cdot \Delta b_{31} + \frac{dv_{\rm DS}(i)}{dt} \cdot \Delta b_{32} \right] + c_3(i) \right\}$$

where i is used to indicate the time sampling at time t_i.

E is the error cost functions for the sum of drain conduction, displacement, and P-BJT currents. Also, $i_D(i)$ is the LSNA measured drain current, and $a_3 = I_D$, $b_3 = Q_D$, and $c_3 = I_{\rm BJT}$ are the desired ANN outputs from the conduction current, FET charge, and P-BJT conduction current, respectively.

A general technique for the derivation of the Jacobians needed for the extraction of arbitrary neural networks from a function and its derivatives was first reported in [15]. This was done with the introduction of adjoint neural networks. As shown in Fig. 19, the original neural network algorithm can be augmented to calculate the derivatives. In the rest of this Appendix, the expressions derived for the Jacobians for the above error function and the neural network used are given to facilitate the reproduction of this work.

A. Backpropagation Algorithm for the Conduction Current

The output layer conduction current Jacobian, which is the derivative of the error cost function E_D with respect to w_2^a,

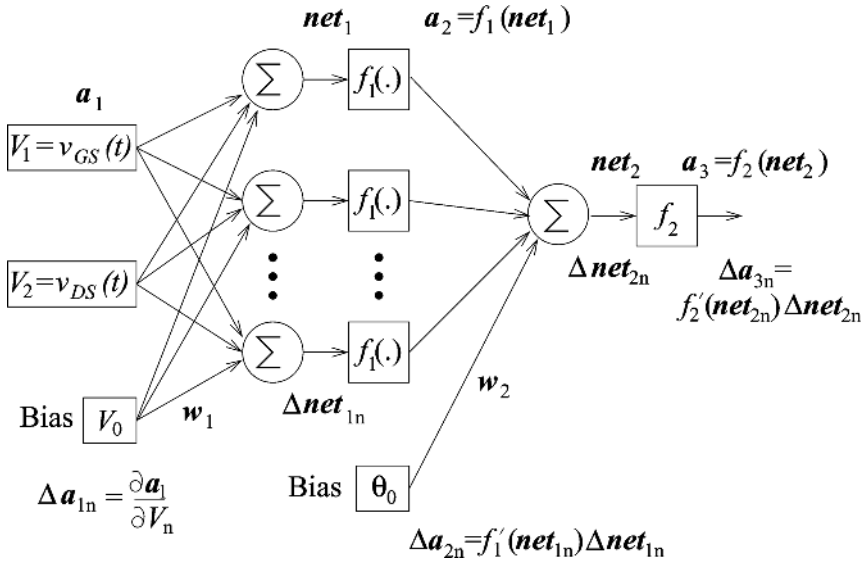


Fig. 19. ANN diagram.

is given by

$$J_{w_2^a}(j) = \frac{\partial E_D}{\partial w_2^a(j)} = -\frac{2}{P}\sum_{i=1}^{P}\delta_2(i)a_2(i,j)$$

where $\delta_2(i) = e_D(i)f_2'[\mathrm{net}_2(i)]$.

The hidden layer conduction current Jacobian, which is the derivative of the error cost function E_D with respect to $w_1^a(j,k)$, is given by

$$J_{w_1^a}(j,k) = \frac{\partial E_D}{\partial w_1^a(j,k)} = -\frac{2}{P}\sum_{i=1}^{P}\delta_1(i,j)a_1(i,k)$$

where $\delta_1(i,j) = \delta_2(i)w_2^a(j)f_1'[\mathrm{net}_1(i,j)]$. The P-BJT current has the same Jacobian derivation as the drain conduction current.

B. Backpropagation Algorithm for Displacement Current

For the displacement current, the first derivatives Δb_{31} and Δb_{32} of the output b_3 with respect to inputs: 1) v_{GS} and 2) v_{DS} is used in the error cost function.

The output layer displacement current Jacobian, which is the derivative of E_D with respect to $w_2^b(j)$, is given by

$$\Delta J_{w_2^b}(j) = \frac{\partial E_D}{\partial w_2^b(j)} = -\frac{2}{P}\sum_{i=1}^{P}\delta_{2d}^A(i)\Delta b_{2d}(i,j) + \delta_{2d}^B(i)b_2(i,j)$$

where

$$\begin{aligned}\delta_{2d}^A(i) &= e_D(i)f_2'\left[\mathrm{net}_2(i)\right]\\ \delta_{2d}^B(i) &= e_D(i)\Delta\mathrm{net}_{2d}(i)f_2''\left[\mathrm{net}_2(i)\right].\end{aligned}$$

The hidden layer displacement current Jacobian, which is the derivative of E_D with respect to $w_1^b(j,k)$, is given by

$$\begin{aligned}\Delta J_{w_1^b}(j,k) &= \frac{\partial E_D}{\partial w_1^b(j,k)}\\ &= -\frac{2}{P}\sum_{i=1}^{P}\delta_{1d}^A(i,j)\Delta b_{1d}(i,k) + \delta_{1d}^B(i,j)b_1(i,k)\end{aligned}$$

where

$$\begin{aligned}\delta_{1d}^A(i,j) &= \delta_{2d}^A(i)w_2^b(j)f_1'\left[\mathrm{net}_1(i,j)\right]\\ \delta_{1d}^B(i,j) &= \delta_{2d}^A(i)w_2^b(j)\Delta\mathrm{net}_{1d}(i,j)f_1''\left[\mathrm{net}_1(i,j)\right]\\ &\quad + \delta_{2d}^B(i)w_2^b(j)f_1'\left[\mathrm{net}_1(i,j)\right].\end{aligned}$$

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