ASIC Design of Reversible Adder and Multiplier

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ABSTRACT
Reversible logic is one of the promising research areas in low power applications such as quantum computing, optical information processing and low power CMOS design. In this paper we present a reversible carry look ahead adder and an array multiplier. The circuits are designed such that they result in less garbage outputs, constant inputs, and less gate count compared to previous existing designs. We also gain better improvements in terms of power and area when compared to conventional adders and multipliers. The implemented designs are simulated using NC launch and synthesized by RTL compiler.

Keywords
Reversible, Garbage constant, Garbage output.

1. INTRODUCTION
Power dissipation is one of the important problems faced now a day in VLSI design [4]. The combinational circuit dissipates $KTlog_2$ [1] Joules of heat for every bit of information to be lasted, irrespective of the technology used .where K is Boltzmann constant and T is temperature. Heat dissipation reduces the life span of the circuits. The information is lost when input bits are not able to recover from the output vectors. Reversible gates naturally take care of heat, since input vectors are uniquely recovered from the output vectors. That is there is one-to-one correspondence between input vectors and output vectors. Each output of the Reversible gates is used once, that is the Reversible circuit is feedback free. Some of the terms related to Reversible logic are [2, 3].

1.1 Garbage Outputs
The output of the Reversible gates which are not used further in the design, the efficient Reversible design must have less garbage bits. It is denoted by letter G in the whole paper.

1.2 Constant Inputs
The inputs of Reversible gates which are assigned to either logic '1' or logic '0',to obtained required Boolean expression. A good design should have minimal constant inputs.

1.3 Quantum Cost
Number of basic 2*2 Reversible gates used to implement required Reversible gates.

For Reversible gates 2*2 gates are the unit gates.

An efficient Reversible gate must have following features:

1. Total garbage outputs in the design as less as possible.

2. Design must be acyclic.

3. Minimization of the Reversible gates and constant inputs.

In following sections the paper organized as follows. In section 2 we propose some of the reversible gates used in the design. Section 3 describes the conventional designs and its reversible implementation. Section 4 presents work carried out, simulation results and comparison of the area and power results. Section 5, 6 discusses the future work conclusions.

2. REVERSIBLE GATES
Feynman gate (FG) [5] is a 2*2 gate shown in Fig 1. It has A, B as input vectors and output vector as

$$P = A \quad (1)$$

$$Q = AB'+A'B \quad (2)$$

And Quantum cost is equal to 2. ⊕ Operation shows the exclusive – or operation between the operands.

Fig 1: 2-input FG gate.

Fredkin gate (FRG) is a 3*3 gate shown in Fig 2. It has A, B and C as input vector and output vector as

$$P = A \quad (3)$$

$$Q = A'B+AC \quad (4)$$

$$R = A'C+AB \quad (5)$$

Quantum cost of FRG gate is 5.

Figure 2: 3-input Fred kin gate.

Fredkin gate (FRG) is a 4*4 gate shown in Fig 3. It has X, A B and C as input vector and output vector as

$$P = X \quad (6)$$

$$Q = AX'+XC \quad (7)$$

$$R = BX'+AX \quad (8)$$

$$S = CX'+BX \quad (9)$$

Fig 3: 4-input Fredkin gate.

Toffoli gate (TG) [6] is a 3*3 gate shown in Fig 4. It has A, B

and C as input vector and output vector as

$$P = A \quad (10)$$

$$Q = B \quad (11)$$

$$R = AB \oplus C \quad (12)$$

Fig 4: 3-input Toffoli gate.

Peres gate (PG) is a 3*3 gate shown in Fig 5. It has A, B and C as input vector and output vector as

$$P = A \quad (13)$$

$$Q = A \oplus B \quad (14)$$

$$R = AB \oplus C \quad (15)$$

Fig 5: 3-input Peres gate.

New gate (NG) is a 3*3 gate shown in Fig 6. It has A, B and C as input vector and output vector as

$$P = A \quad (16)$$

$$Q = AB \oplus C \quad (17)$$

$$R = A'C' \oplus B' \quad (18)$$

Fig 6: 3-input New gate.

3. RELEATED WORK

3.1 Carry look Ahead Adder

In conventional carry look ahead adder carry propagation is eliminated to decrease the delay due to carry propagation. The carry is obtained from the propagating and generating bits. The expressions for generating, propagating bits and carry are

$$G = AB \quad (19)$$

$$P = A - B \quad (20)$$

$$C_i = G + PC_{i-1}. \quad (21)$$

Where C_{i-1} will be the previous carry. For start bits we consider carry bit as 0.C_i be the carry for next operation. The block diagram of conventional Carry Look ahead Adder (CLA) [7, 9] is shown in Fig 7. For implementing carry look ahead adder here we consider 4-input Fredkin gate, 3-input Fredkin gate and FG gate.

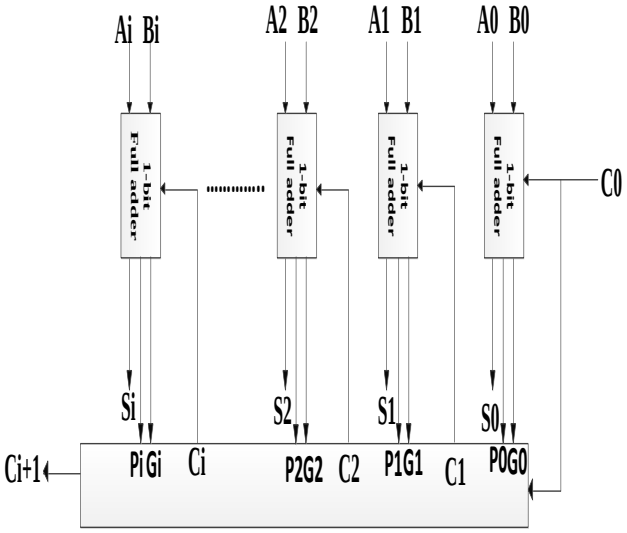

Fig 7: Block Diagram of Conventional CLA.

The Reversible implementation of carry block from propagating and generating bits is shown in Fig 8 with 5 garbage outputs and four constant inputs. By making X=A, A=B, C=0 and D=1 in 4-input Fredkin gate, propagating and generating bits are obtained. The propagating bit and previous is given to 3-input Fredkin gates [10] A=$C_{i-1,}$ B=0 and C=P, we came across result PC_{i-1}. Where P is the propagating input. Now the result PC_{i-1} is given to the Fredkin gate along with the previous carry bit, here we got the next carry input.

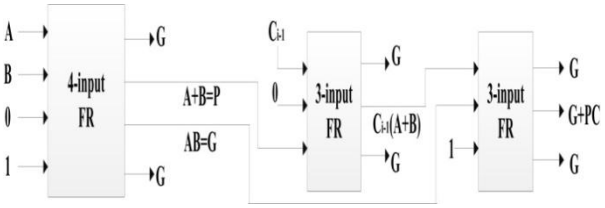

Fig 8: Reversible gate for carry generation.

Next we are going to add the operands by using the two FG gates shown in Fig 9. For first FG gate A=A and B=B given as inputs, the obtained result is given to another FG gate along with carry to obtain A⊕B⊕C_{i-1}.The implemented CLA [11,12]is having less garbage outputs and constant inputs compared to previous design. Power and area report are compared with conventional CLA design.

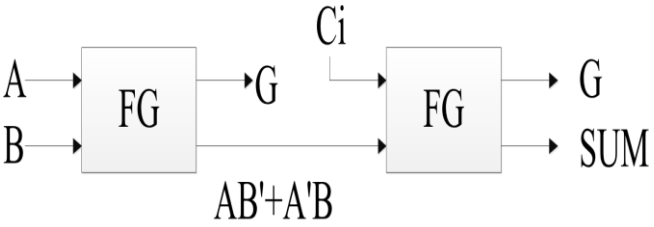

Fig 9: Reversible gate for sum

3.2 Array Multiplier

The array multiplier [8] is carried out by simple shifting and accumulation of partial products. Fig 11.Shows the 8-bit conventional array multiplier. The partial products are added by simple adder.

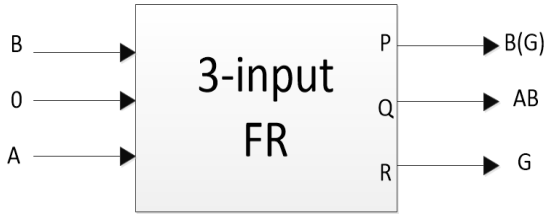

Fig 10: 3-input Fredkin gate.

The Reversible implementation of partial products is using 3-input Fredkin gate is shown in Fig 11. By making A=A, B=0 and C=B we get the partial products as A_iB_i. Obtained partial products are added by using the above implemented carry look ahead adder [13].

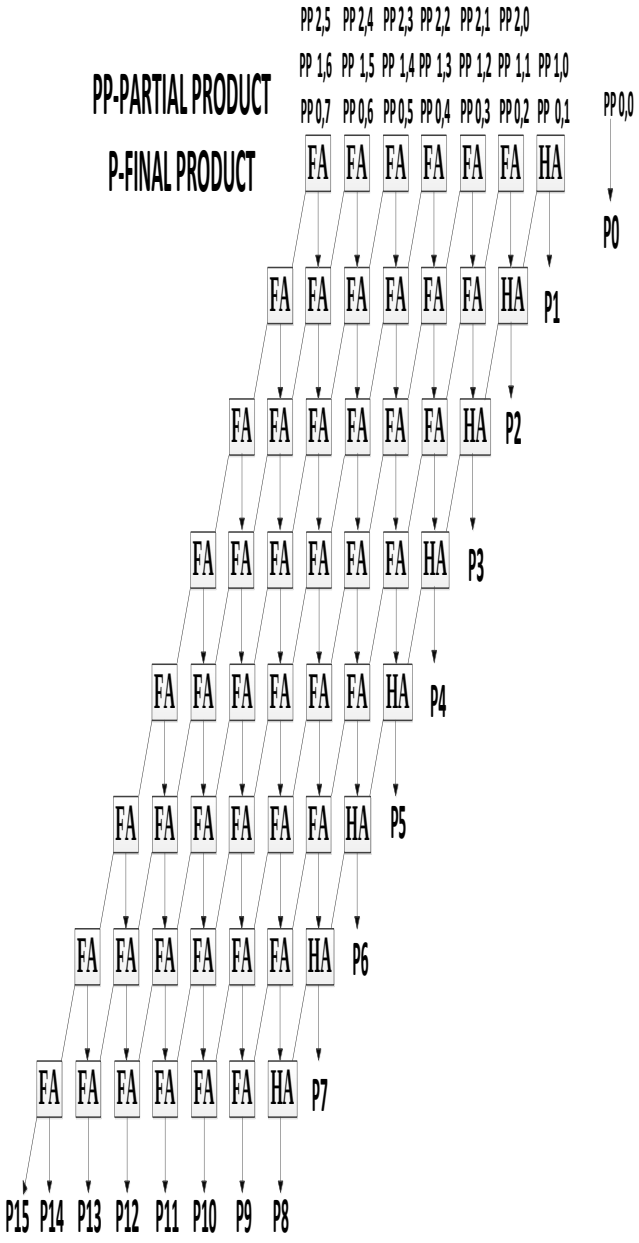

Fig 11: Block diagram of conventional multiplier.

4. SIMULATION RESULTS

Implementation of adder and multiplier in conventional and reversible logic stated, displayed the comparison among adder and multiplier both in area and power of them was determined by Table I and II .

Table I: Comparision of Power and Area between Reversible implementation and conventional design for CLA.

Design	Area	Power(mw)
Conventional CLA	75	0.03
Reversible CLA	230	0.01

Table II: Comparison of Power and Area between Reversible implementation and conventional design for Array Multiplier.

Design	Area	Power(mw)
Conventional array multiplier	1438	0.19
Reversible array multiplier	1833	0.14

A. Carry look ahead adder

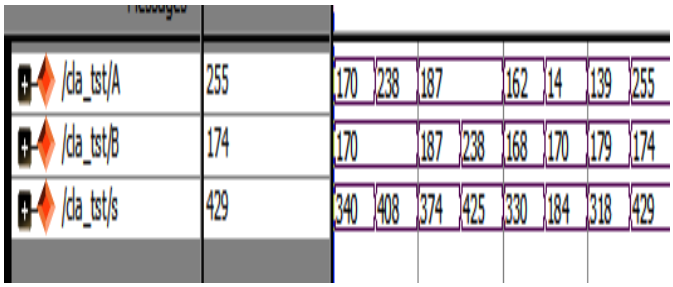

Fig 12: Simulation results for carry look ahead Adder.

B. Array Multiplier

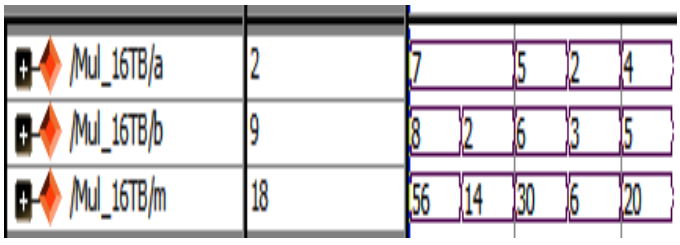

Fig 13: Simulation results for Array Multiplier.

In the above shown Fig 12 simulation result of the carry look ahead adder coding done by using verilog language [14].Fig 13 shows the simulation result obtained by the reversible array multiplier. And the backend chip layout of the adder and multiplier shown in the Fig 16 and 17. In generating conventional and Reversible adder sum, multiplicand for multiplier shows same output, difference in their Area and Power were determined in Fig 14 and 15 graphical .

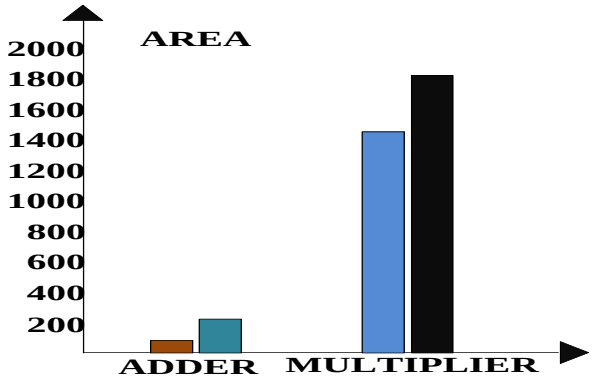

Fig 14: Comparison of area between conventional and reversible circuits

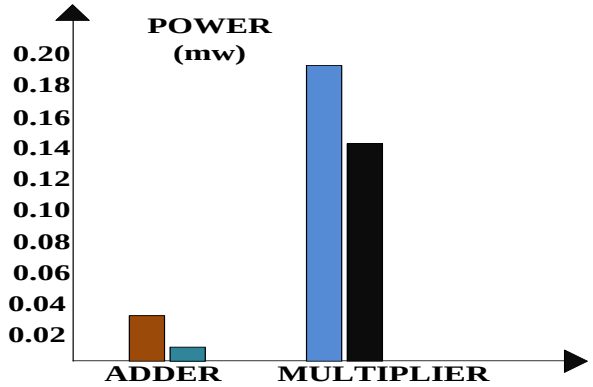

Fig 14: Comparison of area between conventional and reversible circuits

Conventional CLA
Reversible CLA
Conventional array multiplier
Reversible array multiplier

In next step we gone for ASIC (Application Specific Integrated Circuit) implementation of two designs carried out by using available tool in Cadence (Soc Encounter) here they are indicated as chip layout in Fig 16 followed by Fig 17 for adder and multiplier.

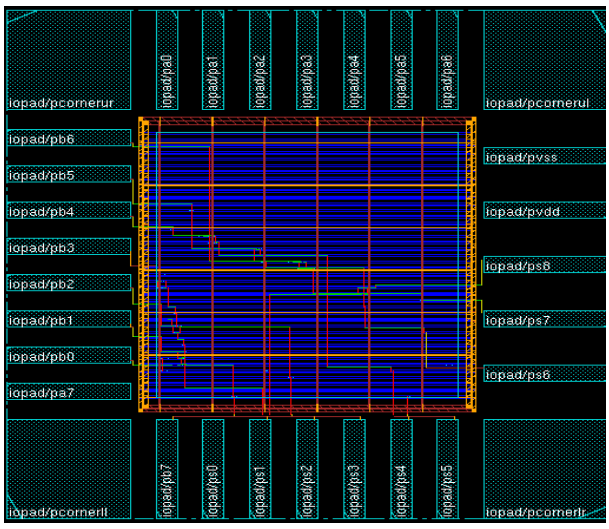

Fig 16: Chip layout of CLA

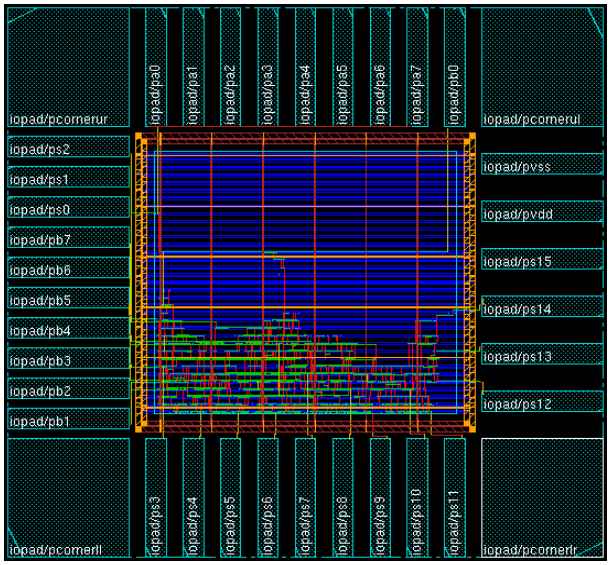

Fig 17: Chip layout of Multiplier.

5. FUTURE WORK

The prolongation of this method is to design different ALU's and Multipliers using reversible gates which are advantageous in terms of Garbage outputs, Constant inputs and Gate count helpful in the improvement in power consumption and timing delay.

6. CONCLUSION

In this paper we have implemented an 8-bit adder and multiplier using reversible logic, the results obtained are compared with conventional carry look ahead adder and array multiplier in terms of power consumption ,area of reversible gates are explored in terms of required functionality with less constant inputs and garbage outputs. There we having different reversible gates which results decrease in the number of constant inputs and garbage outputs compared to different papers. Simulation results are carried out by the NC launch and the power generation carried out by the RTL complier of CADENCE Tools

7. REFERENCES

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