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Aspect-Ratio-Dependent Copper Electrodeposition Technique for Very High Aspect-Ratio Through-Hole Plating

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Copper electrodeposition in high-aspect-ratio through-holes micromachined by deep reactive ion etching is one of the most essential processes for fabricating through-wafer interconnects, which will be used in developing future generation high-speed, compact 3D microelectronic devices. Although copper electrodeposition is a well-established process, completely void-free electroplating in very deep and narrow through-holes remains a challenge, where local current distribution does not remain uniform, resulting in void formation in the via. In this paper, we report the fabrication of very high aspect ratio through-wafer copper interconnects by an innovative copper electroplating technique. Completely void-free electroplating in very deep (~500 μm) and narrow through-holes was accomplished by a proposed "aspect-ratio-dependent electroplating technique." In this technique, electroplating parameters were continuously varied along with changing unfilled via depth. Continuously varying current density improves the local distribution of current as per the changing depth and helps in minimizing void formation. The hydrophilic nature of the via surface was also enhanced by wet surface treatment to improve the interaction between the copper electrolyte and via surface. Very fine pitch (~80 μm), through-wafer copper interconnects having an aspect ratio as high as 15 were fabricated by the above innovative technique.
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Through-wafer interconnect is one of the key technologies for fabricating next-generation compact 3D microelectronic devices. In this technology, several integrated circuit microelectromechanical system (IC/MEMS) devices are interconnected in vertical axis by through-wafer vias filled with copper or other conductive materials. Compared to existing interconnect technologies, such as wire bonding, tape-automated bonding, and flip chip, etc. through-wafer interconnects offer the shortest possible interconnect distance which results in the least parasitic losses, resistance-capacitance (RC) delay, and flight time and thus, the fastest possible response. They also offer several other advantages such as reduced packaging area, light weight, low cost, higher interconnection density, high reliability, excellent electrical performance with lower resistance, suitability for high-frequency applications, and device-scale packaging of microsystems.[1,2]

From the satisfactory system performance and reliability point of view, completely void-free filling of conductive material in the through-holes is important. Voids or seams formed in the through-holes may cause serious reliability issues. At present, copper is used as an interconnect material due to its high electrical conductivity and higher electromigration resistance when compared to aluminum.[3] In most cases copper is deposited by electroplating process,[4-8] as it is able to deposit several hundred micrometer thick metal layers. Compared to other physical deposition processes like sputtering, E-beam evaporation, and chemical vapor deposition, (CVD) the electroplating process is cheaper, faster, and requires lower temperatures.

Although copper electroplating is a well-established process and its principles have been known for decades, completely void-free filling in very deep and narrow through-holes is still a challenging task. Previous research work in through-wafer electroplating is limited to aspect ratio in the order of 10.[4] One of the major reasons behind the incomplete metal filling and void formation in high-aspect-ratio through-wafer electroplating is the uneven local current density distribution at each point inside the through-holes. In high-aspect-ratio (>10) through-hole electroplating, current density does not remain uniform along the depth. At the entry and exit of via, current density is higher than that at the center. Due to higher current density, copper deposition rate is greater at the entrance and exit of vias. As a result of higher copper deposition at the entrance, vias are blocked at the top and bottom and a void is formed in the center.[9,10]

Insufficient wetting of through-hole side walls with copper electrolyte is also a possible reason behind void formation. In very deep and narrow through-holes, the electrolyte does not wet via surface completely and in some cases even does not reach all places.[11] At present, deep and narrow through-holes in silicon are made by deep reactive ion etching (DRIE). During the passivation step of the DRIE process, a thin layer of polymer is deposited on the sidewalls that protect it from lateral etching. This polymer [poly(tetrafluoro) compound] is a hydrophobic material which prevents the wetting of the via surface with copper electrolyte. Due to insufficient interaction between copper electrolyte and some local points on the via surface, current density distribution varies, which results in nonuniform copper deposition along the through-via surface. At some local points, copper deposition does not occur at all and voids are formed. In order to get completely void-free electroplating, the via surface is required to be properly wetted by copper electrolyte, which is not possible in narrow and deep through-holes where the vias opening size is in the order of a few micrometers.[12]

In this paper, an innovative aspect-ratio-dependent copper electroplating technique is presented which is used to deposit copper in high-aspect-ratio through-holes of varying opening sizes and depths. Prior to the electroplating process, a surface treatment process was attempted to improve the hydrophilic nature of the via surface. Through-wafer copper interconnects with fine pitch and aspect ratio as high as 15 are successfully fabricated by this technique.

Experimental

Wafer sample preparation steps.— Schematic fabrication process flow diagram of through-wafer copper interconnects is illustrated in Fig. 1. Through-holes of varying opening sizes and depths were electroplated by various electroplating techniques such as continuous plating, pulse plating, pulse reverse plating, and the proposed aspect-ratio-dependent electroplating technique. Instead of a conventional plating technique, where a seed layer is deposited on the sidewalls of through-holes, "bottom-up" electroplating technique was used. The bottom-up electroplating approach utilizes two wafers that are termed as device wafer and contact wafer. The device wafer has through-holes that need to be electroplated.

In the experiments, electrical contact is provided through a 300-nm-thick seed layer that was deposited on the contact wafer by a sputtering process. Gold was preferred over other conductive metals due to its superior electrical conductivity and excellent oxidation resistance. Through-holes of varying dimensions from 20 to 40 μm were etched by the DRIE Bosch process. Table I shows the DRIE process parameters used in the high-aspect-ratio through-hole etch-

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Table I. DRIE process parameters used in high-aspect-ratio through-hole etching.

Parameters	Value
SF_6 flow rate	120 sccm
C_4F_8 flow rate	85 sccm
O_2 flow rate	14 sccm
Etch time	12 s
Passivation time	7 s
Coil power	600 W
Platen power	16 W
APC	75%

ing. After making through-holes, thin layers of SiO_2 and Si_3N_4 were deposited. Device and contact wafers were temporarily bonded by photoresist.

Surface treatment of DRIE-etched through-holes.— In order to enhance the wetting characteristics of the via surface with copper electrolyte, the hydrophilic nature of the via surface needs to be increased. In the experiments the contact angle of the substrate and insulation materials were measured to find out their respective wetting characteristics with copper electrolyte by a commercial contact angle measurement setup [fluorotrialkoxypilane (FTA) analyzer]. Three samples include bare silicon and DRIE-etched through-holes prior to silicon oxide deposition (polymer-coated silicon) and after silicon oxide deposition (with SiO_2 surface). After measuring the contact angle without any surface treatment, all the samples were cleaned in SC1 solution (30% H_2O_2, 25% NH_4OH, and deionized (DI) water in 1:1:5 ratio) at 75°C for 30 min, followed by DI water rinsing and nitrogen drying. Samples were wetted with copper electrolyte and their mutual contact angles were measured again to unearth the effect of surface treatment. The contact angle of samples with copper electrolyte prior to and after the surface treatment process are given in Table II.

Through-wafer copper electroplating.— Electroplating setup.— All electroplating experiments were carried out in a homemade electroplating system, whose schematic diagram is shown in Fig. 2. A silicon wafer was mounted on a wafer holder, which was immersed in a copper plating bath. In order to maintain uniform current distribution, electrical contact to gold seed layer was provided by a circular contact ring. The diameter of the anode was kept twice at that of the wafer holder to provide sufficient copper ions. Copper electrolyte was provided by ATOTECH (Germany). This electrolyte has three main components: base solution containing copper sulfate, sulfuric and hydrochloric acid, and organic additives, i.e., brightener and leveler. Following is the optimum concentration of these ingredients: copper 40 g/L, sulfuric acid 150 g/L, chloride 50 mg/L, leveler 15 ml/L, and brightener 10 ml/L. Electrolyte was pumped symmetrically against the wafer in the form of stagnant flow. A simple mechanism of rack and pinion was used to vary the interelectrode gaps between the copper plate and wafer holder. A thick coating of Teflon was applied over the outer surface of the wafer holder to isolate wafer surface and to minimize the current

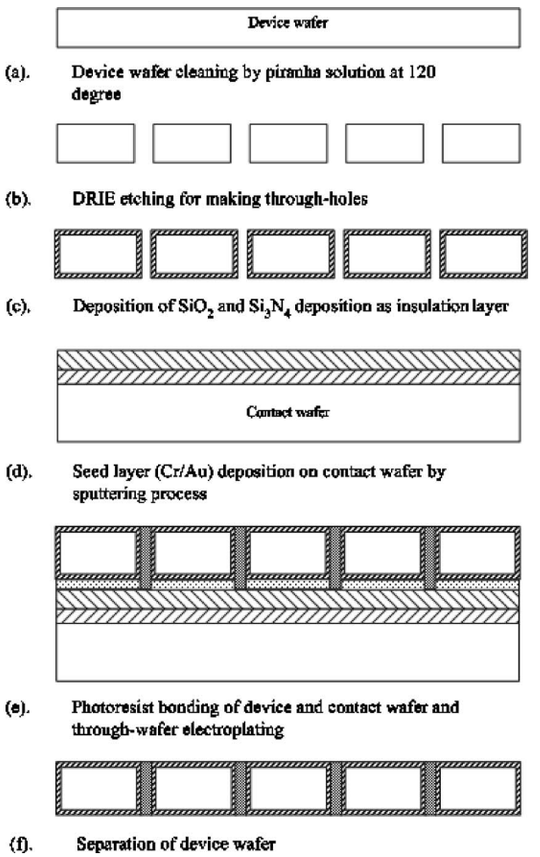

Figure 1. Schematic process flow diagram showing the fabrication of 3D through-wafer interconnects by copper electroplating.

loss. Various current waveforms, i.e., continuous, pulse, and reverse pulse waveform of varying current and on/off time period, were generated by a pulse rectifier supply unit.

Bottom-up electroplating approach.— Uniform and void-free copper filling requires that copper deposition rate remains the same all along the depth. In the case of very deep and narrow through-holes, current distribution does remain uniform at all local points. Nonuniform current distribution becomes more severe when the aspect ratio exceeds more than 10 and opening size of the through-hole is in the order of 20 μm.

In order to avoid the blocking of vias opening, a "bottom-up" electroplating technique was used. As indicated by its name, in bottom-up electroplating, metal deposition starts at the bottom and gradually grows upwards, eliminating the possibility of via blocking at the entrance. The basic difference between bottom-up and conventional electroplating techniques is given in Fig. 3. In contrast to conventional electroplating techniques where seed layer is deposited on the sidewalls, in bottom-up electroplating electrical contact is

Table II. Contact angle of different samples with copper electrolyte.

Sample	Surface treatment	Contact angle (°)
Si	At room temperature, without cleaning	25
Si + thermal SiO_2	1.8 μm thermal SiO_2 grown at 1100°C	69
DRIE-etched Si	Sample etched in Bosch DRIE process	47
DRIE-etched Si + thermal SiO_2	1.8 μm SiO_2 grown DRIE-etched sample	59
DRIE-etched Si + thermal SiO_2 + SC1 treatment	DRIE-etched sample with grown SiO_2 Treated in SC1 solution at 75°C for 30 min	34

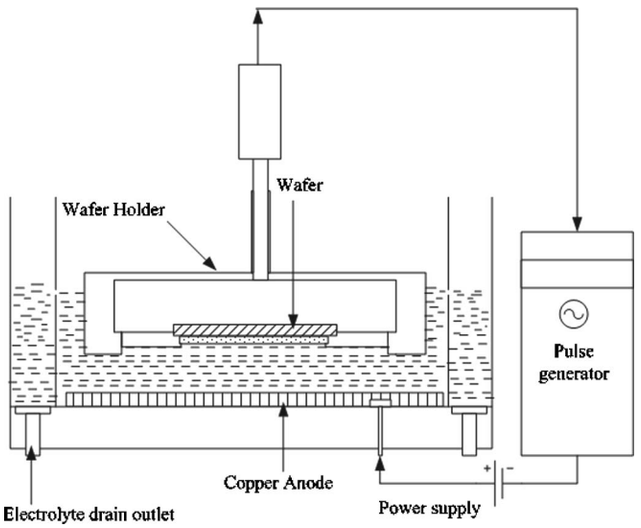

Figure 2. Schematic representation of copper electroplating setup.

provided by a seed layer deposited on another wafer. Although bottom-up electroplating minimizes the chances of void formation, it is not able to eliminate them completely. Through-hole electroplating of vias having an aspect ratio in the order of 20 remains very difficult.

In normal electroplating processes, all the process parameters such as current density and pulse-on and -off time are chosen according to the aspect ratio of through-holes, which is defined as the ratio of depth of through-via H to the opening size of through-hole a. From the beginning to the end of the electroplating process, the parameters remain constant.

Aspect-ratio-dependent electroplating technique.— In this paper, a new scheme of electroplating is proposed to deposit copper uniformly in very high aspect ratio through-holes. A simple rule of thumb, "the higher the aspect ratio, the lower the forward current density and the higher the reverse current density," forms the foundation of this proposed technique. This proposed technique considers the unfilled depth of through-holes or "effective aspect ratio" as the main criteria to decide the electroplating current parameters. Effective aspect ratio (EAR) is termed as the ratio of "unfilled depth of through-holes" to the opening size of the through-via.

Figure 4 gives the simple concept of EAR and unfilled depth of through-hole. When the electroplating process starts, metal ions begin to deposit on the bottom of through-holes. As a result of continuous metal deposition, effective unfilled depth of through-holes continuously reduces with electroplating process time. Thus, the aspect ratio of unfilled vias or EAR also continuously reduces with time. At the beginning of the electroplating process ($\tau = 0$), the depth of vias is H, which is reduced to $(H\text{-}h)$ after τ time of electroplating process. Hence, EAR is reduced from H/a, at $\tau = 0$, to $(H\text{-}h)/a$, at $\tau = \tau$. The EAR continuously reduces until the end of electroplating process.

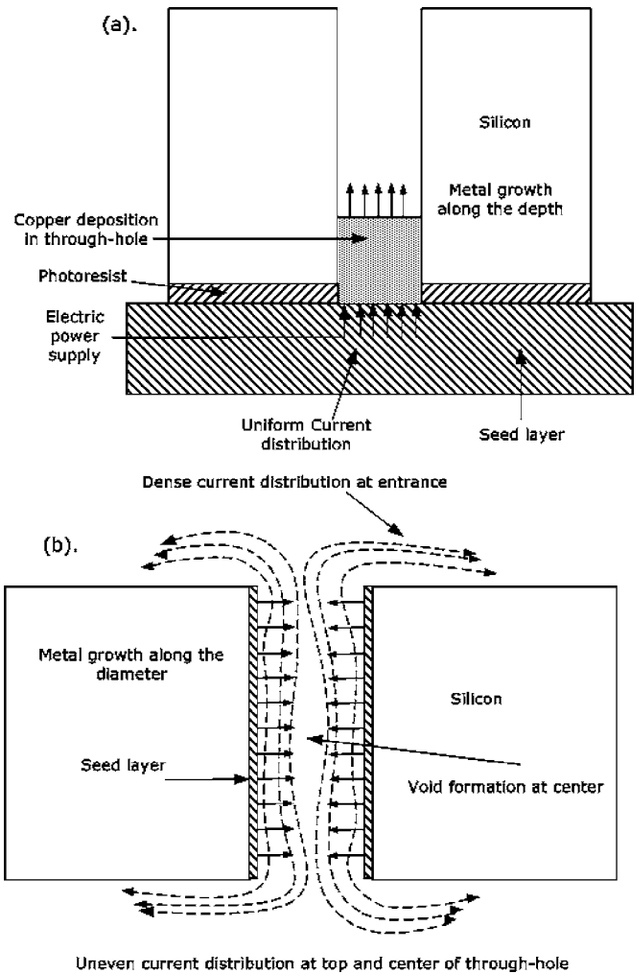

Figure 3. (a) Bottom-up electroplating–uniform metal deposition as metal starts depositing from the bottom; (b) conventional electroplating–uneven current distribution at top and center of through-hole, resulting in void formation.

As the effective unfilled depth is continuously reducing, electrolyte kinetics and cupric ion mass transfer does not remain uniform. As shown in Fig. 5, primary current distribution, which is a result of ohmic potential drop through the electrolyte, is strictly a function of electrolyte path length, i.e., the depth of through-holes through

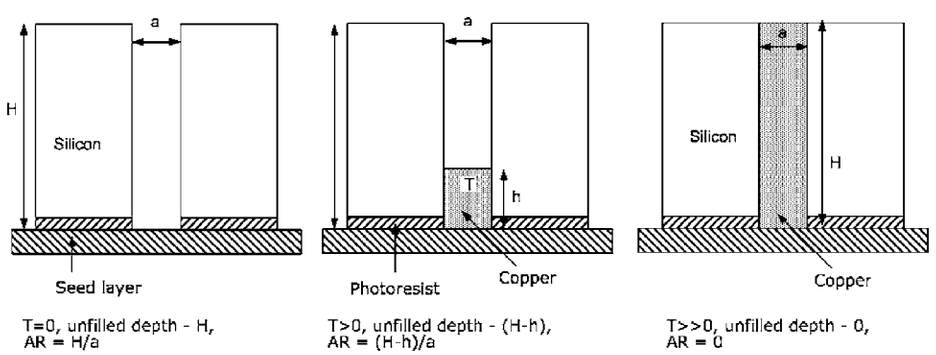

Figure 4. Schematic diagram showing basic representation of EAR.

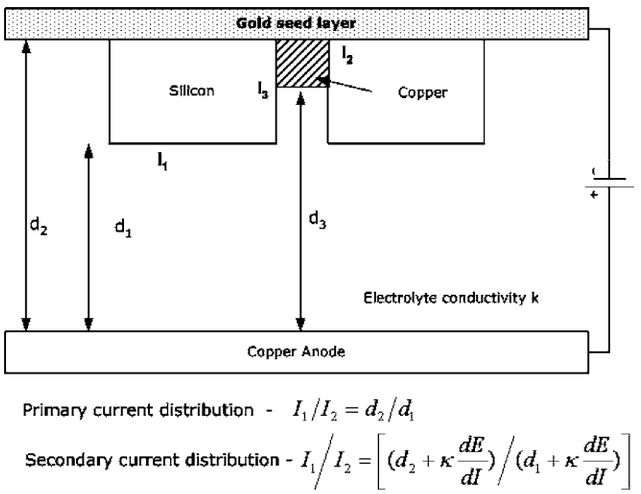

Figure 5. Schematic diagram showing dependence of primary and secondary current on electrode path length.

which electrolyte travels. Primary current distribution at the opening of through-holes (I_1) and at the bottom of through-holes (I_2) can be expressed as

$$\frac{I_1}{I_2} = \frac{d_2}{d_1} \quad [1]$$

Similarly, secondary current distribution, which is due to the various polarization effects, can be expressed by the following equation

$$\frac{I_1}{I_2} = \left[\frac{d_2 + k\dfrac{dE}{dI}}{d_1 + k\dfrac{dE}{dI}} \right] \quad [2]$$

where k is the electrolyte conductivity.

As a result of variation in distance from anode d_3 ($d_1 \leqslant d_3 \leqslant d_2$), current distribution inside the deep through-hole also becomes nonuniform. Uneven uniformity in current distribution and mass transfer of cupric ion affects the uniformity of copper deposition, which results in void formation, incomplete filling, rough grain formations, and other undesired results.[13-15]

To maintain the uniform current distribution when the distance between anode and deposited metal is continuously reducing, process parameters such as current density and pulse-on time need to be varied as per changing unfilled depth. The same has been proposed and implemented in "aspect-ratio-dependent electroplating." A variation of current density distribution with electroplating time is given in Fig. 6, along with that of conventional pulse reverse electroplating. This figure clearly illustrates that in contrast to conventional reverse pulse electroplating technique, in which the electroplating parameters such as forward current density, reverse current density, and pulse-on time are kept constant during the electroplating process, process parameters continuously vary in the new technique (Fig. 6).

In the beginning of the electroplating process when the depth of through-holes is very high (d_2), relatively low forward current density (J_1) with high reverse current density (J_2) is used so that copper grains can be deposited on the bottom without any voids. During pulse-on time (t_1), low current flows in a forward direction and fine grain copper is deposited on the bottom of through-holes. Low forward current density also helps in forming good contact between the deposited copper and gold seed layer. In reverse pulse on period (t_2), reverse current removes copper from predeposited locations, thus making the metal distribution more uniform. As the electroplating process continues, forward current density (J_1) is increased gradually while reverse current density (J_2) is reduced. Figure 7 shows the variations in forward and reverse current density with respect to electroplating time. Brief details of the process parameters used in proposed high-aspect-ratio through-hole copper electroplating technique are given in Table III.

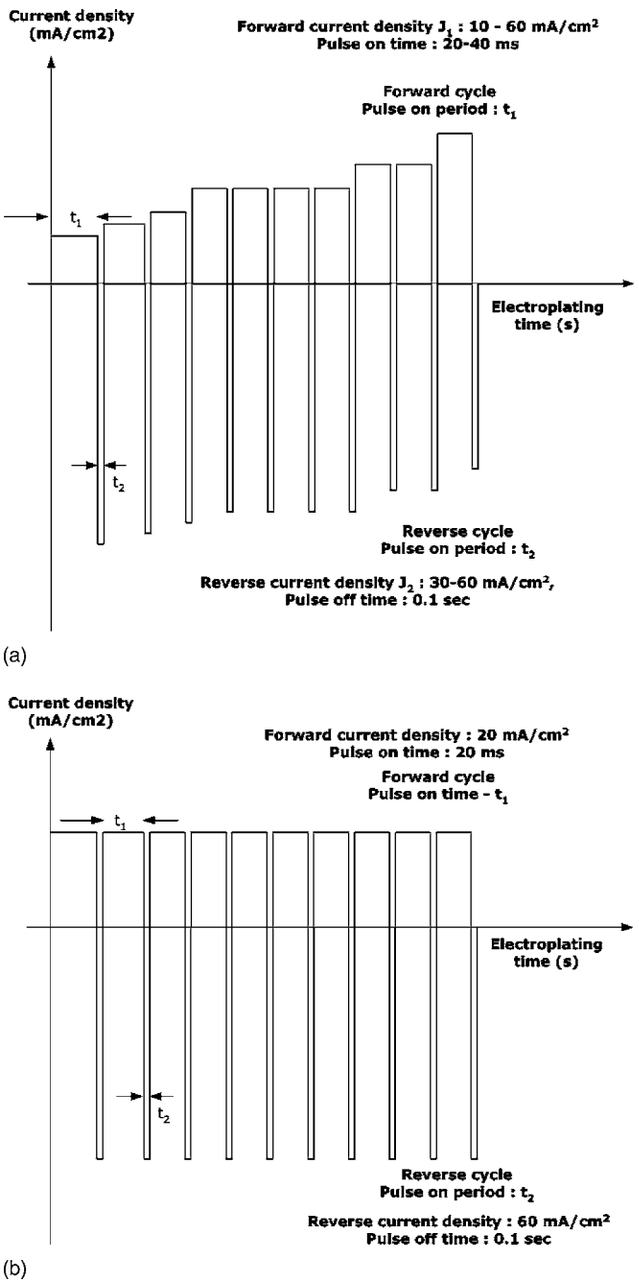

Figure 6. Current density distributions with electroplating time: (a) proposed aspect-ratio-dependent electroplating technique and (b) reverse pulse electroplating technique.

Results

DRIE-etched through-holes.— Through-holes of varying opening size from 20 to 40 μm were etched in the device wafer by the DRIE process. A 1.8-μm-thick SiO_2 layer was used as a mask layer along with 5 μm AZ9260 photoresist. Thickness of used device wafers varied from 200 to 400 μm; hence, DRIE-etched through-holes

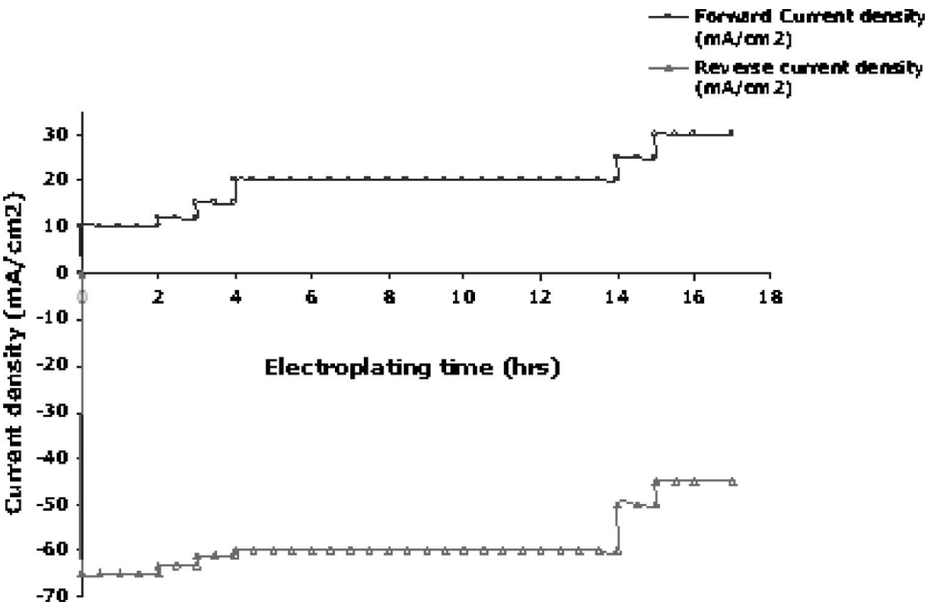

Figure 7. Variation in forward and reverse current density with electroplating time.

of varying aspect ratios from 5 to 15 were obtained. Etch rate varied for different via opening sizes. Figure 8 shows the aspect-ratio-dependent characteristics of the DRIE process. It is clear from this figure that etch rate reduces as aspect ratio of through-holes increases. After 30 min of etching, the etch rate for 20 μm diameter was 2.5 μm/min, while for 50 μm diameter, it was 3.6 μm/min. After 150 min of etching, the etch rate reduced to 1.6 and 1.8 μm/min, respectively.

In the case of small-diameter through-holes, less fluoride ions are available for reaction with silicon than large diameter areas. Due to less fluoride ions, the possibility of silicon etching minimizes and thus, the etch rate reduces for small through-holes. The main reason for deceleration of silicon etching in high-aspect-ratio through-holes seems to be the loss of etchant species due to the sidewall reactions combined with feature closure by ion-limited passivation polymer etching. Figure 9 shows the cross-sectional image of DRIE-etched through-holes.

Surface treatment of DRIE-etched through-holes.— To enhance the hydrophilic nature of via surfaces, a DRIE-etched device wafer was cleaned by SC1 solution. Contact angles, prior to and after the surface treatment, were measured to evaluate the effect of surface treatment on the wetting characteristics. From Table II, it is clear that the contact angle of the DRIE-etched sample (47°) is more than bare silicon (25°). Increment in contact angle is due to polymer deposition in the DRIE Bosch process. In the passivation step of the Bosch cycle, passivation gas carbon tetrafluoride (C_4F_8) is used to deposit a thin layer of polymer on the sidewalls. This polymer layer protects the sidewalls in the etching cycle, reduces the lateral etching, and helps in making vertical profiles; however, being a hydrophobic material, it also reduces the wetting characteristics of via surfaces with copper electrolyte. When the DRIE-etched sample with grown SiO_2 was cleaned with SC1 solution, the contact angle reduced to 34°, enhancing its hydrophilic characteristics with electrolyte. Significant enhancement in contact angle after SC1 treatment is due to the absorption of hydroxyl group together with amino group, which has contributed to enhanced wettability characteristics.

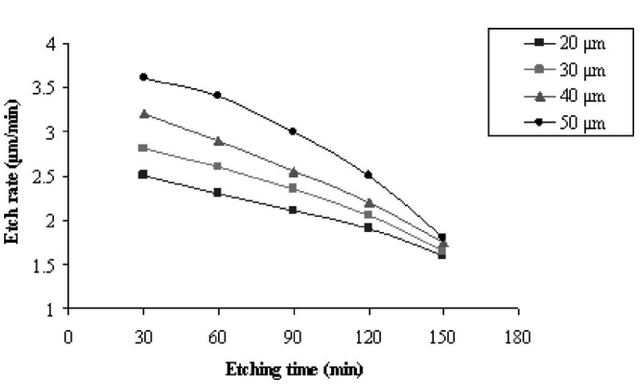

Figure 8. Variation in etch rate for varying opening size with etching time.

Effect of electroplating conditions on the void formation.— In this work, a series of experiments with varying electroplating conditions were carried out in order to understand the mechanism of void formation in high-aspect-ratio through-holes. DC continuous plating, pulse reverse plating, and proposed aspect-ratio-dependent electroplating techniques were tried. Table IV gives the details of process parameters of dc continuous, reverse pulse, and proposed aspect-ratio-dependent electroplating.

DC continuous and pulse reverse plating.— Figure 10 and 11 show the scanning electron microscopy (SEM) cross-sectional images of through-holes electroplated by dc continuous plating and reverse pulse plating. These images show the effect of current density on copper deposition morphology in both dc continuous and reverse pulse electroplating. Figure 10a and b shows the cross-sectional images of through-holes electroplated by continuous dc plating at 10 and 20 mA/cm^2, respectively. Although in both cases voids are clearly visible in the center and bottom of through-holes, the size and number of voids are more in the case of higher current density

Table III. Process parameters of aspect-ratio-dependent electroplating technique.

Sample no.	No. of cycles	Forward current density (mA/cm^2)	Reverse current density (mA/cm^2)	Pulse-on time (ms)	Pulse-off time (ms)
1	2	10	65	40	1
2	2	15	60	30	1
3	8	20	60	20	1
4	1	25	50	20	1
5	1	30	45	20	1

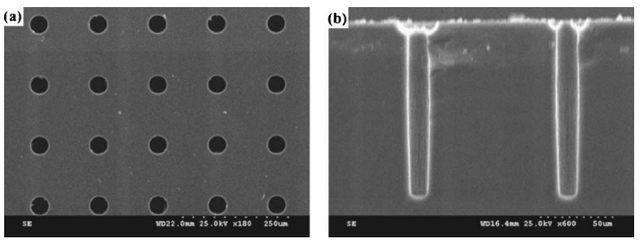

Figure 9. SEM image of DRIE-etched through-holes: (a) top view of through-holes and (b) cross-sectional image of partially etched vias.

(Fig. 10b). Copper deposition is more uniform when low current density is used (Fig. 10a). Formation of voids in dc plating is attributed to the current density mismatch at the top opening sharp corners and at the center. Operation at low current density improves the copper deposition process.

Effect of current density is also visible in Fig. 11, where similar through-holes are electroplated by reverse pulse electroplating technique. The magnitude of forward current density is varied from 20 to 30 mA/cm^2 while keeping the reverse current density constant, i.e., 60 mA/cm^2. At higher forward current density (Fig. 11b), copper deposition is not uniform and a lot of unfilled voids are present, which may be attributed to the rapid electrodeposition rate at the through-hole opening. Although voids are also formed with forward current density of 20 mA/cm^2, copper uniformity is better in this case than that of 30 mA/cm^2. Electroplating copper deposition morphology is strongly influenced by the magnitude of forward current density in reverse pulse electroplating, and the optimum current density seems to be 20 mA/cm^2.

The effect of the electroplating technique can be seen by comparing Fig. 10b with 11a. In both cases, the forward current density is 20 mA/cm^2; however, in the second case, reverse pulse electroplating is used. Improvement in the quality of electrodeposition can be easily seen, which is attributed to the reverse current.

Aspect-ratio-dependent electroplating.— When similar through-holes are electroplated by the aspect-ratio-dependent electroplating technique, the number of voids is reduced significantly. Because cutting the electroplated through-holes along the center is a difficult task, cross-sectional images of through-holes having aspect ratios up to 8 are shown. For higher aspect ratio electroplated through-holes, the silicon etching technique has been used.

SEM images in Fig. 12 show the complete copper filling in high-aspect-ratio through-holes. Through-holes, having diameter 40 μm and depth 325 μm, are completely filled with copper without any void or defect. Copper growth is also very uniform along the depth. Compared to continuous dc plating and pulse reverse electroplating (Fig. 10 and 11), the results obtained by using the electroplating technique are better (Fig. 12). The effect of variable current density as per changing effective depth of through-holes is clearly visible in this cross-sectional image.

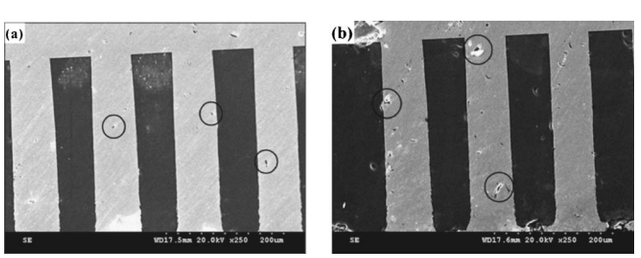

Figure 10. Cross-sectional image of 60-μm-diameter electroplated through-holes in 300-μm-thick silicon wafer by continuous power supply at different current densities: (a) 10 and (b) 20 mA/cm^2. Voids are shown in circle.

Table IV. Process parameters of copper electroplating process.

Chemical composition of electrolyte bath	
$CuSO_4$	40 g/L
H_2SO_4	150 mg/L
HCl	50 mg/L
Brightener	10 mL/L
Leveler	15 mL/L
Electroplating conditions—DC continuous plating	
Cathode	Silicon wafer
Anode	Copper plate
Current density	10–20 mA/cm^2 for dc plating
	15–60 mA/cm^2 for pulse plating
Temperature	30°C
pH	1.0
Reverse pulse electroplating parameters	
Current density	20–30 mA/cm^2 (forward), 60 mA/cm^2 (reverse)
Pulse-on time	20 ms (forward), 1 ms (reverse)
Aspect-ratio-dependent electroplating parameters	
Current density	10–30 mA/cm^2 (forward), 35–65 mA/cm^2 (reverse)
Pulse-on time	20–40 ms (forward), 1 ms (reverse)
Electroplating time	16–24 h (for different thickness wafers)

Compared with dc plating, which has one nucleation step (continuous plating) and continuous growth of copper ions, this technique has several repeated sequences of nucleation and growth steps, which results in fine grains due to the slower grain growth rate. Simultaneously, cathodic deposition during the on-time of the pulse cycle depleted the dissolved Cu^{++} concentration at the cathode surface, but the concentration can be restored to the bulk concentration by mass transfer during the off-time of the pulse. In addition, this technique is also superior in several aspects such as effective mass transfer control, controllable microstructure of electrodeposits, dense fine-grained deposits, freedom from dendrite growth, almost no pinholes, and better current efficiency.

Compared to conventional reverse pulse plating, this approach seems to be better. Since the magnitude of forward and reverse current density varied as per varying unfilled depth of through-holes, local current distribution is more uniform. As a result of higher

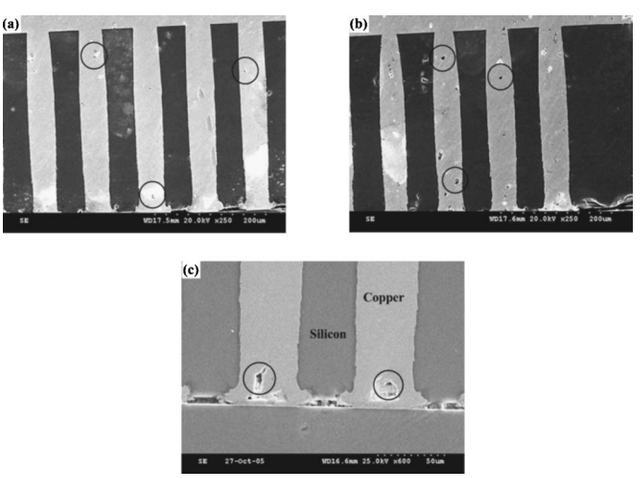

Figure 11. Cross-sectional images of 40-μm-diameter through-holes in 325-μm-thick silicon wafer by reverse plating. (a) Forward/reverse current density 20/60 mA/cm^2. (b) Forward/reverse current density 30/60 mA/cm^2. (c) Closer view of voids formed at the bottom of through-holes.

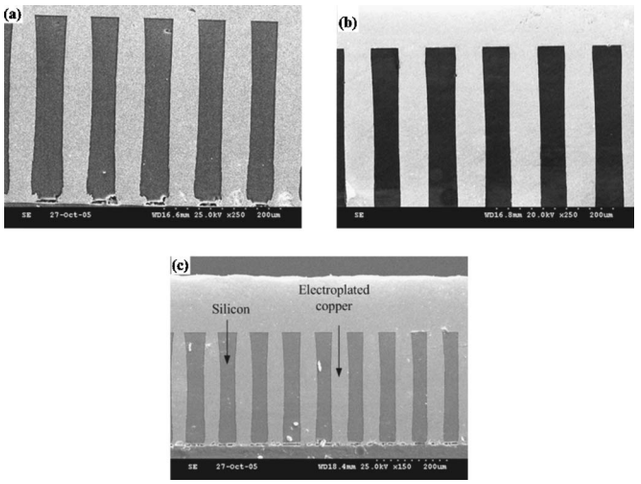

Figure 12. Cross-sectional SEM images of 40-μm through-holes in 325-μm-thick silicon wafer. (b) Closer view of through-holes cross section. (c) Through-wafer copper interconnects fabricated in silicon.

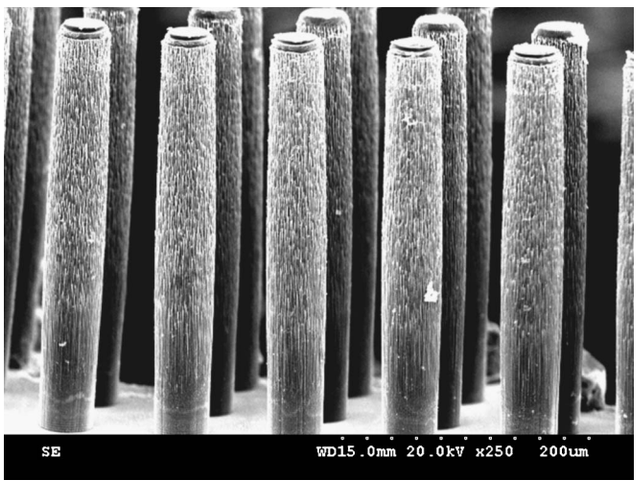

Figure 14. High-aspect-ratio, vertical electroplated copper interconnects after silicon dissolution by KOH at 80°C.

reverse current density, the concentration gradient between the top and bottom of the vias reduces, which results in better filling phenomenon. As the electroplating process progresses, the unfilled depth reduces, which results in a shorter conductive path available between cathode and anode that in turn affects the primary current distribution. To maintain the current distribution uniformly, forward current density is increased while reverse current density is reduced slightly. This sequence of adjusting process parameters continues until the through-holes are completely filled.

High-aspect-ratio through-wafer copper interconnects.— As mentioned above, cutting the electroplated through-hole along its center and throughout its depth is difficult, as the ductile material (copper) is between the brittle materials of silicon. To overcome this problem, silicon between the copper pillars was dissolved away by KOH solution at 80°C. When the silicon was completely dissolved, through-wafer copper interconnects in the form of vertically standing pillars were exposed, which were characterized by SEM.

SEM images of through-wafer interconnect after copper electroplating are given in Fig. 13. It is clear from Fig. 13 that the surface is very rough near the bottom of through-holes, which is due to nonuniform DRIE etching. Figure 14 shows an array of electroplated copper interconnects after the complete dissolution of the silicon. As seen by the SEM images, the sidewalls of copper pillars are very smooth. Copper grains along the vertical directions are very fine. Copper grains are elongated in vertical axis, which is the prime characteristic of the bottom-up electroplating approach. As grain roughness directly affects the electrical properties such as electrical resistivity, electromigration resistance, etc. the electrical performance and reliability of fabricated copper interconnects seem suitable for packaging applications. An other important feature of the proposed electroplating technique is its ability to produce identical copper interconnects, which is visible in Fig. 14.

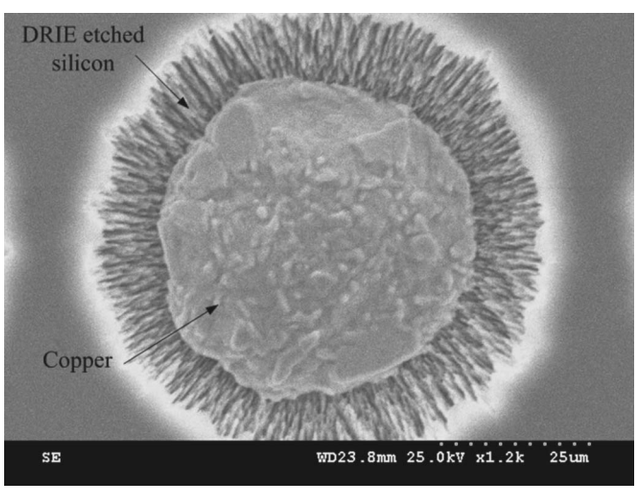

Figure 13. Close view of electroplated through-wafer copper interconnects before silicon dissolution.

While conventional pulse reverse electroplating technique is able to fill in copper through-holes having an aspect ratio only in the order of 10, this new approach is able to fill through-holes of aspect ratio as high as 15 with success. Efforts are being made to achieve an aspect ratio of 30, i.e., to electroplate very narrow holes of 15–20 μm diameter and 450-μm-deep through-holes and to fabricate next-generation 3D wafer-stacked IC devices.

Conclusion

In this paper, we have presented a novel aspect-ratio-dependent electroplating technique which is used to solve the problem of void formation and incomplete filling in high-aspect-ratio through-holes. In this proposed technique, electroplating process parameters, such as current density and pulse-on time, are continuously varied with electroplating process time. To enhance the quality of copper deposition and to minimize the chances of void formation, wetting characteristics of the inner through-hole surface are improved by surface treatment prior to the electroplating process. Through-holes having a diameter as low as 30 μm and depth of 450 μm are etched by the DRIE Bosch process and then these through-holes are electroplated by using this new technique. To demonstrate its superior ability of filling very high aspect ratio through-holes (aspect ratio $\approx$ 15) over conventional electroplating techniques, experiments are also done by dc continuous and reverse pulse electroplating technique. The quality of fabricated copper interconnects by the proposed technique has shown the superiority of this technique. Fabricated high-aspect-ratio copper interconnects have a lot of potential applications, such as in 3D wafer level packaging, 3D radio frequency inductor, and resonator and ultrasonic transducers.

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