Aspects of Systems and Circuits for Nanoelectronics

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A tremendous number of devices, a limitation of wiring, and very low power dissipation density are design constraints of future nanoelectronic circuits composed of quantum-effect devices. Furthermore, functional integration, which is the possibility of exploiting quantum effects to obtain a function specific behavior, becomes a core design principle. This paper analyzes the effect of this technological progress on the design of nanoelectronic circuits and describes computational paradigms revealing novel features such as distributed storage, fault tolerance, self-organization, and local processing. In particular, linear threshold networks, the associative matrix, self-organizing feature maps, and cellular arrays are investigated from the viewpoint of their potential significance for nanoelectronics. Although these concepts have already been implemented using present technologies, the intention of this paper is to give an impression of their usefulness to system implementations with quantum-effect devices.

Keywords*—*Artificial neural networks, nanoelectronics, quantum-effect devices, system architectures.

I. INTRODUCTION

Today, commercially manufactured nanoelectronic systems seem to be far away, because the research has just reached the level of single logic gates and memory cells [36]. To outline the development of microelectronics until the time when quantum-effect devices will gain industrial relevance, the Semiconductor Industries Association (SIA) has published a study containing a road map from now until the year 2010. During this period, the silicon-based CMOS circuitry will be the dominating technology for microelectronics [4], [89]. The study predicts that in 2010, the integration level for example will reach about 40 billion devices for memories and a clock frequency of about 1 GHz for logic. The minimum feature size of this advanced CMOS technology will be in the range of 50 nm, so that quantum effects are not yet dominant. The prediction of this study seems reasonable considering the present development of technology. Fig. 1 illustrates SIA data and displays the degree of performance as product of device number and clock frequency. Concerning the location of nanoelectronics in this prediction, it is assumed that a change in technology will only occur if the overall performance improves by at least about two orders of magnitude. In this case, the total number of devices should be at least 1 billion for a nanoelectronic system. To limit the power dissipation, the clock frequency may be in the range of only several 100 MHz.

Analyzing the recent work on the field of quantum effects, today there are intensive efforts to realize fine structures and to develop sophisticated devices as functional blocks. There are only few activities, however, to endeavor novel circuit architectures that meet the demands of nanoelectronics. Similar to the progress in microelectronics in the past 30 years, the commercial success of nanoelectronics strongly depends on the availability of adequate system concepts. Therefore, the main intention of this paper is to emphasize that nanoelectronic circuits should be developed from both sides, that is, from the technological and the system point of view (Fig. 2).

In detail, we combine several computational systems that stay beyond classical microprocessor solutions with quantum-effect devices. Although some of these systems have been intensively studied and implemented in CMOS-VLSI, it is obvious that, at the moment, this paper can convey only a rough overview on this evolving area since the adaptation of these systems to the requirements of nanoelectronics is nearly at the same level as the devices themselves.

This paper is structured as follows. In Section II we concentrate on some general principles of device properties and system design. The subsequent section contains a short review of important quantum-effect devices and first circuit applications. Section IV comprises linear threshold networks for arithmetic computations, the associative matrix, self-organizing feature maps, and other nonclassical, partly biologically inspired systems. The last section describes the relationship between solid-state nanoelectronics and other

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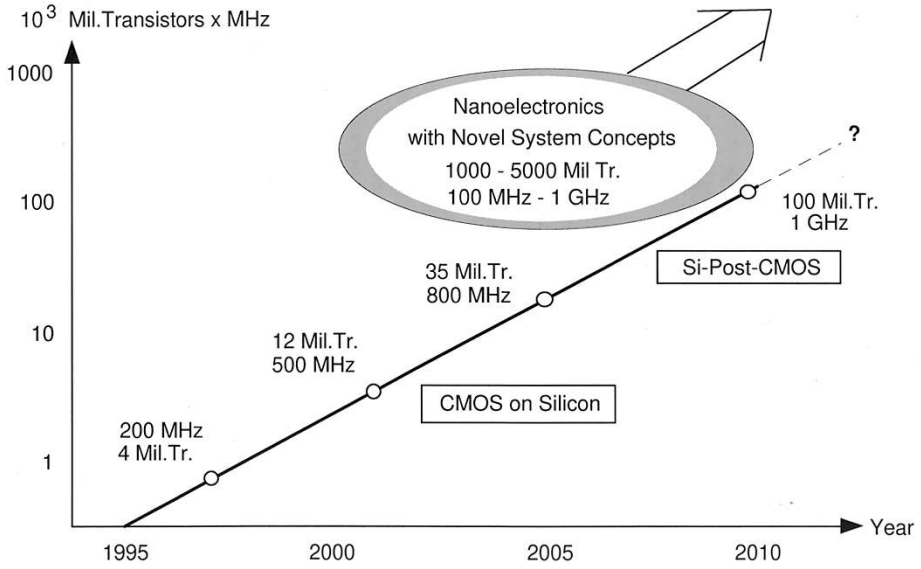


Fig. 1. The SIA roadmap as performance over time and the location where nanoelectronics will be placed at the time of its expected appearance. The performance indicated is the product of integration level and clock frequency.

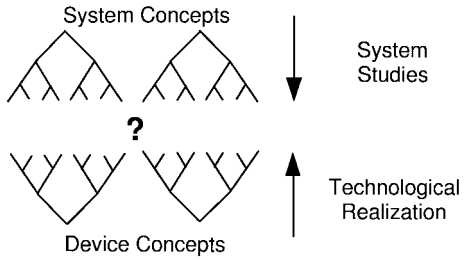


Fig. 2. A possible strategy for developing nanoelectronics: starting from both the device and system level.

future technologies for information processing, such as superconductivity and molecular electronics.

II. Challenge of Nanoelectronic Systems: From Device to Function

Since mid-1980's, semiconductor technology has provided us with structures on the order of atomic length scales. This technological progress results in novel quantum-effect devices with nonlinear current–voltage characteristics. Before discussing the key question in which way the system design based on these devices differs from our present technology, we review some important steps in the development of microelectronics systems in the past to derive some general guiding rules which might be relevant for nanoelectronics, too. A look back at the development of electronics reveals that every key invention in technology has initiated a milestone in systems. For example, the integration of transistors on one chip was followed by the logic families such as TTL and ECL. Later, the very large scale integration (VLSI) technique led to the idea of the microprocessor. In a similar way, the appearance of nanoelectronics with an integration level in the order of billions of quantum-effect devices will be accompanied by innovative systems.

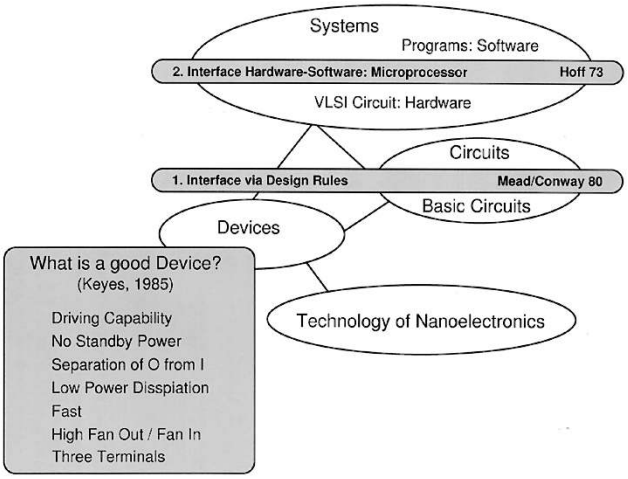


Fig. 3. Hierarchical structure of microelectronic systems. The two interfaces are located first between the technology and circuit level and second between software and hardware.

During the development of microelectronics, the separation of technology and systems by means of an invariant interface to simplify the design was substantial progress (Fig. 3). Mead and Conway introduced this important concept in the late 1970's [50]. Until now, this has been an essential and outstanding step in the development of microelectronics to cope with the complexity of the design. It is almost certain that this principle of hierarchical design, or a related one, will also be valid for nanoelectronics in the future.

A further interface in the hierarchical structured design has already been introduced in 1973 by Hoff when developing the first microprocessor. This interface has solved the problem of the narrow application window of most of the complex VLSI circuits. The idea of a microprocessor is to integrate basic components of a von Neumann computer

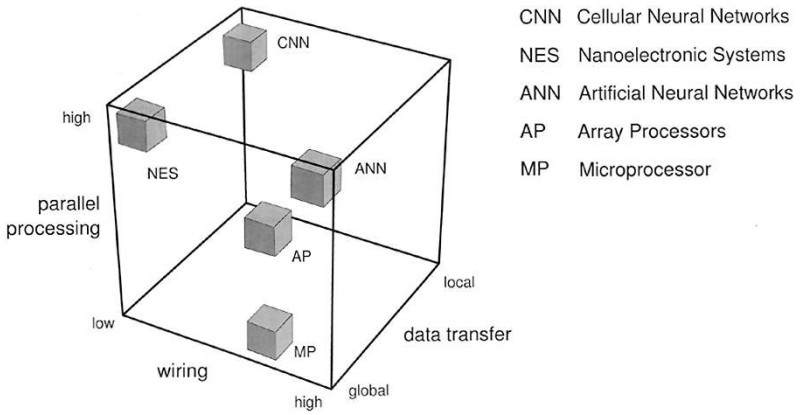


Fig. 4. Classification of different implementations of computation with regard to wiring, degree of parallelism, and data transfer.

on one chip. Together with memories and a few other standard VLSI chips, this has yielded to the development of flexible systems by application-specific software on a high level. At this point, only a quick look on the growth rates of the semiconductor industry is necessary to understand the economic meaning of microprocessors and memories. The connection between the universal hardware platform and the application-specific software is done by translating the program to the machine language with help of a compiler.

Classifying different popular computational paradigms, some characteristic features that become relevant in nanoelectronics are the amount of wiring, the degree of parallelism, and the range of data transfer (Fig. 4). The difference between wiring and data transfer is that the first uses physical interconnections, that is, metallic wires, whereas data transfer may be realized without direct physical wiring. In this case, long-range data transfer is done by sending a signal from module to module, analogous to systolic structures. It is obvious that today parallel operation and locally interconnected modules are of less significance in the traditional microprocessor-memory architecture. In contrast, the basic elements of cellular automata and artificial neural networks process the given input data fully parallel. Additionally, Fig. 4 specifies the region of highly parallel operating and locally interconnected nanoelectronic systems.

The serious interconnection problem is commonly accepted and will soon become relevant in advanced CMOS technology. According to Keyes, the wiring density of a chip increases nearly exponentially with the number of devices [35]. Furthermore, the decreasing supply voltages will affect the driving capabilities and a reliable signal transfer becomes questionable. Apart from these technological barriers, the costs for the wiring of the devices become much more expensive than the devices themselves. Thus, avoiding long-range interconnections has an economic motivation, too. The ways in which cellular neural networks or cellular automata are possible solutions is one topic of Section IV. Obviously, the tremendous amount of wiring in fully interconnected neural networks, that is, the large number of synaptic interconnections, has to be reduced.

Apart from the specific structure of a quantum-effect device, there are some general rules that are still valid in the future, since a device should possess the following features: the input has to be well separated from the output and the devices should have a sufficient driving capability. It should consume only low power in a nonactive state and switch sufficiently fast [34]. These are indispensable requirements for all thinkable kinds of classical and quantum-effect devices whether implemented within solid-state nanoelectronics, molecular electronics, or optoelectronics.

Concerning the nonlinear behavior of quantum-effect devices, on the one hand this enables the design of very compact gates and memory cells [5]. On the other hand, dealing with distinctive nonlinearities is not in the usual way to design a circuit. The expectation is that taking benefit directly from quantum effects will reduce the number of interconnections and devices in a basic building block. Due to the importance of this principle for nanoelectronics, quantum-effect devices are often named quantum functional devices [62]. The term "functional integration" characterizes this novel strategy of circuit design.

Finally, we like to argue that the question "What is a good computer device?" [33] also strongly depends on the way of interconnecting the devices to perform a basic computation. Let us suppose a simplified worst case scenario to illustrate these ideas. Assume that the first generation of quantum-effect devices would increase the power dissipating of a single device by a certain amount. Now on the first view, there is no reasonable advantage, except if an effective use of functional integration increases the area efficiency at the same time. With this second assumption, the implementation is justified under the precondition that the area efficiency compensates the power dissipation of a single device. Furthermore, it may be worthwhile to study in which way quantum-effect devices and system architecture with an increased degree of parallelism act together. In the best case, the number of clock cycles to calculate the given operation declines and less energy might be consumed when computing an arithmetic function or a

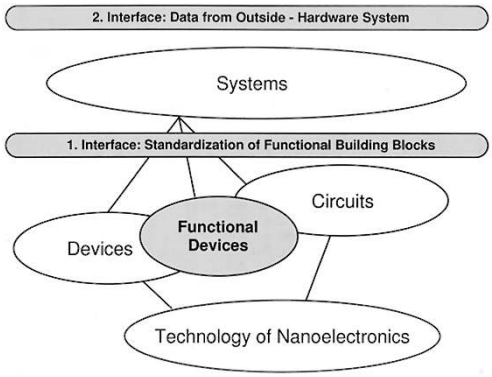


Fig. 5. Possible scenario for nanoelectronic systems implemented with functional devices.

complete algorithm. Thus, functional integration relates parallelism and area efficiency. To emphasize this argument, implementing a circuit with an ineffective architecture that does not satisfy the demands of the technology leads inevitably to a reduced performance compared to existing technologies. During further generations of quantum-effect devices technological improvements also should reduce the power dissipation of single devices. The worst case scenario described here underlines that technological problems might be compensated by the novel design principle of functional integration.

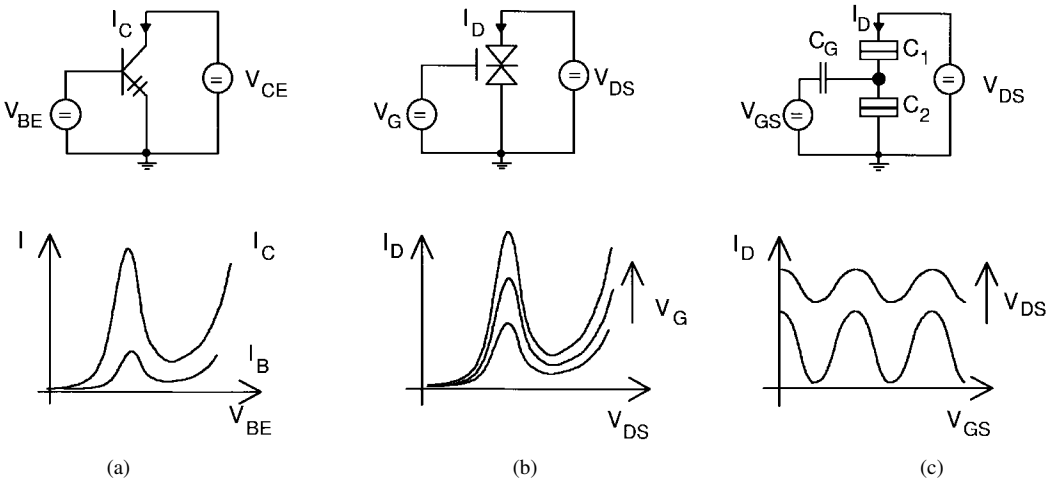
When introducing the principle of functional integration, an obvious question is what happens with the hierarchy of the design, mentioned at the beginning of this section. Do we have the same interfaces as in microelectronics? Giving up the technology invariant design of Mead and Conway, one would clearly loose some advantages. Fig. 5 depicts a possible scenario for nanoelectronics. Building more compact circuits with less devices moves technology, devices and basic circuits more closely together. Thus, the bottom level of design is shifted to a higher level. The second interface in Fig. 5 appears between the external world and the system level, especially for autonomous systems, since they reveal a certain degree of self-organization, as we will see later. Consequently, the strong dominance of software concerning specific applications declines. This may be a substantial advantage of this kind of nanoelectronic systems in application areas such as visual perception and information preprocessing. However, such a nonclassical information processing implemented in nanoelectronics does not mean the end of our conventional computers, because they are still needed for the numerical simulation of new devices, technology processes, and to carry out system studies on a higher level. Generally, a kind of coexistence of both computing paradigms is to be expected.

Nanoelectronics in combination with these novel computational paradigms will take on a significance in those application areas where traditional technology has reached its limits [26]. Considering economic aspects, this effect is possibly strengthened if nanoelectronics offers a more cost-efficient way to produce complex chips. Another motivation to search for new devices results from the prospect to take up powerful circuit concepts from the past, e.g., threshold logic and multiple-valued logic. In most cases their former rejection resulted from missing an area-efficient implementation with existing technologies. With the opportunity to realize these ideas within nanoelectronics, they could reach a practical relevance, as will be outlined in Section IV. Although we always have to keep in mind that the overall performance of such systems has to be superior to the brute force solution consisting of a traditional processor, a large random-access memory, and a sophisticated algorithm. Thus, one should continuously deliberate the advantages and the costs of a new technology. In that context, Landauer claims a critical assessment for new technologies to avoid false estimations, such as happened in the case of optical computing [42].

III. Characteristic Features of Nanoelectronic Devices and Circuits

Today, there are several promising ideas to implement nanoelectronic devices. The most current ones are resonant tunneling devices and single-electron transistors. The fundamental physical principle of single-electron devices is the Coulomb-blockade resulting from the quantization of the elementary charge in isolated node of a double-junction structure [43], [41], [54]. Resonant tunneling devices are based on electron transport via discrete energy levels in quantum-well structures. Since 1974, when Esaki and Chang first observed resonant tunneling [10], the progress in heterostructure epitaxy has lead to quantum-effect devices operating at room temperature with tunable peak current densities and peak voltages. Fig. 6 describes several three-terminal devices and their electrical characteristics. Resonant tunneling is applied in the bipolar quantum resonant tunneling transistor and relatives as well as in the gated resonant tunneling diodes [66], [61]. The single-electron transistor (SET) is an application example of the Coulomb-blockade [Fig. 6(c)] [23]. Since at least three terminals are a precondition to isolate the input from the output, the original two-terminal resonant tunneling diode has been placed into the base-emitter region of a bipolar transistor [9]. Another approach in that direction is extending the diode by a gate contact to change the area or to control the potential inside the quantum well [61]. Regarding a low-power operation, low-valley currents are significant because the valley current in resonant tunneling circuits is related to the off state of the device. Here, CMOS logic gates, dissipating only low power in the nonactive state due to subthreshold leakage, are the guiding example. Thus, the reduction of the valley currents is a challenge to heterostructure epitaxy and might be solved by higher barrier structures of metal–insulator quantum wells [77] or P-N double-well resonant interband tunneling structures [82].

Due to the principle of functional integration, originating from a negative differential conductance or resistance, respectively, the computational capabilities of a single



(a) (b) (c)

Fig. 6. Examples of three-terminal devices based on (a), (b) the effects of resonant tunneling and (c) single charge effects.

quantum-effect device are increased in comparison to field effect (FET) and bipolar transistors [55]. Discussing the application of these functional devices with respect to a functional integration, there are two different strategies. The first one is to extend conventional digital AND-OR-NOT gates to implement more complex Boolean functions such as the XNOR-function with a smaller number of devices. Based on this new logic family, full adder circuits consisting of resonant hot electron transistors or resonant tunneling bipolar transistors have been demonstrated [78].

While this approach primarily aims at reducing the total number of transistors compared to CMOS full adder circuits, the functional integration furthermore enables it to extend the digital logic in the direction of multiple-valued logic (MVL) and neural-like VLSI. Compared to purely digital logic, MVL has some advantages when designing high-speed arithmetic components by avoiding time-consuming carry propagation being inherently in Boolean gates [55]. However, there are several disadvantages, since MVL-circuits often have to be embedded into a conventional digital system and therefore additional circuitry is needed to transform MVL in digital signals and vice versa. Thus, the global system performance plays an important role, too. Furthermore, when reducing the supply voltages, the noise margin for the logic levels in MVL-RTD (resistance temperature detector) circuits decreases and affects the reliability.

On the other hand, multiple-valued logic for storing synaptic weights in neural circuitry preserves a certain robust information processing and reduces the number of circuit components per artificial synaptic circuit [46]. Especially for monolithically integrated neural systems, multistate RTD-memory cells [70] are a promising way to implement area efficient multiple-valued logic circuits. Here, the hope is that the fault tolerance of neural circuits will compensate the errors caused by smaller noise margins.

Recently, in the field of single-electron transistors there have been approaches to build neural-like circuits with an adaptive behavior [24]. The main argument in favor of a neural-like architecture is that randomly fluctuating offset charges on the isolated node of a SET-double junction structure might be compensated by self-adaptation of the circuit. Apart from that, inherent parameter variation when fabricating ultrasmall structures should be considered. This underlines that exploiting the potential of quantum-effect devices is strongly related to the creativity of system designers who decide if a device is suitable for a useful computation or not.

Other physical effects which have not been discussed so far, for example ballistic transport and the electrons wave-like behavior, will become dominant if the fundamental device length is less than the scattering length [18]. This principle leads to electron waveguide devices where the switching between different logic levels is achieved by destroying or conserving the phase coherence of Y-shaped quantum wires [60]. To detect quantum interference effects and exploit them for switching, the operation temperature of these devices is restricted to cryogenic temperatures, that is they operate near the thermal equilibrium [6]. Low-temperature operation avoids the broadening of the resonance effects in the case of temperature-dependent electron phonon scattering. Additionally, temperature-independent scattering processes, that is for example electron-electron interactions, are a disadvantage in that cannot be solved by low temperatures. Thus, it is questionable if quantum interference will satisfy the demands to gain a practical relevance in future integrated circuits.

During the beginning of nanoelectronics, the hybrid integration of quantum-effect devices and conventional field effect transistors is a further approach [56]. Monostable-bistable transition logic elements (MOBILE) incorporate nonlinear effects directly and are aimed to develop linear threshold gates (LTG) [2], [12]. Basically such a hybrid gate consists of two resonant tunneling diodes in series whose peak current is modulated by a gate or by means of a parallel connected field-effect transistor (FET) (Fig. 7). Applying a bias voltage oscillating between the peak voltage V_P and the double peak voltage 2 V_P], the output

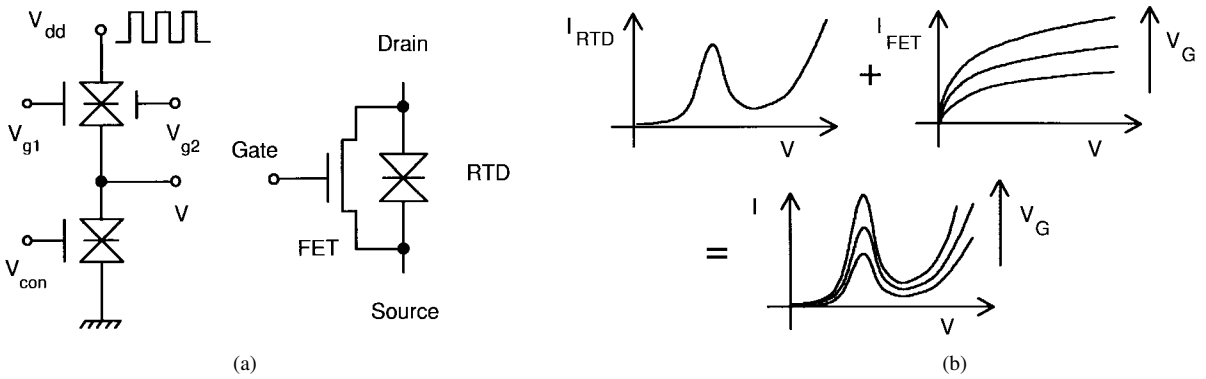


Fig. 7. Application of a MOBILE as a threshold element and schematic illustration of the modulation of the current by hybrid integration of resonant tunneling diode and field effect transistor.

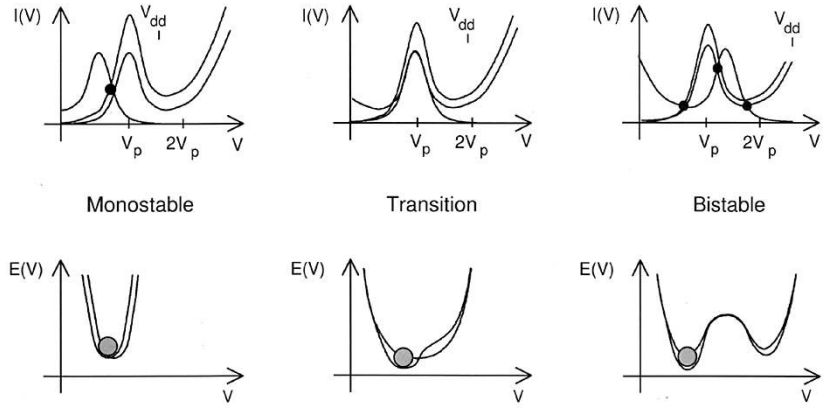


Fig. 8. Current–voltage characteristics and system energy during the transition of a MOBILE from monostability to bistability [52].

node is either monostable or bistable (Fig. 8). The switching of these devices is equivalent to a bifurcation in the theory of dynamical systems. Bifurcation means that the global qualitative behavior, that is whether the output is monostable or bistable, can be changed by varying a control parameter. Here, the control parameter is given by an oscillating bias voltage causing a bifurcation at twice the peak voltage. In the metastable transition state, the MOBILE reacts sensitively to small differences in the peak currents of the upper and lower resonant tunneling diode. This forces the output node voltage V either into the logic high or low level. If the peak current of the diode is modulated with multiple gates or multiple FET's, the resulting modulation current is summed up and the MOBILE performs a threshold function with digital output. It must be emphasized that a circuit family based on threshold logic is able to compute every Boolean function in a network with several layers. The logic function of a single MOBILE depends on the threshold value. By adjusting the control voltage $V_{\rm con}$ at the gate of the lower resonant tunneling diode, the threshold value can be modified after manufacturing. This enables a flexible design of circuits being programmable at the device level. To obtain a reliable switching during the transition, a sufficient difference in the peak currents of the upper and lower branch and a peak-to-valley ratio is necessary. Classifying the signal

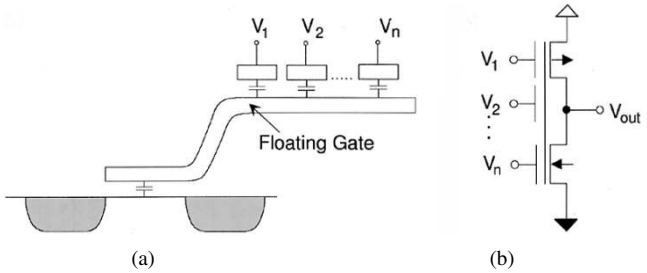


Fig. 9. (a) Neuron-MOS-element and (b) neuron-CMOS inverter, which uses simple capacitive coupling.

codification of MOBILE circuits, these threshold gates might be regarded as a mixed analog–digital gate, because they include the analog computation of the weighted sum as well as reliable digital signal coding of the input and output states. Moreover, a MOBILE behaves as a reset-set-flip-flop with a single parallel FET for each RTD when using a fixed bias voltage [11]. In that case, the set signal is applied to the upper FET and forces the flip-flop in the high state, whereas the reset signal is applied to the lower FET. The prospect to integrate logic functions together with an area efficient static memory is a promising indication to establish nanoelectronic circuits.

A second way to implement a threshold gate on the device level is the Neuron MOS transistor (νMOS) [72].

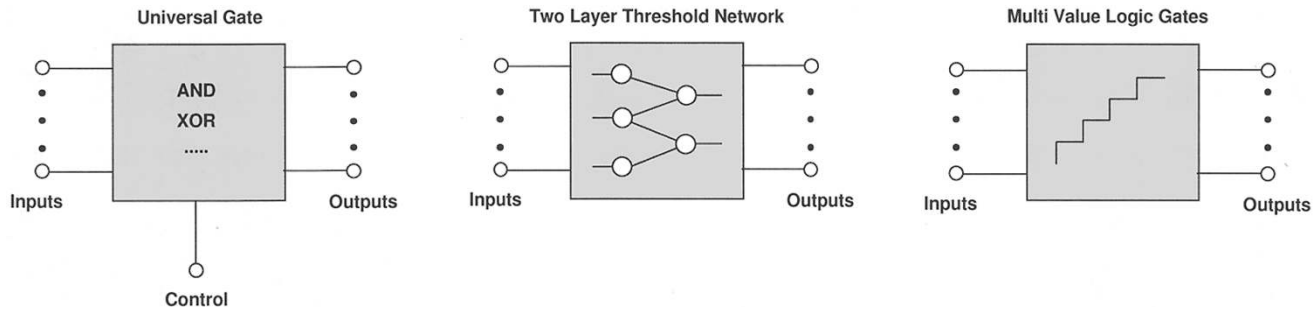


Fig. 10. Programmable universal gates, linear threshold networks, and multiple-valued logic gates as extensions to conventional digital gates.

The νMOS transistor consists of a floating-gate-MOSFET which is capacitively coupled to multiple input gates (Fig. 9). Unlike a MOBILE threshold gate with a signal weighting due to different widths of the input FET's, here each input is weighted by the corresponding coupling capacitor. If the potential of the floating gate exceeds the threshold voltage the MOS-transistor will be switched on. The advantage of the νMOS transistor is the ease of its implementation in CMOS-technology. These functional integrated devices could play an important role in the transition phase between subμm-CMOS and nanoelectronics to build innovative systems and architectures in the next 10–15 years [87].

Summarizing the activities on the level of basic circuit components one hopeful approach is to search for building blocks with an increased functionality. Fig. 10 illustrates the extension of conventional Boolean gates for digital logic by means of soft programmable gates, linear threshold networks, and multiple-valued logic. In connection with universal gates one should also take into consideration Fredkin's idea of reversible digital gates. Reversible logic gates are a special logic family that avoids an energy dissipation caused by the loss of information during a logic transition [21]. The universal behavior of a Fredkin gate results from adding a third input to a two-terminal gate. This third terminal has a certain similarity to the control input of a threshold gate. Apart from their implementation, programmable gates require some memory to store the control signal. Therefore, area-efficient information storage is a precondition for programmable logic circuits. In a certain way, such a soft-programmable hardware may be understood as a kind of downscaling of today's free programmable gate arrays (FPGA's) to the level of post VLSI circuits.

IV. System Architectures

For the design of ultra-large-scale nanoelectronic circuits, fault tolerance, distributed storage, self-organization, modular architecture, and local processing become significant features. They are necessary to overcome the input–output limitations, to solve the testability of the systems, to get a handsome design and integration technology, and may help to eliminate the bottleneck at the interconnection level.

In the following we discuss linear threshold networks, cellular networks, the associative memory, self-organizing feature maps, and biological-orientated networks as new computational paradigms. They may serve as a kind of prototypes for nanoelectronic systems, but at the first sight there seems to be no relationship between them. A deeper analysis of the underlying phenomena shows that all these systems reveal a complex and nonlinear behavior resulting from the fact that they consist of a huge number of interacting subsystems. Furthermore, these phenomena are of great importance when striving for an understanding of macroscopic pattern formation in physics, chemistry, and biology. Here, well-known examples are phase transitions in spin glasses due to interacting magnetic ions [76] and chemical oscillations [19].

Concerning nanoelectronic systems, one strategy is to incorporate certain phenomena appearing in nature, such as self-organization, fault tolerance, parallelism, and adaptive behavior. As mentioned in Section I, these features are recommended to guarantee a reliable computation with nanoelectronic circuits being composed of unreliable switching elements. This opinion may be justified by the fact that the evolution of microelectronics to nanoelectronics will bring us close to physical and technological limits of information processing. An important point is to transfer only some basic principles into an algorithm and not to design a mimicry of a specific part of nature. The prospect is then to implement these algorithms within nanoelectronic circuits. To be more concrete, the analogy between the cellular automata, the well-known Hopfield model of artificial neural networks, and spin glasses results from arranging the basic constituents, e.g., automata, neural cells or ions on a rectangular grid. In addition the interaction of this basic constituents are expressed by a set of similar mathematical equations which can be treated with methods derived in statistical physics [58], [31]. Only this mathematical abstraction allows to later search for a possible implementation, which is then restricted by physical, technological, and economic boundary conditions. Similar ideas have been discussed in the past by Wolfram in connection with "complexity engineering" [92], in the field of synergetics by Haken [28], and in bio-inspired VLSI by Vittoz and Mead [85], [51]. Asking for a short and pregnant characterization of these strategy, the art of nanoelectronic engineering is strongly related to our capability to cope with large interacting systems. Designing these systems, which are inspired by phenomena emerging in nature, is a

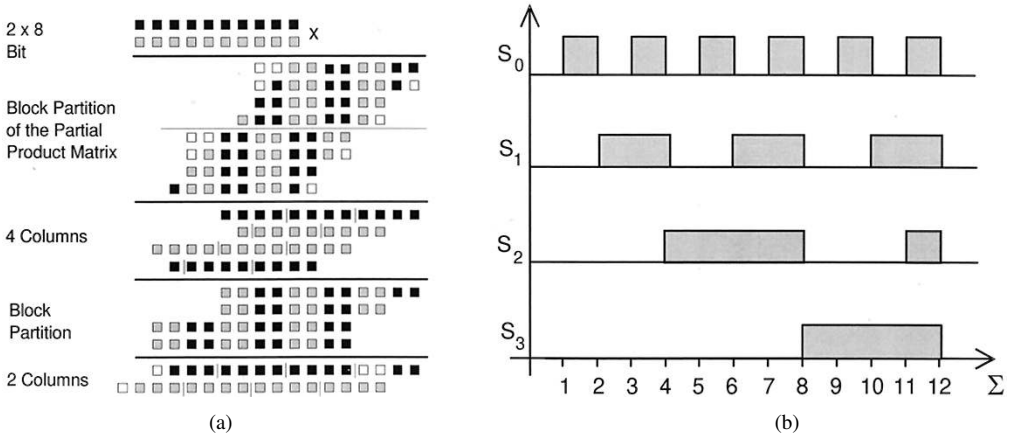


Fig. 11. Hierarchical block-save addition for multi-operand addition with linear threshold networks. The output bits are periodic functions of the weighted sum. (a) Multiplication algorithm. (b) Output bits of a single 4×2 block.

great challenge for scientists and engineers, especially when we consider there is no existing computational paradigm today, including all the famous features in one we have stated in short. The recent work done in the field of neural VLSI, threshold logic, and cellular networks gives the first impression of how to encounter this challenge [25], [27], [13], [14].

A. Computation of Arithmetic Functions with Linear Threshold Networks

Before we focus on neural circuits, we outline the application of linear threshold gates (LTG's) for digital computation. Although LTG's are equivalent to McCulloch–Pits neural cells, they are also capable of computing arithmetic function. Usually, the idea behind neural VLSI is an approximation of a given input–output relationship after the network has finished a learning algorithm. In contrast to that, the following section describes how to exactly calculate Boolean functions in a linear threshold network (LTN) with fixed weights. In a previous section, we have seen that LTG's might be implemented with a few number of devices as MOBILE or νMOS. The advantages of LTG's are the higher computational capabilities compared to Boolean gates commonly used in purely digital logic [75]. Although LTG's are capable of emulating AND, OR and NOT gates, a purely replacement of those gates would be a very trivial method. Normally, this procedure leads to large feed-forward networks with a depth of many layers and long delay time. In this case, there is only a less increased overall performance. A more adequate and less resource consumptive approach are networks of small depth being optimal adapted to a prescribed arithmetic function. Here, block save addition and other algorithms serve as an example to increase the speed of digital multiplication by an efficient reduction of a multi-operand matrix [17], [83], [84].

The reduction of a multi-operand sum consisting of $m \times n$ bit operands toward a two operand sum is a key component for fast multiplication. The multi-operand sum results from a bitwise multiplication of the binary multiplicands and the shifting of the partial products afterwards. Summarizing the steps of the algorithm, the operands are arranged in a matrix and used as inputs for a linear threshold network. Each square in Fig. 11(a) represents a bit of the partial product matrix. The idea is now to partition the matrix into blocks of at the most (4×2) bits. Each block-sum is a parallel counter with eight inputs and calculates an output of 4-bit word length. The intention to perform a matrix partition is to avoid a carry propagation, the main time-consuming operation during the addition. Arranging the sum bits in a nonoverlapping way allows an efficient reduction of the partial product matrix. After two successive block save operations, the former partial product matrix is reduced to two operands which could be added with a fast carry look ahead adder. Fig. 11(b) shows that the output bits are a periodical symmetric function of the weighted input sum Σ. Thus, an intrinsic relationship between the weighted input sum and the desired output simplifies the evaluation of the block-sum to depth-2 networks (Fig. 12). The network's task is now to detect all those intervals where the output equals the logic high level. Nevertheless, there is no doubt that LTG's will only become an alternative to traditional Boolean logic, if the costs of a single threshold gate are comparable to those of Boolean gates. This example conveys an impression about the mutual dependence of an advanced technology (MOBILE and νMOS circuits) on the one hand and advanced systems (LTN's) on the other hand. In the past, the area inefficiency of single LTG was the main reason that similar algorithms for fast multiplication had no relevance in practice.

B. Cellular Array-Based Computation

By arranging linear threshold gates on a rectangular grid and restricting the interconnections to the local neighborhood, one obtains a regular two-dimensional processing array. Today there exist several variations, such as cellular automata (CA) and the cellular neural networks (CNN) [15], [29], [57], [58] (Fig. 13). In principle, one has to distinguish between a discrete and a continuous time behavior, as well as between the discrete and continuos

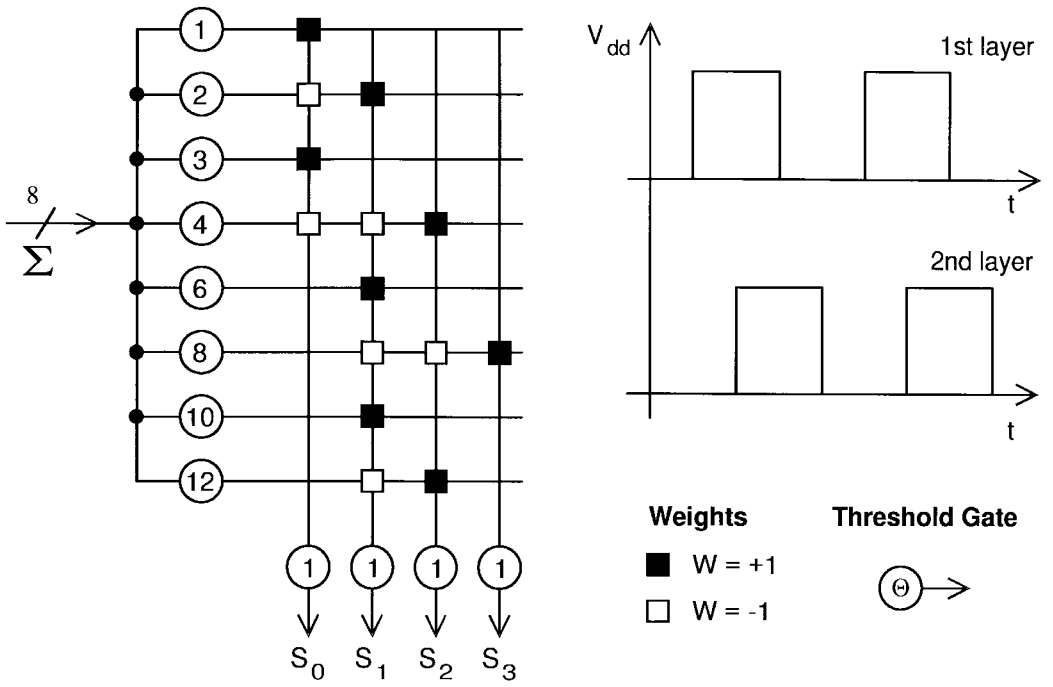


Fig. 12. Depth-2 linear threshold network for the computation of the digital block sums. The connection array consists of bipolar weight connections.

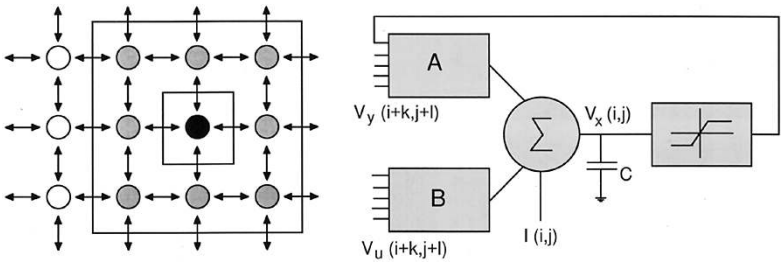


Fig. 13. Topology of a cellular neural network and block scheme of a cell.

states of the locally coupled processing units. However, the temporal evolution of the processing units is given either by a system of differential (difference) equations for cellular neural networks or by a special code that has to be stored in a look up table in the case of cellular automata. As a consequence of this regular arrangement, spatial homogeneous cellular arrays find an application as the preferred method for parallel image processing. The cellular arrays that are of interest for nanoelectronics are those revealing a specific structure defining the directed information flow inside the network. This means automata networks with an arbitrary function and a special topology have to be mapped onto a cellular array of quantum-effect devices. To simplify the manufacturing of those arrays, they should be as homogeneous as possible, thus being in a certain contradiction to function specific structures. With respect to self-organizing phenomena the fourth class of cellular automata reveals some aspects of the desired behavior [91]. Starting from an initial state, they create localized and propagating structures, which might be used for information processing [88]. A disadvantage is the missing of a simple programming method via the edges of an array. Neuromorphic architectures are a possible solution for low-level perceptual tasks. They consist of coupled quantum dot arrays and are the ultimate level of solid-state electronics [5]. Apart from the underlying quantum mechanical treatment of the electrons, the main difference between these quantum dot arrays and our solid state circuits today is the fact that there will be no wires between the devices. The data between two devices could be transferred by electrostatic coupling or by tunneling processes. Nevertheless, the key question will be, how to implement the modifiable connections to change the interaction rules between the quantum dot cells. Consequently, one has to tackle the problems arising from a missing long-range data transfer in a specific direction and from a lack of an easy programming method.

A well-known system architecture that has been developed for special-purpose computers and reveals a great topological similarity to the cellular arrays is the systolic array [40]. The dataflow in this two-dimensional array is inspired by the blood circulation and leads to a pipelining of the data [Fig. 14(b)]. The boundaries of the array serve as an external connection for data input.

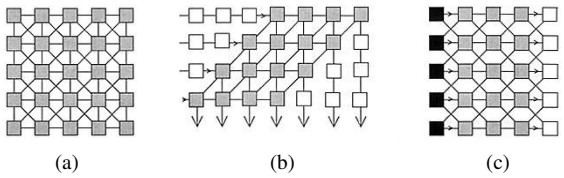


Fig. 14. Cellular array-based computation with several locally interconnected architectures. (a) Cellular neural network/cellular automata. (b) Systolic array. (c) Sparsely interconnected feed-forward network.

Here, the main differences compared to CNN and CA are a defined, directed signal path connecting the processing units that calculate simple arithmetic functions. The main application of systolic arrays is digital signal processing. Like in cellular neural networks for image processing, the application determines the interconnections and the function of a single cell. Thus, the searching for an optimal interconnection in a systolic array chip is comparable to the adaptation of the weight connection (templates) in a CNN. If there are suitable methods to design a systolic algorithm for a given application, an implementation with quantum-effect devices would allow to increase the density of the processing units for high-performance digital signal processing circuits.

In addition, sparsely interconnected feed-forward networks [Fig. 14(c)] consisting of an input layer, several hidden layers, and an output layer are a further possibility for realizing a directed signal path [1]. Although these architecture is inspired by feed-forward neural networks, their applications are not necessarily restricted to the field of neural algorithms and depends on the capabilities of the cells. When extending cellular arrays, the connections among the cells may be composed of nonmonotonous functions similar to fuzzy-membership functions [64]. That is to say, each cell becomes a kind of primitive fuzzy processor. In connection with a multiple-layer architecture, this approach aims at hybrid information processing systems, where some preprocessing tasks take place in a cellular fuzzy system, whereas subsequent layers contain adaptive components.

C. Distributed and Fault-Tolerant Storage Principles in the Associative Matrix

Two-layer linear threshold networks with modifiable weight connections are a simple method to implement a memory with distributed storage and associative behavior. This kind of memory is commonly known as associative matrix [59] and consists of an $n \times m$ matrix W with binary connection weights that correspond to the synapses of an artificial neural net (Fig. 15). Due to a shallow network topology without feedback-loops and hidden layers, the basic operation is very simple. Using digital inputs and outputs,

an associative matrix maps, a finite set of input patterns $\boldsymbol{X}$ onto a corresponding set of output patterns $\boldsymbol{Y}$.

In the phase of an associative recall the matrix computes a response Y to an input X by parallel evaluation of the

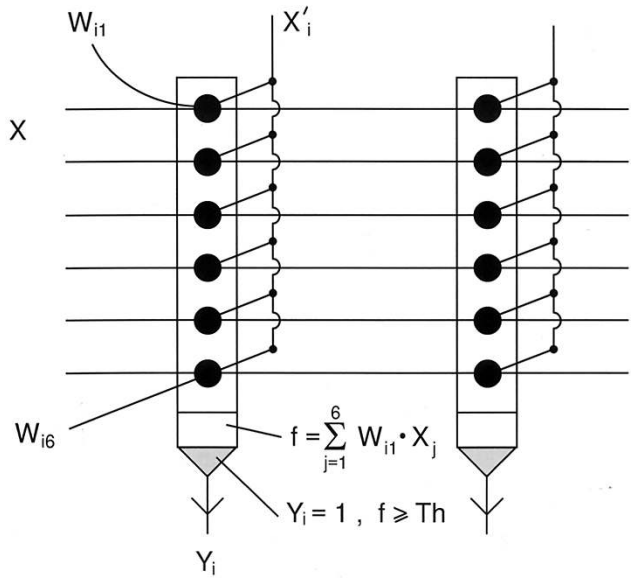


Fig. 15. Functional diagram of the associative matrix. During programming, the learning rule sets the binary weights to one if both the input and output are high.

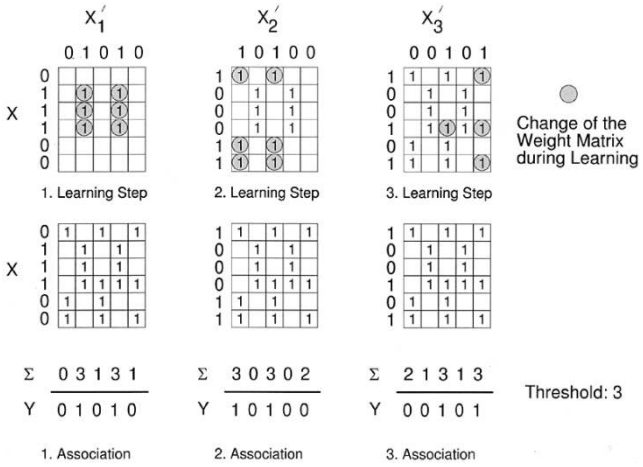


Fig. 16. Function of the associative matrix, demonstrated for an simplified 6 × 5 matrix.

activation of the neurons. During learning, the synaptic weights are set by a "one-shot" learning method. For every pair of training patterns (X', Y) the weight W_{ij} (element of matrix W) is set to one, if both X'_i and Y_j equal one. Otherwise, the weight remains unchanged. The learning thereby obeys to the simple Hebbian rule, that is, the weight of a synapse is changed in order to support the correlation of activations of the neurons it connects.

Since an output Y_j is computed from the weighted sum of all inputs to column j, the information is stored in a distributed way (Fig. 16). From the learning procedure it is obvious that the matrix can only store a certain number of pattern-pairs. The information amount stored in the matrix will reach zero again if all weights are set to one. Palm has shown that the asymptotic storage capacity of an associative matrix is 0.69 $n\,m$ bit [59]. Both input and output patterns should be sparsely coded, i.e., l out of n bits in X and

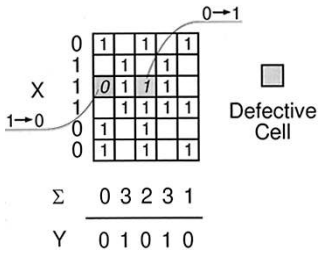


Fig. 17. Fault tolerance of the associative matrix for the example shown in Fig. 16.

k out of m bits in Y are set to one while l and k are small compared to n and m, respectively. The number of patterns that can be stored in an associative matrix then is approximately $(0.69\ n\ m)/(l\ k)$ and hence much larger than the number of neurons. The error rate of an associative recall depends on the amount of stored information and is a drawback of this kind of memory architecture. Restricting the number of weights storing a one reduces the number of errors as well as the whole storage capacity.

The threshold value applied in the neurons corresponds to the number l of ones of the input patterns. If the computation should compensate faults in the inputs and/or in the matrix itself, the threshold value has to be lowered. Naturally, this will decrease the storage capacity further. Besides hetero-association, a fault-tolerant auto-association can be implemented if a mapping of X to X is stored in a symmetrical $n \times n$ matrix.

The associative memory has been designed in different VLSI architectures using digital, digital/analog, and analog circuit techniques [65]. A preliminary step are compact memories that store the weights of the synapses and include the learning algorithm. The cell can easily be implemented since it only consists of a bistable element and some additional switches. The modular circuit design and the associative operation make this concept attractive to nanoelectronics. If the number of memory cells becomes very large, the fault-tolerance against hardware failures and data errors compensates the disadvantage of the limited storage capacity (Fig. 17).

D. Self-Organizing Feature Maps

The challenge of modeling the function of the brain has lead to the concept of self-organization in artificial neural networks. Self-organizing feature maps, invented by Kohonen [37], are very powerful neural networks that can project a set of d-dimensional vectors onto a two-dimensional array of $(n \times m)$ processing units. Each processor unit stores a d-dimensional vector of real values, which is determined by a learning algorithm during the training phase of the map. The algorithm arranges similar vectors closely together and preserves the topological relations of the data structures. The self-organizing feature map determines independently the location of the stored vectors in a useful and ordered manner (self-optimization). During the learning phase the input vectors are fed into the array of processing units via d input lines in parallel and in random sequence. Each processor unit computes the information distance of the input vector and the stored vector. After searching for the winning neuron with the most similar vector, the vectors of the winning neuron and its neighborhood change to resemble the input vector.

This change occurs according to an adaptation function that increases and contracts slowly during the training of the map. Fig. 18(b) shows the adaptation strength of the winning neuron and its neighbors in one adaptation step. The adaptation algorithm of a self-organizing feature map reveals a similarity to partial differential equations. With certain modifications, basically the introduction of a system energy measuring the distance of a given input to the weight vectors, this similarity leads to a local adaptation equation. Concerning the type of the differential equations, Schrödinger-like equations as well as the diffusive Haken model have been studied [81], [69].

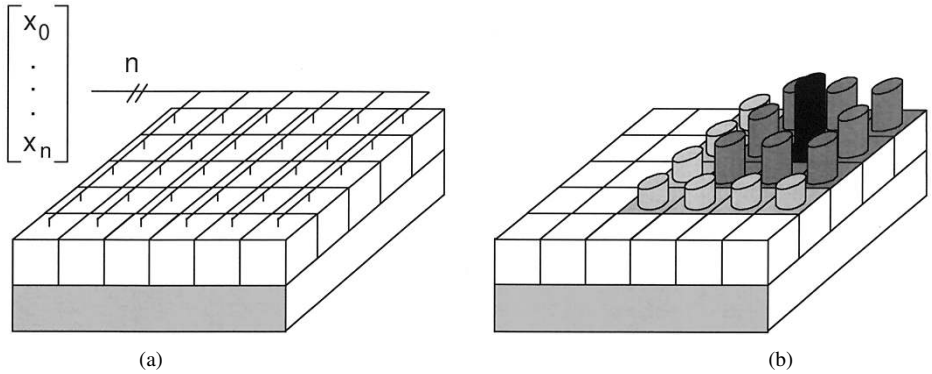
The topological preserving and dimensionality reducing mapping of a self-organizing feature map can be used for unsupervised feature extraction (Fig. 19). In a hybrid system, i.e., a system that combines different computational paradigms to solve a given task of cognition, a self-organizing feature map might be a successful system for the preprocessing of data. Important properties of the self-organizing feature map for its functional integration in VLSI or ULSI hardware are adaptiveness, modularity, and fault tolerance of the structure [67].

Apart from the denotation of self-organization to characterize an unsupervised learning algorithm, in nanoelectronics, the term self-organization often stands for creating fine structures without external influence, for example atoms that organize themselves in a way to form pyramids on a substrate [90]. It follows that self-organization is relevant both for manufacturing ultrasmall structures and in the development of adaptive algorithms.

E. Perception in Highly Dynamical, Neural-Like Systems

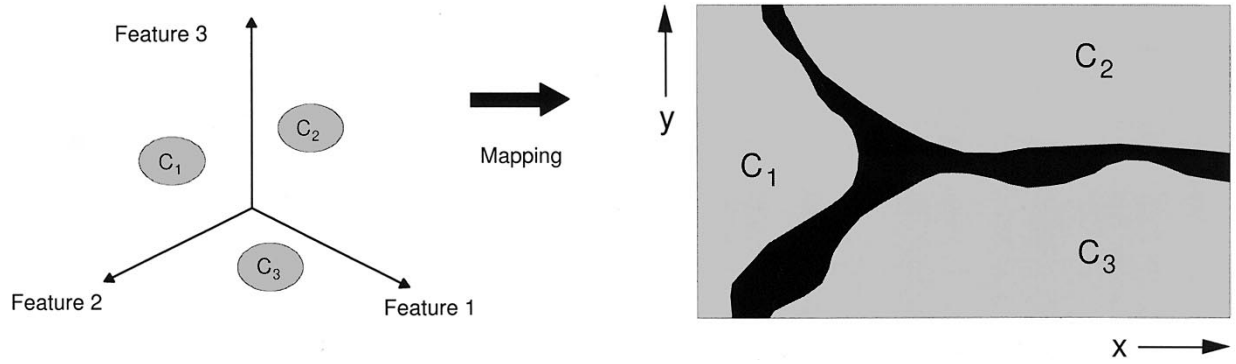
The performance of the biological system "brain" has grown in an evolutionary process to meet the requirements of the environment in an excellent way. Today, we are able to explain only basic phenomena and are still far away of comprehending the total complexity of brains. However, the VLSI designers can take benefit from some fundamental principles of information processing and storage. These are actually understood and comply with the requirements of nanoelectronic systems like self-organization, fault-tolerance, and high-performance computation due to massive parallelism. In addition, aspects like local learning algorithms and dynamic processing will probably play an important role for the future design of adaptive systems, too.

In nanoelectronics, problems of long-path data transfer as mentioned above make global learning methods unsuitable for the systems. Biological-oriented artificial neurons use local strategies where only signals in the neighborhood of the neuron are needed, for example a modified Hebbian learning rule combined with a nonlinear adaptation [30], [49]. Time-continuous signals achieve the task of local



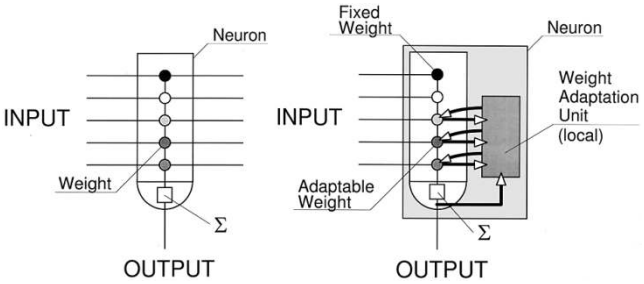
(a) (b)

Fig. 18. (a) Self-organizing feature map and (b) adaptation of the weights in the neighborhood of the best matching cell.



(a) (b)

Fig. 19. (a) Application of a self-organizing feature map for clustering and (b) dimensionality reduced mapping of the data clusters from a three-dimensional space onto the map.



(a) (b)

Fig. 20. Comparison of (a) a conventional perceptron and (b) a neural cell including a local weight adaptation without the necessity of global information.

learning as well as local input–output processing at the same time on a cell level (Fig. 20). On the way toward adaptive nanoelectronic systems, these approaches may play an important role. Connecting such cells we can perform complex autonomous systems for controlling purposes with a small number of neurons [8]. The important feature of dynamic processing and adaptation in the approach of Fig. 21 is based on a continuous flow of signals through the whole system. In this case, the characteristic properties are dynamical processes on two different time scales; short-term dynamic is introduced to process the actual data. The introduction of the nonlinear characteristic of the cells is suitable for causal detection purposes and for storing time-dependent dynamic information. With a view to hardware implementation, the correlation of signals can be detected by applying nonlinear low-pass filtering. Long-term dynamic exploits this effect in the low-dynamic part of the neuron to adapt the coupling between different cells. The analysis of actual information in the short-term memory leads to an increase or decrease of the low-dynamic weights in the long-term memory. These have a direct impact on the actual information processing. The introduction of fixed weights realizes a "hard-wired" behavior of the system. Beside the ideas mentioned above, other approaches deal with the implementation of biological concepts for low-level perception such as the silicon retina [51] or the modeling of biological neural elements and their implementation into electrical systems [48], [45]. In developing even larger neural-like systems, complex nonlinear dynamics might play a decisive role. The investigation of biological systems, especially parts of the brain, indicate computation based on nonlinear dynamics and deterministic chaos. A detailed investigation of the olfactory system and its dynamics had been conducted by Freeman *et al.* [93], [22]. Conclusions drawn from EEG-diagrams point out that deterministic chaos is the property that makes perception possible. The macroscopic measurements by the EEG have been simulated and investigated on the microscopic level by systems of coupled neurons. The attractors of the dynamical systems refer to different stimuli that have been trained,

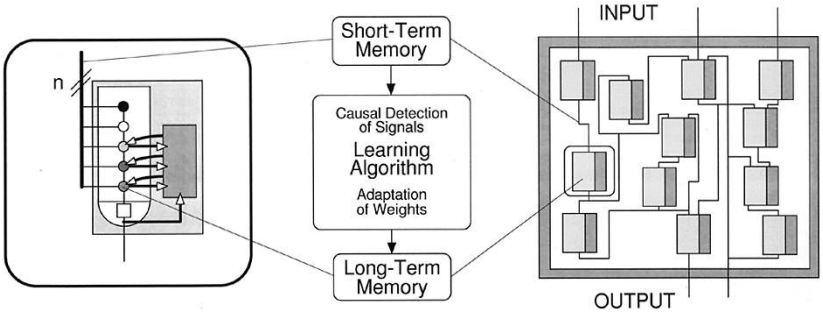


Fig. 21. Realization of an associative memory which operates locally and continuously similar to brains. The correlation between short- and long-term memory is due to the learning algorithm.

both in the biological and in the artificial system. It has to be noted that the attractors actually measured do not refer to fixed points (static attractors) but to patterns of oscillation.

Furthermore, the examination of the whole olfactory system shows a structure of different layers. Each layer refers to different functions, namely sensoring, preprocessing, evaluation, and, through connections of the olfactory cortex and other parts of the brain, correlation with knowledge.

Some similarity can be discovered between these functional layers and the models described above. The close locality of sensor receptors that respond to similar stimuli indicate a similar formation like in the self-organizing feature map. The massively correlated action of the neurons in the olfactory bulb indicates a training of the synapses by the Hebbian rule. On the lowest dynamical level, the bulbwide activity hint at a distributed and highly fault-tolerant memory storage found in a large associative matrix. But real understanding of the perception is expected only from the study of high order dynamical systems. Today, research in connectionist models, i.e., artificial neural networks, are dominated by the investigation of geometrical models instead of dynamical ones [71]. This is justified if the asymptotic states are represented by static attractors. A serious drawback of dynamical connectionist models lies in their limited explanation capabilities. A problem connected with this is that explicit knowledge cannot be easily integrated in the system. But investigations of models that combine knowledge and connectionism in hybrid systems are in the line of current research [71].

High dynamic systems can also be studied in a cellular automaton (CA). It is important to note that unlike in the brain, the cells in a CA are only locally connected. In 1986, Wolfram proposed methods for complexity engineering [92] using his model of CA. This and other paths are followed by a working group on "computational mechanics" of the Santa Fe Institute [68]. The research is driven by the question "How is information processing embedded in dynamical behavior?" Approaches elsewhere include quantum mechanical systems [63], fractals, and many more [86].

Even if connectionist models will be restricted to applications in the lowest level of perception, i.e., analysis and recognition of signals, there are plenty of tasks in this area that have not yet been solved successfully. Models of human perception become more and more important in information transmission [32], as transfer rates approach a technical limit. This might soon be the case for information processing, too. In this connection, a very interesting observation is the significance of nonlinear dynamics in quantum-effect devices and in biological information processing. As we have seen, certain nonlinear phenomena, such as relaxation into equilibrium points and bifurcations appear in the MOBILE circuits (Section III) as well as in temporal patterns, e.g., limit cycles and chaotic behavior of biological neural networks. The link between this two different levels is the common mathematical formulation.

V. Potential of Future Technologies

At the moment, CMOS technology on silicon is the dominating technology for microelectronic systems as mentioned in Section I. Fig. 22 shows a technology landscape until the year 2015 to give an overview about the whole area of potential technologies for information processing. Apart from solid-state nanoelectronics other technologies such as optoelectronics, superconductive and molecular electronics are depicted.

By means of lateral nanostructuring, it is expected that today's quantum-well devices are extended in the directions of quantum wires and quantum dots. Thus, two- and three-dimensional quantized structures currently being a intensive topic of fundamental research might find an application. An important question with economical consequences is whether the quantum-effect devices can be monolithic integrated on silicon or not. In the worst case, when nanoelectronics is limited only to III-V semiconductors, it is doubtful if the semiconductor industry will leave the established field of silicon material and invest into cost-intensive III-V semiconductor fabrication lines. In spite of this, from the technological point of view it seems to be useful to develop quantum-effect devices in a first phase within III-V semiconductors and to transfer some device principles to nanoelectronics based on silicon afterwards.

An interesting solution to overcome the interconnection problem is the monolithic integration of optoelectronic devices for data transfer together with quantum-effect devices for computation. These hybrid technologies with optical interconnection networks are discussed for the interchip and

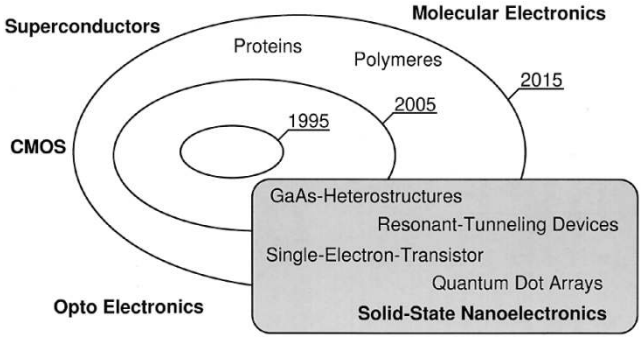


Fig. 22. Landscape of different technologies for future information processing.

interboard communication of high-performance computing systems [47]. Furthermore, artificial neural networks with high-density optical interconnections between the several neural chips have been demonstrated [39], [80]. Combining light-emitting devices with nanoelectronic processing units is not as speculative as it seems when considering that both are based on III-V semiconductor heterostructures.

Superconductivity originating from a pair of interacting electrons (Cooper pair) had only limited success in circuit design. The main advantages of superconductive electronics is the high-speed operation of the devices and the simple design of static memories, where a signal is stored within a superconducting current loop. In spite of the advantages on the field of high-temperature superconductors, the problem of cooling has not been solved under consideration of compatible technologies. The combination of superconductivity for memory function and single-electron transistors as switching devices may be a solution which should also be considered on a long-term range.

Computing at the molecular scale is a further vision for the future [16], [74]. The signals in molecular computing are represented by the concentration of a special kind of molecules in the chemical reactor (watery solution). Information transfer inside this chemical reactor takes place by means of Brownian motion. This solves the urgent problem of wiring in an elegant way by the thermal motion of molecular information packets, but this data transfer being free of costs is very slow compared with electrons in semiconductors or metals. A further drawback is that chemical reactions of a specific sort of molecules, here being equivalent to the processing of signals, occur only with a certain probability. Consequently, computing on a molecular scale incorporates statistical phenomena, and fault-tolerant computing paradigms are a condition to solve the problem of a reliable computation with unreliable components. The simulation of computation with unreliable elements is simplified by the analogy to evolutionary processes in bit-string. In computer science the term "emergent computation" is used for this new paradigm [3].

At the horizon the quantum computer appears as final goal of human-made information processing [20], but it is still an open question whether quantum mechanical computation is an outstanding solution or is just a fata morgana. In this field, applications such as quantum cryptography and quantum teleportation have been demonstrated [7]. Today, these ideas today are far away from an implementation.

VI. Conclusion and Outlook

Scientists and engineers engaged in the design of nanoelectronic systems and devices have to demonstrate the capability to realize complete powerful integrated circuits including memory functions and logic on one chip as it is possible with silicon CMOS technology. The main intention of this paper is to emphasize the requirement of adequate system architectures. Furthermore, the presented systems have been related to the intrinsic properties of future devices, since the total performance of nanoelectronic systems strongly depends on the usefulness of functional integration as design principle. With respect to the prediction of the SIA roadmap and an average time-to-market of about 15 years for a new technology, monolithically integrated circuit components based on quantum-effect devices should be developed until the year 2000. In this case, solid-state nanoelectronics might reach a level to compete with a post CMOS silicon technology in the year 2015. Within the next five years, the development of a silicon-based nanoelectronics should become a main goal of the technology to combine quantum-effect devices with present electronics based on CMOS.

References

[1] L. A. Akers, D. K. Ferry, and R. O. Grondin, "Synthetic neural systems in the 1990s," in *An Introduction to Neural and Electronic Networks*, S. Zornetzer *et al.*, Eds. New York: Academic, 1995, pp. 359–387.

[2] T. Akeyoshi, K. Meazawa, and T. Mitzutani, "Weighted sum threshold logic operation of MOBILE (Monostable-Bistable Transition Logic Element) using resonant-tunneling transistors," *IEEE Electron Device Lett.*, vol. 14, no. 10, pp. 475–477, Oct. 1993.

[3] W. Banzhaf, "Self-replicating sequences of binary numbers—The build-up of complexity," *Complex Syst.*, vol. 8, pp. 205–215, 1994.

[4] D. Bartelink *et al.*, "Processes of the future," *Solid State Technology*, vol. 38, no. 2, 1995, pp. 43–54.

[5] R. T. Bate, "Introduction to nanoelectronics," *Texas Instrument Tech. J.*, vol. 6, pp. 2–49, 1989.

[6] ——, "Requirements for a post-VLSI integrated circuit technology," *Future Electron Devices J.*, vol. 4, pp. 5–9, 1993 suppl.

[7] T. Beth, M. Grassl, and T. Pellizzari, "Codes for quantum erasure channel," *Phys. Rev. A*, vol. 54, no. 4, pp. 2698–2703, 1996.

[8] A. Buehlmeier, G. Manteuffel, M. L. Rossmann, and K. Goser, *Robot Learning in Analog Hardware*, in *Artificial Neural Networks—Proc. ICANN 96*, C. von der Marlsburg *et al.*, Eds. Berlin: Springer, 1996, pp. 311–316.

[9] F. Capasso *et al.*, "Quantum-effect devices," in *High Speed Semiconductor Devices*, S. M. Sze, Ed. New York: Wiley, 1990.

[10] L. L. Chang, L. Esaki, and R. Tsu, "Resonant tunneling in semiconductor double barriers," *Appl. Phys. Lett.*, vol. 24, no. 12, pp. 593–595, 1974.

[11] K. J. Chen, T. Akeyoshi, and K. Meazawa, "Reset-set flip-flop based on a novel approach of modulating resonant-tunneling current with FET gates," *Electron. Lett.*, vol. 30, no. 21, Oct. 1994, pp. 1805–1806.

[12] K. J. Chen, T. Akeyoshi, and K. Meazawa, "Monolithic integration of resonant tunneling diodes and FET's for monostable-bistable transition logic elements (mobile's), *IEEE Electron Device Lett.*, vol. 16, no. 1, pp. 70–73, Feb. 1995.

[13] L. O. Chua, L.Yang, "Cellular neural networks: Theory," *IEEE Trans. Circuits Syst.*, vol. 35, no. 10, Oct. 1988, pp. 1257–1272.
[14] L. O. Chua and L. Yang, *Cellular Neural Networks: Application*, *IEEE Trans. Circuits Syst.*, vol. 35, Oct. 1988, no. 10, pp. 1273–1290.
[15] L. O. Chua and T. Roska, "The CNN paradigm," *IEEE Trans. Circuits Syst.-I*, vol. 40, no. 3, Mar. 1993, pp. 147–156.
[16] M. Conrad, "The lure of molecular computing," *IEEE Spectrum*, vol. 23, pp. 55–60, Oct. 1986.
[17] L. Dadda, "Some schemes for parallel multipliers," *Alta Frequenza*, vol. 43, pp. 349–356, 1965.
[18] J. H. Davies and G. Timp, "The smallest electronic device: An electron waveguide, in heterostructures and quantum devices," N. G. Einspruch, Ed. New York: Academic, 1994, pp. 385–416.
[19] I. R. Epstein, "Chemical oscillators and nonlinear chemical dynamics," in *Proc. 1989 Complex Systems Summer School*, Santa Fe, NM, and *Lectures in Complex Systems*, vol. II, Erica Jen, Ed., Santa Fe Institute Studies in the Science of Complexity. Dedham, MA: Addison-Wesley, pp. 213–269.
[20] R. P. Feynman, "Quantum mechanical computer," *Optics News*, vol. 11, pp. 11–20, 1985.
[21] E. Fredtkin and T. Toffoli, "Conservative Logic," *Int. J. Theoretical Physics*, vol. 21, pp. 219–253, 1982.
[22] W. J. Freeman, "The physiology of perception," *Sci. Amer.*, vol. 264, pp. 34–41, Feb. 1991.
[23] L. J. Geerlings, "Charge quantization effects in small tunnel junctions, in physics of nanostructures," in *Proc. Thirty-Eight Scottish Universities Summer School in Physics*, July 1991, NATO Advanced Study Institute, pp. 171–204.
[24] M. Goosens and A. H. M. van Roermund, "Single Electron Tunneling Technology for Neural Networks," in *Proc. Sixth Int. Conf. on Microelectronics for Neural Networks and Fuzzy Systems*, Lausanne, Feb. 1996, pp. 125–130.
[25] K. Goser, U. Hilleringmann, U. Rueckert, and K. Schumacher, "VLSI technologies for artificial neural networks," *IEEE Micro 9*, 1989, pp. 28–45.
[26] K. Goser, "Tunneling and thermal noise as limiting factors in microelectronics," in *Proc. Microelectronics and Reliability 28*, 1988, pp. 605–611.
[27] K. Goser, "Implementation of artificial neural networks into hardware: Concepts and limitations," *Mathematics and Computers in Simulation*, vol. 41, pp. 161–171, 1996.
[28] H. Haken, *Information and Self-Organization—A Macroscopic Approach to Complex Systems*, Springer Series in Synergetics. Berlin: Springer, 1988.
[29] H. Harrer and J. A. Nossek, "Discrete-time cellular neural networks," *Int. J. Circuit Theory Appl.*, vol. 20, pp. 453–468, 1992.
[30] D. O. Hebb, *The Organization of Behavior*. New York: Wiley, 1949.
[31] J. J. Hopfield, "Computing with neural circuits: A model," *Science*, vol. 233, pp. 625–633, Aug. 1986.
[32] N. Jayant, J. Johnston, and R. Safranek, "Signal compression based on models of human perception," *Proc. Inst. Elec. Eng.*, vol. 81, pp. 1385–1422, Oct. 1993.
[33] R. W. Keyes, "What makes a good computer device?," *Science*, vol. 230, pp. 138–144, 1985.
[34] R. W. Keyes, "Physics of digital devices," *Rev. Modern Phys.*, vol. 61, pp. 279–287, 1989.
[35] R. W. Keyes, "Electronics in large systems," in *Molecular Electronics and Molecular Electronic Devices*, vol. 1, K. Sienicki, Ed. Boca Raton, FL: CRC, 1993, pp. 1–30.
[36] S. Kimura, A. Asai, and S. Okayama, "Progress of QFD projects at each company," *FED J.*, vol. 6, suppl. 2, 1995, pp. 20–23.
[37] T. Kohonen, "The self-organizing map," *Proc. IEEE*, vol. 78, pp. 1464–1480, 1990.
[38] B. Kosko, *Neural Netwoks and Fuzzy Systems, A Dynamical Systems Approach to Machine Intelligence*. Englewood Cliffs, NJ: Prentice Hall, 1992.
[39] A. Krishnamoorthy *et al.*, "A scaleable optoelectronic neural system using free-space optical interconnects," *IEEE Trans. Neural Networks*, vol 3, no. 3, pp. 404–413, May 1992.
[40] H. T. Kung, "Why systolic architectures?," *IEEE Computer*, 1982, pp. 37–46.
[41] L. S. Kuzmin, P. Delsing, T. Claeson, and K. K. Likjarev, "Single-electron charging effects in one-dimensional arrays of ultrasmall tunnel junctions," *Phys. Rev. Lett.*, vol. 62, 1989, pp. 2539–2542.
[42] R. Landauer, "Needs for critical assessment," *IEEE Trans. Electron Devices*, Oct. 1996, pp. 1637–1639.
[43] K. K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions," *IBM J. Res. Develop.*, vol. 32, no. 1, pp. 144–158, 1988.
[44] H. C. Lin, "Resonant tunneling diodes for multi-valued digital applications," in *Proc. 24th Int. Symp. Mulitvalue Logic*, 1994, Boston, MA, IEEE Computer Society Press, pp. 188–195.
[45] B. Linares-Barranco *et al.,* "A CMOS implementation of Fitz–Hugh–Nagumo neuron model," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, July 1991, pp. 956–965.
[46] H. J. Levy and T. C. McGill, "A feedforward artificial neural network based on quantum effect vector-matrix multipliers," *IEEE Trans. Neural Networks*, vol. 4, no. 3, May 1993, pp. 427–433.
[47] A. Louri and H. Sung, "3D optical interconnections for high-speed interchip and interboard communications," *IEEE Computer*, vol. 27, no. 10, Oct. 1994, pp. 27–37.
[48] M. Mahowald and R. Douglas, "A silicon neuron," *Nature*, vol. 354, 1991, pp. 515–518.
[49] G. Manteuffel, "Neuronal analog models with plastic synapses for neurobiological teaching and robotics," in *Applications of Neural Networks*, H. G. Schuster, Ed. Weinheim: VCH, 1992, pp. 155–162.
[50] C. Mead and L. Conway, *Physics of Computational Systems, an Introduction to VLSI Systems*. Dedham, MA: Addison-Wesley, 1980.
[51] C. Mead, *Analog VLSI and Neural Systems*. Dedham, MA: Addison-Wesley, 1989.
[52] K. Meazawa, "Analysis of switching time of monostable-bistable logic elements based on simple model calculation," *Jpn. J. Appl. Phys.*, vol. 34, 1995, pp. 1213–1217.
[53] M. Mehring, "Concepts of molecular information storage," *Solid-State Sciences*, vol. 91, p. 242, 1989.
[54] U. Meirav and E. B. Foxmann, "Single-electron phenomena in semiconductors," in *Semiconductor Sci. Technol.*, vol. 10, 1995, pp. 255–284.
[55] L. Micheel *et al.*, "Multi-value logic computation circuits using micro- and nanoelectronic devices," in *Proc. 23rd Int. Symp. on Mulitvalue Logic*, 1993, Sacamento, CA, IEEE Computer Society Press, pp. 164–169.
[56] C. Mikkelson *et al.*, "Coupled-quantum-well field effect resonant tunneling transistors for multi-valued logic/memory applications," *IEEE Trans. Electron Devices*, vol. 41, no. 2, Feb. 1994, pp. 132–137.
[57] J. von Neumann, *Theory of Self-Reproducing Automata*, Univ. of Illinois Press, 1966.
[58] N. H. Packard and S. Wolfram, *Two-Dimensional Cellular Automata*, *J. Statistical Phys.*, vol. 3, Mar. 1985, pp. 901–946.
[59] G. Palm, "On associative memory," *Biological Cybernetics*, vol. 35, pp. 19–31, 1980.
[60] T. Palm and L. Thylen, "Analysis of an electron-wave Y-branch switch," *Appl. Phys. Lett.*, vol. 60, p. 237, 1992.
[61] W. C. B. Peatman *et al.*, "Novel resonant tunneling transistor with high transconductance at room temperature," *IEEE Electron Device Lett.*, vol. 15, no. 7, July 1994, pp. 236–238.
[62] P. M. Petroff, "Quantum structure with reduced dimensionality and quantum functional devices," *Future Electron Device J.*, vol. 5, suppl. 2, 1994, pp. 5–19.
[63] K. H. Pribam, Ed., "Rethinking neural networks: Quantum fields and biological data," in *Proc. 1st Appalachian Conf. on Behavioral Neurodynamics*. Hillsdale, NJ: Lawrence Erlbaum Assoc., 1993.
[64] G. Privat and K. Goser, "Analog VLSI cellular fuzzy automata netwoks for relaxation labeling," in *Proc. Fourth Int. Conf. on Microelectronics for Neural Networks and Fuzzy Systems*, Turin, IEEE Computer Society Press, 1994, pp. 163–169.
[65] U. Ramacher and U. Rueckert, *VLSI Design of Neural Networks*. Boston: Kluwer, 1991.
[66] M. Reed *et al.*, "Realization of a three-terminal resonant tunneling device: The bipolar quantum resonant tunneling transistor," *Appl. Phys. Lett.*, vol. 54, pp. 1034, 1989.
[67] S. Rueping, K. Goser, and U. Rueckert, "A chip for selforganizing feature maps," *IEEE Micro*, vol. 15, no. 3, June 1995, pp. 57–59.
[68] Santa Fe Institute. *Computational mechanics archive*. Available: http://www.santafe.edu/projects/CompMech/, 1994.
[69] M. Schmutz and W. Banzhaf, "Robust competitive networks," *Phys. Rev. A*, vol. 45, no. 6, Mar. 1992, pp. 4132–4145.

[70] A. C. Seabaugh *et al.*, "Nine-state resonant tunneling diode memory," *IEEE Electron Device Lett.*, vol. 13, no. 9, Sept. 1992, pp. 479–481.
[71] R. Serra and G. Zanarini, *Complex Systems and Cognitive Processes*. Berlin: Springer, 1990.
[72] T. Shibata and T. Ohmi, "An intelligent MOS-transistor featuring gate-level weighted sum and threshold operations," in *Proc. Int. Electron Device Meet., Tech. Dig*., Washington DC, Dec. 8–11, 1991, pp. 919–922.
[73] M. H. Shieh and H. C. L. Lin, "A multiple-dimensional multistable SRAM cell using resonant tunneling diodes," *IEEE J. Solid-State Circuits*, vol. 29, no. 5, pp. 623–630, May 1994.
[74] K. Sienicki, *Molecular Electronics and Molecular Electronic Devices*, vol. 1. Boca Raton, FL: CRC, 1993.
[75] K. Y. Siu and J. Bruck, "Neural computation of arithmetic functions," *Proc. IEEE*, vol. 78, no. 19, Oct. 1990, pp. 1669–1675.
[76] D. L. Stein, "Spin glasses," *Sci. Amer.*, vol. 7, pp. 36–42, 1989.
[77] T. Suemasu *et al.*, "Theoretical and measured characteristics of metal (CoSi2)-insulator (CaF2) resonant tunneling transistors and the influence of parasitic elements," *IEEE Trans. Electron Devices*, vol. 42, no. 12, Dec. 1995, pp. 2203–2210.
[78] M. Takatsu *et al*., "Logic circuits using resonant-tunneling hot-electron transistors (RHET's)," *IEEE J. Solid-State Circuits*, vol. 27, no. 10, Oct. 1992, pp. 1428–1430.
[79] C. Tien-Hsin, "An integrated optoelectronic automatic target recognition processor workshop—A decade of neural networks: Practical applications and prospects," *JPL- Proc.*, JPL pub. 94-10, May 11–13, 1994.
[80] J. R. Tower and N. Farhat, "The transversal imager: A photonic neurochip with programmable synaptic weights," *IEEE Trans. Neural Networks*, vol. 6, no. 1, pp. 248–251, Jan. 1995.
[81] V. Tryba and K. Goser, "A modified algorithm for self-organizing maps based on the Schroedinger equation," in *Proc. IWANN'91*, Granada, 1991, pp. 33–47.
[82] H. H. Tsai, "P-N double quantum well resonant interband tunneling diode with peak-to-valley current ratio of 144 at room temperature," *IEEE Electron Device Lett*., vol. 15, no. 9, Sept. 1994, pp. 337–359.
[83] S. Vassiliadis *et al.*, "Block save addition with telescopic sums," in *Proc. 21st EUROMICRO Conf*., Como, Italy, Sept. 4–7, 1995, IEEE Computer Society Press, pp. 701–707.
[84] S. Vassiliadis *et al.*, "Block save addition with threshold gates" Tech. Rep. 1-68340-44(1995)04, Delft University of Technology.
[85] E. A. Vittoz, "Analog VLSI signal processing: Why, where and how," *J. VLSI Signal Processing*," vol. 8, Joint Special Issue on Analog VLSI Computation, July 1994, pp. 27–44.
[86] L. Wang and D. L. Alkon, Eds., *Artificial Neural Networks: Oscillations, Chaos, and Sequence Processing*. Los Alamitos, CA: IEEE Computer Society Press, 1993.
[87] W. Weber *et al.*, "On the application of the neuron MOS transistor principle for modern VLSI design," *IEEE Trans. Electron Devices*, vol. 43, no. 10, Oct. 1996, pp. 1700–1708.
[88] G. Weisbuch, *Complex Systems Dynamics—An Introduction to Automata Networks*, Lecture Notes, vol. II, Santa Fe Institute Studies in the Science of Complexity. Dedham, MA: Addison Wesley, 1991, pp. 7–21.
[89] A. W. Wieder, "Status, trends and challenges in microelectronics for the next 10 to 15 years," *Electrical Engineering*, vol. 79, pp. 79–84, 1996.
[90] G. M. Whitesides, J. P. Mathias, and C. T. Seto, "Molecular self-assembly and nanochemistry: A chemical strategy for the synthesis of nanostructures," *Science*, vol. 254, pp. 1312–1319, 1991.
[91] S. Wolfram, "Computational theory of cellular automata," *Communications in Mathematical Physics*, vol. 96, pp. 15–57, Nov. 1984.
[92] ——, "Approaches to complexity engineering," *Physica D*, vol. 22, pp. 385–399, Oct. 1986.
[93] Y. Yao and W. J. Freeman, "Model of biological pattern recognition with spatially chaotic dynamics," *Neural Networks*, vol. 3, 1990, pp. 153–170.
[94] T. Yatagai, S. Kawai, and H. Huang, "Optical computing and interconnects," *Proc. IEEE*, vol. 84, pp. 828–952, 1996.

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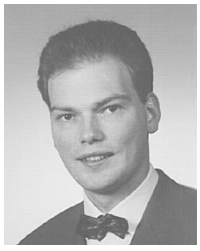

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