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Assessment of pseudo-bilayer structures in the heterogate germanium electron-hole bilayer tunnel field-effect transistor

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We investigate the effect of pseudo-bilayer configurations at low operating voltages ($\leq$0.5 V) in the heterogate germanium electron-hole bilayer tunnel field-effect transistor (HG-EHBTFET) compared to the traditional bilayer structures of EHBTFETs arising from semiclassical simulations where the inversion layers for electrons and holes featured very symmetric profiles with similar concentration levels at the ON-state. Pseudo-bilayer layouts are attained by inducing a certain asymmetry between the top and the bottom gates so that even though the hole inversion layer is formed at the bottom of the channel, the top gate voltage remains below the required value to trigger the formation of the inversion layer for electrons. Resulting benefits from this setup are improved electrostatic control on the channel, enhanced gate-to-gate efficiency, and higher I_{ON} levels. Furthermore, pseudo-bilayer configurations alleviate the difficulties derived from confining very high opposite carrier concentrations in very thin structures. © *2015 AIP Publishing LLC*.
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Extensive research has been devoted in the last years to explore more efficient configurations based on tunnel field-effect transistors (TFETs) in order to make this type of devices become a feasible alternative to conventional MOSFETs for sub-0.5 V operating voltages.[1–3] Their strongest point is the remarkable steepness of point and average subthreshold swings, SS_{pt} and SS_{av}, respectively, that they may feature below the 60 mV/dec thermal limit due to band-to-band tunneling (BTBT) injection mechanisms.[4,5] However, TFETs have been repeatedly reported to suffer from low ON-currents compared to their MOSFET counterparts.

At early stages of development, it was found that the orientation of BTBT phenomena was important in order to allow the gate a better control over them.[6] Simulation results[7–9] and some recent experimental evidences[10] indicate that the optimal scenario is attained when the tunneling direction and the gate-induced electric field are arranged to be aligned. Taking this into account, electron-hole bilayer TFETs (EHBTFETs) were proposed to exploit the benefits of dimensionality[11] for BTBT between 2-D electron and hole gases.[12] Later on, a heterogate structure for the EHBTFET (HG-EHBTFET) was introduced in order to avoid parasitic lateral BTBT processes.[13] Nevertheless, quantization of conduction and valence bands due to field-induced confinement led to reduced I_{ON} values for TFETs in general,[14–16] and for EHBTFETs, in particular.[13,17]

In this letter, we show that a certain asymmetry between top and bottom gates delays the appearance of the electron inversion layer at the top of the channel thus giving rise to a pseudo-bilayer configuration that can be preserved for low operating voltages (we take $V_{TG} = V_{DD} = 0.2$, 0.3, 0.4 and 0.5 V). We demonstrate that for a chosen top gate operating voltage (bottom gate voltage, V_{BG}, will be used to induce the asymmetric setup), there exists an optimized degree of asymmetry which minimizes the shortest tunneling distance, d_{tunn}, at $V_{TG} = V_{DD}$. The use of pseudo-bilayer configurations keeps the energy subbands for electrons unpinned and enhances the gate-to-gate efficiency as defined in Ref. 18. A similar suggestion pointing to the direction of minimizing electron quantum capacitance while maximizing hole quantum capacitance was done in Ref. 19.

The HG-EHBTFET depicted in Fig. 1 features a source p^+ region (10^{20} atoms/cm^3), intrinsic channel region with central overlap and side underlap regions (10^{15} atoms/cm^3), and drain n^+ region (10^{20} atoms/cm^3). The body thickness, t_{body}, is chosen to be 10 nm. Top and bottom gate dielectrics are 3 nm-thick HfO_2 layers. Drain bias will be set at 0.3 V throughout this work and V_{BG} initially set to 0 V. The different asymmetric configurations will be induced by gradual negative values of V_{BG}. Optimized workfunctions for avoiding parasitic lateral BTBT[13] and for fixing subband alignment at very low V_{TG} (namely, we choose $V_{TG,align}$ to be 0.04 V in our study) are chosen as $\phi_{tg,ol} = 3.06$ eV, $\phi_{tg,ul} = 4.25$ eV, $\phi_{bg,ul} = 4.40$ eV, and $\phi_{bg,ol} = 5.05$ eV at $V_{BG} = 0$ V. For these values, the top gate voltage at which the electron inversion layer is formed, V_{inv}, calculated as done in Ref. 20, turns out to be V_{inv} ($V_{BG} = 0$ V) = 0.05 V. As we want the onset of vertical BTBT to remain fixed at the same V_{TG} value (0.04 V), and given that variations in the electron and hole subband alignment will be produced by applying gradual negative V_{BG} values, $\phi_{tg,ol}$ will be readjusted in every case to guarantee that $V_{TG,align}$ occurs at 0.04 V. The rest of the workfunctions will be kept constant throughout our study. Notice that a fixed $V_{TG,align}$ value implies that the overdrive voltage will be raised as we increase V_{TG}.

The quantization direction is along the [100] crystal orientation of Ge. Along this direction, the L electron valleys

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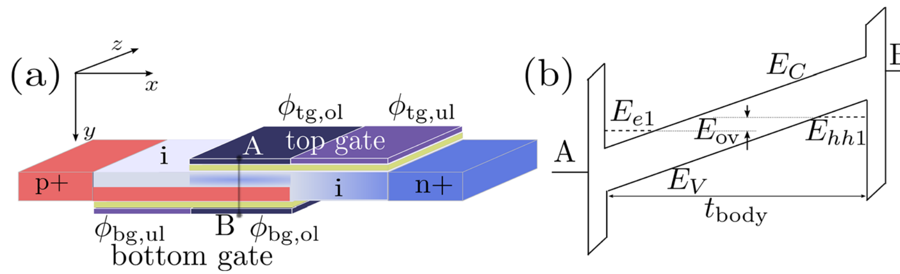

FIG. 1. (a) Schematic cross-section (not to scale) of Ge HG-EHBTFET considered in this work. The heterogate structure is introduced in both top and bottom gates. (b) Band profile along the vertical $\bar{AB}$ segment with vertical BTBT allowed between the first energy subband for heavy holes, E_{hh1}, and that for electrons, E_{e1}. E_{ov} stands for the energy overlap once alignment has been surpassed.

are fourfold degenerate with quantization effective mass $m_y = 0.12m_0$ and transverse effective masses $m_x = 0.15m_0$ and $m_z = 0.58m_0$. For the Γ valley, effective masses for heavy holes, light holes, and electrons are $m_{hh} = 0.33m_0$, $m_{lh} = 0.044m_0$, and $m_e = m_{lh}$, respectively.[9]

The simulation setup accounting for quantum confinement was carefully described in Ref. 13 and is based on a TCAD hybrid integration that combines the most recent versions of the two most widely used simulators: Silvaco ATLAS (v.5.20.2.R)[21] and Synopsys Sentaurus (v.2014.09).[22] Similar approaches have been very recently used in the literature.[23]

For analyzing Fig. 2 (and later on Fig. 3), three premises need to be clearly stated: (i) bottom gate sweeps must be understood not as conventional rampings, but rather as a comparison between multiple potential scenarios, each of which is characterized by a V_{BG} value (and its associated $\phi_{tg,ol}$); (ii) along each curve where $V_{TG} = V_{DD}$, the only voltage that we vary is V_{BG}; and (iii) given the dependence of V_{inv} with V_{BG} (see inset) at a fixed drain bias (recall that we take $V_{DS} = 0.3$ V throughout all the paper), it is obvious that along the curve $V_{TG} = V_{inv}$, both V_{BG} and V_{TG} vary.

Taking this into account, we observe that when no asymmetry is induced, i.e., $V_{BG} = 0$ V, efficiency remains extremely low ($\lesssim 0.18$) for all the curves corresponding to $V_{TG} = V_{DD}$; and jumping from one V_{DD} to another at $V_{BG} = 0$ V has little impact on it. This is due to the fact that for $V_{BG} = 0$ V, V_{inv} is 0.05 V (see inset) and, therefore, all the curves with V_{TG} fixed to V_{DD} verify that they stand for situations where V_{TG} is above V_{inv}. In other words, this implies that for $V_{BG} = 0$ V, the inversion layer for electrons is formed in all cases, the energy subbands pinned and, thus, the gate efficiency severely degraded. As we increase the asymmetry between both gates (making V_{BG} gradually more negative), so does the gate efficiency go up because V_{inv} is raised (again, see inset). It is straightforward to understand that for a given V_{BG}, the further we keep V_{TG} below V_{inv} the higher the efficiency that we obtain. For example, let us focus on $V_{BG} = -0.2$ V, which provides $V_{inv} = 0.33$ V. Observe that, in that case, for V_{DD} values of 0.4 and 0.5 V (i.e., $V_{DD} > V_{inv}$) their corresponding curves feature efficiencies of 0.24 and 0.17, respectively. However, for $V_{DD} = 0.2$ and 0.3 V, we have that $V_{DD} < V_{inv}$ and, consequently, for those curves, the electron inversion layer is not formed yet and the subbands remain unpinned. For these V_{DD} values, we report efficiencies of 0.48 and 0.4, respectively. Moreover, we notice that for very strong asymmetric configurations, gate efficiency tends to saturate to a value of 0.57. Impact of quantum confinement on limiting gate-to-gate efficiencies below 1 has been discussed in Ref. 18 and more recently in Ref. 19.

Once we established that growing asymmetric layouts feature increasing efficiencies for low operating voltages,

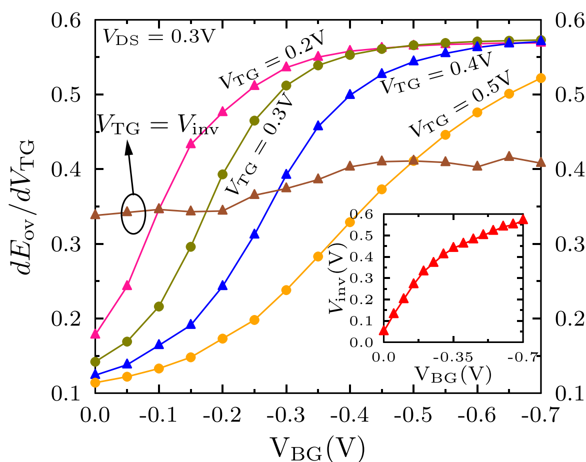

FIG. 2. Gate-to-gate efficiency controlling the energy overlap between first energy subbands as defined in Ref. 18, at fixed $V_{DS} = 0.3$ V. For each V_{TG}, efficiency increases as we induce stronger asymmetries saturating at $dE_{ov}/dV_{TG} = 0.57$. The inset shows the growing behavior of V_{inv} for increasing asymmetric configurations.

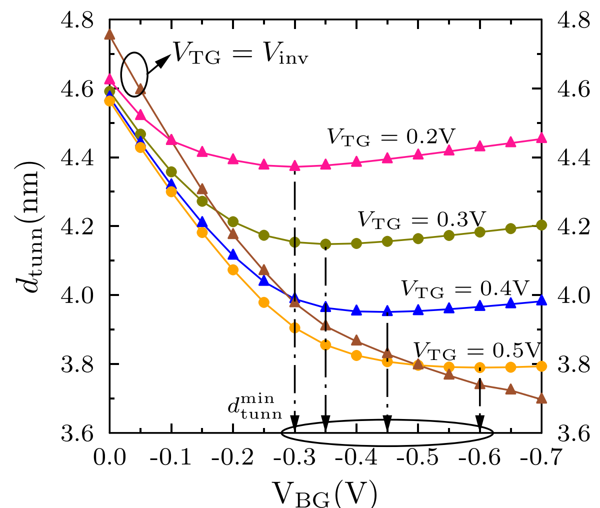

FIG. 3. Dependence of minimum vertical BTBT distances, d_{tunn}, on V_{BG} for $V_{TG} = V_{DD} = 0.2$, 0.3, 0.4, and 0.5 V. V_{DS} is fixed to 0.3 V in all cases. For each top gate bias, there exists an optimized value of V_{BG} that minimizes d_{tunn}. Notice that all d_{tunn}^{min} verify that $V_{TG} < V_{inv}$.

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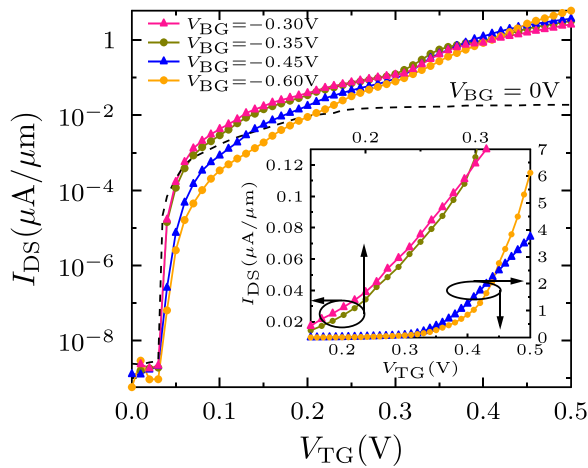

FIG. 4. $I_{DS}-V_{TG}$ curves for every operating voltage corresponding to the different optimized V_{BG} values. Switching behavior is gradually degraded for increasing degrees of asymmetry. Dashed line stands for the transfer characteristic when no bottom bias is applied. V_{DS} is fixed to 0.3 V.

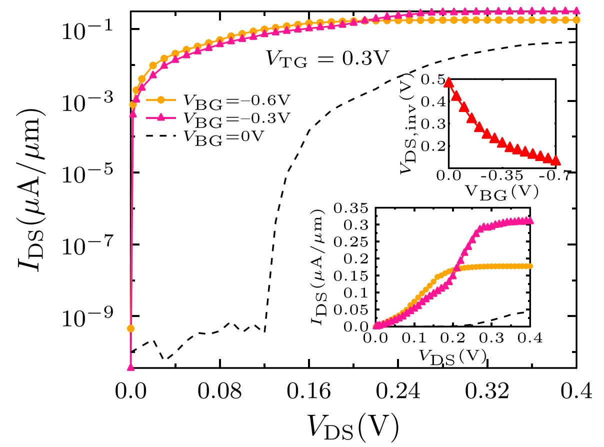

FIG. 5. $I_{DS}-V_{DS}$ curves at fixed $V_{TG}=0.3$ V for the configurations corresponding to $V_{BG}=0$, -0.3, and -0.6 V. Bottom inset illustrates the transition between superlinear regime and saturation, whereas top inset shows the values of V_{DS} at which the electron inversion layer is formed.

one important question arises: is there a privileged degree of asymmetry for a given $V_{TG}=V_{DD}$ so that its minimum tunneling distance could be optimized? The answer turns out to be positive and indeed a favored asymmetric setup can be found for a chosen V_{DD}. In Fig. 3, we show the evolution of d_{tunn} as we increase (in negative terms) V_{BG}. Notice how for each fixed value of V_{TG}, d_{tunn} presents a minimum which, in turn, matches with an asymmetric configuration where V_{TG} lies below V_{inv}. This means that the optimized asymmetries correspond to configurations of the HG-EHBTFET where, instead of a mostly symmetric electron-hole bilayer structure, electron concentrations at the top of the channel are reduced giving rise to a more properly named pseudo-bilayer structure. Notice that the increasing behavior of d_{tunn} observed at the right side of Fig. 3 is due to the switching from triangular band profiles to more rounded ones taking place at the bottom of the channel as a result of the hole strong inversion induced by high $|V_{BG}|$ values.

The transfer characteristics for $V_{DD}=0.2$, 0.3, 0.4, and 0.5 V at the optimized bottom biases of Fig. 3 are shown in Fig. 4. In each case, V_{BG} could be absorbed into the corresponding bottom gate workfunctions, $\phi_{bg,ul}$ and $\phi_{bg,ol}$, so that its value could be readjusted to 0 V. For the sake of comparison, we have also included the transfer characteristic when no asymmetry is applied showing that considerably lower current levels are attained in that case.

Table I summarizes the optimized setup for each V_{DD}. Electron and hole concentrations correspond to the maximum densities obtained along the $\overline{AB}$ cut of Fig. 1(a). It can be noted that, consistently, the closer V_{TG} is to its corresponding V_{inv}, the higher the maximum electron concentration proves to be. In any case, for $V_{TG}=V_{DD}=0.5$ V, the maximum concentration for electrons remains still more than one decade below that for holes. SS_{pt} is calculated at $V_{TG,align}$; and SS_{av} is taken from $V_{TG,align}$ to $V_{TG}=V_{DD}$. Notice that these SS values have been obtained assuming perfectly sharp band edges and not accounting for a potential finite DOS distribution extending into the forbidden gap. More realistic treatments taking this into account would be expected to degrade to a certain extent the values shown in Table I.

Finally, for the sake of completeness, it is interesting to show the impact of some of these asymmetries on the output characteristics of the device. In Fig. 5, we depict the aspect of the $I_{DS}-V_{DS}$ curves for the layouts with $V_{BG}=0$, -0.3 and -0.6 V corresponding, respectively, to the non-optimized case and to the cases described by the first and last rows of Table I. All the curves were obtained taking $V_{TG}=0.3$ V. For the two cases with $V_{BG}=-0.3$ and -0.6 V, the curves indicate that subband alignment had been already attained for $V_{DS}=0$ V; whereas for $V_{BG}=0$ V, subbands align at $V_{DS}=0.12$ V. Inspecting the shape of the curves in linear scale (see bottom inset), we confirm the expected transition between a superlinear regime and a saturation region.[24] Top inset displays the behavior of the drain voltage required to form the electron inversion layer, $V_{DS,inv,}$ as a function of V_{BG}. Both trends, the one shown in the top inset of Fig. 5 and that reported in the inset of Fig. 2, are consistent. The reason is simple. If the formation of the electron inversion layer depends on the voltage difference between the top gate and the drain; then, whatever the impact that a

TABLE I. Optimized bottom gate biases and resulting values for $V_{TG}=V_{DD}=0.2$, 0.3, 0.4, and 0.5 V with $V_{TG,align}=0.04$ V in the Ge HG-EHBTFET.

V_{DD} (V)	V_{BG} (V)	$\phi_{tg,ol}$(eV)	V_{inv} (V)	d_{tunn}^{min} (nm)	Electron concentration (cm^{-3})	Hole concentration (cm^{-3})	SS_{pt} (mV/dec)	SS_{av} (mV/dec)
0.2	−0.3	3.30	0.41	4.37	1.613×10^{16}	8.159×10^{18}	2.57	26.83
0.3	−0.35	3.32	0.44	4.15	1.071×10^{17}	1.065×10^{19}	2.58	36.27
0.4	−0.45	3.35	0.48	3.95	4.433×10^{17}	2.036×10^{19}	4.80	44.86
0.5	−0.60	3.39	0.54	3.79	1.284×10^{18}	4.002×10^{19}	5.45	49.89

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negative ramping of V_{BG} may have on one of these electrodes for triggering the formation of the inversion layer, it will entail the opposite effect on the other, provided that each time we keep fixed the bias of the electrode not being analyzed.

In this work, we have shown that for low operating voltages in the heterogate germanium electron-hole bilayer tunnel field-effect transistor, there exists an optimal asymmetric configuration that: (i) enhances the gate electrostatic control over the channel, keeping the gate efficiency very high (close to the saturation value) for the whole V_{TG} ramping and (ii) minimizes the lowest tunneling distance at the ON-state. We have demonstrated that these optimized asymmetric layouts feature pseudo-bilayer structures of electrons and holes in which the maximum electron concentrations turn out to be around two decades lower than their hole counterparts. The effect of these optimized asymmetries on the output characteristics of the device has been also elucidated.

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