Electr Eng
DOI 10.1007/s00202-011-0212-8

ORIGINAL PAPER

Asymmetric transistor sizing targeting radiation-hardened circuits

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Received: 18 February 2009 / Accepted: 22 May 2011

Abstract This article proposes a technique to improve the dependability of circuits under energetic particle irradiation by resizing transistors in the most critical paths. First, the SET vulnerability of a mapped circuit is analyzed to identify the most sensitive nodes. The sensitivity of the circuit is defined by the logical and electrical masking. Once the most critical nodes are selected, a transistor sizing algorithm is able to resize the pull-up and pull-down transistors separately. The asymmetric resizing offers interesting area and performance trade-off in comparison with gate sizing and gate duplication techniques. Results show very small area and performance penalties for circuits operating at ground level for a 130-nm technology process.

Keywords Circuit sensitivity · Radiation-hardened circuits · Asymmetric transistor sizing · Transient propagation

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1 Introduction

In deep submicron technologies, decreasing feature sizes and lower operating voltage levels cause an increase in the soft error rate (SER) in integrated circuits. If a particle strikes a sensitive region of a semiconductor device, the resulting electron-hole pair generation may change the logical state of the circuit node. If this transient disturbance occurs in a combinational logic circuit, the effect is known as single event transient (SET). SETs may lead a system to an unexpected response if it propagates to a memory element or a primary output (PO) of a circuit.

If a particle directly hits a memory element, the logic value stored may be changed causing the erroneous operation of the circuit. This change of the value stored in memory elements is known as single event upset (SEU). Historically, memories have been the major concern. Efficient solutions to memory protection are presented in [1–3]. However, since the transition time of the logic gates is getting shorter and clock frequencies are significantly increasing in nanometer scale technologies, errors in combinational logic are increasing and error rates may reach the same level as in memories in the near future. A recent work predicts SERs in combinational logic circuits comparable to memory elements by 2011 [4]. Hence, the design of combinational logic tolerant to radiation effects is mandatory.

This paper proposes a new transistor sizing method for SET protection in combination logic circuits. The main characteristic of the proposed methodology is the ability to find the smallest accepted transistor widths to attenuate SETs in the nodes of a combinational circuit, before it propagates to a memory element or a primary output.

Another important point is that pull-up and pull-down transistors are independently sized, minimizing the area overhead. In other words, we apply asymmetric transistor sizing

Published online: 15 June 2011

to attenuate SETs with minimized area overhead. Works presented in the literature are based on symmetric models to size pull-up and pull-down blocks.

This paper is organized as follows. Related work is discussed in Sect. 2. A background to the proposed technique is given in Sect. 3. The proposed transistor sizing strategy is presented in Sect. 4. Sections 5 and 6 present the transistor sizing algorithm in detail. Finally, results and conclusions are presented.

2 Related work

Radiation hardened combinational logic has been discussed in the last years due to the importance that SET effects have shown in submicron technologies at ground level. Radiation hardened techniques are basically based on redundancy. This redundancy can be *spatial* or *temporal*. Spatial redundancy consists on the replication of certain elements of a circuit in order to avoid the pulse propagation. Temporal redundancy usually compares a signal in different moments of time. These techniques are briefly discussed in this section.

The main spatial redundancy-based technique is the triple modular redundancy (TMR), which consists in triplication of parts of a circuit, or even the whole circuit. Thus, if one of the three elements fails, the correctness of the system is guaranteed by the other two elements, which operate correctly.

An example of temporal redundancy is presented in [5]. The Code Word State Preservation (CWSP) technique consists on the insertion of special gates in the primary outputs. These gates are composed by delay blocks. Transient pulses with duration smaller than the delay of the block are attenuated.

A gate duplication methodology is presented in [4]. It is clear that the area overhead is significantly smaller than other techniques such as TMR, although special attention has been given in the last years to find better solutions.

A SER analysis in combinational logic circuits and a partial gate redundancy methodology for soft error protection is proposed in [6,7]. These works present a very important contribution in relation to SET analysis. The SET propagation is analyzed with respect to logical and electrical masking. A drawback of this partial redundancy method is the complexity to test cells sharing the same inputs and outputs.

A gate sizing method is proposed in [8]. Gate sizing consists in exchanging a gate by a larger version. This gate sizing technique targets soft error rate reduction by selectively sizing the most sensitive nodes. In their work, the maximum critical charge considered was 0.3 pC and they achieved an average area overhead of 33% for 90% coverage.

The sensitivity analysis in combinational logic circuits has been discussed, for instance, in the works presented in [9] and [10]. An accurate and computer efficient model for SET is presented in [11]. The model evaluates the behavior of a SET in a circuit node as function of the driving gate resistances and the capacitance loading at the stuck node. The work presented in this article uses this model to analyze the sensitivity of circuit nodes. Section 4 gives further details about the model.

3 Sensitivity analysis background

The sensitivity analysis of circuits has been presented in several works [7]. Most of them include the structure of the gates and layout details. The analysis of the structure of a gate consists on evaluating the propagation of a fault as a function of transistor connections. Sensitivity analysis considering the circuit layout takes into account the probability of a particle to hit a region of the layout. For example, a large drain area has a higher probability of being hit than a smaller one.

In this work, the structure of the gate and its layout is not considered. Differently, we consider only particle hits at the drains of the transistors connected to the output node of the logical gate, i.e., particle hits that cause direct charge injection at the output node. Particle hitting internal nodes of the gate will necessarily cause a smaller SET at the output node [14]. It is important to highlight that layout characteristics are not taken into account in the sensitivity analysis because we consider the sensitivity of a gate after sizing becomes zero to a given critical charge.

In this work we refer to the circuit sensitivity S_{circuit} as the probability of a transient fault occurring in a node n to be propagated to the primary outputs (PO). This probability is defined by taking into account the logical and electrical masking.

The logical masking represents the probability of a transient pulse to be masked by a logic path of the circuit, and the electrical masking describes the attenuation of a transient pulse before it reaches the primary outputs or memory elements. Thus, the sensitivity of a circuit is given by

$$S_{\text{circuit}} = \sum_{n=1}^{N} (1 - L_n) \cdot (1 - E_n) \tag{1}$$

where L_n is the logical masking and E_n is the electrical masking. The logical masking L_n is a probability value. Larger logical masking means a smaller probability of a transient pulse to be propagated to the circuit outputs. The electrical masking E_n is a Boolean value, where "1" means that the transient pulse is totally attenuated and "0" indicates that the transient can be propagated to the outputs.

3.1 Logical masking

The *logical masking* occurs if a transient pulse induced by a particle is not propagated to a primary output (PO) due

Table 1 Probability of a node as a function of the gate equation [12]

Logic function	Resulting probability
AND	$P_Z(1) = P_a(1) * P_b(1)$
NAND	$P_Z(1) = 1 - P_a(1) * P_b(1)$
OR	$P_Z(1) = 1 - (1 - P_a(1)) * (1 - P_b(1))$
NOR	$P_Z(1) = (1 - P_a(1)) * (1 - P_b(1))$
XOR	$P_Z(1) = P_a(1) + P_b(1) - 2 * P_a(1) * P_b(1)$
XNOR	$P_Z(1) = 1 - P_a(1) - P_b(1) + 2 * P_a(1) * P_b(1)$
BUF	$P_Z(1) = P_a(1)$
INV	$P_Z(1) = 1 - P_a(1)$

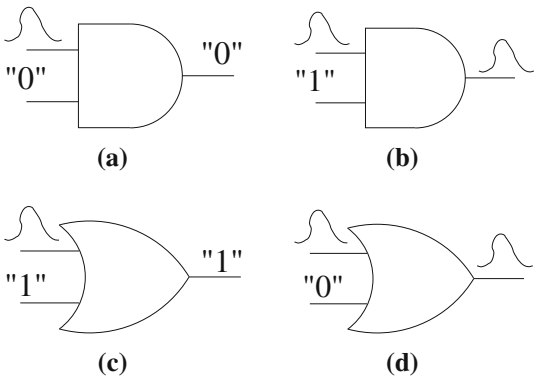


Fig. 1 The logical masking **a** masked SET pulse in a AND gate, **b** not masked SET pulse in a AND gate, **c** masked SET pulse in a OR gate, **d** not masked SET pulse in a OR gate

to the logic chain. In other words, the pulse is masked as function of the vector applied to the primary inputs (PI) of the circuit. Controllability and observability techniques are used to define the logical masking of a node. Controllability is defined as the ability that set a given logic value to an internal node applying a pattern to the PIs. Observability is a measure of how well a state in an internal node can be known at the primary outputs (PO).

The controllability of the gate output node is obtained by the logic function of the gates as shown in Table 1 [12]. Considering the probability $P_z(1)$ of a gate output z have "1" as function of the gate input probabilities $P_a(1)$ and $P_b(1)$. Table 1 shows how to propagate the probabilities through the circuit node in order to obtain controllability and observability values. The propagation of the controllability probability is done for the entire circuit, from the PIs through each gate until the POs are reached.

Figure 1 illustrates the logical masking in a gate. A pulse in one of the gate inputs is propagated through the gate only if a non-controlling value is applied at the other input. Fig. 1a shows the logical masking in the AND gate as a function of the controlling logic value "0" at the input. Otherwise, the logical masking does not happen if a non-controlling value is applied (Fig. 1b).

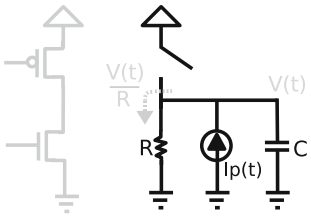


Fig. 2 Equivalent circuit for calculating circuit response to an energetic particle hit

In an OR gate, the same situation is considered, where the pulse propagates through the gate only if the non-controlling value is applied to the other input. Figure 1c shows the logical masking as function of a controlling value and Fig. 1d shows the case where there is no logical masking.

3.2 Electrical masking

Electrical masking can be defined as the electrical attenuation of a pulse by the gates in the logic path down to a level that the SET does not affect proper operation. This electrical attenuation is also considered as pulse degradation in this paper, based on the work presented in [14]. This degradation is the basis of the electrical masking, where the pulse is degraded as a function of the electrical characteristics of the gates in the path.

4 An analytical model for SET

The sensitivity model used in our transistor sizing strategy was proposed in [11]. The model is based on two electrical device parameters. The effective loading capacitance C lumped onto the output node of a gate g and the effective resistance R of the "ON" transistors of this gate.

For modeling purposes, circuit response for the energy particle is modeled as the network depicted in Fig. 2, and may be represented by

$$C\frac{\mathrm{d}V(t)}{\mathrm{d}t} + \frac{V(t)}{R} = I_p(t) \tag{2}$$

where the term $\frac{V(t)}{R}$ is related to the discharging current in the transistor, represented by the resistor R. $I_p(t)$ represents the current caused by the particle hitting the device and the last term $C\frac{\mathrm{d}V(t)}{\mathrm{d}t}$ represents the current in the capacitor C. The model derivation has a strong relation with the electrical devices behavior and allows the evaluation of the critical charge Q_c needed to induce a SET in a node, and the transient pulse duration, as well.

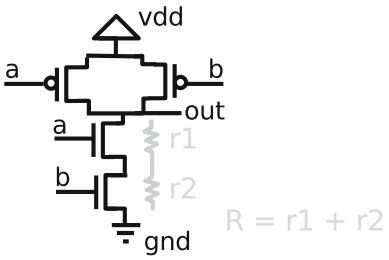


Fig. 3 A transistor modeled as a resistance

4.1 Modeling resistances and capacitances

The use of linear resistors to model transistor paths is a widely known method [18]. Thus, the effective resistance R can be analytically determined by

$$R = \frac{1}{\mu_0 C_{\text{ox}} \left(\frac{W}{L}\right) (V_{\text{gs}} - V_{\text{th}})} \tag{3}$$

where μ_0 is the mobility of the transistor channel. C_{ox} is the oxide capacitance, which is given by $\frac{\varepsilon_0 \varepsilon_{SiO_2}}{t_{\text{ox}}}$. ε_0 is the dielectric constant, ε_{SiO_2} is the oxide relative dielectric constant and t_{ox} is the gate oxide thickness. V_{gs} is the gate-source voltage and V_{th} is the threshold voltage.

All these parameters are constants related with the technology process, except the $\left(\frac{W}{L}\right)$ ratio that represents the transistor dimensions. Based on this aspect ratio, we are able to explain the relation between the transistor width and the resistance. The smaller the transistor width, the higher the resistance.

Figure 3 illustrates two stacked transistors modeled as resistors. Assuming NMOS transistors are "ON" in the NAND gate of the example due to input signals a = "1" and b = "1". The effective resistance R is given by the sum of the resistances r_1 and r_2.

The effective capacitances C is defined by the sum of three capacitances connected to the output node.

$$C = C_{\text{diffusion}_{\text{g1}}} + C_{\text{connection}} + C_{\text{gate}_{\text{g2}}} \tag{4}$$

where $C_{\text{diffusion}_{\text{g1}}}$ is the sum of all PN junction capacitances of the driving gate. $C_{\text{connection}}$ is the wiring and parasitic capacitances, and $C_{\text{gate}_{\text{g2}}}$ is the gate capacitance of all transistors connected to the output node. The diffusion capacitance is given by

$$C_{\text{diffusion}_{\text{g1}}} = \sum_{d}^{D} C_{\text{ja}} A_d + C_{\text{jp}} P_d \tag{5}$$

where C_{ja} is the junction capacitance per μ^2, A_d is the diffusion area, C_{jp} is the periphery capacitance per μ and P_d is the diffusion perimeter. The third term of the capacitance C is the gate capacitance. Thus, $C_{\text{gate}_{\text{g2}}}$ is defined according to the region the gate g2 is operating.

Table 2 Approximation of intrinsic MOS gate capacitance

Parameter	Off	Non-saturated	Saturated
C_{gb}	$C_{\text{ox}} A$	0	0
C_{gs}	0	$\frac{1}{2} C_{\text{ox}} A$	$\frac{2}{3} C_{\text{ox}} A$
C_{gd}	$C_{\text{ox}} A$	$\frac{1}{2} C_{\text{ox}} A$	0
$C_{\text{g}} = C_{\text{gb}} + C_{\text{gs}} + C_{\text{gd}}$	$C_{\text{ox}} A$	$C_{\text{ox}} A$	$\frac{2}{3} C_{\text{ox}} A$

Table 2 presents the gate capacitance according to the region of operation. Based on this information, the gate capacitance is defined by

$$C_{\text{gate}_{\text{g2}}} = \sum_{\text{g}_{\text{off}}} C_{\text{ox}} A_{\text{g}} + \sum_{\text{g}_{\text{on}}} \frac{2}{3} C_{\text{ox}} A_{\text{g}} \tag{6}$$

These analytical equations allow to model the behavior of the transient pulse as a function of the electrical characteristics of the devices.

4.2 Single event transient model

The single event model uses the double exponential equation proposed in [13] as follows.

$$I(t) = \frac{Q}{\tau_\alpha - \tau_\beta} \left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right) \tag{7}$$

where Q is the injected charge and may be positive or negative, τ_α is the collection time constant of the junction and τ_β is the time constant for initially establishing the ion track. τ_α and τ_β are constants and depend on several process-dependent factors.

In the double exponential, the τ_β is responsible to shape the rising of the current pulse and the τ_α shapes the fall time of the curve. The curve presents a fast rise time with smaller τ_β, as well as the fall time is faster with smaller τ_α.

Important characteristics about the transient pulse can be obtained through (7). Models presented in [11] are derivations of the double exponential to obtain the peak time t_{peak} and the voltage peak V_{peak}. It is important to remark that the τ_β is considered to be much smaller than τ_α ($\tau_\alpha \gg \tau_\beta$) in the formulations. In other words, the model assumes a very fast rise time to the double exponential.

The differential equation shown in (2) can be solved in order to obtain the voltage $V(t)$ at the struck node. Thus, $V(t)$ is given by

$$V(t) = \frac{I_0 \tau_\alpha R}{\tau_\alpha - \text{RC}} \left(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\text{RC}}}\right) \tag{8}$$

The time t_{peak} at which the node voltage reaches its maximum value can be evaluated by

$$t_{\text{peak}} = \frac{ln\left(\frac{\tau_\alpha}{\text{RC}}\right) \tau_\alpha \text{RC}}{\tau_\alpha - \text{RC}} \tag{9}$$

and, inserting (8) into (9) leads to the peak transient voltage V_{peak} reached at the struck node.

$$V_{peak} = \frac{I_0 \tau_\alpha R}{\tau_\alpha - RC}\left(\left(\frac{\tau_\alpha}{RC}\right)^{\frac{RC}{RC-\tau_\alpha}} - \left(\frac{\tau_\alpha}{RC}\right)^{\frac{\tau_\alpha}{RC-\tau_\alpha}}\right) \quad (10)$$

where R is the effective resistance of the pull-up path (if PMOS transistors are "ON") or the effective resistance of the pull-down path (if NMOS transistors are "ON") and C is the effective capacitance loading lumped onto the output node.

The critical charge Q_c can be derived from (10) once the V_{peak} of a transient pulse is known. Thus, the critical charge Q_c is given by

$$Q_c = \frac{V_{peak}(\tau_\alpha - RC)}{R\left(\left(\frac{\tau_\alpha}{RC}\right)^{\frac{RC}{RC-\tau_\alpha}} - \left(\frac{\tau_\alpha}{RC}\right)^{\frac{\tau_\alpha}{RC-\tau_\alpha}}\right)} \quad (11)$$

The voltage at the struck node shows a double exponential behavior in which the transient voltage V_{peak} is reached at time t_{peak}. The voltage starts to decrease exponentially after t_{peak}.

$$\tau_n = t_{peak} - RC ln\left(\frac{\frac{1}{2}VDD}{V_{peak}}\right) - \tau_\alpha ln\left(\frac{\frac{1}{2}VDD}{V_{peak}}\right) \quad (12)$$

Equation (12) shows the transient pulse duration τ_n, where the second term corresponds to the analytical solution if RC time is much greater than τ_α and the last term corresponds to the analytical solution if τ_α time is much greater than RC.

4.3 Single event transient propagation

The analysis of the transient pulse propagation shows that the pulse degradation is directly influenced by the propagation delay τ_g. In other words, larger τ_g leads to greater degradation of the transient pulse.

Wirth et al. [14] proposed a pulse degradation model based on curve fitting. The model considers a k parameter equal to the minimum ratio τ_n/τ_g needed to propagate a SET to the next stage in a circuit path.

For an input transient with small duration, the output voltage peak does not reach $\frac{1}{2}$VDD and complete attenuation must be considered. Thus, the model for the first case is given as

$$\tau_{n+1} = 0, \quad if(\tau_n \leq k\tau_g) \quad (13)$$

where τ_n and τ_{n+1} are the transient pulse durations at the nth and at the $(n+1)$th stages, respectively.

Second and third cases are related to a partial degradation in the transient pulse according to the relation with the SET duration τ_n and the gate delay τ_g.

$$\tau_{n+1} = (k+1)\tau_g(1 - e^{(k-(\tau_n/\tau_g))}), \quad if(\tau_g < \tau_n \leq (k+1)\tau_g)) \quad (14)$$

The model for the third case considers a smaller degradation than the second case.

$$\tau_{n+1} = \frac{\tau_n^2 - \tau_g^2}{\tau_n}, \quad if((k+1)\tau_g < \tau_n \leq (k+3)\tau_g) \quad (15)$$

The fourth degradation case consists on situations where the pulse is not degraded from a stage to another or it can be neglected.

$$\tau_{n+1} = \tau_n, \quad if(\tau_n > (k+3)\tau_g) \quad (16)$$

These four degradation cases are the basis to the sizing algorithm because of its propagation properties. These properties can be useful also to obtain the maximum acceptable transient pulse duration in a node. We consider maximum acceptable transient pulse in a node the maximum SET duration that is attenuated before the primary outputs. In other words, the maximum acceptable SET duration is a pulse which is not propagated to any PO.

One important remark is that a transient pulse does not need to be attenuated in the node n (except in cases where gates are connected to outputs). The SET may be attenuated through the gates in the whole path between the node n and the primary outputs. The complete attenuation of a SET in a net may result in unnecessary oversize transistors.

5 The transistor sizing strategy

The transistor sizing strategy proposed in this article consists in finding the smallest transistor width of each circuit gate which assures SET attenuation. The formulations previously discussed are the basis to the sizing algorithm.

Algorithm 1: The transistor sizing for SET attenuation.

Require: Set of gates G, Set of Nets N, Set of outputs O, Maximum sensitivity M, Max critical charge Q_c, Desired circuit sensitivity $S_{desired}$
Ensure: Set of gates with sized transistors G_{new}
1: $G_{new} \Leftarrow \emptyset$
2: **for all** $n \in N$ **do**
3: $L_n \Leftarrow$ calculateLogicalMasking(n);
4: $E_n \Leftarrow$ calculateElectricalMasking(n, Q_c);
5: $S_n \Leftarrow (1 - L_n) \cdot (1 - E_n)$
6: **end for**
7: $V \Leftarrow O$ {Nets to visit, starting from the outputs.}
8: **while** $V \neq \emptyset$ **do**
9: **for all** $n \in V$ **do**
10: $g \Leftarrow$ getFaninGateConnectedToNet(n);
11: **if** $S_n > M$ **then**
12: $\tau_n \Leftarrow$ getMaximumSET(n, g);
13: $g_{new} \Leftarrow$ sizeTransistors(s, g, τ_n);
14: $G_{new} \Leftarrow G \bigcup \{g_{new}\} \setminus \{g\}$
15: **end if**
16: $I \Leftarrow$ getGateInputs(g);
17: $V \Leftarrow V \bigcup I \setminus \{n\}$
18: **end for**
19: **end while**

The proposed transistor sizing strategy is presented in Algorithm 1. First lines (2–6) define the circuit sensitivity as shown in (1). The transistor sizing strategy starts at line 8, where every node n of the circuit is visited in order to find the minimum transistor width to each gate g connected to this node. It is important to note that only nodes with the sensitivity bigger than the maximum defined sensitivity M are sized (line 11).

Function `getMaximumSET(n, g)` (line 12) finds the maximum pulse duration τ_n in the node n that is suppressed before the primary outputs. The transistor sizing algorithm to a gate g is function of this SET duration τ_n.

Function `sizeTransistors(s, g, τn)` (line 13) continuously increases the transistors width until the SET in the node n is smaller than τ_n. When this situation is reached, we consider the transistors of the gate g are sized as expected to the charge Q_c.

The implementation of these functions are discussed in details in Sect. 6. Other lines of the strategy shown in Algorithm 1 give some idea about the navigation in the nets. The algorithm evaluates every node of the combinational logic, from the primary outputs (PO) to the primary inputs (PI). This is done because the delay of the gates is changed after sizing. When transistors of a gate are sized, the delay usually becomes smaller and a transient pulse propagates with a smaller degradation.

Erroneous interpretation concerning the SET propagation happens if the transient pulse is evaluated before the sizing of the gates in the path to the POs. Thus, when the SET is evaluated in a node n, we guarantee that every gate in the path between this node n and the POs was already sized.

6 The transistor sizing model

The transistor sizing technique proposed in this thesis is basically separated in three steps. These steps are related to the sensitivity of a circuit node as a function of a particle hitting the circuit and the minimum transistor width needed to attenuate a SET (electrical masking).

The first step is the sensitivity analysis, which is represented in lines 2–6 (Algorithm 1). The sensitivity of a node n is given by the logical and electrical masking. Function `getMaximumSET(n, g)` (line 18) finds the maximum SET duration τ_n for a net n that is attenuated just before the primary outputs. Assuming SET duration at the primary outputs $\tau_{out} = 0$, equations from [14] were modified to find an acceptable SET duration in the net n. In other words, we derived those equations to obtain the SET duration τ_n at the inputs of each gate as a function of the SET duration τ_{n+1} at its output.

Model proposed in [14] presents cases where the pulse is attenuated or propagated according to curve fitting. Through simulation, a parameter k is defined and used to determine how the pulse is attenuated. Based on the work presented in [14], we propose the following equations in order to find the maximum acceptable SET pulse duration in a node.

These equations were derived as follows.

$$\tau_n = \tau_g \left(k - ln \left(1 - \frac{\tau_{n+1}}{\tau_g (k+1)} \right) \right) \tag{17}$$

Situations where τ_n is larger than $k\tau_g$ and smaller than $(k+1)\tau_g$ are treated by (17).

$$\tau_n = \frac{\tau_{n+1} + \sqrt{\tau_{n+1}^2 + 4\tau_g^2}}{2} \tag{18}$$

Situations where τ_n is larger than $(k+1)\tau_g$ and smaller than $(k+3)\tau_g$ are treated by (18).

Total attenuation (filtering out) is considered if τ_n is smaller than k times τ_g, and propagation without attenuation if τ_n is larger than $(k+3)$ times τ_g. Function `sizeTransistors(s, g, τn)` finds the smallest transistors width for a gate g according to the transient pulse duration τ_n. The idea is to increase "ON" transistors according the resistance associated to them and the resulting diffusion capacitance of this sizing.

The transistor sizing is modeled based on the equations presented in Sect. 4. The algorithm consists on applying the bisection method [15] to find the width of each pull-up and pull-down transistor of the gate.

Table 3 The proposed transistor sizing to single event transient attenuation

Circuit	Gate sizing		duplication		Asymmetric	
	timing (%)	Area (%)	timing (%)	Area (%)	timing (%)	Area (%)
S838	0.4	39.4	12.7	32.9	8.9	23.3
S1196	16.3	57.0	33.8	37.7	1.0	43.3
S1488	20.1	26.2	26.0	37.4	11.7	18.7
S5378	12.9	50.6	33.1	42.4	5.6	33.8
S9234	10.2	41.0	30.0	37.3	5.7	22.1
S13207	3.7	45.3	23.0	41.3	7.4	25.1
S15850	6.5	44.8	32.6	42.3	10.7	23.6
S35932	50.0	43.2	43.7	45.5	26.9	19.6
S38417	10.6	48.6	37.8	42.8	11.0	27.7
S38584	31.2	49.0	40.3	47.1	11.9	28.2
Average	16.3	44.5	31.3	40.7	10.0	26.5

Results show the area and timing overhead for some ISCAS'89 Circuits for particles with charge $Q = 0.2$ pC

7 Results

Table 3 shows some results obtained by the proposed transistor sizing strategy. Results include a comparison

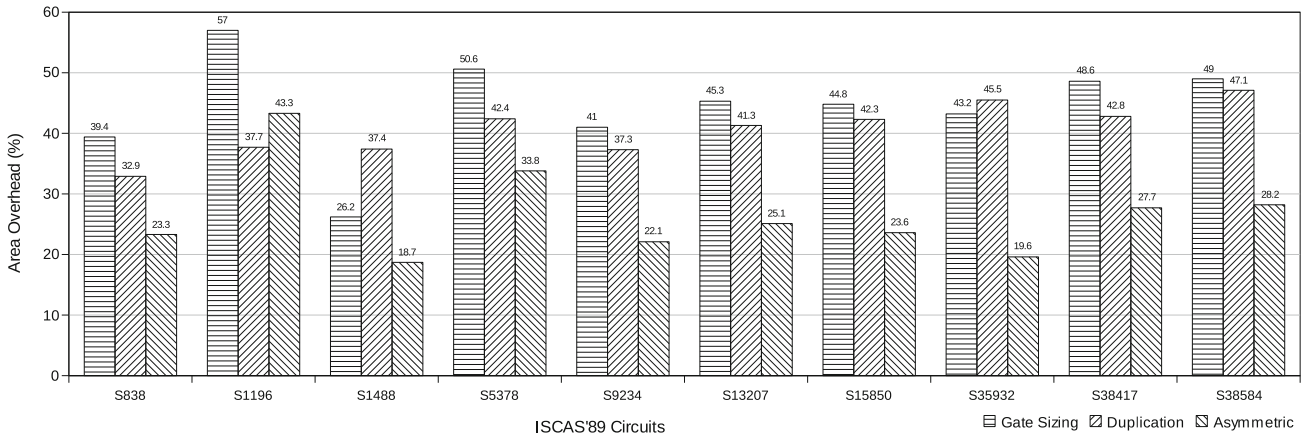
between symmetric and asymmetric sizing methodologies for a 130-nm technology process [16]. The transient pulse propagation parameter k was defined by HSPICE simulations to be equal to 0.8 for this particular technology and energetic particles of interest.

A study presented in [8] shows that the deposited charge of very few particles at ground level is higher than 0.2 pC for 130 nm technologies. In our experiments, we consider this to be the worst case deposited charge. The technique here proposed is compared with gate sizing technique presented in [8] and gate duplication techniques [6,7]. For the gate sizing technique, gates are exchanged by larger versions, with larger driving capability. Gate duplication consists in inserting other gates in parallel.

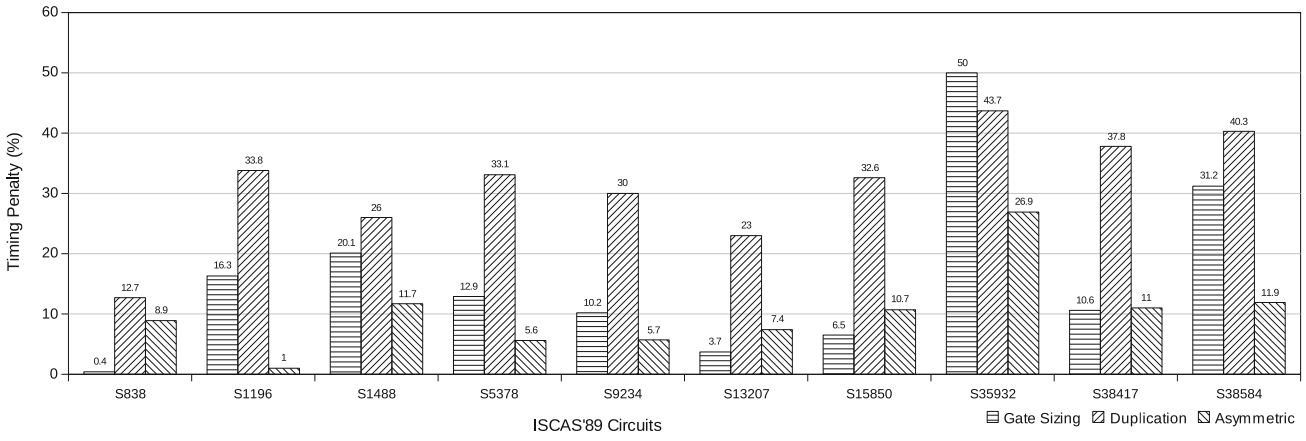
It is important to note that the approach here presented is adequate for circuits operating at terrestrial environment. For circuits operating in aero-space applications, the approach presented here may not be adequate. In aero-space applications heavy ions may be found. Heavy ions may deposit large amounts of charge, and in this case transistor sizing is not accepted as a SET mitigation technique. Indeed, if heavy ions with high energy are a concern, transistor sizing may even increase circuit sensitivity to SET [17].

The first important point shown by these results is the small overhead presented by the proposed methodology. The worst case was 28% area overhead for complete protection (0% sensitivity) against particles with charge $Q = 0.2$ pC. Results show an average 44.5% area overhead for the gate sizing, 40.7% for the duplication technique and 26.5% for the asymmetric sizing. Results show average timing penalties of 16.3, 31.3 and 10% for gate sizing, duplication and asymmetric sizing, respectively.

PMOS and NMOS transistors have different electric behavior and, for this reason, effects of particles hitting the device are different when output signal is stable in "1" or "0". The area overhead of the gate sizing technique can be explained because, even if gates present balanced rise–fall timing, they do not guarantee a balanced SET attenuation.



(a)



(b)

Fig. 4 The proposed transistor sizing to single event transient attenuation. Results show the area overhead **a** and timing penalties **b** for some ISCAS'89 circuits for particles with charge $Q = 0.2$ pC as shown in Table 3

In the case of gate duplication, another important point is that the wire insertion needed to put gates in parallel also contributes to the huge timing penalty.

8 Conclusions

A new transistor sizing algorithm aiming at protecting combinational logic circuit against single event transients is presented in this paper. The sensitivity of the circuit is analyzed by taking into account the logical and electrical masking.

The proposed technique consists on sizing only transistors directly related to the SET attenuation. It is known that PMOS and NMOS transistors have different characteristics in relation to mobility, impurity concentration and, as consequence, the delay. For a given particle with charge Q, PMOS and NMOS transistors present different attenuation characteristics. Thus, the model considers independently pull-up and pull-down blocks.

The model takes into account propagation characteristics in which the degradation of the transient pulse is considered in order to reduce sizing penalties. Results show smaller area, and timing penalties if compared to a symmetrical sizing methodology.

Figure 4 graphically illustrates the results shown in Table 3. Note that the asymmetric sizing presents a good trade-off concerning occupied area and timing penalties in relation to the other techniques. Besides the asymmetric sizing is very effective regarding the occupied area, the technique is very competitive with the gate sizing methodology when timing penalties are evaluated.

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