Asymmetrical Multi-level DC-link Inverter for PV Energy System with Perturb and Observe Based Voltage Regulator and Capacitor Compensator

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***Abstract*—In this paper, a perturb and observe (P&O) based voltage regulator (POVR) and a capacitor compensator (CC) circuit are proposed for the implementation on 31-level asymmetrical switch-diode based multi-level DC-link (MLDCL) inverter. Since the application of MLDCL in a standalone photovoltaic (PV) system requires constant DC voltages from PV panels, the POVR strategy is deployed to regulate the voltage along with the capability to deliver the maximum power at full load. Boost DC-DC converters are used as the interface between the panels and the inverter for the POVR operation. The results show that POVR is capable of achieving the desired fixed DC voltages even under varying environmental and load conditions, with a steady 230 V at the output. At full load, the standalone system successfully delivers 97.21% of the theoretical maximum power. Additionally, CC is incorporated to mitigate voltage spikes at the output when supplying power to inductive loads. It successfully eliminates the spikes and also reduces the total harmonic distortion (THD) of output current and voltage from more than 10% to less than 5%, as recommended in IEEE 519 standard.**

***Index Terms*—Multi-level inverter, photovoltaic (PV) system, maximum power point, voltage regulator, capacitor compensator (CC).**

I. Introduction

RENEWABLE energy sources receive increased attention due to the initiatives towards increasing the capacity of renewable energy production [1], and reducing the dependency on fossil fuels that will cause the environmental pollution and climate change in the long run [2]. Since photovoltaic (PV) energy is clean, environmentally friendly, readily available and free to harvest, it has become one of the most common types of renewable energy source in both residential and industrial areas [3]. It is used in a variety of applications such as water pumping system, battery charging station, solar vehicles and standalone system for off-grid applications [4]-[7].

The real-time application of an off-grid PV energy system consists of PV panels, DC-DC converter, DC-AC inverter and load [8]. However, the output of a PV panel is not constant since it depends significantly on solar irradiation and temperature [9]. Maximum power point tracking (MPPT) algorithm can be implemented to harvest peak energy from PV panels [10]. The DC-DC converter is a necessary element when MPPT is to be considered since it works by continuous duty cycle adjustment [11], [12].

Considering the necessity of employing DC-AC inverter in a PV system, multi-level inverter (MLI) is preferable nowadays compared to the conventional voltage source inverter (VSI) due to its capability to produce power quality with minimal error [13]. Traditional MLIs such as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) possess one common drawback, which is the massive amount of components required [14]. The number of devices is also directly related to the number of MLI level, which in turn causes the overall system to be costly, bulky and complex [15]. Researchers have been working to reduce the number of required devices. Several reduced switch MLIs have been proposed in the literature with their own merits and demerits [16], [17].

MLI can be divided into isolated or non-isolated DC source. Isolated MLI implements separate DC sources, while non-isolated MLI requires only a single source [15]. Isolated MLI is further categorized into symmetrical or asymmetrical source configuration. Symmetrical configuration uses equal voltage for each DC source, while asymmetrical configuration uses different values for the DC sources either by the binary or trinary methods [14]. Some MLI topologies pro-

Manuscript received: March 9, 2019; accepted: December 9, 2019. Date of CrossCheck: December 9, 2019. Date of online publication: September 3, 2020.

This work was supported in part by the Postgraduate Fellowship from Universiti Sains Malaysia and in part by University Sains Malaysia (No. RUI 1001/PELECT/8014027).

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DOI: 10.35833/MPCE.2019.000147

posed in [18] can work in both ways. Asymmetrical source configuration is a better choice in a PV system, especially in a low- to medium-voltage application since the number of PV modules N_{pv} required can be optimized. For instance, most binary sources based asymmetrical MLI can produce up to $2^{N_{pv}+1}-1$ output levels compared to only $2N_{pv}+1$ output levels when using symmetrical sources. A lot of emerging MLIs use H-bridge as a polarity generator. Such topologies are not suitable for high-voltage applications since the voltage stress at the H-bridge can be very high [19]. Isolated MLI is ideal for PV integration since separate PV panels can be directly used as independent sources. In non-isolated MLI such as NPC and FC, voltage balancing of capacitors might be a challenge [20].

Multi-level DC-link (MLDCL) inverter is one of the most commonly-used reduced switch MLI [21]. It uses a significantly lower number of switches than traditional MLI. Further reduction in the switch can be realized by removing one switch from each stage and replacing it with diodes. This configuration is suitable for low-voltage applications [17]. However, voltage spikes will be introduced by the replacement at the output under inductive loads [22]. The presence of these voltage spikes will cause several power quality problems such as over-voltage, distorted current waveform and a significant increase in total harmonic distortion (THD). Some literature limits the operation of such configuration based on an acceptable power factor range at which the voltage spikes produced on the output are minimal [23]. In [24], only resistive loads are used to avoid the production of voltage spike.

To use PV as the input to an inverter, it is compulsory to have a voltage control technique for producing constant DC voltage. For a standalone system, the proportional-integral (PI) controller can be implemented to adjust the duty cycle of a DC-DC converter by taking the output of the converter and comparing it with the desired reference value [25]. However, the PI controller does not consider MPPT, and it is not possible to control the same DC-DC converter using both MPPT algorithm and PI controller. Several methods have been proposed to tackle this issue in a standalone PV system. One of them is implementing artificial intelligence (AI) such as fuzzy, particle swarm optimization (PSO) and genetic algorithm (GA) to auto-tune the PI controller for voltage regulation [26], [27]. Another proposed method is cascading two DC-DC converters, one for MPPT and the other for voltage regulation [28]. In some literatures, MLDCL inverter is typically implemented with MPPT. However, the DC-link control is not considered, and the outputs are controlled by the load [24], or under constant input irradiance and temperature [29].

In this paper, the design of standalone PV system using 31-level asymmetrical switch-diode based MLDCL inverter integrated with proposed perturb and observe (P&O) based voltage regulator (POVR) and capacitor compensator (CC) is presented. Due to the feasibility of using isolated MLI in a PV system, the MLDCL topology is an excellent choice due to its number of DC source with low ratio of voltage level. The proposed POVR acts as the DC-link voltage controller. It does not require any PI controller and is capable of delivering maximum PV power even under varying irradiance, temperature and load conditions. Besides, it provides a wide range of voltage regulating capability and eliminates the need for different DC-DC converters under different operation conditions. From the literature review, there are little discussions on voltage control technique for the application of MLDCL in a standalone PV system. CC is also proposed to counter-measure the production of voltage spikes under inductive loads at the output, improving the THD significantly. Simulation is conducted to evaluate the proposed system under several conditions using MATLAB/Simulink.

II. Modelling of Proposed System

A. PV Module and Boost DC-DC Converter

In this paper, a single diode model of PV module is used and modelled accurately for the simulation where shunt resistance R_P and series resistance R_S are taken into consideration. The boost converters are used to boost and regulate the PV voltages before feeding them to the MLDCL inverter. The diagram of a boost converter and its feedback mechanism used in each PV stage is shown in Fig. 1, where C_{in} and C_{out} are the input and output capacitors, respectively; I_{pv} and V_{pv} are the current and voltage of PV, respectively; and V_{err}, V_{DC}, and V_{ref} are the voltage error, the actual output voltage of the boost DC-DC converter, and the reference DC voltage, respectively. C_{in} is required to ensure continuous output from PV panel [30].

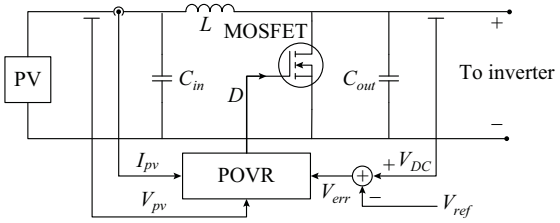

Fig. 1. Boost converter with PV source and proposed POVR.

B. 31-level Asymmetrical Switch-diode MLDCL Inverter

MLDCL inverter is a type of hybrid MLI which consists of two stages. The first stage is the level generation part, where positive and zero voltage levels are generated to synthesize the waveform of stair-case output voltage. The second stage is the polarity generator part used to reproduce the second half-cycle of the generated waveform into negative levels. Figure 2 shows the circuit diagram of the 31-level asymmetrical switch-diode based MLDCL inverter.

For the asymmetrical operation of the MLDCL topology, it is more appropriate to use the binary source configuration where the voltage levels are determined by geometric progression (GP) with a factor of 2 [14]. Thus, in this paper, the voltage sources for the 31-level MLDCL are V_{DC}, $2V_{DC}$, $4V_{DC}$, and $8V_{DC}$. The relationship can be given as:

$$\frac{V_{DC2}}{V_{DC1}}=\frac{V_{DC3}}{V_{DC2}}=\frac{V_{DC(n)}}{V_{DC(n-1)}}=2 \tag{1}$$

It is important to analyse the voltage across the switches and the peak inverse voltage V_{PIV} of the diodes in order to select the most suitable components to be used. Selected devices for the implementation should have the maximum block-

ing voltage V_B and V_{PIV} rating higher than the blocking voltage and V_{PIV} measured. The blocking voltages of all the switches and PIV of all the diodes in this topology are given by:

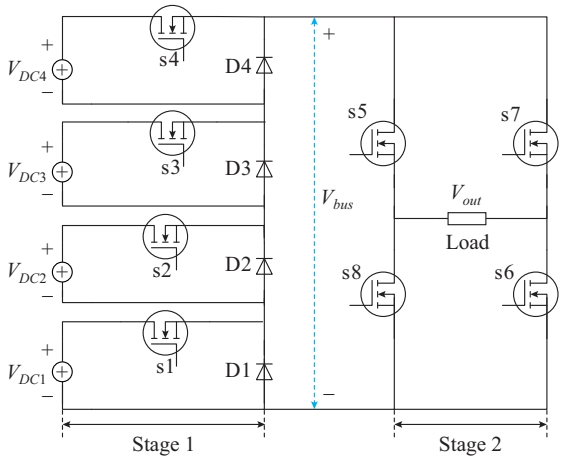

Fig. 2. Topology of 31-level asymmetrical switch-diode based MLDCL inverter.

$$V_{B,s1} = V_{PIV,D1} = V_{DC} \tag{2}$$

$$V_{B,s2} = V_{PIV,D2} = 2V_{DC} \tag{3}$$

$$V_{B,s3} = V_{PIV,D3} = 4V_{DC} \tag{4}$$

$$V_{B,s4} = V_{PIV,D4} = 8V_{DC} \tag{5}$$

$$V_{B,s5} = V_{B,s6} = V_{B,s7} = V_{B,s8} = 15V_{DC} \tag{6}$$

where $V_{B,sn}$ is the blocking voltage of switch; and $V_{PIV,Dn}$ is the PIV of each diode.

On the other hand, the maximum current I_m flowing through each switch or diode is the same as the load current I_{Load}, and it is zero when they are not conducting [31]. It can be given as:

$$I_{m,s1} = I_{m,D1} = \ldots = I_{m,sn} = I_{m,Dn} = I_{Load} \tag{7}$$

where $I_{m,sn}$ is the maximum current through the switch; and $I_{m,Dn}$ is the maximum current through the diode. Table I presents the switching states of the generation stage for the 31-level asymmetrical switch-diode MLDCL inverter. The switching states are the same for both half-cycles. The switching states at the polarity generation stage are given in Table II. The overview of the proposed standalone PV system is shown in Fig. 3, where PWM stands for pulse width modulation.

TABLE I
SWITCHING STATES AT STAGE 1 OF 31-LEVEL ASYMMETRICAL SWITCH-DIODE MLDCL INVERTER

Level	Switching state			
	s1	s2	s3	s4
$15V_{DC}$	1	1	1	1
$14V_{DC}$	0	1	1	1
$13V_{DC}$	1	0	1	1
$12V_{DC}$	0	0	1	1
$11V_{DC}$	1	1	0	1
$10V_{DC}$	0	1	0	1
$9V_{DC}$	1	0	0	1
$8V_{DC}$	0	0	0	1
$7V_{DC}$	1	1	1	0
$6V_{DC}$	0	1	1	0
$5V_{DC}$	1	0	1	0
$4V_{DC}$	0	0	1	0
$3V_{DC}$	1	1	0	0
$2V_{DC}$	0	1	0	0
$1V_{DC}$	1	0	0	0
0	0	0	0	0

TABLE II
SWITCHING STATES AT STAGE 2 OF 31-LEVEL ASYMMETRICAL SWITCH-DIODE MLDCL INVERTER

Polarity	Switching state			
	s5	s6	s7	s8
Positive (+)	1	1	0	0
Negative (–)	0	0	1	1

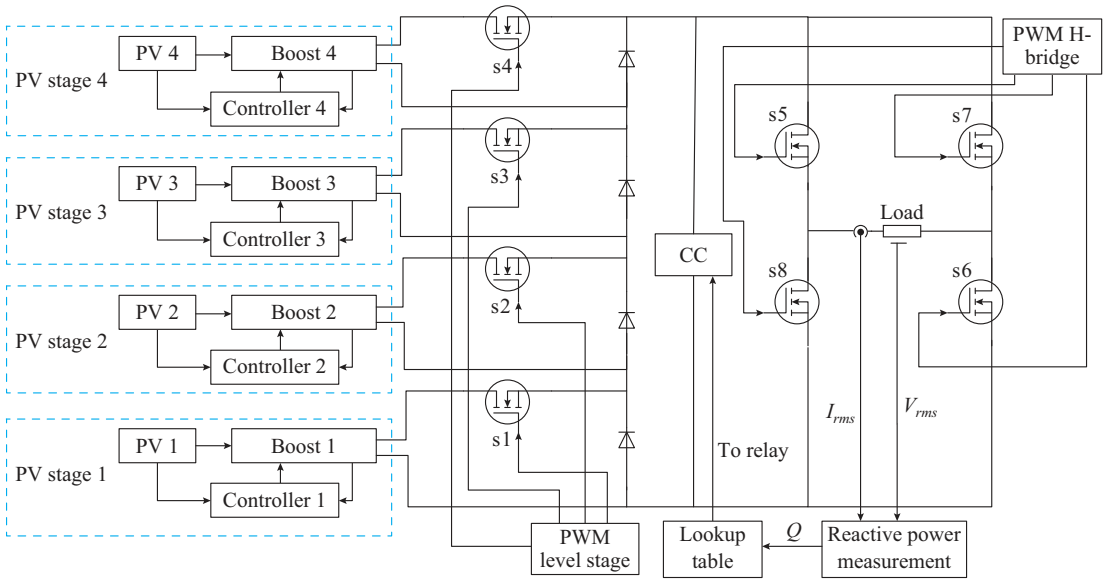

Fig. 3. Overview of proposed system and controller scheme.

C. Circuit of CC

At the inductive load, the output current of an inverter lags the output voltage by an angle α. During the time between 0 and α, the output power is negative. This phenomenon causes the voltage spikes in the output voltage waveform for the application of switch-diode based MLDCL topology as shown in Fig. 4. It can be observed that the voltage spikes are produced at the beginning of both positive and negative cycles of the voltage waveform during which the power is negative. If the power factor is lower, the value of α will be higher. Thus, wider voltage spikes will occur and further increase the THD of the AC output voltage.

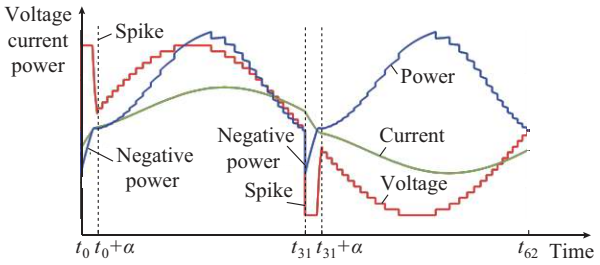

Fig. 4. Inductive load effect on MLDCL inverter.

To tackle this issue, a CC circuit is introduced as shown in Fig. 5. CC is placed between the first and second stages of the MLDCL inverter as depicted in Fig. 3. It operates by providing leading power factor components to compensate the lagging power factor components from the inductive loads.

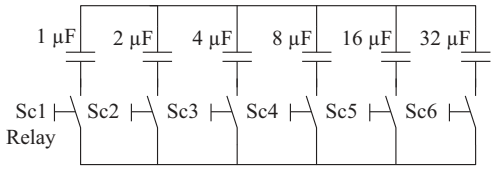

Fig. 5. Diagram of proposed CC circuit.

In this paper, CC consists of six capacitors connected in series by means of relays. Relays are used instead of switches to avoid additional power switches into the existing topology and it is suitable for the low-voltage application of the system. The value of compensating capacitors C can be chosen using the following equation:

$$C = \frac{Q_C}{2\pi f V_{rms}^2} \tag{8}$$

where Q_C is the reactive output power; f is the output frequency; and V_{rms} is the root mean square (RMS) value of output voltage.

The selected values of capacitors in this paper are 1 μF, 2 μF, 4 μF, 8 μF, 16 μF and 32 μF. This combination is capable of producing capacitance values ranging from 1 μF to 63 μF. The designed CC circuit is able to produce compensating reactive power from 10 var to 1148 var. The maximum power $S_{\max}$ used by CC is given by:

$$S_{\max} = \frac{P}{pf} = \frac{Q_m}{\tan\left(\cos^{-1}(pf)\right)\cdot pf} \tag{9}$$

where P is the active power; Q_m is the maximum compensating reactive power; and pf is the power factor.

In this paper, the minimum pf is assumed to be at 0.6 lagging. The operation of CC can be divided into four modes as shown in Fig. 6 and they can be explained as follows.

1) Mode 1 (t_0 - $t_0+\alpha$). I_{bus} flows from the load to the CC circuit through the freewheeling diode of s5 and returns to the load through the freewheeling diode of s6 due to inductive load. I_{CC} acts as the return current since I_{bus} is blocked by the diodes and could not be returned to the sources.

2) Mode 2 ($t_0+\alpha$ - t_{31}). I_{bus} flows to the load through s5 and returns to the source through s6. I_{CC} flows in the same direction which is from CC circuit to s5, and returns through s6.

3) Mode 3 (t_{31} - $t_{31}+\alpha$). I_{bus} flows from the load to the CC circuit through the freewheeling diode of s7 and returns to the load through the freewheeling diode of s8 due to inductive load. I_{CC} acts as the return current since I_{bus} is blocked by the diodes and could not be returned to the sources.

4) Mode 4 ($t_{31}+\alpha$ - t_{62}). I_{bus} flows to the load through s7 and returns to the source through s8. I_{CC} flows in the same direction which is from the CC circuit to s7, and returns through s8.

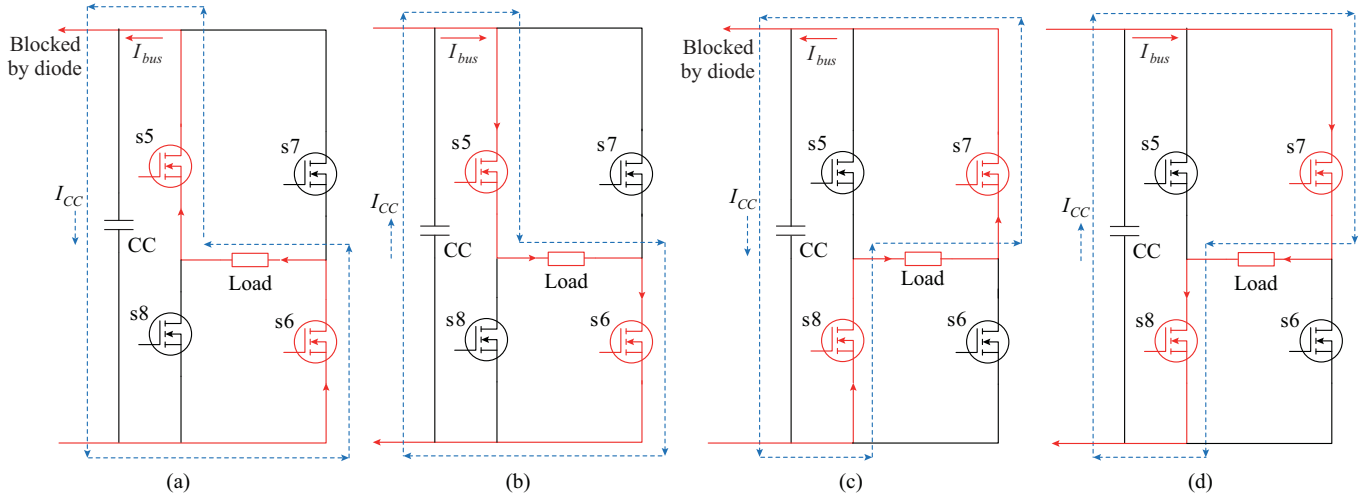

Fig. 6. Scheme of CC circuit operation. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

III. Control Strategies

A. Proposed POVR

A DC-link voltage controller based on P&O MPPT technique is proposed in this paper in order to achieve fixed output voltage from a DC-DC converter while maintaining the capability to deliver the maximum power to the loads from the PV panel. The proposed algorithm is designed mainly for the control of the standalone MLI and is an alternative to PI-based regulator. The complete understanding of the operational concept can be obtained from the flowchart of the proposed POVR, as shown in Fig. 7.

The proposed POVR also aims to combine the operation of MPPT and voltage regulation into a single algorithm without affecting the modulating index of switching PWM at generation level. Compared with the original P&O MPPT algorithm, the main difference in the operation of the proposed POVR is the addition of V_{err} inspection stage upon checking the PV power, before proceeding with the next stage of P&O. This enables the algorithm to achieve the required voltage regulation. Referring to Fig. 7, this technique contains additional yes/no loops for the checking of voltage and changing of duty cycle, which are not available in the original P&O algorithm.

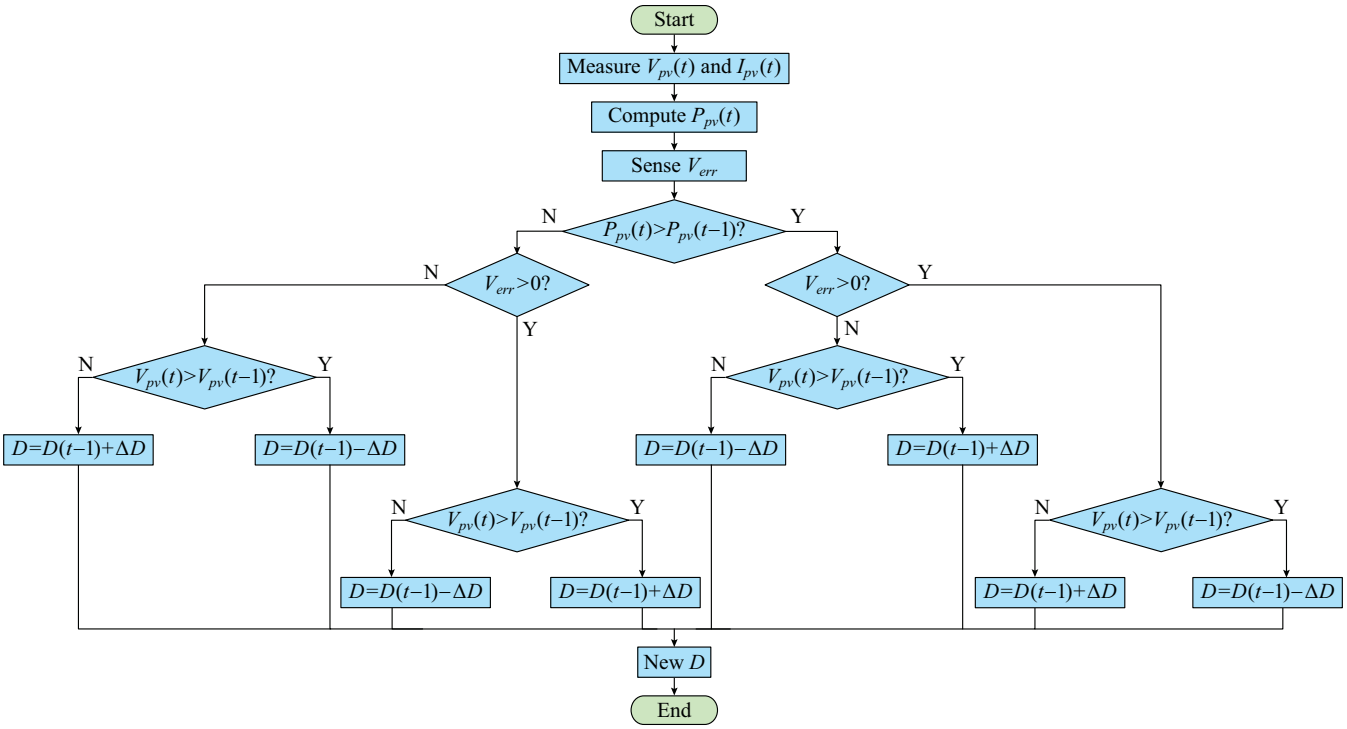

Fig. 7. Flowchart of proposed P&O based voltage regulator.

Thus, the proposed algorithm will require the acquisition of V_{err} which is the difference between V_{ref} and V_{DC}, as shown in Fig. 1. It works by enabling the tracking algorithm to operate at the wide range of the panel P-V curve in comparison to the classic PI regulator. PI regulator always works near the open-circuit voltage V_{oc}. Thus, the problem arises when the reference voltage is set at a voltage level lower than the voltage at the maximum power point V_{mpp} when a boost converter is used. In this case, a buck or buck-boost converter will be required.

The proposed regulation technique has a wider operation range, and a single type of DC-DC converter can be used within the operation range. For instance, it can operate at the range of input voltage from 0 V up to V_{mpp}. Thus, by controlling the duty cycle D, the range of output voltage from a boost converter will be from 0 V to $V_{mpp}/(1-D)$ as demonstrated in Fig. 8. At full load, the algorithm will ensure the maximum power delivery to the load. At another load level, V_{pv} will be tracked to the P-V curve accordingly.

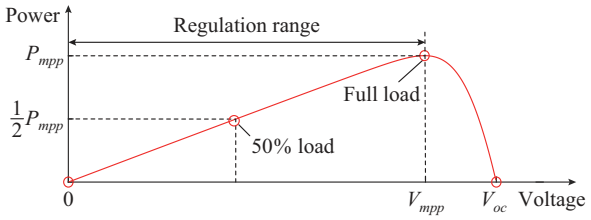

Fig. 8. Operation region of POVR.

When using a boost converter, even if the reference voltage is set lower than V_{mpp}, the algorithm can still work by reducing the PV voltage V_{pv} to the point that is possible to achieve the desired voltage level by stepping up the operation of the converter. In case of a buck converter, when the reference is set higher than V_{mpp}, the algorithm will increase the V_{pv} until it can be stepped down to achieve the targeted value.

Another demerit of the classic PI controller based voltage regulator in a standalone PV system is the demand for proper tuning in order to achieve the desired regulated DC volt-

age. It is also important to note that the controller might need to be re-tuned at the changing load rate, irradiance and reference value. Additionally, the PI controller does not track for MPP, which makes it difficult to be operated at full load. Self-tune techniques of PI controllers that implement AI methods such as fuzzy, PSO, and GA can be used. Even though AI-based optimizations are accurate, which are quite complex to be implemented. The proposed voltage regulator completely gets rid of the demand for PI controller, and it is capable of delivering the maximum power at full load.

B. Control of CC Circuit

The proposed CC generally operates upon the value of reactive power for the inverter output. The RMS values of output voltage and current are measured to calculate the reactive power Q. The value of Q can be obtained as:

$$S = V_{rms} I_{rms} \tag{10}$$

$$P = V_{rms} I_{rms} \cos\alpha = V_{rms} I_{rms} \cdot pf \tag{11}$$

$$Q = \sqrt{S^2 - P^2} \tag{12}$$

where I_{rms} is the RMS value of output current; and S is the apparent power. Next, from the obtained value of reactive power, a lookup table is used to control an appropriate combination of capacitors to be injected into the circuit by switching on/off the relay operation based on (8). All the control actions explained for CC operation can be implemented by using voltage sensor, current sensor and microcontrollers. For the purpose of simulation, a MATLAB/Simulink function block is used to control the relay action based on the lookup table. Digital signal processing (DSP) unit or similar controllers can be used if the control scheme is to be implemented experimentally.

C. PWM Technique

Similarly, like other MLI topologies, several PWM techniques can be implemented for the operation of reduced switch MLDCL inverter. The most popular PWM strategy is the carrier-based sinusoidal PWM. The only difference is the combination of the signals to be compared using relational operators in generating gate pulses. The combination can be determined from the switching states given in Table I and Table II. Besides, pre-determined switching angles or selective harmonic elimination (SHE) technique can also be used if the operation is to be implemented using a controller. Figure 9 demonstrates the generated switching signals for all the switches.

IV. Results and Discussion

The proposed system is tested using the MATLAB/Simulink platform to evaluate its performance under several test conditions. The specification under standard operation conditions (SOCs) of the PV panel model SPM100-M from solar power mart used in the simulation is given in Table III. Using the binary asymmetrical configuration, the reference values at the output of each boost converter are set at the ratio of $V_{DC1}:V_{DC2}:V_{DC3}:V_{DC4} = 1:2:4:8$. The selected values and the configuration of PV panels at each stage are given in Table IV.

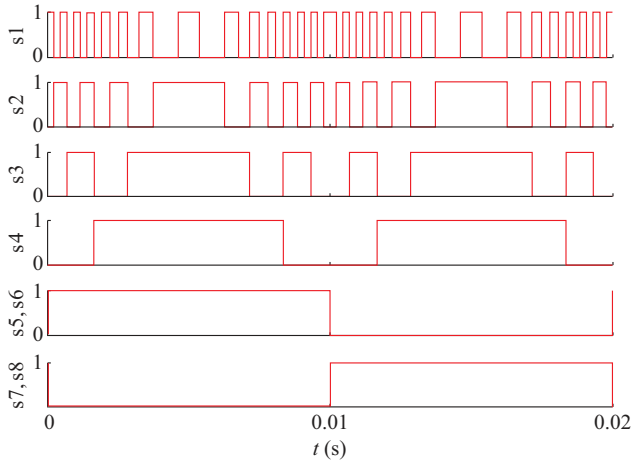

Fig. 9. Generated switching signals.

TABLE III
Parameters of PV Panel Model SPM100-M

Parameter	Value
Maximum power P_{mpp} (W)	100.125
Voltage at MPP V_{mp} (V)	18.75
Current at MPP I_{mp} (A)	5.34
Open-circuit voltage V_{oc} (V)	22.53
Short-circuit current I_{sc} (A)	5.7
Temperature coefficient of V_{oc} (%/°C)	–0.35
Temperature coefficient of I_{sc} (%/°C)	0.05
Temperature of normal operation cell (°C)	25

TABLE IV
Panel Arrangement and Respective DC Reference

Stage	Panel No.	Connection	Reference DC voltage (V)
1	1	Series	21.68
2	2	Series	43.37
3	4	Series	86.74
4	8	Series	173.48

These reference values are selected in order to achieve the peak voltage of 325.27 V and the RMS value of output voltage of 230 V. The same switching frequency of 20 kHz is used in all boost converters.

A. Resistive-inductive (RL) Load and CC Test

The irradiance value of 800 W/m^2 at the temperature of 31 °C is selected as the test condition. Several combinations of RL loads are chosen to produce different values of reactive power at the inverter output with power factor ranging above 0.6. The simulation results under inductive loads are given in Table V. The table includes the combined capacitance values when CC operates and the percentage contribution of active power towards the apparent power indicated as $(P/S)^2$.

From Table V, it is proven that the implementation of the CC circuit has improved the quality of the output waveforms and complies with the THD standard as recommended in IEEE 519. Under all combinations of RL loads, both the voltage and current of THD values are above 5% and reach

as high as 33.43% when the CC circuit is turned off. They are successfully improved with the CC circuit where THD values go down to 3% below for voltage and 1% for current, respectively. It can also be seen that the contribution of active power towards the apparent power is increased with the operation of the proposed CC circuit since the power factor is slightly improved and the voltage spikes are completely removed.

TABLE V
SYSTEM ANALYSIS UNDER RL LOAD

CC	Resistance (Ω)	Inductance (mH)	Power factor	Apparent power (VA)	Active power (W)	Reactive power (var)	THD of voltage (%)	THD of current (%)	CC capacitance (μF)	$(P/S)^2$ (%)	$(Q/S)^2$ (%)
Off	684.0	730	0.93	74.16	69.10	26.91	19.13	7.52	0	86.83	13.17
On			0.95	74.13	70.41	23.19	2.68	0.66	1	90.21	9.79
Off	125.0	243	0.83	377.78	313.87	210.25	30.88	9.95	0	69.03	30.97
On			0.86	367.08	316.35	186.20	2.59	0.64	11	74.27	25.73
Off	54.0	146	0.74	812.64	605.01	542.53	33.15	10.25	0	55.43	44.57
On			0.78	758.41	590.24	476.24	2.63	0.66	28	60.57	39.43
Off	32.6	122	0.64	1208.06	776.72	925.27	33.43	10.04	0	41.34	58.66
On			0.67	1069.41	721.15	789.67	2.65	0.68	47	45.47	54.53

To further demonstrate the effectiveness of the CC circuit, the output waveforms, before and after its inclusion, are shown in Fig. 10(a). It is clear that without the CC circuit, voltage spikes occur at each zero crossing until the angle of α. With the CC circuit, the voltage pikes are almost completely mitigated.

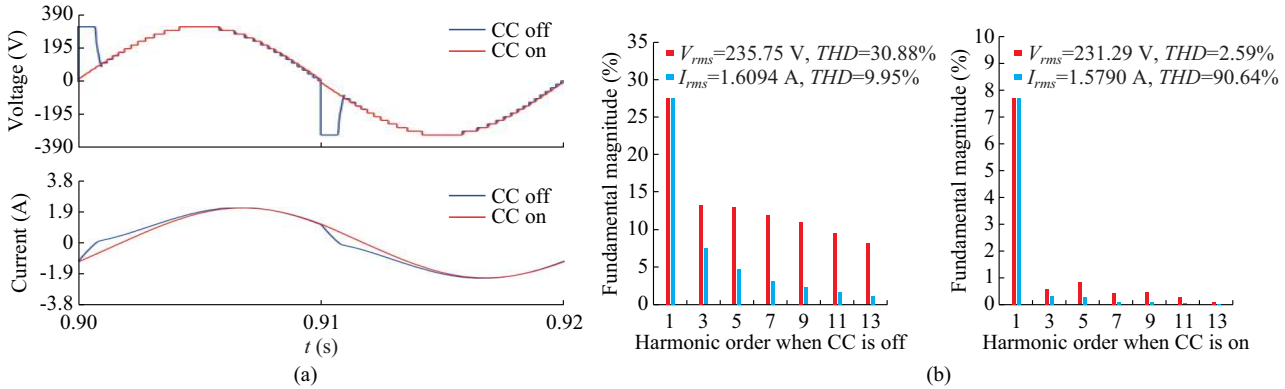

Fig. 10. Comparison with and without CC circuit under RL load (125 Ω, 243 mH). (a) Output waveforms. (b) Fast Fourier transform (FFT) analysis.

Next, the harmonic spectrums for both operations are illustrated in Fig. 10(b) for the operation without and with CC circuit as labelled in the figure, respectively. Figure 11 shows the startup operation of the system using RL load of 125 Ω, 243 mH. At 0.36 s, the system has reached the targeted RMS value of output voltage of 230 V with the final CC capacitance value of 11 μF at the reactive power of 186.20 var. Figure 12 presents the effect of CC circuit at the other RL loads.

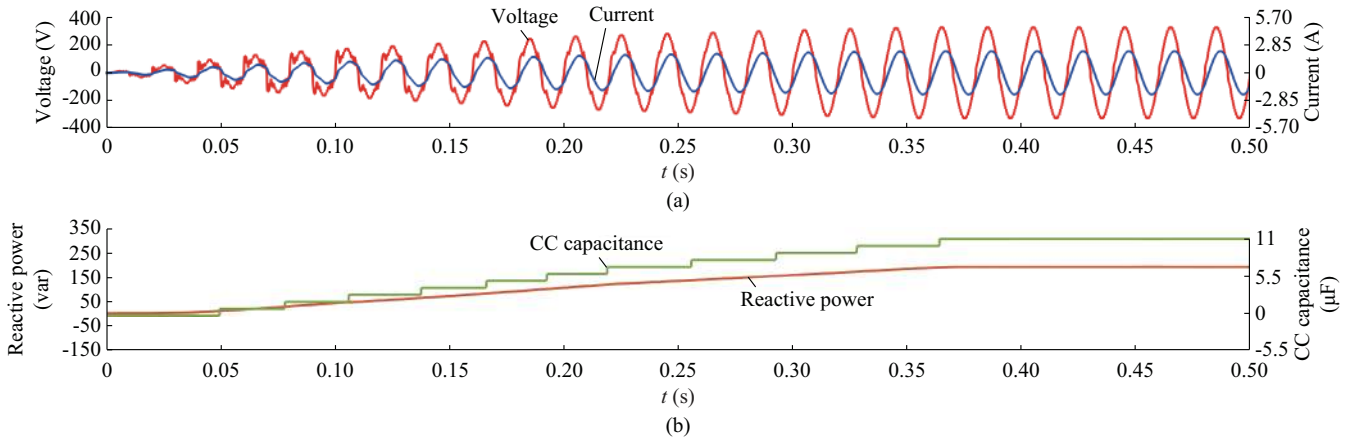

Fig. 11. Startup behavior. (a) Output voltage and current. (b) Measured reactive power and CC capacitance.

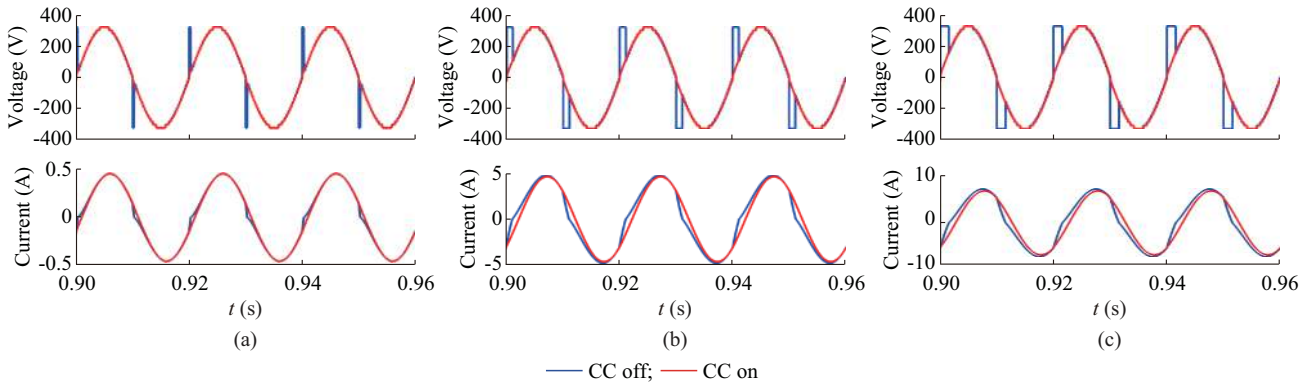

Fig. 12. Output waveform with and without CC circuit at different RL loads. (a) 684 Ω, 730 mH. (b) 54 Ω, 146 mH. (c) 32.6 Ω, 122 mH.

B. Proposed POVR Test

In order to validate the the performance of the algorithm in maintaining the desired DC-link voltage, the POVR is tested with a constant load under varying solar irradiance and voltage reference. The output from a boost converter is observed in this test. The third stage is selected which consists of four PV panels connected in series to produce the reference DC voltage of 86.74 V. The obtained DC-link voltage under sudden changes in irradiation at a fixed temperature of 31 °C is shown in Fig. 13(a). It can be observed that the proposed regulation technique has a faster initial response time without overshoot to achieve the desired output in comparison to the classic PI controller. It also takes minimal time to re-track for the desired voltage at the point of irradiance change. The initial overshoot from PI controller can be minimized with careful tuning. However, different tuning might be required when there is a change in load, environmental condition and reference value.

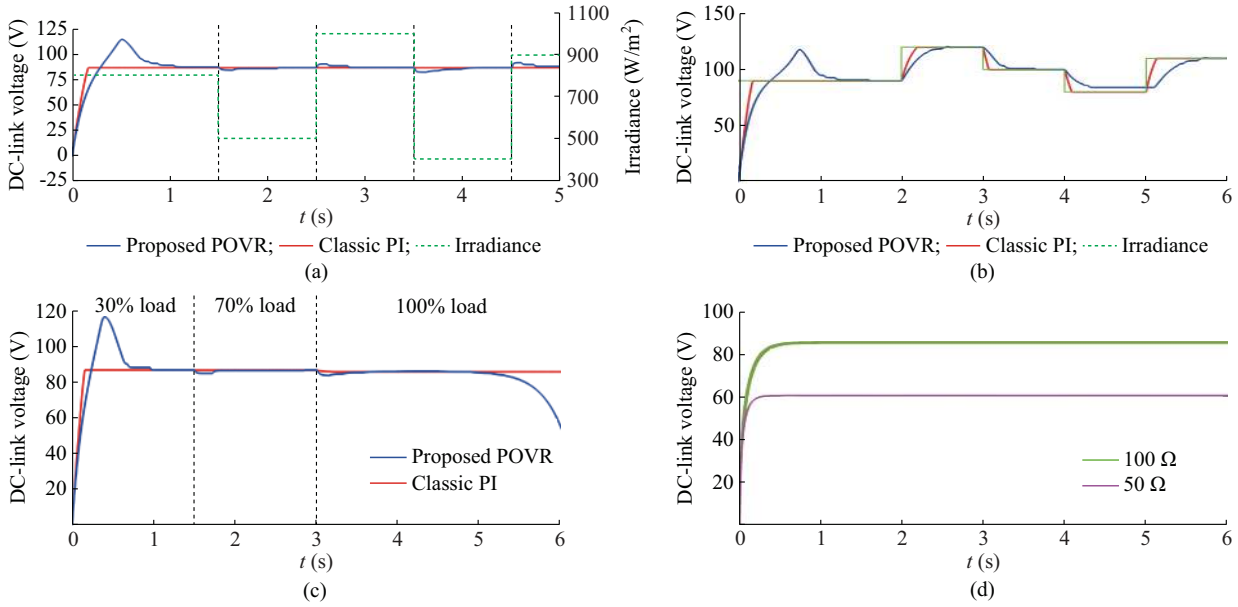

Fig. 13. DC-link voltage. (a) Under varying irradiance. (b) Using different reference values. (c) Using different load ratings. (d) Using different loads with the maximum value.

Meanwhile, the DC-link voltage obtained at different reference value is demonstrated in Fig. 13(b). Again, the proposed POVR requires less time to achieve the desired output, and it is able to track for all the selected reference values. For time duration from 4 s to 5 s, the PI regulator fails to achieve the reference value since the V_{pv} is higher than the V_{mpp}, and the reference value is set lower than the V_{mpp}. Therefore, a boost converter cannot be used with the PI controller.

Lastly, the DC-link voltage obtained at different load ratings is given in Fig. 13(c). Here, the PI controller seems to fail in maintaining the desired output voltage at 100% load in comparison to the proposed POVR. These tests prove that the proposed algorithm is able to regulate DC-link voltage even under varying environmental condition, load and reference value. Moreover, in a real-time application, the conditions do not change at a sudden rate as in the simulation.

The simulation is done in such manner to test the reaction of the proposed algorithm under extreme environmental conditions.

Another aspect that is worth discussing is the boosting capability of the converters when implementing the POVR. In

general, the voltage from a PV panel can be boosted according to the following relationship:

$$V_B = \frac{0 \rightarrow V_{mpp}}{1-D} \tag{13}$$

where V_B is the theoretical output voltage of boost converter. The voltage boosting capability is limited by the maximum power of the PV panel used. Thus, different boosting ranges can be expected at different loads as given by:

$$V_{O,\max} = \sqrt{P_{mpp} R} \tag{14}$$

where $V_{O,\max}$ is the maximum output voltage of boost converter; and R is the load resistance. For instance, a single PV panel operating at 31 °C and 800 W/m^2 of irradiance has P_{mpp} of 78.25 W. If the load of 100 Ω is used, the PV voltage can be boosted up to 88.46 V based on (14). At the load of 50 Ω, it can only be boosted up to 62.55 V.

Figure 13(d) shows the simulated output voltages of the boost converter at the tested loads. Thus, in designing a system with this strategy, a proper selection of the total number of PV strings is essential in ensuring the capability of the boost converters to produce the desired output. In this paper, the tested system is designed to optimally operate at the irradiance of above 700 W/m^2 and the temperature of up to 40 °C with the power of up to 1 kW while producing 230 V at the output. Lower irradiance can be operated at lower power. A wider operation range can be achieved by increasing the number of PV panels per stage.

C. Maximum Power Test

To further demonstrate the capability of POVR to deliver the maximum power in the proposed standalone PV system, the system needs to be examined under full load operation since the output power of a standalone PV system is limited by the load. Theoretically, at full load, the power will be at P_{mpp}.

Irradiance value of 800 W/m^2 at the temperature of 31 °C is again selected as the test condition. Since the number of PV panels used at each PV stage are different, the maximum power of each stage also differs. With the configuration described in Table IV, the maximum power that can be extracted from each PV stage under the selected test condition is 78.25 W, 156.3 W, 312.5 W, and 624.7 W, respectively. The total maximum power will be 1171.75 W. Therefore, a resistive load of 45.15 Ω is selected for testing purpose so that the system operates at full load according to the following equation:

$$R = \frac{V_{rms}^2}{P_T} \tag{15}$$

where P_T is the total maximum power at the combined PV stages. Table VI presents the simulation results of the power at different stages of the system. The total output power and power ratio for the system are 1142.05 W and 98.40%, respectively.

TABLE VI
POWER ANALYSIS UNDER FULL LOAD OPERATION

Stage	Output power (W)		Power ratio (%)	
	PV	Boost	MPPT	Boost
1	73.97	71.55	94.53	96.73
2	153.00	149.80	97.89	97.91
3	310.50	306.00	99.36	98.55
4	623.10	614.70	99.74	98.65
Total	1160.57	1142.05	99.05	98.40

It can be seen that the proposed POVR algorithm is capable of delivering the power required at full load with the ratio of 98.40% through the simulation, which does not include the effect of switching and conduction losses in the power devices. The purpose is to test the viability of the algorithm under ideal operation. The output voltage and current waveforms under testing condition are shown in Fig. 14(a) with their harmonic spectrums given in Fig. 14(b). The THDs of voltage and current are both 2.88%. This is well below the 5% limit as specified in IEEE 519 standard. By using the purely resistive load, the CC circuit is not operated since there is no reactive power component and the power factor is at unity. The waveform of the voltage and current are also similar except for the amplitude. Figure 14 clearly shows the 31-level output on both waveforms.

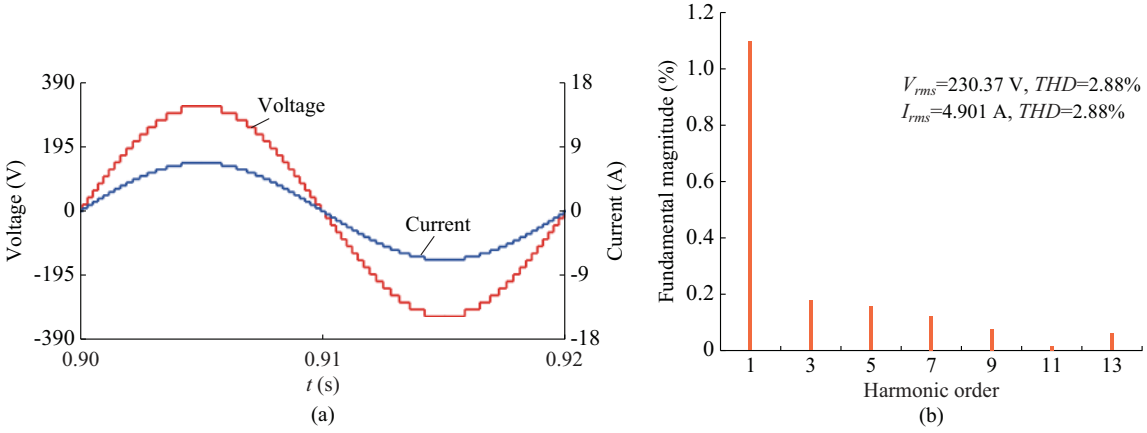

Fig. 14. Operation under full load operation. (a) Output waveforms. (b) FFT analysis.

D. Dynamic Load Test

A dynamic load test is carried out by changing the load during the system operation to check whether it is capable of maintaining its targeted AC output. Figure 15(a) shows the output voltage and current waveforms under changing load from purely resistive load of 106 Ω to an inductive load of 125 Ω and 243 mH. It is observed that the time taken for the CC circuit to operate after the sudden load change is around one electrical cycle before the spikes are removed. Next, the load is changed again from the previous 125 Ω, 243 mH inductive load to another inductive load of 54 Ω, 146 mH and the system response is shown in Fig. 15(b). Again, the CC circuit takes around one electrical cycle to change its relay switching pattern to mitigate the spikes when involving the inductive loads with different power factor levels. The test aims to simulate the capability of the system to work in real-time application since some types of loads such as the fluorescent lights might be operated dynamically.

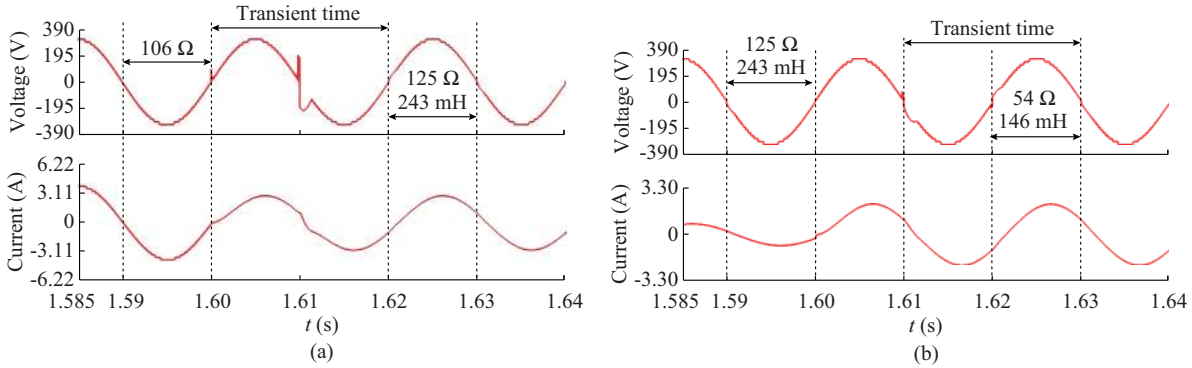

Fig. 15. Dynamic change. (a) *R* (106 Ω) to *RL* (125 Ω, 243 mH). (b) *RL* (125 Ω, 243 mH) to (54 Ω,146 mH).

V. Conclusion

The operation of a 31-level asymmetrical switch-diode based MLDCL inverter has been presented in this paper. A POVR for a standalone system is proposed to maintain the desired voltage level at the output of each DC-DC boost converter while maintaining the ability of delivering the maximum power under full-load operation even under varying environmental conditions. In the full-load test, the power obtained at the output of the system is found to be at 97.21% of the theoretical maximum power of the PV panels. This proves the tracking ability of the proposed algorithm for the maximum power. It is also observed that the regulation technique is able to re-track the desired DC-link voltage under a rapid change in irradiance, reference value and load with very minimal response time. In addition, a CC circuit is also proposed to mitigate voltage spikes at inductive loads. It is found that the THD values for both AC voltage and current can be reduced down to 5% below which complies with IEEE 519 standard. Without the CC circuit, THDs are greater than 5% and up to 33.43%. A further test at dynamic loads is carried out to prove the robustness of the whole system. The system takes one electrical cycle of response time at most to reproduce the desired inverter output when the load is suddenly changed from purely resistive to inductive load, and from inductive load to another inductive load at different power factor levels.

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