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Asymmetrical PCB Interconnect Tree Modelling with Coupling Effect

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***Abstract*— The paper describes integrity analysis of the signal propagating on asymmetrical tree with coupling from neighboring lines. Theoretical principle illustrating the modelling methodology and the developed routine algorithm is mathematically established. The developed model was applied to 2:1 asymmetrical microstrip tree with neighboring single lines at 10-to-100µm distance. Frequency- and time-domain analyses were conducted to check the coupling influence onto the signal distribution tree due to the substrate dielectric dispersion using broadband model. Examples of applications from DC to 10GHz were investigated to evaluate the influence of the coupling on the asymmetrical tree responses. It was shown that ringing effects and distorted signals were occurring from the two tree branch outputs. Furthermore, time-domain analyses were performed with 8-bits high speed input signal data with 0.5 Gbps rate. It was found that the signal quality was degraded and the amplitude of the shared signals was slightly affected by the coupling.**

Index Terms*— Behavioral model, asymmetrical tree, signal integrity, interconnect network, SIMO/SISO-transform.

I. INTRODUCTION

Signal and power integrity (SPI) and electromagnetic compatibility (EMC) phenomena become crucial when operating frequency, processing speed and integration density of digital electronic systems (DRAM, MPU, DIMM packages, etc. …) are increased [1-3]. Design and fabrication engineers have to respect required compliances notably in the interconnection networks such as memory buses (DDR4, GDDR5, XDR, IO2, HBM), front side bus (quick path interconnect, hypertransport), cable (USB, HADMI, FireWire Cat X), Ethernet (XAUI, XFI, CEI-6GLR, SONNET), etc. [3]. Fig. 1 illustrates an example of complex signal distribution interconnect tree [4]. Such a structure in the modern high speed memory system is challenging on the SPI and EMC constraints effects on interconnect lines (ILs) due to channel attenuation, crosstalk, reflection, delay and distortion [5-6]. So, prediction methods were developed based on various IL based approaches, such as RC- and RLC- models [7-8].

More generally, different models of interconnect tree topologies were developed [9-12]. But those models are not valid for structures presenting asymmetrical behavior, such as comb-tree depicted in Fig. 2. However, analytical model including the unbalanced interconnect tree was recently proposed in [13]. Firstly, the model assumed that the IL can be described by an RLCG equivalent circuit with frequency varying per unit length parameters ($R_u(f)$, $L_u(f)$, $C_u(f)$ and $G_u(f)$) by denoting f the frequency variable. Secondly, the circuit equivalent approach was used with the single input multiple output (SIMO) structure transformed into single input single output system (SISO) [13].

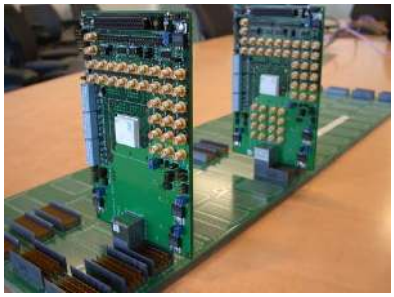

Figure 1. Electronic boards with complex interconnect tree network [4].

The analytical operations were handled with ABCD-to-Z matrix transform (to generate the IL impedance matrix), Z-to-Y matrix transform (to extract the equivalent parallel lines), and Y-to-ABCD matrix transform (to find the equivalent transfer parameters) [14-15]. The output responses across different paths from the single input N_{in} to any output N_m (m={1,…,8}) were mathematically formulated via the voltage transfer functions:

$$H_m = V_m / V_{in}. \quad (1)$$

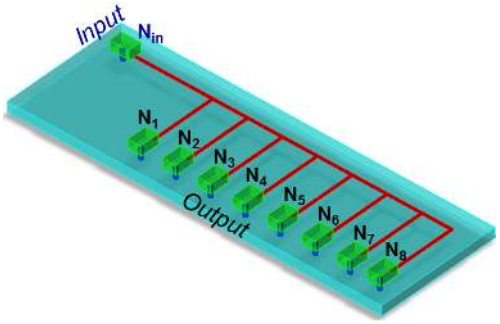

Figure 2. Example of 8:1 comb or asymmetrical interconnect tree.

That modeling method was applied to perfectly isolated asymmetrical tree structure. However, for systems using high density PCBs, the interconnections can be significantly localized and can create unintentional EM coupling or crosstalk effects [16-17]. This paper addresses that case, with modelling methodology enabling to predict crosstalk on asymmetrical tree. The model developed herein is the synergy of the tree topology presented in [13] and the coupling model in [18].

II. METHODOLOGY WITH CIRCUIT TRANSFORM

Throughout this paper, we will focus on asymmetrical 2:1 tree topology, similar to that proposed in [13], with single input and two-outputs. Then, a neighboring line is placed in the proximity of the tree network branches in order to investigate the coupling effect.

We shall assume that the transmission lines (TL) constituting the tree are characterized by their characteristic impedance Z_c, physical length d, phase constant γ, and electrical length :

$$\theta = \gamma \cdot d \ . \qquad (2)$$

A. Topology of Asymmetrical 2:1 Tree Interconnect Understudy

The building blocks of the theoretical presented SI process are fundamentally constituted by the implementation of the equivalent circuit theory. Fig. 3(a) represents the circuit configuration of the 2:1 asymmetrical tree. The single input with internal impedance Z_s is excited by v_{in}. The asymmetrical tree outputs are loaded by impedances Z_{L1} and Z_{L2}, and the branches are essentially comprised of pieces of input lines TL_0 (connected between nodes N_{in} and N_0) and output lines TL_1 (between N_0 and output node N_1) in parallel with output lines TL_{21} cascaded with TL_{22} (between N_0 and N_2).

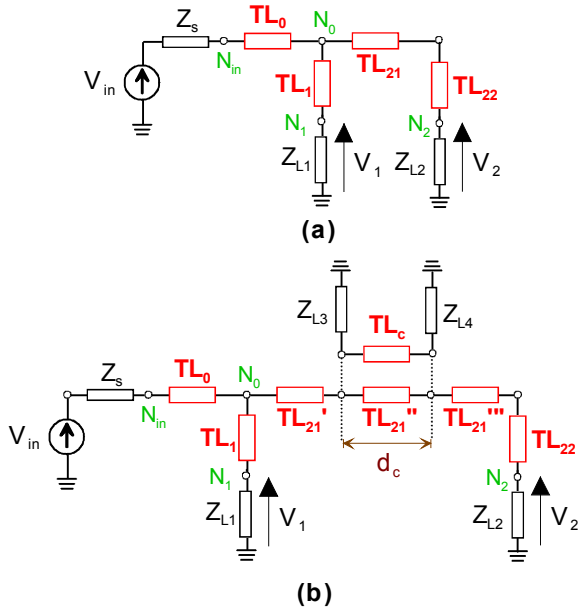

Figure 3. (a) 2:1 comb tree topology and (b) comb tree topology including coupling line TL_c.

We will compare this isolated circuit tree with the tree shown in Fig. 3(b) containing neighboring line TL_c placed in proximity of TL_{21}. We propose to replace TL_{21} by cascaded pieces of lines TL_{21}', TL_{21}'' and TL_{21}''', with the length of TL_{21}'' the same as TL_c here denoted as d_c. As described in [18], the overall coupled line impedance and admittance matrices are denoted:

$$[Z(\omega)] = [R(\omega)] + j\omega[L(\omega)], \qquad (3)$$

and

$$[Y(\omega)] = [G(\omega)] + j\omega[C(\omega)], \qquad (4)$$

respectively (j is the complex number $\sqrt{-1}$ and ω is the radian frequency). The even- and odd- mode impedances and electrical angles of coupled branches TL_{21}"-TL_c are denoted ($Z_e(\omega)$, $Z_o(\omega)$) and ($\theta_e(\omega) = \gamma_e(\omega) \cdot d_c$, $\theta_o(\omega) = \gamma_o(\omega) \cdot d_c$). The ABCD matrix $[T_{N2N0}]$ of equivalent to N_0N_2 is determined by the relation:

$$[T_{N_2N_0}] = [T(TL_{21}')] \cdot [T(TL_{21}'')] \cdot [T(TL_{21}''')] \cdot [T(TL_{22})], \qquad (5)$$

where the elementary line ABCD matrices are written as:

$$[T(TL_m)] = \begin{pmatrix} \cosh(\theta_m) & Z_{c_m} \cdot \sinh(\theta_m) \\ \sinh(\theta_m)/Z_{c_m} & \cosh(\theta_m) \end{pmatrix}_{m=21,22}, \qquad (6)$$

The ABCD matrix of the coupled lines (TL_{21}"-$TL_c \equiv TL_{21c}$) is analytically defined as:

$$[T(TL_{21c}'')] = \left[eig[Z \cdot Y] \cdot [T_x] \cdot eig[Z \cdot Y]^{-1} \right]_{k,l=\{1,2\}}, \qquad (7)$$

where the four elements of the matrix $[T_x]$ are:

$$\begin{cases} [T_x](1,1) = [T_x](2,2) = \begin{bmatrix} \cosh(\theta_e) & 0 \\ 0 & \cosh(\theta_o) \end{bmatrix} \\ [T_x](1,2) = \begin{bmatrix} Z_e \sinh(\theta_e) & 0 \\ 0 & Z_o \sinh(\theta_o) \end{bmatrix} \\ [T_x](2,1) = \begin{bmatrix} \sinh(\theta_e)/Z_e & 0 \\ 0 & \sinh(\theta_o)/Z_o \end{bmatrix} \end{cases} . \qquad (8)$$

Next, we shall apply SIMO/SISO transform for the transfer function extraction along electrical paths $N_{in}N_m$ (m={1,2}).

B. Asymmetrical Input-Output Path Equivalent SISO Circuit

Thanks to the TL and circuit theory, we establish the electrical circuit corresponding to path link from input N_{in} and each tree outputs $N_{1,2}$. After classical electrical transforms, we generate the SISO equivalent circuits of 2:1 tree shown in Figs. 4 and Figs. 5 for the electrical paths $N_{in}N_1$ and $N_{in}N_2$, respectively.

We can see that the reduced circuits have parallel impedances $Z_{in,m}$ (m=1,2) expressed with the classical relation between impedance- and ABCD-matrices. After inclusion of the parallel impedances with the coupling effects, the asymmetrical tree transfer functions as defined in (1) are mathematically established for m={1,2}:

$$H_m = \frac{1}{[T(TLN_m N_{in})](1,1)}. \qquad (9)$$

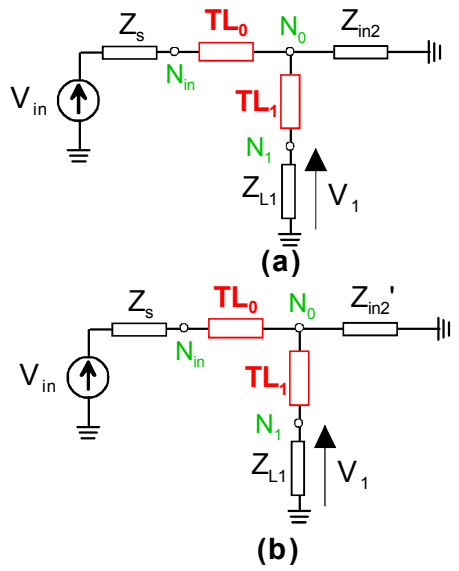

Figure 4. Equivalent SISO circuits for extracting the output V_1.

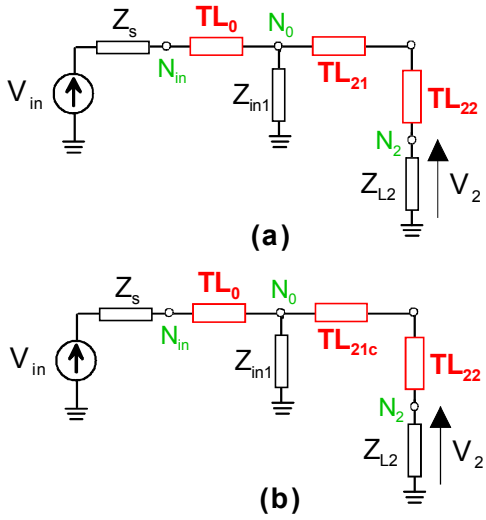

Figure 5. Equivalent SISO circuits for extracting the output V_2.

By combining all the previous analytical elements of each piece of line defined before, we have the associated ABCD matrix for each output branch written as:

$$[T(TL_{N_1N_{in}})] = \begin{bmatrix} 1 & Z_s \\ 1 & 0 \end{bmatrix} \cdot [T(TL_0)] \cdot \begin{bmatrix} 1 & 1 \\ 1/Z_{in2} & 0 \end{bmatrix} \cdot [T(TL_1)] \cdot \begin{bmatrix} 1 & 1 \\ 1/Z_{L_1} & 0 \end{bmatrix}. \qquad (10)$$

$$[T(TL_{N_2N_{in}})] = \begin{bmatrix} 1 & Z_s \\ 1 & 0 \end{bmatrix} \cdot [T(TL_0)] \cdot \begin{bmatrix} 1 & 1 \\ 1/Z_{in1} & 0 \end{bmatrix} \cdot [T(TL_{21}')] \cdot [T(TL_{21c}'')] \cdot [T(TL_{21}''')] \cdot \begin{bmatrix} 1 & 1 \\ 1/Z_{L_2} & 0 \end{bmatrix}. \qquad (11)$$

To check the validity of this behavioral model, examples of applications were considered and analyzed using numerical calculations with Matlab.

III. APPLICATIONS

A microstrip interconnect tree was considered as the numerical proof of concept of the model developed in the previous section. The frequency- and time-domain analyses were also performed for the circuit.

A. Substrate Permittivity Broadband Model

The model presented in this paper can be advantageously extended to structure including broadband frequency influences. As the test application, the interconnect tree circuit substrate was defined with Svesson-Djordjevic model proposed in [19-20], as shown below:

$$\varepsilon_{rf}(j\omega) = \varepsilon_r + a \cdot \ln\left[\frac{2\pi f_L + j\omega}{2\pi f_H + j\omega}\right], \qquad (12)$$

with

$$a = -j\varepsilon_r \tan(\delta) / \ln\left[\frac{f_L + jf_0}{f_H + jf_0}\right], \qquad (13)$$

$\varepsilon_r = 4$, $\tan(\delta) = 0.02$, frequency f_0 = 1.5GHz at which ε_r and $\tan(\delta)$ are specified, low roll-off frequency $f_L = 0.1$GHz and high roll-off frequency $f_H = 10$GHz.

B. Description of Asymmetrical Circuit for Numerical Test

We designed an arbitrary chosen physical lengths (width and lengths) 2:1 distribution tree network as an IL under test. The structure was intentionally folded in order to show the EM coupling between the interconnect branch lines. Then, lumped loads inspired from realistic PCBs were considered to find out the feasibility of the method with different load parameters.

Fig. 6 shows schematic layout illustrating the configuration of the 2:1 asymmetrical interconnect tree considered here as the application example. This structure is comprised of the microstrip interconnect tree driven by the numerical source v_{in} with internal impedance Z_s=25Ω and loaded by capacitors 10pF which form impedances Z_{L1} and Z_{L2}. The electrical paths $N_{in}N_1$ and $N_{in}N_2$ are set with physical lengths of 2.5mm and 9mm, respectively. The coupled perturbation line has physical length of 7.5mm and is loaded by Z_{L3}=25Ω and Z_{L4} corresponding to 10pF capacitor.

Investigation on the comparison between the responses of the 2:1 interconnect tree without and with the perturbation coupling line was performed by plotting the outputs (v_1,v_2) and (v_{c1},v_{c2}) respectively.

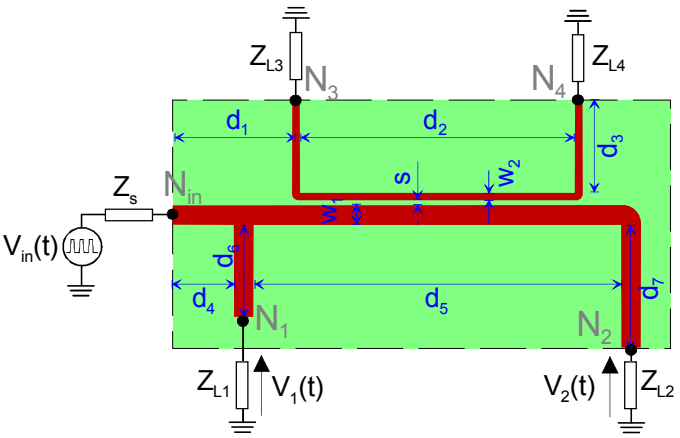

Figure 6. Layout schematic of 2:1 asymmetrical interconnect tree including the neighboring perturbation line considered for the numerical analyses: d_1=2mm, d_2=4.5mm, d_3=1.5mm, d_4=1mm, d_5=6mm, d_6=1.5mm, d_7=2mm, w_1=0.3mm, w_2=0.1mm and s=0.1mm.

C. *Frequency Analysis Results*

As aforementioned, the start point of the modelling was the extraction of the frequency dependent broadband *RLCG*(*f*) per unit lengths parameters of each branch of the tree. Then, by following the methodology suggested in Section II, the frequency dependent ABCD- and Z-matrices were calculated with Matlab. By using expressions (9), (10) and (11), we establish the transfer function corresponding to the electrical path $N_{in}N_{1,2}$ without the coupling line, represented by:

$$H_{1,2}(j\omega)=V_{1,2}(j\omega)/V_{in}(j\omega). \qquad (14)$$

Then, it is compared with that one with the coupling line defined as:

$$H_{c1,2}(j\omega)=V_{c1,2}(j\omega)/V_{in}(j\omega). \qquad (15)$$

Figs. 7 display the frequency responses (magnitudes labelled in left side and phases labelled in right side) corresponding to these expression applied to the structure understudy which is presented in Fig. 6. The response from the asymmetrical PCB tree without and with coupling effects are respectively plotted in solid and dashed lines. The classical behaviors of low pass structures are occurred for the both tree outputs. Moreover, a significant resonance effect occurs at about 0.61GHz along the path $N_{in}N_1$. This is due to the stub effect from the other branch of the tree. As we can see, due to the crosstalk between the coupled branches of the tree the coupled responses are influenced noticeably above 5GHz.

The introduced calculation results are performed very fast on a typical modern computer running Matlab and are of the order of about hundred milliseconds.

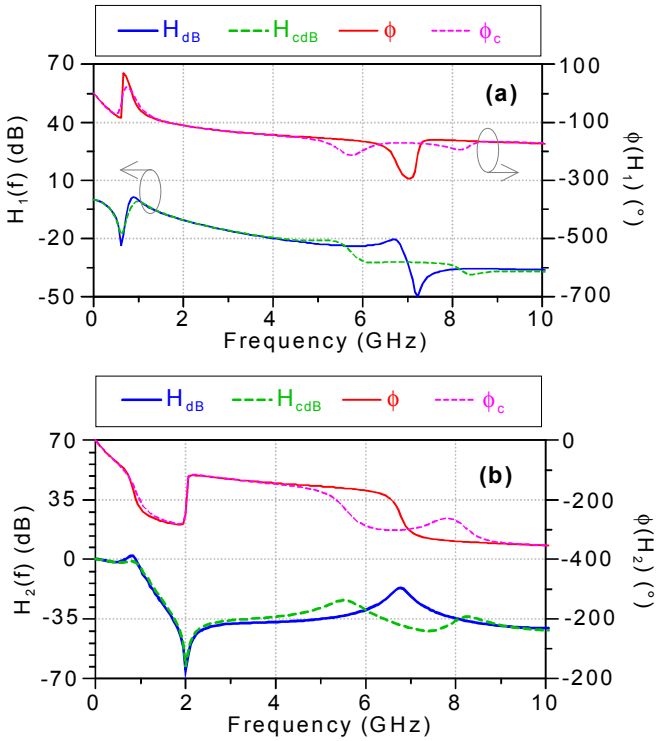

Figure 7. Frequency responses of the 2:1 asymmetrical tree presented in Fig. 6 without (solid lines) and with (dashed lines) coupling influences.

D. *Matrix Impedance Analyses*

The frequency analysis of the previous transfer functions can be additionally completed with further investigation the behavior of the asymmetrical tree network impedances $[Z]$. To do this, we realized the comparison between the transfer impedances Z_{N3Nin} and Z_{N4Nin} respectively corresponding to the electrical paths $N_{in}N_3$ and $N_{in}N_4$. Fig. 8 displays the obtained coupling impedances up to 10GHz.

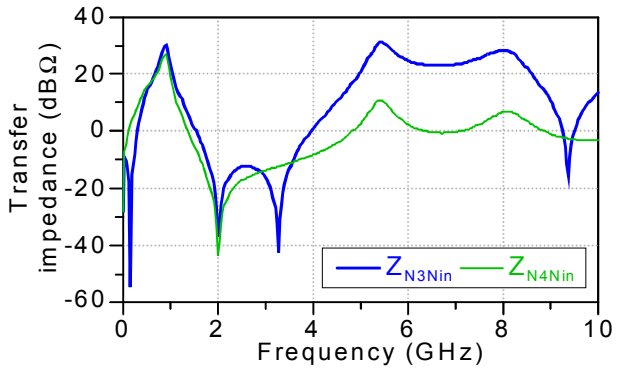

Figure 8. Magnitude of coupling impedances between the main input access N_{in} and the perturbation line N_3N_4.

It can be stated that Z_{N3Nin} presents in one hand transmission zero frequencies at about 0.17GHz, 3.27GHz and 9.37GHz. In the other hand, Z_{N4Nin} transmission zero frequency is occurred at about 2GHz. However, the coupling level is lowered at

about 0.90GHz, 5.43GHz and 8.06GHz for Z_{N3Nin}. These coupling impedances explain the degradation which can change the behavior of the signal propagating along the perturbed interconnect line. This finding can be pointed out with the reflection input access impedance Z_{NkNk} and transfer impedance Z_{NkNin} with the output index k={1,2}. The differences between the own impedances Z_{NkNk} (plotted in solid lines) and disturbed by coupling impedances Z_{cNkNk} (plotted in dashed lines) are highlighted by Figs. 9 and 10.

More illustrative insight on the EMC effect on the distributed SI through the tree understudy can be achieved with the time-domain analysis. This approach constitutes the main object of the next paragraph.

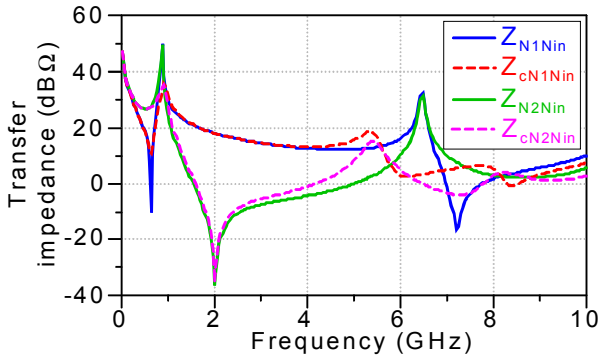

Figure 9. Magnitude of the transfer impedance of the structure under study without (solid lines) and with (dashed lines) coupling influences.

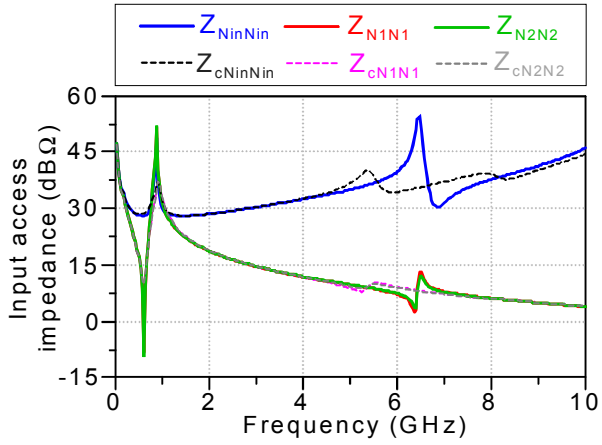

Figure 10. Magnitude of the input access impedances of the structure under study without (solid lines) and with (dashed lines) coupling influences.

E. Time-Domain Analysis Results

During the numerical test for this time-domain investigation, a high speed digital signal represented by eight bits input data "01001000" was assumed as input. The data bits signal was assumed to be trapezoidal with 0.5Gbps rate and 150ps rise and fall times.

The signal plots displayed in Figs. 11 presented the time-domain computed results with the asymmetrical tree understudy. The input signal is traced in solid bold blue line. Moreover, the asymmetrical tree outputs without and with the coupled perturbations are shown as solid red and dashed green lines, respectively.

The results highlight the influence of the parasitic coupling on the asymmetrical interconnect distribution tree. We can see that due to the asymmetrical behavior of the two input branches, the outputs are completely different from each other. It can be stressed that the data SI was significantly degraded with considerable distortion. Moreover, the propagation delays are of about 0.22ns for the electrical path $N_{in}N_1$ and 0.5ns for the path $N_{in}N_2$. A reflection effect is also observed on the path $N_{in}N_1$ which is related to the resonance effect, as seen in Fig. 7(a) introduced in the previous paragraph.

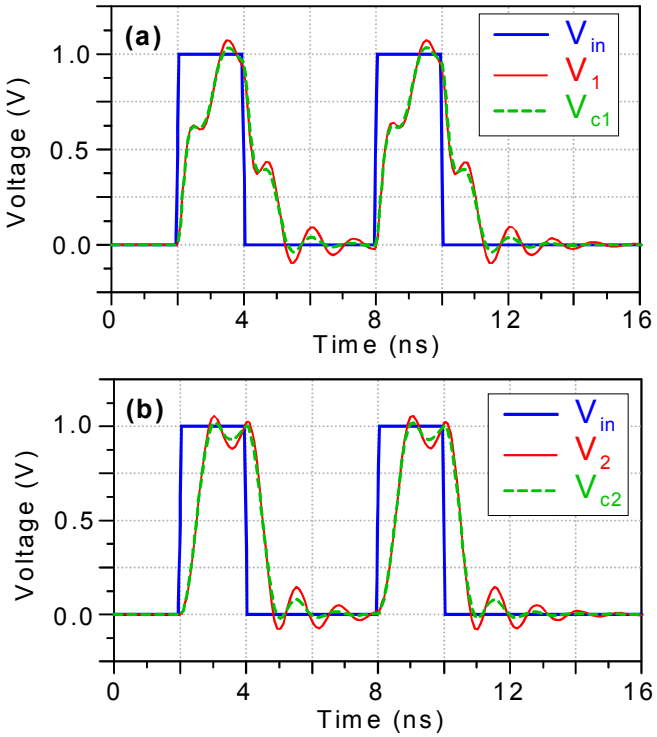

Figure 11. Eight bits data responses of the 2:1 asymmetrical tree presented in Fig. 6 without (solid lines) and with (dashed lines) coupling.

F. Discussion

The developed modelling method confirms the influence of EM coupling caused by the perturbation line on the asymmetrical tree network. The model offers the possibility to predict fastly the tree frequency responses by taking into account the dispersive effects on the substrate materials. Various techniques on analyses based on the transfer functions, matrix impedances and time-domain responses show the electrical behaviors of the 2:1 tree. For the effectiveness analysis, the model was implemented into Matlab. In conclusion, for the considered here example:

- The output signal shapes are quite well preserved because the bandwidth of the input data is lower than 6GHz.
- The time-delay between the two responses is lower than 200ps.
- The slight variation of the output transient voltage amplitudes of about 10% were found when placing the coupling perturbation at 100µm of the tree.

IV. CONCLUDING REMARKS

The investigation was performed of the high speed SI of an asymmetrical 2:1 tree distribution network perturbed by a coupled length of a transmission line. Analytical behavioral model of the network was developed using ABCD, Z and Y matrices. The model can include the broadband dispersion effect of relative permittivity as proposed by Svesson-Djordjevic in [19-20]. The model was implemented in Matlab programming language and is computationally very efficient.

The proposed model was verified on the example of a microstrip asymmetrical tree with parasitic coupled line operating at a high data rate of 0.5 Gbps. Both frequency- and time-domain analyses were performed. It was found that the signal integrity of the asymmetrical microstrip tree with parasitic coupling degraded significantly under the test conditions.

The proposed model is beneficial in terms of flexibility, simplicity and computational speed. It can be useful for the design and manufacture engineers for assessing the degradation of sharing high-speed signals in asymmetric tree. Application areas include miniaturized microelectronic interconnect systems and packaging structures. The prediction of the high density interconnect effects will allow to optimize the packaging structures and also probably to establish a post processing technique for the signal degradation compensation.

ACKNOWLEDGMENT

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