

Asynchronous Counter in QCA Technology Using Novel D Flip-Flop

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Research Article

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Abstract

A strong need for high-speed and low-power consumption devices seems inevitable due to the high speed of technological advancement in the field of microelectronics. Designers are highly interested in designing and making nanoscale devices. The Quantum Cellular Automaton (QCA) is known as one of these technologies, which makes it feasible to implement digital circuits with a high operating speed. In this paper a 4-bits counter, a 3-bits bidirectional counter, a 4-bits counter with a reset terminal, and a 4-bit counter with both set and reset terminals are designed using the proposed D-latch to demonstrate that these circuits function accurately in more complex circuits. According to the results, the area was respectively reduced by 8.33% and 15.38% with a 4.76% reduction in the delay rate in the proposed 4-bits counter and 3-bits bidirectional counter compared to the best previous designs. All the designs and simulation results is being done in the QCAPro and QCADesigner software.

1. Introduction

The scientists have been looking for new methods given the trend toward nanotechnology and the need for higher speeds in small dimensions as well as the development of integration in the VLSI technology aimed at solving the problems in the VLSI such as large area, high power consumption, low speed, and issues related to electric currents [1]. The QCA technology, designed and implemented on a nanoscale, has the potential to resolve all the described shortcomings [2]. Hence, the QCA with such unique characteristics appears as a huge development in the field of computer science and the logic circuit. The elimination of electric current and the capacitor element in the circuit has enhanced the popularity of QCA as well, which considerably reduces power consumption and simplifies the design process [3].

Counters are digital circuits that generate binary numbers or binary-coded decimals (BCDs) with specific patterns at certain time intervals [4]. Counters have many applications in electronic and digital systems such as digital clocks, analog-to-digital converters, frequency dividers, nanotechnologies, industrial robots, etc. [5]. Some designs have been introduced for counters in the QCA technology in the past, each with certain advantages and disadvantages. For example, a 4-bit counter based on a D flip-flop has been proposed in [6], which has a relatively large number of cells, a high occupied area, and high energy consumption despite operating properly. Also, a counter based on a T flip-flop was suggested in [7], which halved the delay besides reducing the number of cells dramatically; however, it has many cells and a large area. Also, a 3-bits bi-directional counter based on T flip-flop was proposed in [8], which had a relatively large area and delay besides having many cells. Therefore, in this article, a 4-bits counter, a 3-bits bidirectional counter, a 4-bits counter with reset ability, and a 4-bit counter with set/reset abilities with the minimum cells number, delay, occupied area, and energy consumption were provided using the proposed D latch and flip-flop structure.

The contents were presented in this article as follows. The second section is focused on the basic concepts and how to make quantum cells in the QCA technology followed by examining the clocking performance in this technology. The third section includes the proposed 4-bits counter circuits, the proposed bidirectional counter, and the proposed 4-bits counter with reset and set/reset capabilities followed by the results of the simulations, which indicate the accuracy of the designed circuits. The fourth section also focuses on the energy analysis.

2. Basics Of Qca

The use of the QCA technology for implementing digital logic circuits is one of the approaches that reduce the power consumption besides decreasing the size of logic circuits and increasing the clock frequency [9]. There is no current

between cells in this technology, and the connection between cells is created by moving the position of electrons inside the cell and the impact of the field of each cell on the adjacent cell [10]. The QCA cell is the basic unit of QCA, each QCA cell is formed of four quantum cavities. There are two free electrons inside each cell that can move freely by tunneling between the cavities [11]. These electrons always occur in a position with the highest distance from each other due to the repulsive force between them. Therefore, there are stable states where the holes (cavities) are occupied diagonally [12]. This issue is illustrated in Fig. 1.

Different types of digital circuits and QCA-based gates can be made by using these cells, including majority gates [13]. The majority gate is recognized as one of the most important and major gates in the QCA logic, which acts as a basis of design in many more complicated circuits in the QCA [14]. This gate has some inputs and one output, and the polarity of the output cell is determined according to the polarity of the majority of inputs. Thus, if the majority of the inputs have a polarity of -1, the polarity of the output cell would become -1. Similarly, if most of the inputs have a polarity of +1, the polarity of the output cell would be +1 [15]. This is shown in Figure (2a). Also, two important and basic gates, i.e., "AND" and "OR" can be made by using the majority gate. Thus, if the polarity of one of the inputs is set given as a constant, for example, if $P = -1$, an AND gate is made, and if the polarity of one of the inputs is given as $P = +1$, an OR gate will be made [16]. The inverter gate is another basic gate used in the QCA circuits, which is obtained by placing the cells diagonally above or below the desired cell; it is shown in Figure (2b). This type of gate is called a simple inverter or uncontrolled NOT gate [17]. This gate has a little noise in the output. Another inverting gate was developed to resolve this problem, which is called a controlled inverter gate. The structure of this gate consists of two simple inverters as shown in figure (C2) [18]. The QCA cells can also be used to make wires. Thus, a wire is formed by placing the base cells next to each other.

The clock in QCA circuits is like an electronic factor compared to traditional circuits, which controls the movement of electrons inside the cell so that each cell can maintain its current state and not react to the change of states of its adjacent cells [19]. The clock is used in the QCA for controlling, the synchronization of parts of the circuit, and also amplifying the signal. Each clock signal includes 4 phases: Rising edge (Switch), high level (Hold), falling edge (Release), and low level (Relax). Its mechanism is clearly shown in Fig. 3 [20].

3. The Design Of The Proposed Counter And Bi-directional Counter (Up And Down Counter) In The Qca Technology

This section was focused on the implementation of the proposed counter and bi-directional counter circuits followed by describing their principles and mechanisms.

3.1. Proposed 4-bits counter

The main block of the proposed 4-bits counter circuit is the D-latch. To design the proposed circuit in this paper, the proposed D flip-flop suitable in terms of the number of cells, delay, occupied area, and energy consumption is first designed. Then, the counter circuit is designed with the minimum number of cells and delay using this flip-flop.

Latches and flip-flops are known as major and significant topics in the design of circuits, which have drawn attention in the QCA technology [21]. The D-latch is one of these, which is widely used in design of counters. Based on its mechanism, if the clock input is equal to one and the D input value is equal to zero, the circuit output would become zero, and if the clock input is equal to one and the input value of D is also equal to one, the output of the circuit would become one. Also, when the clock input value is equal to zero, whether the D input value is zero or one, the circuit output keeps the same state as before [22].

A 4-bits counter is designed in this paper based on proposed D-latch in the QCA technology. This counter is a 4-bits asynchronous counter, and the maximum countable number in this counter ranges from 0 (0000) to 15 (1111). Figure 4 shows the block diagram of the proposed 4-bits counter.

Figure 5 shows the proposed 4-bit counter structure in the QCA technology, which contains 207 cells, an area of $0.22 \mu m^2$, and 4 cycles of the clock delay. This proposed structure has been designed with four falling edges D flip-flops according to the pattern shown in Fig. 4.

The proposed circuits were simulated using the QCADesigner in the Coherence Vector engine mode and these simulations demonstrate the accurate operation of the circuit. Table-1 shows the design parameters in QCADesigner.

Table-1 Coherence vector parameters

Parameter	Value
Cell size	18*18 nm ²
Dot diameter	5 nm
Centre-to-centre distance	20 nm
Temperature	1.000000 K
Relaxation time	1.000000e-015 s
Time Step	1.000000e-016 s
Total Simulation Time	7.000000e-011 s
Clock High	9.800000e-022 J
Clock Low	3.800000e-023 J
Clock Shift	0.000000e+000
Clock Amplitude Factor	2.000000
Radius of Effect	80.000000 nm
Relative Permittivity	12.900000
Layer Separation	11.500000 nm

Figure 6 shows the simulation result of the proposed 4-bits counter in the QCA technology, and it should be noted that the circuit accurately counts the values from 0 to 15. Moreover, the counting started from the number 15 according to the initial values of the output of the flip-flops.

In the rest of this article, the designed D flip-flop circuits were used in the bidirectional counter circuits to demonstrate that they also operate accurately in more complex circuits.

The bidirectional counters have the feature to count both down and up for any given sequence. They can also reverse the counting at any point in the counting sequence and do this by using an additional control input [8].

The main blocks of the proposed bidirectional counter circuit are D flip-flop and multiplexer. Multiplexers are one of the basic, major, and substantial circuits in the design of circuits, which have been considered in the QCA technology [23]. In this paper, the proposed multiplexer suitable in terms of the number of cells, the occupied area, and power was designed to design the proposed circuit. Then, the proposed bidirectional counter circuit was designed with the minimum number of cells and minimum delay using it.

Proposed bidirectional counter is a 3-bits asynchronous up/down counter, which is designed using the D flip-flops and 2:1 multiplexer. The maximum number that can be counted in this counter ranges from zero to seven when the high count selector is active, and when the down count selector is activated, the counting starts from seven and returns to zero. Therefore, the counting string in this counter is as 0, 1, 2, 3, 4, 5, 6, 7 in the up count mode and as 7, 6, 5, 4, 3, 2, 1, 0 in the down count mode. Figure 7 illustrates the proposed block diagram of a bidirectional counter.

In this design, to enable the proposed bidirectional counter block diagram to count the numbers accurately and to make it possible to reverse the count at any point in the counting sequence after the counting, the circuit block diagram was designed as follows: When the circuit is asynchronous and the clock is sensitive to the falling edge, the Q output must go to the next clock input to enable the circuit to count up, and when the circuit wants to count down, the output of \bar{Q} must go to the next clock input. Having said that, the circuit was designed as such to place a multiplexer between each bits of the circuit, and the input of each multiplexer from Q and \bar{Q} was taken from the D flip-flop and the output of the multiplexer was given to the next clock. The circuit mechanism is as such that, when the selectors are zero, the up-counting circuit is activated, and when the selectors are 1, the down-count circuit is activated. With this logic block diagram, when the zero selector is activated, this circuit starts counting from zero and counts up to 7, and at any point of time that the selector is changed from zero to one, the counting is changed from up count to down count.

Figure 8 illustrates the proposed bidirectional 3-bits counter structure in the QCA technology, which contains 214 cells, an area of $0.22 \mu m^2$, and 5 cycles of the clock delay. This proposed structure consists of three falling D flip-flops and two 2:1 multiplexers, which are designed according to the pattern in Fig. 7.

Figure 9 shows the simulation result of the proposed bidirectional counter in the QCA technology and it works as follows: When the first and second selectors are zero, the up count circuit is activated and starts counting from 0 to 7, and whenever the first and second selectors become 1, the down-count circuit is activated and starts counting from 7 to 0. In this simulation result, when the first and second selectors are zero and according to the initial conditions given to the circuit, the circuit starts counting up from 4 and when the selectors get one, the circuit automatically starts counting backward at any point of the counting reaches. Figure 9 indicates the accuracy of the circuit operation.

To add more abilities in the design of counters, the reset ability and set/reset abilities are added to the designed D flip-flop circuit to demonstrate the better performance of these flip-flops besides their application in the counter circuits.

Figure 10 illustrates the block diagram of the proposed 4-bits counter with a reset terminal which is designed with a D flip-flop. In this design, to enable the proposed counter block diagram to count numbers accurately and to enable the circuit to perform the reset operation correctly and start counting from zero again, as requested, the block diagram of the circuit was designed in such a way that the outputs of the flip-flops go to the clock of the next flip-flop. It should be noted that the reset pin of the proposed counter is zero activated, and all the reset terminals of D flip-flops are

connected to have only one reset input in the counter. With this logic block diagram, this circuit starts counting from zero and counts up to 15, and the output becomes zero at any point in time when the reset base is activated.

Figure 11 illustrates the structure of a 4-bits counter with a reset base in the QCA technology, which contains 395 cells, an area of $0.30 \mu m^2$, and 7.5 cycles of the clock delay. This proposed structure consists of four D flip-flops with a reset base, which is designed according to the pattern in Fig. 10.

Figure 12 shows the simulation results of the proposed counter with a reset base in the QCA technology. It should be noted that the circuit accurately counts the values, and when the reset base is activated, the circuit performs the reset action at any point of the counting process.

Figure 13 shows the block diagram of the proposed 4-bits counter with the set/reset terminals. In this design, to enable the proposed counter block diagram to count numbers accurately and to enable the circuit to perform the set/reset operation correctly and start counting again whenever requested, the block diagram of the circuit was designed in such a way that the outputs of the flip-flops go to the clock of the next flip-flop, and since the set/reset are high activated, and at any point of time, if the set terminal is activated, the output of the circuit gets the value of '1' and when the reset terminal is activated, the output of the circuit gets the value of '0', and when both the set and reset terminals are activated simultaneously, the reset terminal is preferred.

Figure 14 illustrates the structure of the 4-bits counter with the set/reset terminals in the QCA technology, which contains 447 cells, an area of $0.38 \mu m^2$, and 7.5 cycles of clock delay. This proposed structure consists of four D flip-flops with a set-reset base, which is designed according to the pattern in Fig. 13.

Figure 15 shows the simulation result of the proposed 4-bits counter with the set-reset base in the QCA technology. It should be noted that the circuit counts the values accurately and when the circuit reset is activated, the output would be zero whatever the input value is, and when the circuit set input is activated, the output would be a logical one whatever the input value is.

Table-2 also shows the comparison of the design of the proposed counters with other similar designs. As revealed, a 4-bits counter with reset capability and set-reset abilities have been designed for the first time. This feature has not existed in the previous articles. Besides having the capabilities of reset and set/reset, these proposed structures have more suitable conditions than the previous designs concerning performance as well as the amount of delay, the occupied area, and power consumption. This has been clearly shown in Table-2 as well.

Table-2 Comparison of proposed counters with previous related designs in QCA technology

References	Bit	Cell count (# Cells)	Area (μm^2)	Cell/bit (# Cells)	Area/bit (μm^2)	Latency ($10^{-12} s$)	Set input	Reset input	Circuit type	Latch type
[24]	3	428	0.48	143	0.16	2	NO	NO	Asynchronous	J-K
[25]	3	287	0.33	96	0.11	2	NO	NO	Asynchronous	J-K
[6]	3	174	0.20	58	0.066	3	NO	NO	Asynchronous	D
[7]	3	140	0.16	47	0.053	2	NO	NO	Synchronous	T
Proposed counter	3	143	0.13	48	0.043	3	NO	NO	Asynchronous	D
[8]	3	204	0.26	68	0.086	5.25	NO	NO	Asynchronous	T
Proposed up down counter(Fig. 8)	3	214	0.22	71	0.073	5	NO	NO	Asynchronous	D
[6]	4	258	0.25	65	0.062	4	NO	NO	Asynchronous	D
[7]	4	196	0.24	49	0.060	2	NO	NO	Synchronous	T
Proposed counter (Fig. 5)	4	207	0.22	51	0.055	4	NO	NO	Asynchronous	D
Proposed counter with Reset(Fig. 11)	4	395	0.30	99	0.075	7.5	NO	YES	Asynchronous	D
Proposed counter with Set Reset(Fig. 14)	4	447	0.38	111	0.095	7.5	YES	YES	Asynchronous	D

Also, based on the comparison findings regarding the counter circuit in Table-2, all the design rules, including the observance of the minimum cell, have been fully observed in all the proposed circuits; however, these rules have not been observed in some of the previous designs, and the numbers obtained in the previous papers have been achieved without adhering to the minimum cell design rules.

4. Energy Consumption Simulations

The circuits built by using the QCA technology have highly remarkable differences concerning the area and power consumption compared to the circuits made by the CMOS technology. This suggests the QCA circuits occupy a much smaller area, and their consumption energy is so much lower than the CMOS circuits [26]. Thus, calculating the energy loss becomes highly important so that a power estimation software, known as QCAPro, has been designed in the QCA to evaluate the power consumption rate [27]. The energy losses of all the proposed designs were assessed

by considering three different levels of tunneling ($0.5E_K$, $1 E_K$, and $1.5 E_K$) at the temperature $T = 2k$. All the equations related to the procedure of calculating energy levels are also given in the Reference [28] and abbreviated in Table-3.

Figures 16, 17, 18 and 19 respectively show the energy consumption rate of the proposed structure of the counter, bidirectional counter, counter with Reset and the counter with Set Reset at the $0.5E_K$ level.

Table-3 Results of average leakage energy dissipation and average switching energy dissipation

Circuit	Average Leakage energy dissipation (meV)			Average Switching energy dissipation (meV)		
	$0.5E_K$	$1.0E_K$	$1.5E_K$	$0.5E_K$	$1.0E_K$	$1.5E_K$
Proposed Multiplexer	2.89	7.72	13.03	8.30	6.96	5.85
Proposed D-Latch	4.92	13.82	22.87	10.77	8.93	6.45
Proposed D-Latch with Reset	7.25	18.64	30.83	12.31	10.10	8.34
Proposed D-Latch with Set and Reset	7.81	20.66	34.46	15.56	12.76	10.54
Proposed counter (Fig. 5)	64.78	180.90	309.05	206.11	169.89	139.92
Proposed up down counter(Fig. 8)	65.75	186.57	321.66	230.48	192.87	160.51
Proposed counter with Reset(Fig. 11)	112.19	318.48	549.29	114.88	95.35	78.75
Proposed counter with Set Reset(Fig. 14)	121.82	343.02	591.27	141.95	121.14	99.22

Conclusion

This paper was focused on the basic concepts in quantum cells and provided some designs of multiplexers, D flip-flops, D flip-flops with reset base, and D flip-flops with set-reset base, as well as some designs of counters, bidirectional counters, resettable counters, and counters with set/reset features. Then, the structure and simulated results of the circuits were provided, which indicated the accurate operation of the circuits. All the design rules were observed in the presented designs. Moreover, the designs were compared with each other based on the number of cells, delay, the area used, and power consumption. Finally, the best design was introduced.

Declarations

Ethics approval and consent to participate: Not applicable.

Consent for publication: Not applicable.

Availability of data and materials: Not applicable.

Competing interests: Not applicable.

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Authors' contributions

Zaman Amirzadeh: Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Resources, Writing - Original Draft, Visualization.

Mohammad Gholami: Conceptualization, Methodology, Investigation, Resources, Writing - Review & Editing, Supervision

Acknowledgements: Not applicable.

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Figures

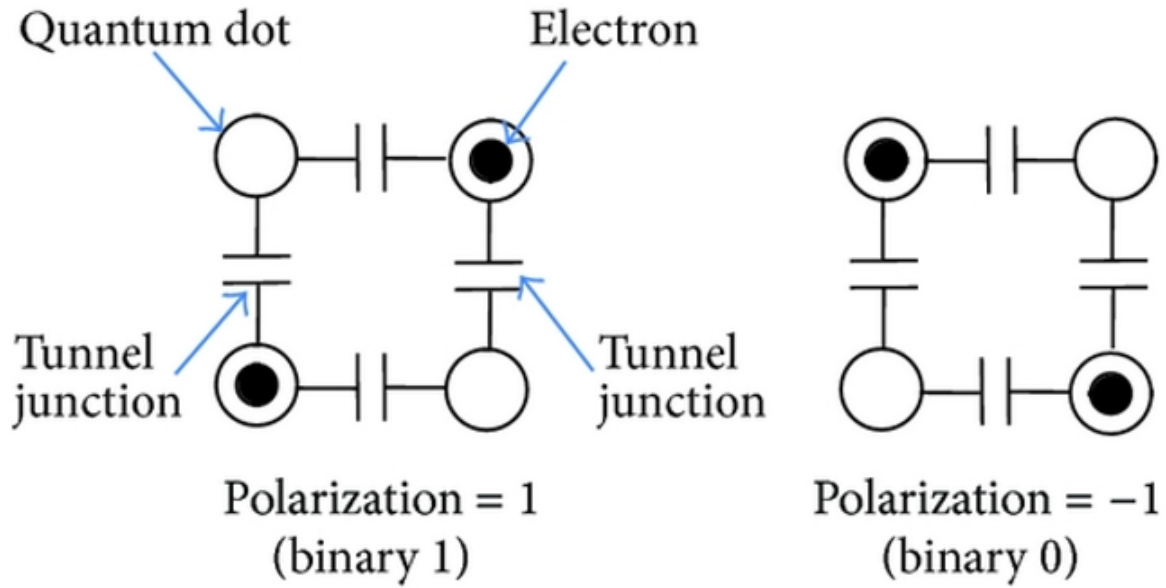


Figure 1

The general shape of the quantum cell and the concept of polarization in QCA

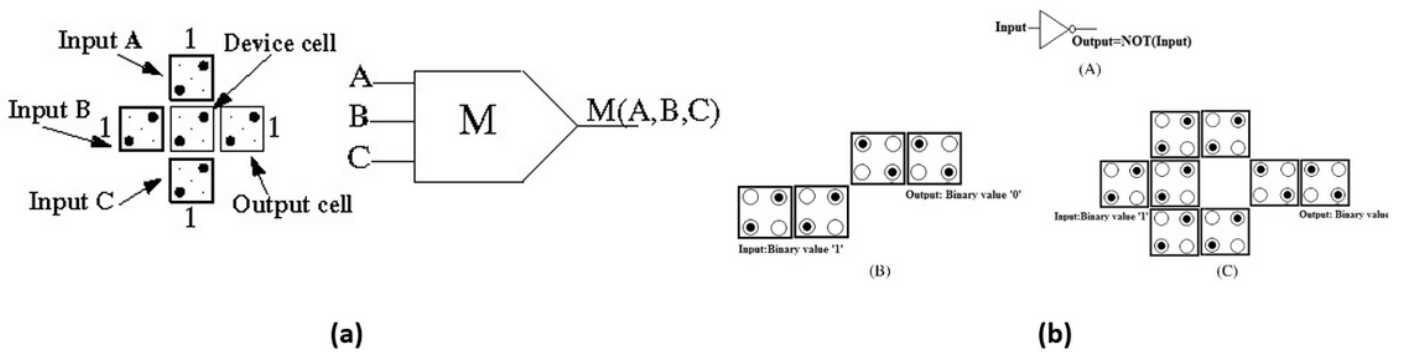


Figure 2

a) Majority gate in QCA, b) Inverter gate in QCA

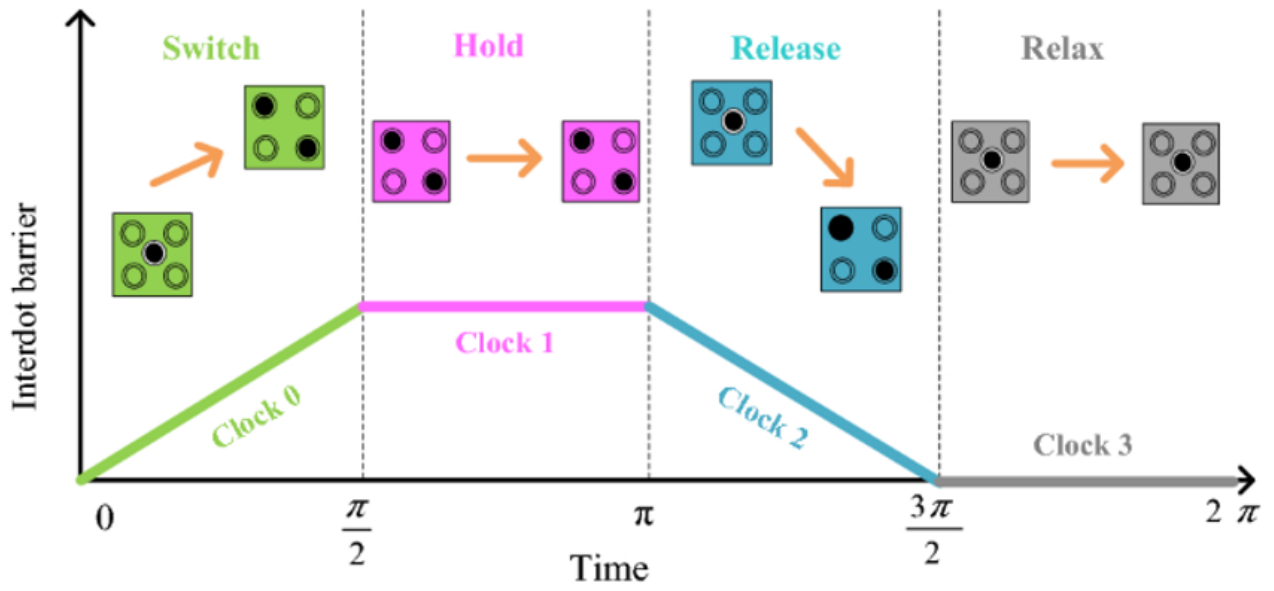


Figure 3

Clock zones in QCA circuit

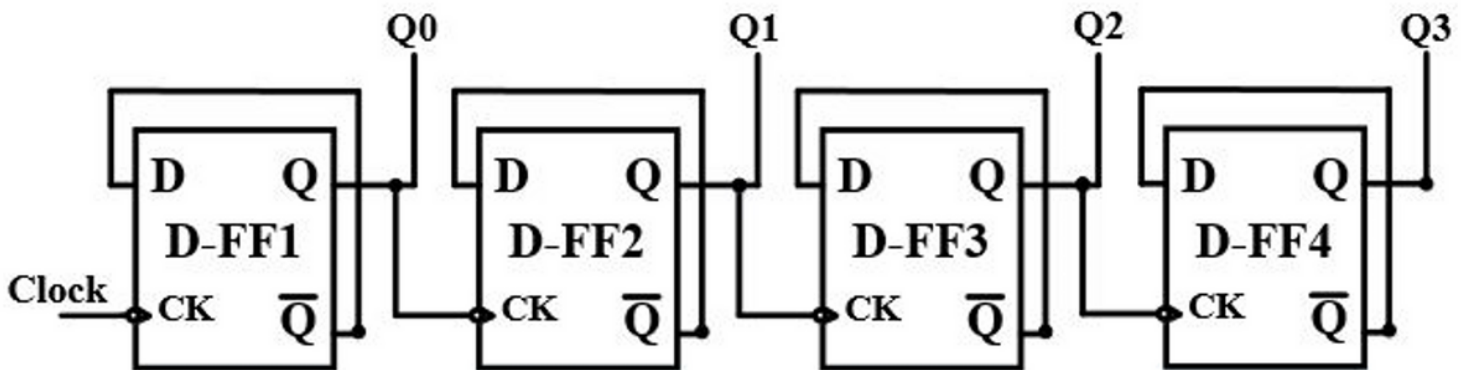


Figure 4

Logical diagram of proposed 4-bits counter.

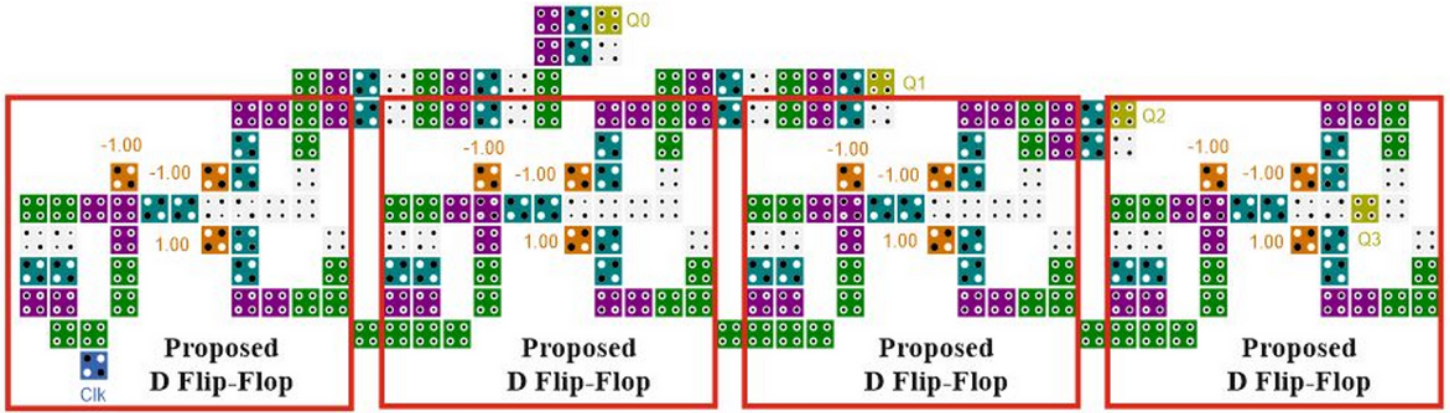


Figure 5

Layout of proposed 4-bits counter in QCA.

Simulation Results

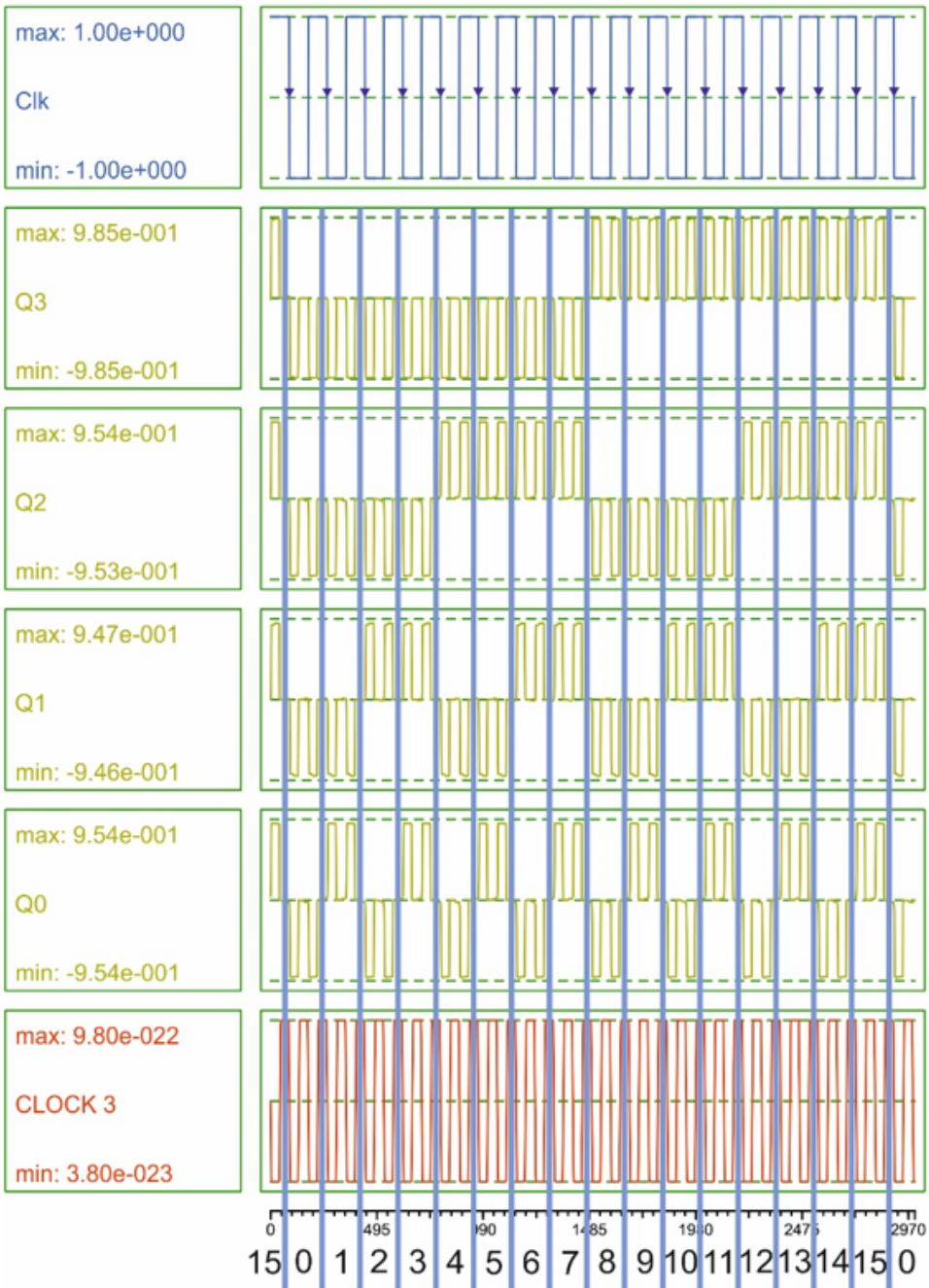


Figure 6

Output waveforms of proposed 4-bits counter in QCA nanotechnology.

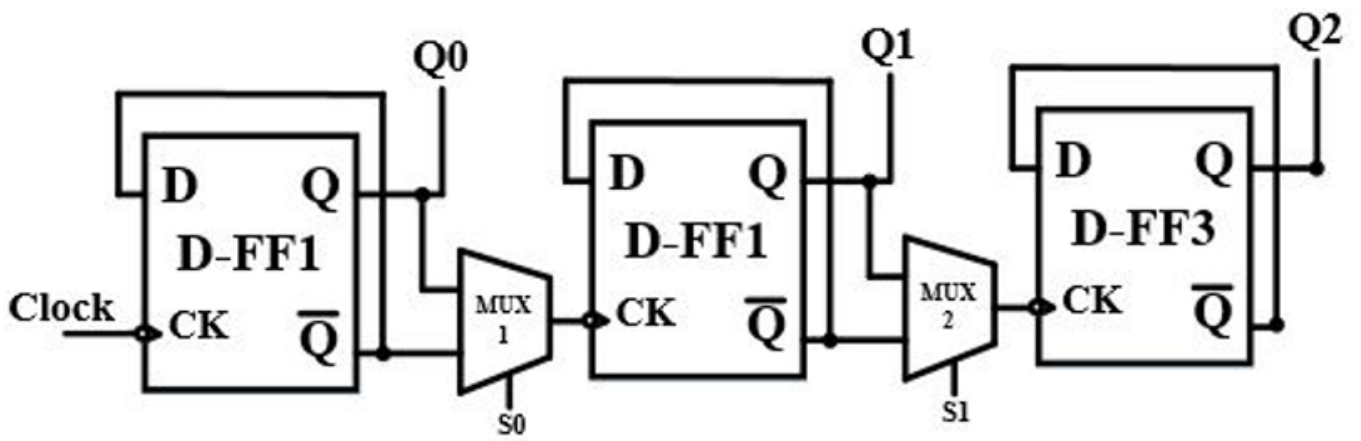


Figure 7

Logical diagram of proposed 3-bits bidirectional counter

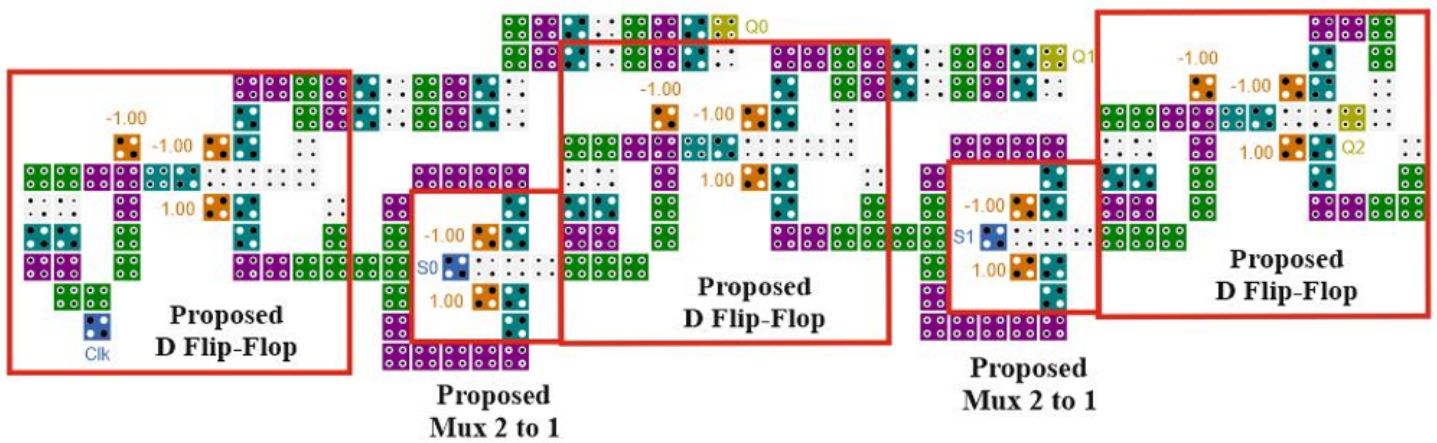


Figure 8

Layout of proposed bidirectional counter in QCA.

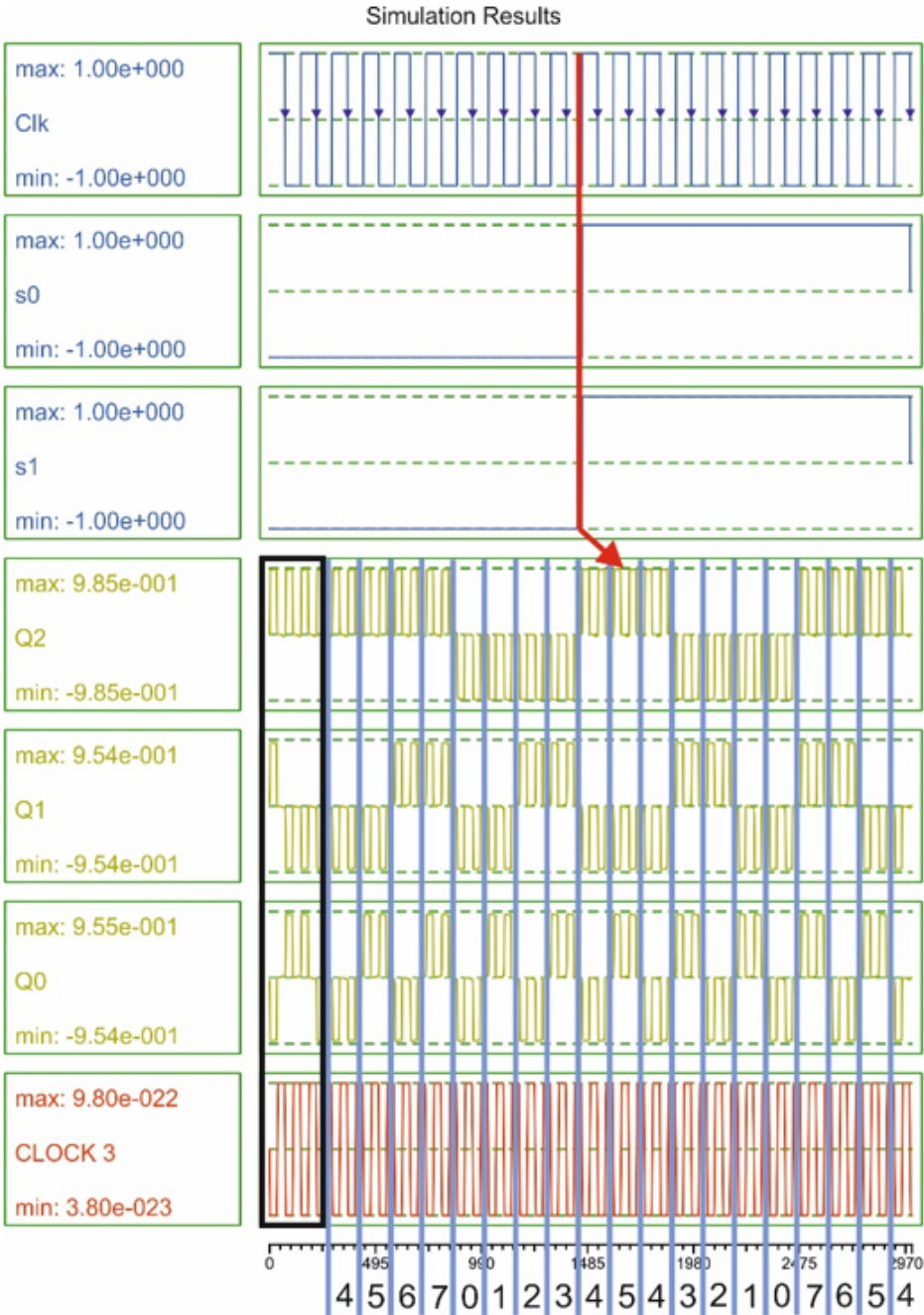


Figure 9

Output waveforms of proposed bidirectional counter in QCA nanotechnology.

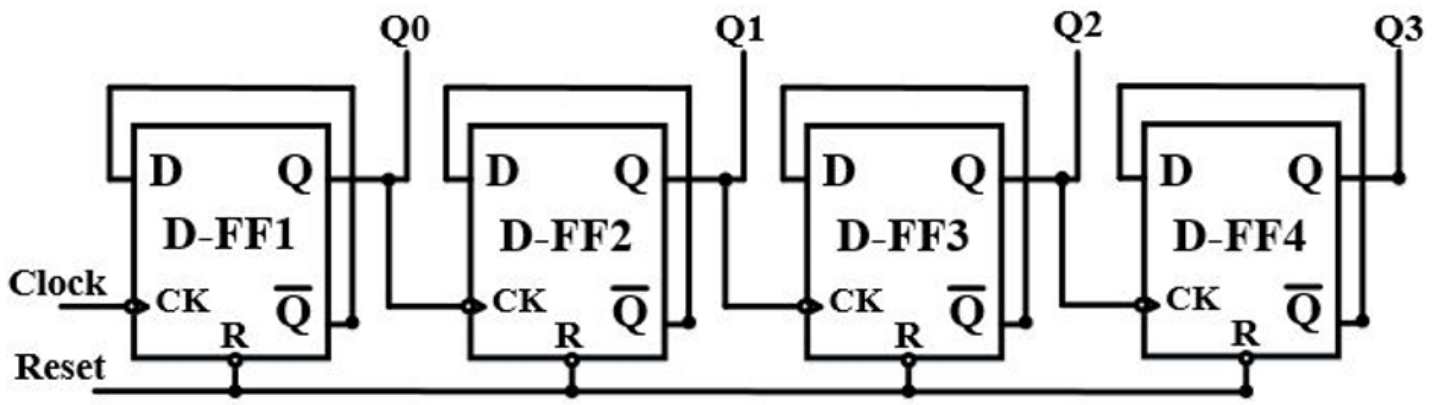


Figure 10

Logical diagram of proposed 4-bits counter with reset ability.

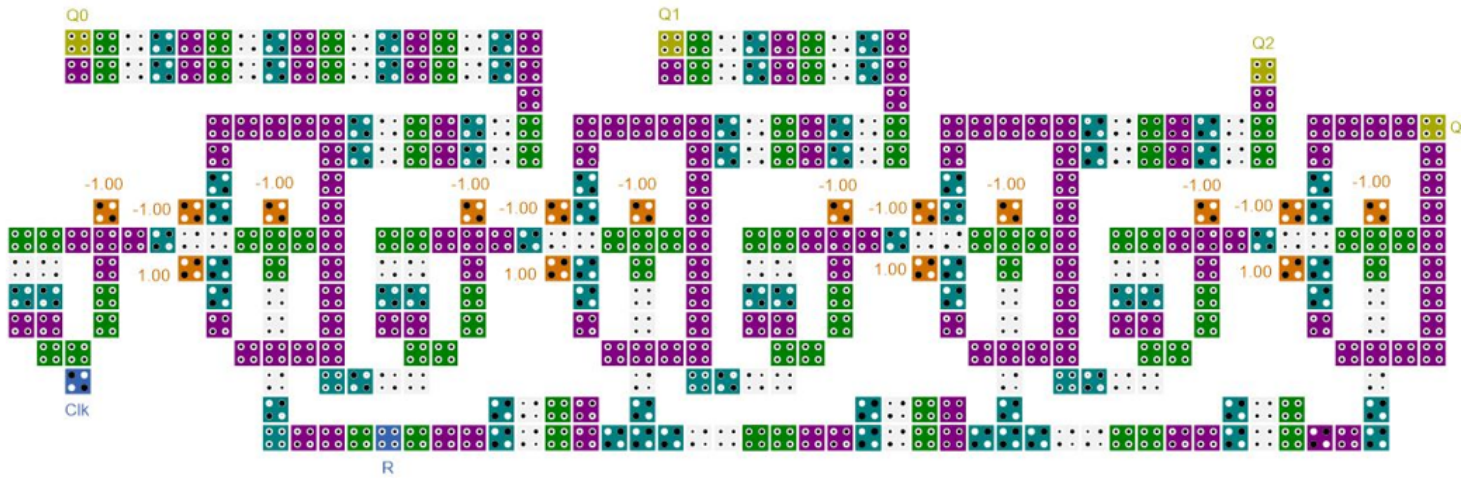


Figure 11

Layout of proposed 4-bits counter with reset ability in QCA.

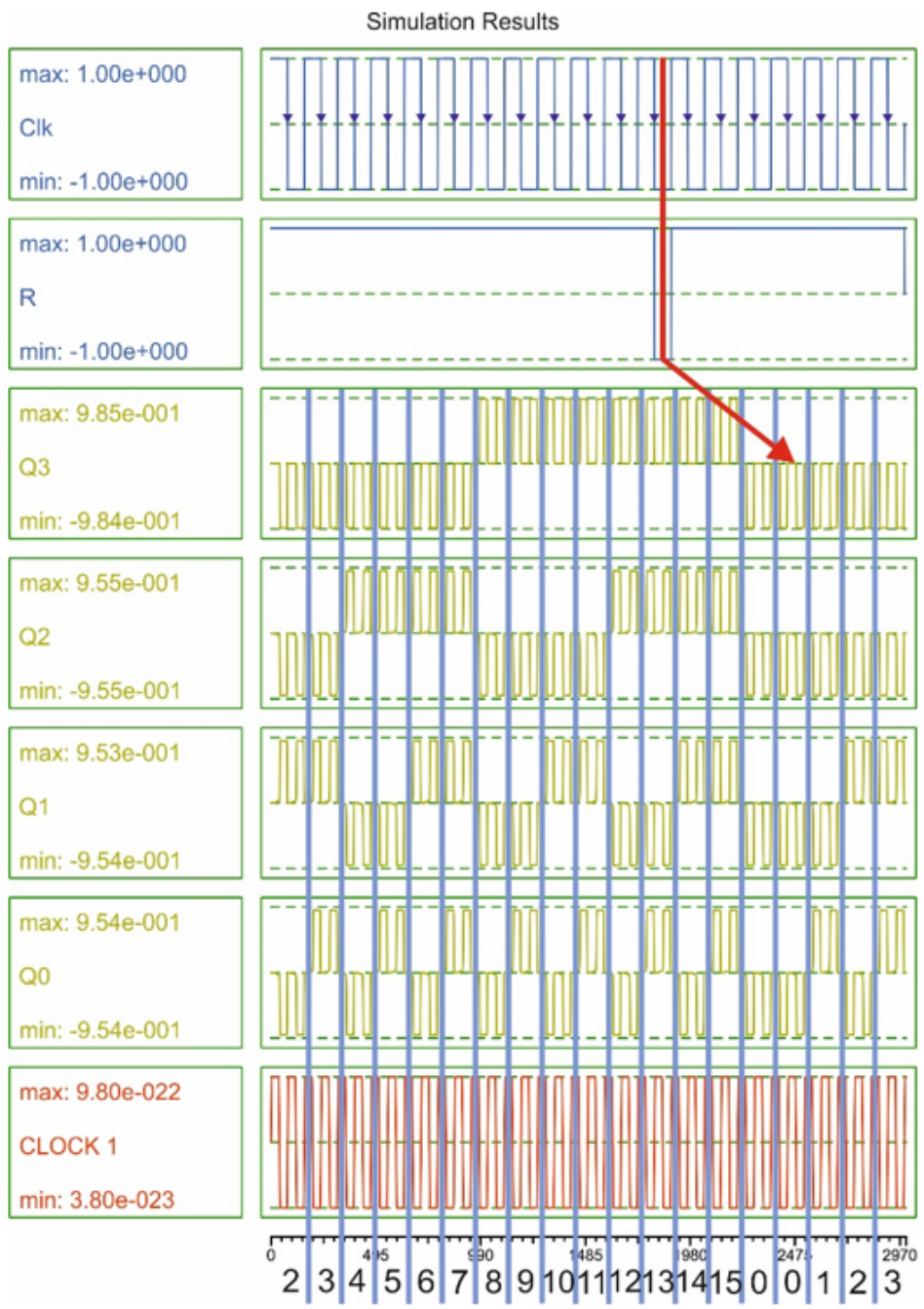


Figure 12

Output waveforms of proposed 4-bits counter with reset ability in QCA nanotechnology.

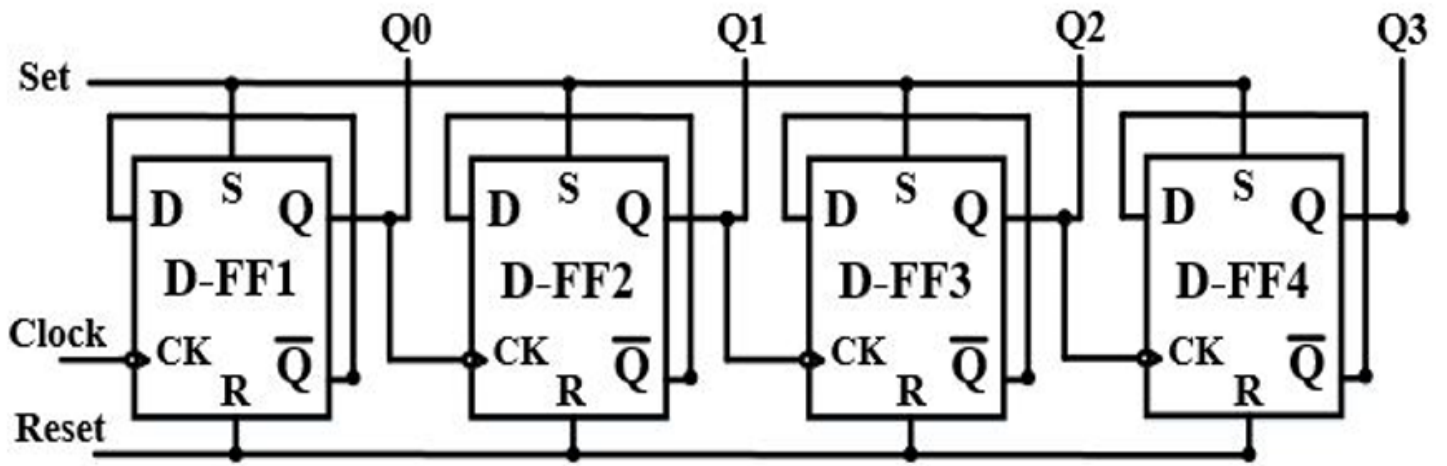


Figure 13

Logical diagram of proposed 4-bits counter with set and reset abilities.

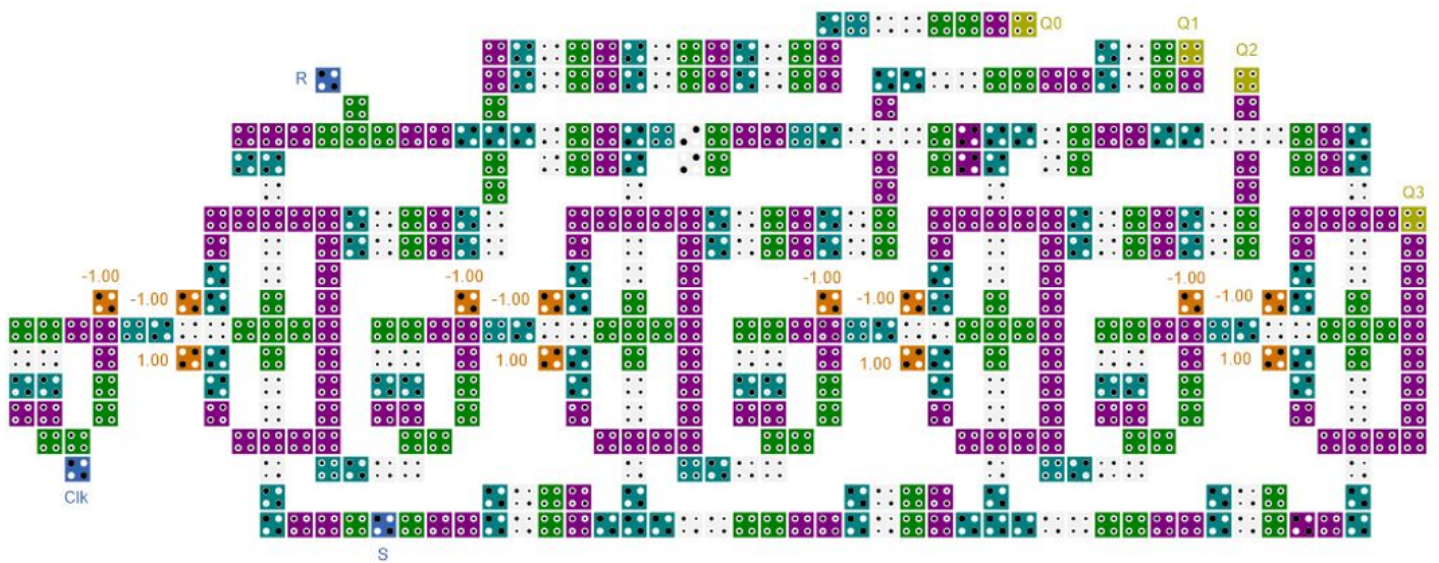


Figure 14

Layout of proposed 4-bits counter with set and reset abilities in QCA.

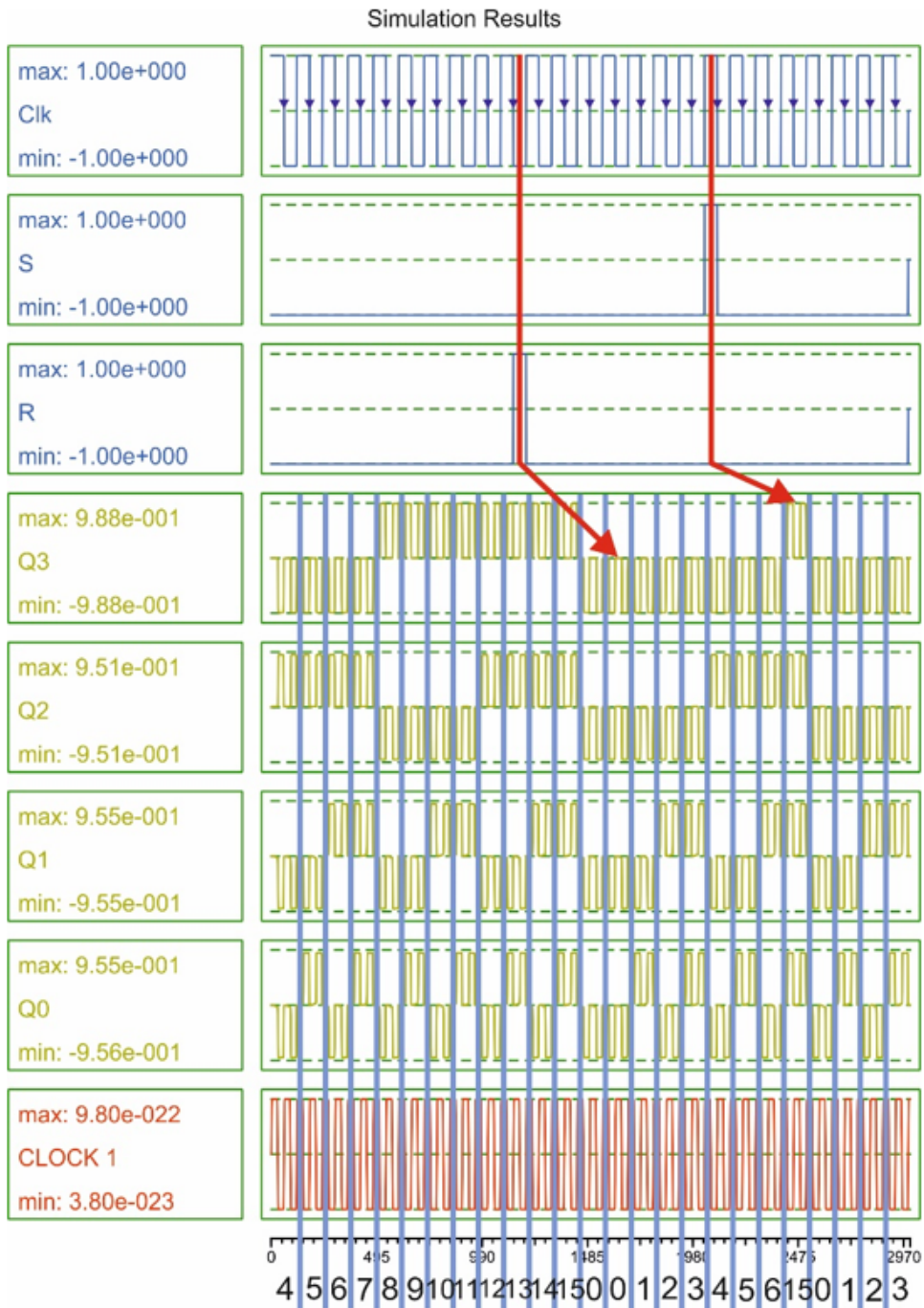


Figure 15

Output waveforms of proposed 4-bits counter with set and reset abilities in QCA nanotechnology.

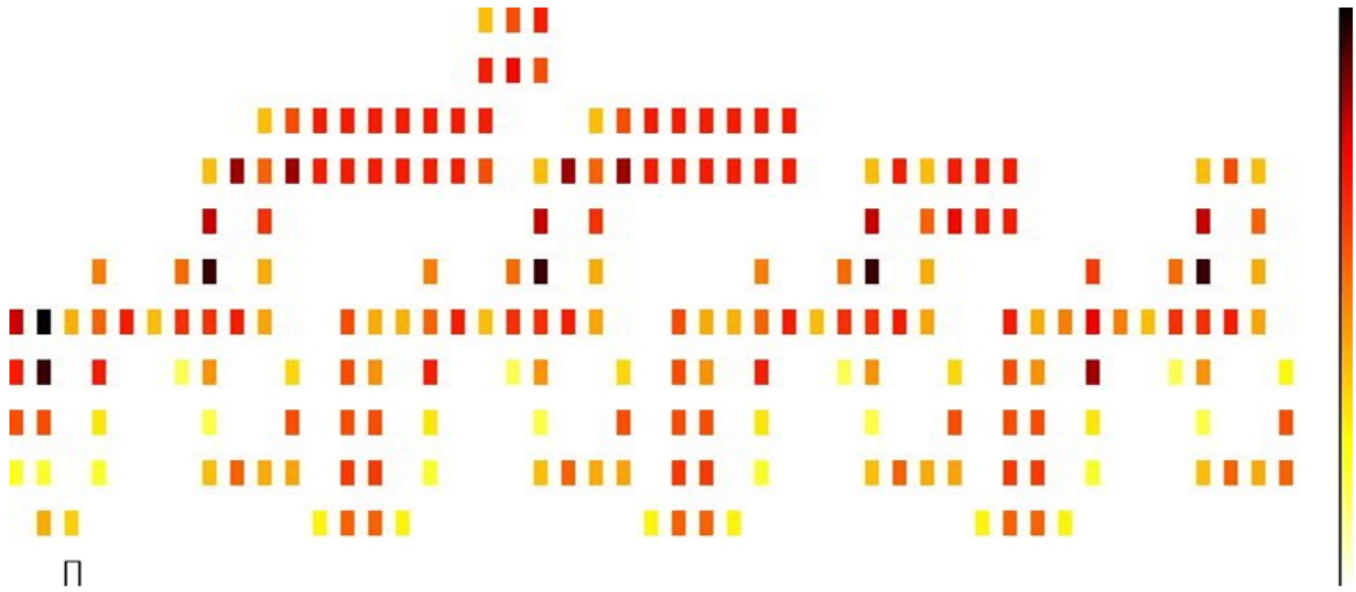


Figure 16

The power dissipation maps of proposed counter

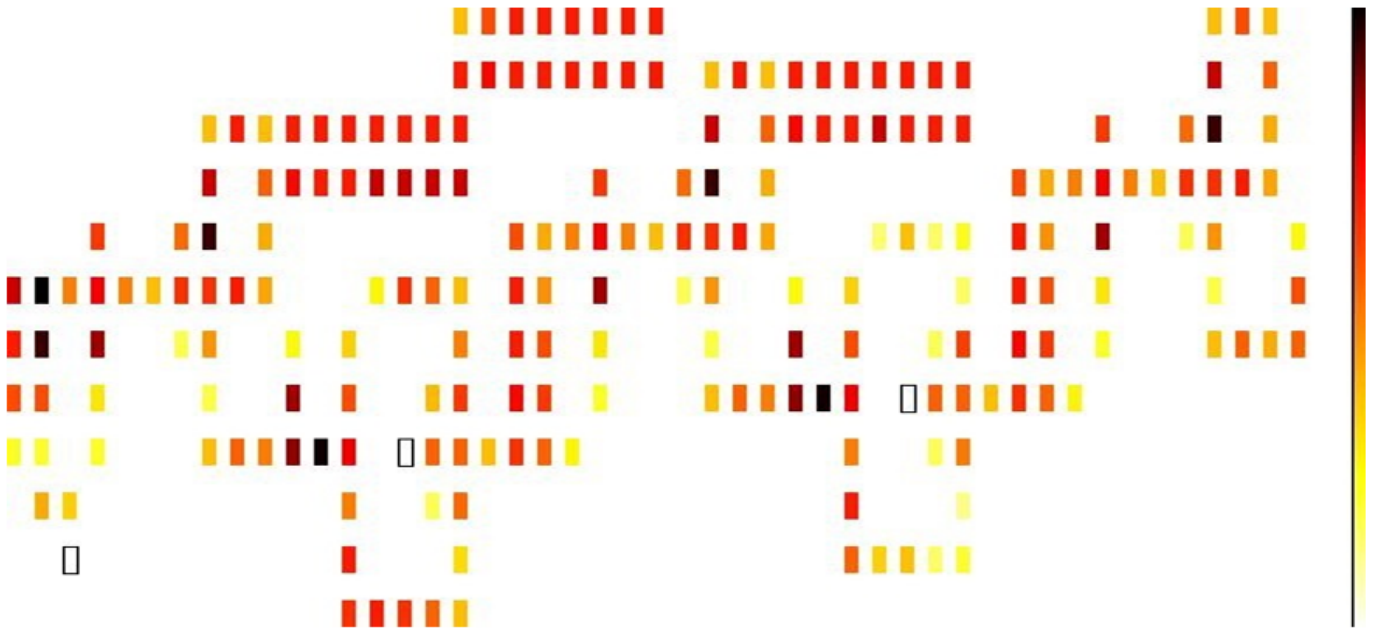


Figure 17

The power dissipation maps of proposed bidirectional counter

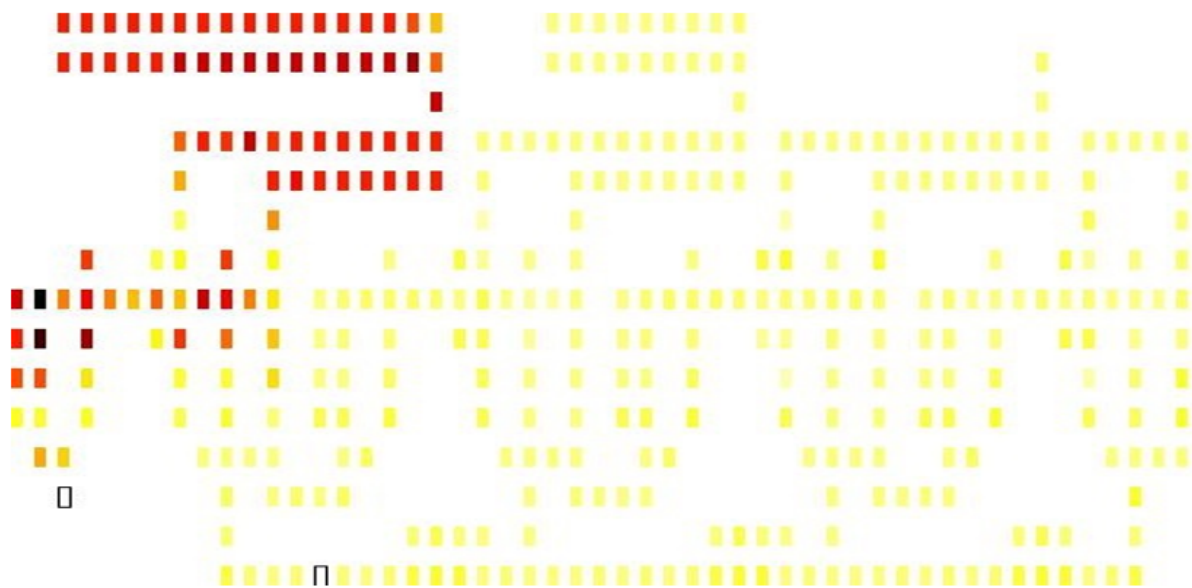


Figure 18

The power dissipation maps of proposed counter with Reset

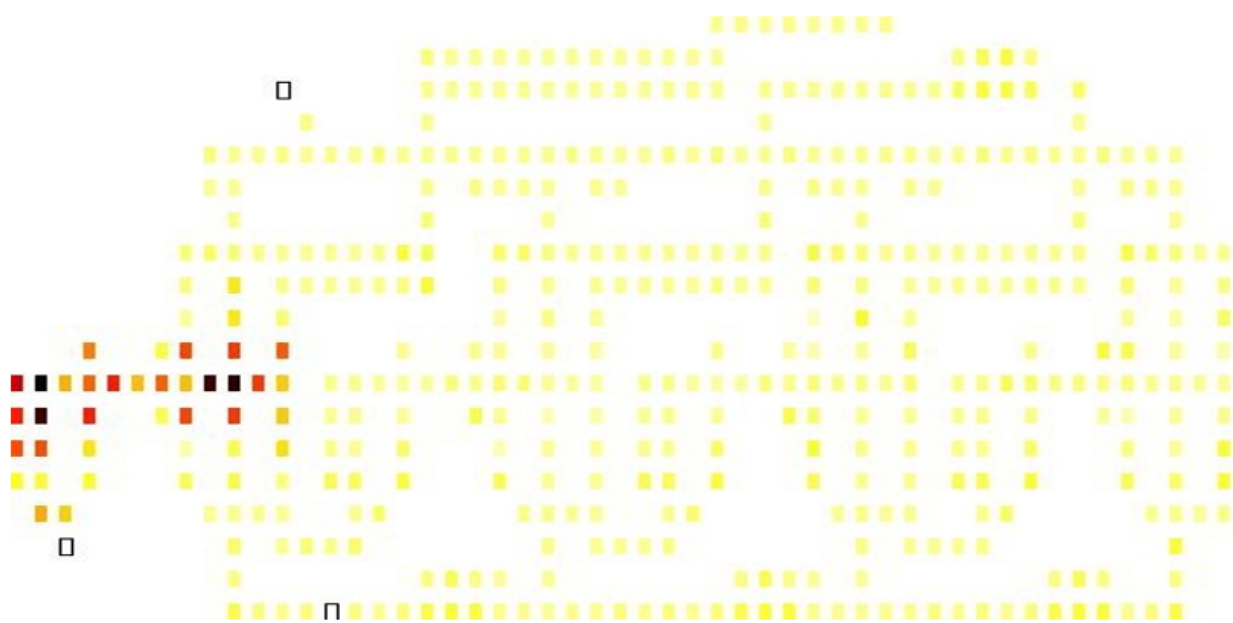


Figure 19

The power dissipation maps of proposed counter with Set/Reset