

## ATLAS Muon Drift Tube Electronics

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**ABSTRACT:** This paper describes the electronics used for the ATLAS monitored drift tube (MDT) chambers. These chambers are the main component of the precision tracking system in the ATLAS muon spectrometer. The MDT detector system consists of 1,150 chambers containing a total of 354,000 drift tubes. It is capable of measuring the sagitta of muon tracks to an accuracy of  $60\ \mu\text{m}$ , which corresponds to a momentum accuracy of about 10% at  $p_T = 1\ \text{TeV}$ . The design and performance of the MDT readout electronics as well as the electronics for controlling, monitoring and powering the detector will be discussed. These electronics have been extensively tested under simulated running conditions and have undergone radiation testing certifying them for more than 10 years of LHC operation. They are now installed on the ATLAS detector and are operating during cosmic ray commissioning runs.

**KEYWORDS:** Electronic detector readout concepts (gas, liquid); Data acquisition circuits; Front-end electronics for detector readout; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases).

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## Contents

<b>1. Introduction</b>	<b>2</b>
1.1 The MDT precision tracker	2
1.2 The MDT drift tube	4
1.3 MDT readout system overview	6
1.4 MDT readout system optimization	9
1.5 MDT readout system data rates	11
<b>2. MDT on-chamber electronics component design</b>	<b>12</b>
2.1 Chamber interconnect boards	12
2.1.1 Front-end interconnect board (signal hedgehog)	13
2.1.2 On-chamber high-voltage distributor board (HV hedgehog)	14
2.2 Front-end electronics - the mezzanine board	15
2.2.1 Amplifier Shaper Discriminator (MDT-ASD chip)	18
2.2.2 Time to Digital Converter (AMT-3 chip)	21
2.3 On-chamber multiplexer - Chamber Service Module (CSM)	25
2.3.1 The passive interconnect	25
2.3.2 The active CSM multiplexer	26
2.4 Monitoring and control - Embedded Local Monitor Board (ELMB)	30
2.5 The calibration system	31
<b>3. On-chamber electronics support services and environmental factors</b>	<b>31</b>
3.1 Low-voltage power	32
3.2 High-voltage distribution	33
3.3 Radiation tolerance of the front-end components	35
3.3.1 Radiation levels in the MDT detector	35
3.3.2 Damage scenarios in electronics devices	35
3.3.3 Levels of test doses and test results	36
<b>4. Off-chamber electronics - MDT Read Out Driver (MROD)</b>	<b>38</b>
4.1 Functionality	38
4.2 Implementation	41
4.2.1 The MRODin FPGA	42
4.2.2 The MRODout FPGA	46
4.2.3 The busy signal	47
4.2.4 Configuration of the FPGAs	48
4.2.5 Software environment	49
4.2.6 Monitoring	49
4.3 Throughput tests	50
<b>5. System tests</b>	<b>50</b>

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## 1. Introduction

The monitored drift tube (MDT) chambers are the main component of the precision tracking system in the ATLAS muon spectrometer [1]. The precisely manufactured MDT chambers are carefully monitored within the ATLAS detector for their position, internal deformations, and environmental conditions like temperature and magnetic field. Due to the combination of mechanical accuracy of each chamber and external position monitoring (“alignment”), the MDT system achieves a sagitta accuracy of  $60\ \mu\text{m}$ , corresponding to a momentum resolution of about 10% at  $p_T = 1\ \text{TeV}/c$ . The 1,150 MDT chambers are made from 354,000 tubes and cover an area of  $5,500\ \text{m}^2$ .

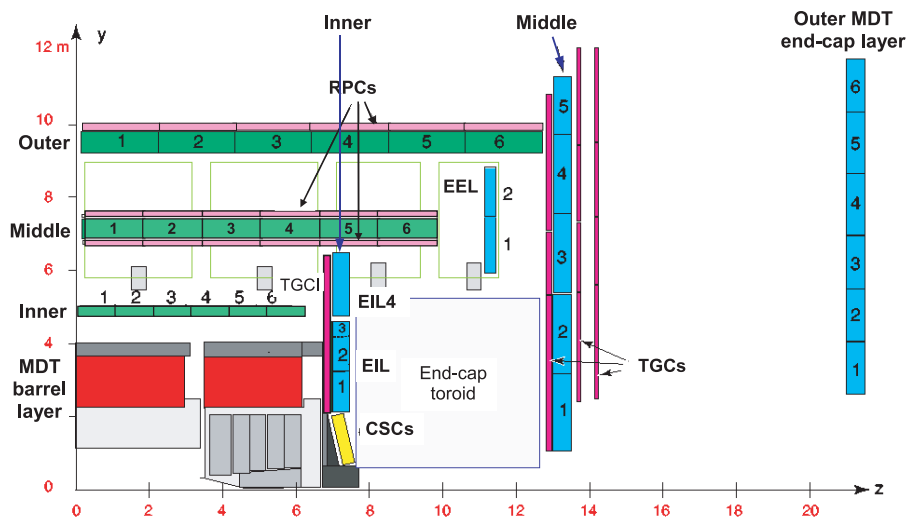
The main task of the readout electronics is to preserve the inherent measurement accuracy of the tubes ( $80\ \mu\text{m}$ ) and to cope with the high hit rates expected at full LHC luminosity (up to 300 kHz per tube). In order to obtain the required tracking accuracy the front-end electronics have been implemented with a low-impedance, low-noise amplifier-shaper-discriminator (ASD) together with a high resolution TDC. To process the high data rates, the system architecture is based on fine segmentation of the readout (24 tubes per TDC), fast local processors, large storage capacities at each level of data processing and high-speed data links. The front-end electronics have also been designed to survive in a high radiation environment and have undergone testing certifying them for more than 10 years of LHC operation. In addition to reading out the MDT chambers, electronics are necessary to control the readout system, to monitor the chamber environment and running conditions, and to supply the necessary low and high voltage power.

The organization of this paper is as follows. In the remainder of this section an overview of the MDT system is presented, which includes a summary of both the chamber mechanical design and the associated readout electronics. Section 2 contains a detailed discussion of the design of the on-chamber electronics for reading out and monitoring the system, while section 3 covers the support services for their operation and the environmental factors that affect them. Section 4 describes the design and implementation of the off-chamber readout electronics. The final two sections discuss the testing of the system with cosmic rays and muon beams, and present some conclusions. An appendix is attached which tabulates the parameters of the individual MDT chambers for reference purposes. Electronics related to chamber alignment are not covered in this paper - see references [2] and [3] for the barrel and end-cap alignment systems respectively.

### 1.1 The MDT precision tracker

The muon spectrometer of the ATLAS detector is illustrated in figure 1. It is designed to detect charged particles exiting the barrel and end-cap calorimeters and to measure their momenta at polar angles greater than  $7.7^\circ$  corresponding to pseudo-rapidity  $|\eta| \leq 2.7$ .

The primary momentum measurement in the muon system is provided by monitored drift tube chambers (MDTs) which consist of pressurized drift tubes with a diameter of 30 mm, operating



**Figure 1.** Cross-section of the muon system in a plane containing the beam axis. MDT chambers in the barrel (green) and in the end-cap (blue) are arranged in three layers around the hadronic calorimeters (red and grey). In the first layer of the end-cap, cathode strip chambers (yellow) are used near the beam-pipe instead of MDTs to cope with the expected high track densities at  $\eta \geq 2.4$ . The chambers marked RPCs and TGCs are the trigger chambers in the barrel and end-cap regions.

with Ar/CO<sub>2</sub> gas (93/7) at 3 bar. In the very forward region ( $2 < |\eta| < 2.7$ ) of the innermost tracking layer cathode strip chambers (CSCs) are used due to their higher rate capability and time resolution [4]. Input to the Level-1 muon trigger [5], which selects muons pointing to the interaction region with transverse momenta above a programmable threshold, is provided by fast tracking detectors. These detectors are resistive plate chambers (RPCs) in the barrel region and thin gap chambers (TGCs) in the end-cap region [4]. Their time resolution guarantees the identification of the interaction bunch crossing, and their readout segmentation in the direction along the MDT wires measures the  $\phi$  coordinate with a resolution of 1 cm.

The MDT chambers are arranged in three layers along the trajectory of the track, which allows a determination of the momentum from the sagitta of the track’s curvature in the magnetic field. In the barrel part of the detector the three layers form coaxial cylinders, in the end-cap part they form large circular disks centered at the beam axis. In the inner MDT layer each chamber consists of eight tube layers which are segmented in two “multi-layers” of four tube layers each. In the middle and outer MDT layers the chambers consist of six tube layers divided into multi-layers of three tube layers. The multi-layers in a chamber are separated by a spacer for structural reasons as well as to permit a crude momentum measurement for low momentum tracks and the construction of a track segment for high momentum tracks. The distance between the multi-layers varies between 6 and 121 mm in the inner layer and between 170 and 317 mm in the middle and outer layers.

MDT chambers are rectangular in the barrel and trapezoidal in the end-cap, being built in various dimensions to optimize solid angle coverage. Apart from the length, all MDT tubes are identical. In the final implementation, the MDT system will consist of 656 chambers in the barrel and 494 chambers in the end-caps. A detailed list of chamber types and dimensions is given in the

appendix in table 12 for the barrel and in table 13 for the end-cap chambers. Construction parameters of the different MDT chamber types and their locations in the detector are presented in [6].

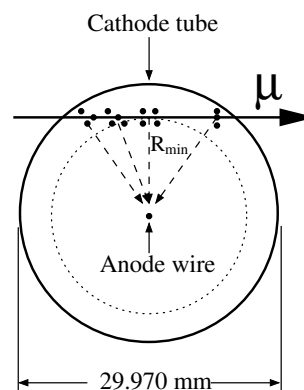
With an average tube resolution of  $80 \mu\text{m}$ , a chamber resolution of  $40 \mu\text{m}$  and  $35 \mu\text{m}$  is achieved for 6 and 8 layer chambers, respectively. A detailed descriptions of the muon system is given in reference [4].

## 1.2 The MDT drift tube

Figure 2 shows the cross-section of a MDT tube. The wall thickness is  $0.4 \text{ mm}$  and the inner radius is  $14.58 \text{ mm}$  ( $R_{\text{max}}$ ). For each track the electrons from the primary ionisation clusters drift to the central wire along radial lines, the corresponding drift lengths ranging from  $R_{\text{min}}$  to  $R_{\text{max}}$ .

In the  $\text{Ar}/\text{CO}_2$  gas the drift velocity shows a strong dependence on the radius, i.e.  $10 \mu\text{m}/\text{ns}$  close to the wall,  $26 \mu\text{m}/\text{ns}$  at  $r = 7,25 \text{ mm}$  and  $52 \mu\text{m}/\text{ns}$  close to the wire. The exact shape of the radius-to-drift time relation ( $r$ - $t$  relation) depends on parameters like temperature, pressure, magnetic field and total hit rate in the tube; the latter being due to field distortions caused by the positive ions. Figure 42 in section 5 displays an example of the drift-time spectrum. In order to make optimal use of the inherent spatial resolution of the MDT tube, the  $r$ - $t$  relation must be known with high accuracy, which is achieved by continuous calibration with tracks in the ATLAS experiment. The operating parameters of the MDT tubes are given in table 1.

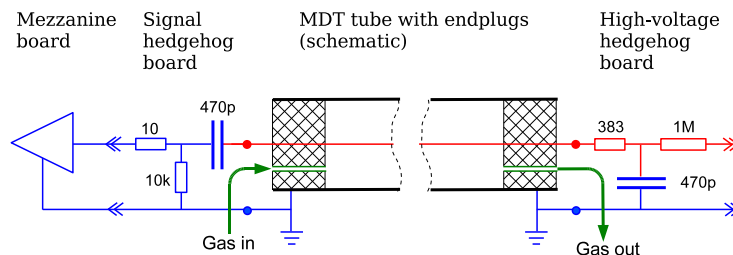
The main sources of the measurement error in the MDTs are diffusion and the uneven distribution of location and ionisation density of the primary clusters along the track. The electrons arriving earliest at the wire will in general come from a point along the track which is slightly displaced with respect to  $R_{\text{min}}$ , leading to an increased travel time to the wire. The operation of the drift tubes at a pressure of three atmospheres reduces diffusion as well as the fluctuation of both ionisation and cluster location. A detailed discussion of the various physics contributions to the



**Figure 2.** MDT tube cross-section with ionisation clusters distributed along a track.

**Table 1.** Main MDT chamber parameters.

Parameter	Design value
Wire diameter	$50 \mu\text{m}$
Gas mixture	$\text{Ar}/\text{CO}_2$ (93/7)
Gas pressure	3 bar (absolute)
Gas gain	$2 \times 10^4$
Wire potential	3080 V
Average drift velocity	$\sim 20.7 \mu\text{m}/\text{ns}$



**Figure 3.** Main service connections to a MDT tube. At the high-voltage side the wire is terminated with the equivalent transmission line impedance of the tube ( $383 \Omega$ ) to avoid reflections. All contacts (round dots) between the chamber and the hedgehog boards are gold plated to ensure a long-term connectivity.

resolution is given in [7]. Though the work described in reference [7] was done for a different gas, the general results are also applicable to the Ar/CO<sub>2</sub> gas [8].

The contribution from *electronics* to the drift time resolution is mainly due to two parameters:

- The rise time of the amplifier combined with the discriminator threshold, which determines the time needed to trigger the TDC. With the performance parameters of the electronics discussed below (see section 1.4) this contributes an average error of 20-25  $\mu\text{m}$ . This error can be further reduced if the charge in the leading edge is measured and a corresponding “slewing” correction is applied (see section 1.4).
- The least significant bit (LSB) error of the TDC, which is  $25 \text{ ns}/32 = 0.78 \text{ ns}$ , corresponding to an RMS-error of 0.23 ns. This contributes an average error of 20  $\mu\text{m}$  to the measurement of  $R_{\min}$ .

In an MDT tube each track creates a sequence of pulses, the duration of which corresponds to the time difference in drifting from  $R_{\min}$  and  $R_{\max}$ . While only the electrons arriving earliest at the wire, namely those coming from the cluster created nearest to the anode wire (approximately from  $R_{\min}$ ), are used for the determination of the track coordinate, the subsequent ones will create additional threshold crossings, inflating the data volume to be read out. Therefore, the electronics have the capability to disable the discriminator for a certain time after the initial threshold crossing by means of a programmable dead-time. A detailed discussion of the time structure of the pulses is given in [9].

A schematic drawing of the MDT drift tube connections to the electrical services is shown in figure 3. At the right end is the high-voltage “hedgehog” board (section 2.1.2) where a  $383 \Omega$  resistor terminates the tube with its characteristic transmission line impedance and which also contains decoupling capacitors and protection components. The termination resistor suppresses signal reflection at the open end of the wire, however, it is also a significant source of thermal noise (see section 1.4). At the left end the signal hedgehog board (section 2.1.1) connects the tube to the “mezzanine” board (section 2.2) which contains the active readout electronics.

An aluminum Faraday cage completely surrounds the electronics at both ends of the chamber to provide shielding from external noise sources. The metallic surface of each tube is grounded at both ends to the hedgehog boards and to the bottom plates of the Faraday cages, which are in turn



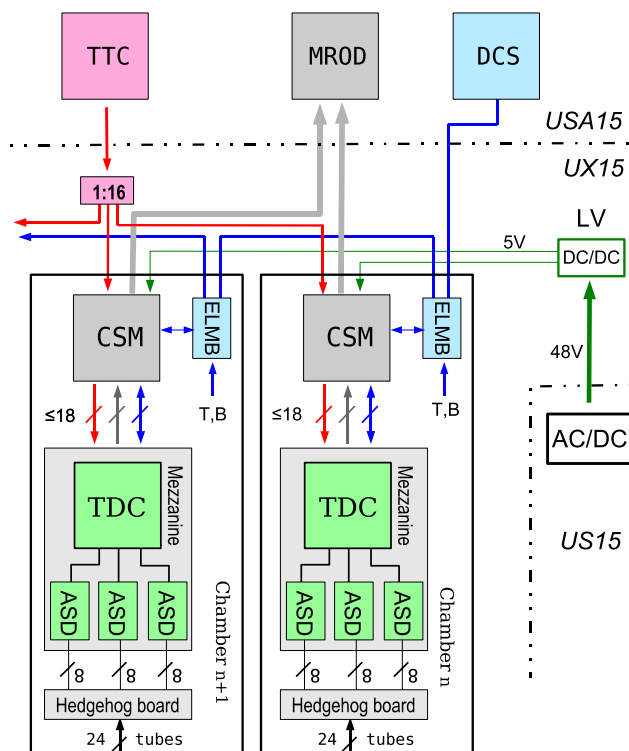
**Figure 4.** A photograph of the readout end of an end-cap MDT chamber where the assembly has been staged in sections to illustrate the tube ends with gas tubelets visible (upper center), one hedgehog board attached to the tube ends (upper right), one mezzanine board plugged through the inner Faraday cover (lower left), and a completely enclosed mezzanine board (lower right). In the center is the “chamber service module” (CSM) without its protective cover, and the red box to its left contains an “embedded local monitoring board” (ELMB).

connected to the aluminum support structure of the chamber. The Faraday cages have undergone a chemical surface treatment (chromatisation) to assure a conductive, unalterable surface.

A photograph of the readout end of an MDT chamber showing the location of the electronics components is shown in figure 4. Individual tube signals and grounds are carried via board-to-board connectors from the hedgehog board to the mezzanine board. Ground planes have been added on the top and bottom layers of the signal hedgehog board to shield the long signal traces on the board from the digital noise on the mezzanine boards. The two boards have also been separated by an aluminum inner wall of the Faraday cage (see figure 4), the so called “box-on-box” design. With this design excellent noise immunity has been achieved.

### 1.3 MDT readout system overview

The architecture of the MDT readout is shown in figure 5. In the first stage, the raw signals from 24 tubes are routed via the signal hedgehog boards to the mezzanine boards where they are amplified, discriminated, and digitized. On the mezzanine board the signals from eight tubes are first processed by one of three custom-designed monolithic Amplifier/Shaper/Discriminator (ASD) chips. The binary differential signals output by the ASDs are then routed to the Time-to-Digital Converter (TDC) chip, where the arrival times of leading and trailing edges are stored in a buffer memory of 256 words. Each time measurement is paired together with an identifier of the corresponding tube. The time is measured in units of the Timing, Trigger and Control (TTC) clock of 40.08 MHz [10], which is the bunch crossing (BC) frequency of the LHC machine. There are 4096 bunches in a ma-



**Figure 5.** Schematic diagram of the MDT readout electronics. Each CSM serves up to 18 mezzanine boards depending on chamber size, each MROD up to 6 CSMs.

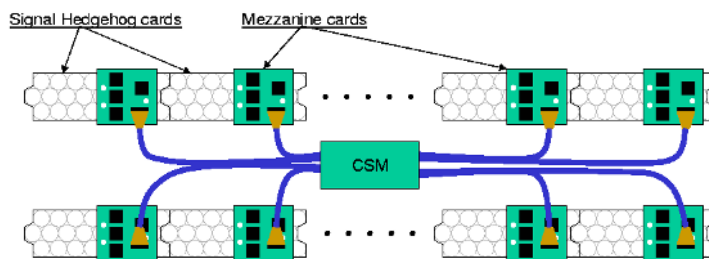
chine cycle, so the BC or “coarse time” is described by a 12 bit word. In the TDC the BC interval of 24.95 ns is subdivided by 32 via a Delay Locked Loop (DLL) resulting in a “fine time” period of 0.78 ns. This leads to an RMS timing error of 0.23 ns in measuring the arrival times.

An additional programmable feature of the ASD is the measurement of the pulse height of the signal, which allows for the monitoring of the gas gain as well as for pulse height dependent “slewing” corrections to the timing. The pulse height is encoded as the time interval between the leading and trailing edge of the ASD output pulse, with an output pulse width of 150 ns corresponding to the maximum input pulse height to be recorded. With this feature enabled the trailing edge of the ASD output pulse does not depend on the discriminator status and the discriminator is disabled until after the pulse height encoding has safely elapsed. Additional discriminator dead-time is also programmable and can be increased up to 750 ns in order to mask multiple hits from the same track.<sup>1</sup>

The mezzanine board containing the TDC chip plus three ASD chips, and serving 24 tubes, is the basic readout element of the MDT chambers. MDT chambers contain up to 18 mezzanine boards which are controlled by a local processor, the Chamber Service Module (CSM), as shown in figure 5. The interconnection scheme between CSMs and mezzanine boards is illustrated in figure 6. High-density 40 pin twisted pair cables are used to transmit control signals as well as supply power.

<sup>1</sup>For tracks passing near the wire there are ionisation clusters extending from the minimum to the maximum times corresponding to  $R_{\min}$  and  $R_{\max}$  respectively, and as a result the shaper circuit has to integrate a large amount of charge. When the shaper is finally “released” the signal may overshoot the baseline outside the dead time window resulting in increased noise at times greater than the maximum allowable.





**Figure 6.** The CSM collects data from up to 18 mezzanine boards which serve 24 MDT tubes each. Data are transmitted via high-density twisted pair cables from the mezzanine boards to the CSM.

JTAG [11] information is distributed by the detector control system (DCS) through a serial bus system called the CANbus [12], using the CANopen protocol [13]. Each chamber contains a CANbus node located on the Embedded Local Monitor Board (ELMB) [14]. The ELMB executes the JTAG operations, loads configuration code into the CSM, and monitors temperature sensors and supply voltages on the CSM and mezzanine boards, as well as temperature and magnetic field values from sensors distributed over the chamber. The ELMB interfaces to the CSM via opto-couplers, such that there is no DC connection between the CSM/chamber ground and the CANbus wires.

Programming of the CSM and of the ASD and TDC chips on each mezzanine board is done over JTAG, allowing for a string of 72 bits for the CSM, of 160 bits per three ASD chips and of 180 bits per TDC chip. In this way, many parameters and functions can be controlled, including the setting of the discriminator threshold and dead-time, triggering of test pulses for calibration, or deactivation of noisy channels.

The CSM communicates with the off-chamber electronics via two fibers, one coming from the TTC distribution box and the other going to the MDT Readout Driver (MROD) [15]. During normal data taking, the CSM broadcasts the TTC control and trigger signals to the TDCs and collects the data coming from the TDCs in response to all the Level-1 triggers. Subsequently, the data are formatted, stored in a de-randomizing buffer, and sent via an optical link to the MROD in the USA15 service cavern. The MROD is a VME module, serving up to six CSMs. Its main task is to assemble the data associated with each event for rapid transfer to the Readout Buffer (ROB) [16] where data are stored until the event has been either accepted or rejected by the Level-2 trigger. Table 2 summarizes the modularity of the readout system.

**Table 2.** Modularity of the MDT readout electronics. The difference between the number of chambers and CSMs in the barrel is due to some CSMs serving a pair of chambers. The allocation of MRODs to the barrel or end-cap is approximate, some MRODs serving CSMs from both regions.

Region	Tubes	ASDs	Mezz. boards	CSMs	Chambers	MRODs
Barrel	191568	24114	8038	624	656	100
Two endcaps	162816	20352	6784	494	494	104
Total	354384	44466	14822	1118	1150	204

**Table 3.** Power consumption of components, a mezzanine board, an "average" MDT, a "maximum" MDT (with 18 mezzanine boards) and the overall system. An average MDT has a calculated 308 tubes, served by approximately 13 mezzanine boards. The current drawn by an average and a maximum MDT is 6.3 and 8.3 A respectively. The average consumption per tube is 82 mW excluding, and 93 mW including the cable loss.

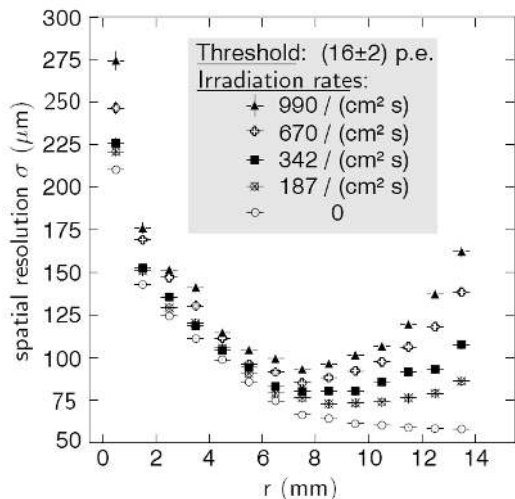
	Component		Mezz.	MDT Chamber		System <i>1150 ch's</i>
	<i>mW</i>	<i>count</i>		<i>avg.</i>	<i>max.</i>	
			<i>mW</i>	<i>W</i>	<i>W</i>	<i>kW</i>
ASD	300	3	900			
AMT		1	360			
Drivers / Receivers		1	90			
Mezzanine board @ 3.3 V			1350			
Voltage regulator 4 V $\Rightarrow$ 3.3 V			280			
Mezzanine board @ 4 V			1630			
MDT, excluding CSM				21.2	29.3	
CSM (1 A @ 4 V)				4.0	4.0	
Complete MDT at 4 V				25.2	33.3	
Total MDT (excl. supply cables)						29
Supply cable loss ( $\sim 15\%$ )						4
Total MDT (incl. supply cables)						33

An important feature of the MROD is its processing power that allows it to monitor the incoming data. The data streams received from the CSMs can be sampled for tube and chamber occupancies and their deviations from nominal values, possibly pointing to a malfunction. As the MRODs see the full Level-1 event rate, they can accumulate significant statistics in a short time, allowing for an early recognition of errors. Depending on average event size and Level-1 rate, a variable fraction of the events will be monitored in order to not slow down data transfer to the ROB, which has priority.

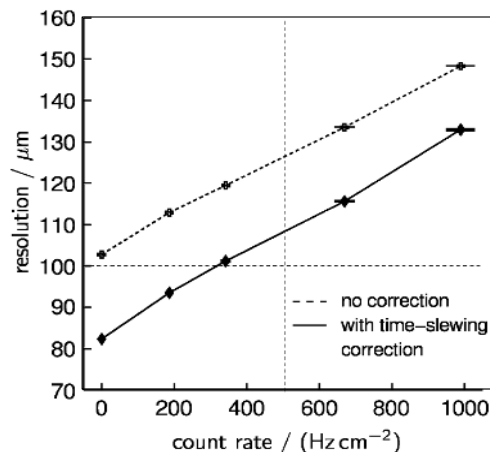
Power for the on-chamber readout electronics is routed via a shielded cable from a single DC source to the CSM and is then distributed separately to the analog and digital circuitry on the mezzanine boards. The source voltage is adjusted to deliver approximately 4 V at the CSM. Each mezzanine board draws about 270 mA for the analog part and 140 mA for the digital part at about 4 V, which is regulated to 3.3 V by on-board regulators. Thus the total power consumption of a mezzanine board is 1.6 W, including the power used by the voltage regulators. The CSM, including its regulators, consumes about 4 W, a large chamber with mezzanine boards for 432 tubes consumes 33 W, and the entire MDT system consumes 37 kW. A breakdown of the power consumption of the MDT readout electronics is given in table 3.

#### 1.4 MDT readout system optimization

Extensive test-beam measurements and simulations have been performed in order to study the spatial resolution of the MDT system under different operating conditions and to optimize the



**Figure 7.** Spatial resolution of a drift tube as a function of the drift distance  $r$  at various levels of  $\gamma$ -irradiation with a threshold of 16 photoelectrons (p.e.).



**Figure 8.** Effect of the time-slewing corrections on the average spatial resolution of a the drift tubes. The maximum rate expected for the MDTs is  $\leq 150$   $\text{Hz}/\text{cm}^2$ .

parameters for the front-end electronics [17, 18]. As an example, figure 7 shows the resolution as a function of the drift distance at different background rates ([9, 19–21]). Background hits, due to converted neutrons and  $\gamma$ 's, lead to space charge in the drift gas and, consequently, to drift field fluctuations which reduce the resolution. This effect, increasing with the distance from the wire, is clearly visible in the figure. The tube signals in the Ar/CO<sub>2</sub> gas and the electronics response have been simulated with the GARFIELD program and are in good agreement with the measured resolution, illustrating that the performance of the MDT system is quite well understood.

The baseline choice for the gas gain of the MDT tubes is  $2 \times 10^4$ . The minimum practical discriminator threshold is five times the noise level, which in the MDTs is dominated by termination resistor thermal noise. Using pre-amplifier peaking times of less than 5 ns does not improve the MDT resolution since the signal-to-noise ratio rapidly becomes worse for such short peaking times.

If the MDTs were operated at a very high gas gain ( $> 10^5$ ), the signal-to-noise ratio would be high, permitting operation at a wide range of discriminator thresholds. In that case the resolution would be best for very fast pre-amplifiers (peaking times of 3–4 ns) and very low thresholds (3–5 electrons). However, owing to the high background rates in the spectrometer, the possible degradation of the chamber performance (ageing) caused by large amounts of charge deposited on the anode wire would be a serious problem. The ageing effects are therefore minimized by operating the chamber at the lowest possible gas gain which is still compatible with the electronic noise and spatial resolution requirements.

Another disadvantage of using a fast pre-amplifier is the sensitivity to individual ionisation clusters which causes multiple threshold crossings per signal and therefore a significant increase in the hit rate. Therefore a choice of a rise time of about 15 ns is the best compromise in terms of resolution, noise sensitivity, overall stability and choice of ASIC technology.

Taking into account only the termination resistor noise, the five times noise level corresponds

to 17 primary electrons for the baseline gas gain. A detailed analysis of the current pre-amplifier design showed that trace capacitances on the board and other parasitic capacitances increase this threshold level to 22–25 electrons [22].

The change in resolution for different thresholds and peaking times is primarily due to time slewing corresponding to different signal rise times from charge fluctuations in the leading edge. By measuring the charge in the leading edge with a short gate ADC (gate time less than twice the peaking time), a correction for the time slewing can be made to improve the resolution [17]. Figure 8 shows the gain in resolution obtained by the slewing correction with little dependence on the background rate. At the maximum expected rate of 150 Hz/cm<sup>2</sup> a resolution of 90 and 110  $\mu\text{m}$  is obtained with and without the correction. To avoid further loss in resolution caused by charge fluctuation, the discriminator time walk should be less than 500 ps (corresponding to an average position error of about 10  $\mu\text{m}$ ) for the entire signal input range.

To minimize the number of threshold crossings per track the discriminator has a programmable amount of hysteresis. For a gas gain of  $2 \times 10^4$  and a threshold of 24 electrons including some hysteresis, 1-2 threshold crossings per signal is typical for the standard tail cancellation with a two stage pole/zero filter used. In order to ignore unwanted secondary hits, the ASD can be operated in a programmable dead-time mode, suppressing trailing hits for a preset interval [23].

In case of a Level-1 trigger all accepted hits within the maximum drift time window are read out. If the pattern recognition algorithm finds a tube to be inefficient it is useful to know the reason for the inefficiency. Reading out the hits within a window preceding the actual drift time window allows one to determine whether an earlier hit (possibly caused by a  $\gamma$ -conversion) could have obscured the hit from the muon track. To minimize bandwidth requirements a single bit is set by the TDC to flag as pile-up the occurrence of any hits prior to the digitization window.

The requirements on bandwidth, buffer memory in the TDC, and serial link speed are mainly determined by the background hit rates. According to detector simulations the maximum count rate per tube in the MDT system is 300 kHz (including a safety factor of five for the uncertainty in the background simulation). The options implemented in the ASD-TDC design for various quantities of interest (leading and trailing edges, integrated signal leading edge and multi-hit information) are discussed in the following sections.

### 1.5 MDT readout system data rates

The flow of data through the front-end is subject to the rate of hits in the MDT tubes and varies widely over the span of chambers. Estimates of the rates (with a safety factor of five) for chambers at small angles to the beam line and for the inner layers, approach saturation of the TDC processing capacity at  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  luminosity. The majority of the hits are not from muon tracks but from photon and neutron induced ionisation. The TDC is designed to remove old hits from its buffer when average tube rates exceed 300 kHz (see section 2.2.2).

Table 4 displays the data flow rates from the TDC through the CSM. The ATLAS wide maximum trigger rate, 100 kHz, is used in the rate calculation along with an 800 ns TDC “search window” for each trigger. The maximum rate on the TDC-CSM link is 80 Mbit/s. Four different tube hit rates chosen for illustration. The 0 kHz value is included to show the bandwidth occupied by synchronization words (called headers and trailers) and mask words that flag prior hits. Each

**Table 4.** The relationship between tube hit rates in kHz and the link occupancy at low, medium and high hit rates of the MDT tubes. A hit rate of 0 is included to illustrate the bandwidth occupied by TDC headers, trailers, and mask words.

Ungated hit rate per tube [kHz]		⇒	0	75	150	300
Gated tube hit rate	[kHz]		0	6	12	24
Gated TDC hit rate	[kHz]		0	144	288	576
Gated TDC word rate	[kHz]		300	588	876	1452
Gated TDC bit rate	[Mbits/s]		10.8	21.2	31.5	52.3
Fraction of TDC ⇒ CSM link	percentage		13.5%	26.5%	39.4%	65.3%
Per 18 mezz board chamber	[Mbits/s]		172.8	338.7	504.6	836.4
Fraction of CSM ⇒ MROD link	percentage		12.6%	24.7%	36.8%	61.0%

TDC sends one each of these three words for each trigger. The first row of table 4 represents ungated hit rates. The remaining rows represent data selected for output by the trigger and gate width. The processing bandwidth of the CSM is designed to pass all incoming data. The removal of hits at high rates is left exclusively to the TDC where a flag is provided with each data word to indicate when prior hits were lost.

Data flows from the CSM to the MROD over a 1.6 Gigabit/s link and consists of TDC output from up to 18 mezzanine boards, two optical synchronization words and one readout cycle synchronization word (see section 2.3.2). The available bandwidth for chamber data is thus reduced by an 18/21 ratio to 1.37 Gigabit/s. The rate of data transmission from CSM to MROD exceeds the sum of the total input rate from 18 mezzanine boards and yields a slightly lower percentage occupation in each case in the table. It should also be noted that the chambers in the regions with the highest rates have 16 or fewer mezzanine boards. See figure 34 for a more detailed evaluation of the expected data rates into the MRODs.

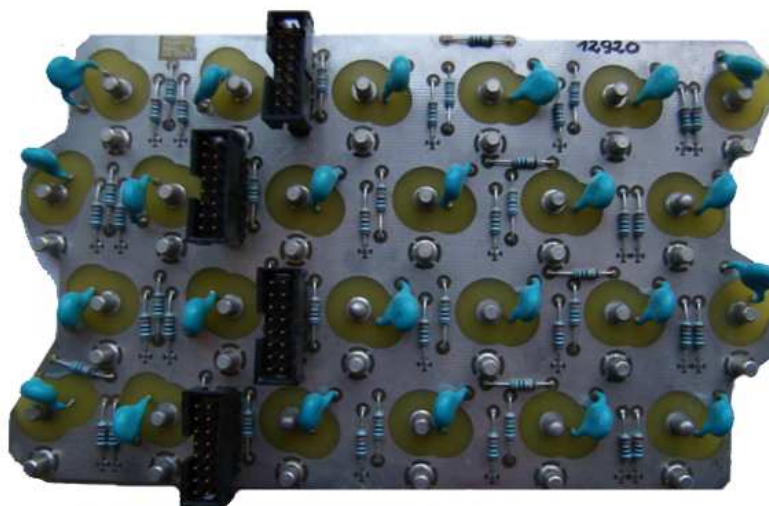
Flow control within each MROD is provided by a ROD busy output, and a logical OR of all such busy signals inhibits triggers. The ROD busy design is an ATLAS wide feature and not exclusive to the muon system.

## 2. MDT on-chamber electronics component design

The on-chamber electronics components consisting of the hedgehog boards, the mezzanine boards, the chamber service module (CSM), and the local monitor board (ELMB), are described in detail in this section.

### 2.1 Chamber interconnect boards

At both ends of an MDT chamber there are interconnect (“hedgehog”) boards which passively terminate the drift tube wires with capacitors and resistors. At one end the signal hedgehog boards couple the tubes with the front-end readout electronics (section 2.2), while at the other end the high-voltage (HV) hedgehog boards connect the tubes to the high-voltage distribution system (sec-



**Figure 9.** A signal hedgehog board for 4 tube layer chambers.

tion 3.1). Each hedgehog board services 24 tubes. At each end of the chamber the hedgehog boards are enclosed in Faraday cages to shield the tube connections.

### 2.1.1 Front-end interconnect board (signal hedgehog)

An example of a signal hedgehog board is shown in figure 9. For each tube this board contains both signal and ground receptacles together with a HV-decoupling capacitor and two resistors that form a protection network (see figure 14 in section 2.2). A mezzanine board plugs directly onto the pin headers of the hedgehog board.

The signal hedgehog is a four-layer printed circuit board with the signal traces routed on the two internal layers. The two external layers are ground planes covering as much surface area as possible taking in consideration the necessary clearance around the HV receptacles. The ground planes are required to shield the signal traces from HF noise generated by the TDC clock on the mezzanine board.

There are four different types of signal hedgehogs, two of each for the 3-layer and 4-layer MDT chambers respectively. For each kind of chamber the two types geometrically fit the shapes of the two multi-layers. The 3-layer boards have 8 channels (tubes) per layer and the 4-layer boards have 6 channels per layer, both totaling 24 channels. The board shown in figure 9 is for a 4-layer chamber.

The HV-decoupling capacitor is a 470 pF, 6.3 kV ceramic capacitor produced by Murata. The same type is used in the HV hedgehogs. It is placed in series with the signal path, so the signal quality could possibly be degraded by its performance. For this reason, its stability was extensively tested under different HV, temperature and humidity conditions. Its mean failure rate has been measured to be 0.0004% per unit for every 1000 hours of operation [24].

Each of the 24 MDT tubes serviced by a signal hedgehog board is connected to a unique TDC channel on the attached mezzanine board, and the TDC channel number is the identifier for that

**Table 5.** The mapping between the MDT tube location and the TDC channel number for the four signal hedgehog board types. The orientation and placement of the different hedgehog types depends on chamber type and location within the detector [25], [26].

Type	Row	TDC Channel # for Tubes in Layer
I (3-layer)	1	1, 3, 5, 7, 6, 0, 4, 2
"	2	9, 11, 13, 15, 14, 8, 12, 10
"	3	17, 19, 21, 23, 22, 16, 20, 18
II (3-layer)	1	1, 3, 5, 7, 6, 4, 2, 0
"	2	9, 11, 13, 15, 14, 12, 10, 8
"	3	17, 19, 21, 23, 22, 20, 18, 16
III (4-layer)	1	5, 3, 4, 2, 0, 1
"	2	11, 9, 10, 8, 6, 7
"	3	17, 15, 16, 14, 12, 13
"	4	23, 21, 22, 20, 18, 19
IV (4-layer)	1	3, 1, 5, 0, 2, 4
"	2	9, 7, 11, 6, 8, 10
"	3	15, 13, 17, 12, 14, 16
"	4	19, 21, 23, 18, 20, 22

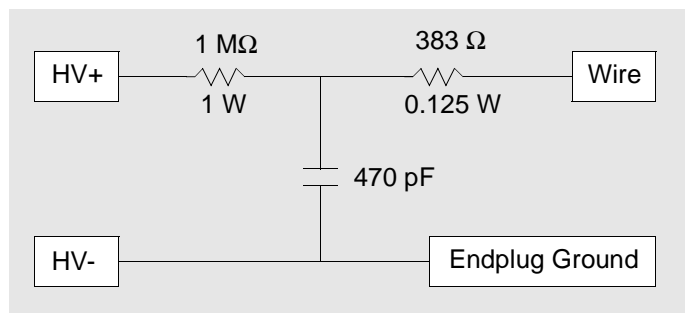
tube in the output data stream. The mapping between tube location and TDC number is different for each hedgehog type and is given in table 5.

The signal hedgehog boards are conformally coated with Dow Corning R4-3117 RTV. This eliminates leakage current between the traces as long as the relative humidity is less than approximately 50%. The insulation properties of this product were shown to be adequate after both neutron and gamma radiation.

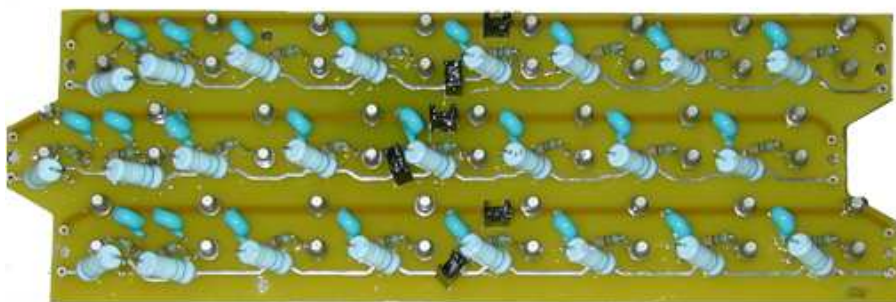
### 2.1.2 On-chamber high-voltage distributor board (HV hedgehog)

The distribution of high-voltage to the MDT tubes is done by the HV hedgehog board, which is mechanically interfaced with the tubes using the same receptacles as on the signal hedgehogs. The schematic of a single channel of this board is shown in figure 10. The combination of the 1 M $\Omega$  resistor and 470 pF capacitor filters the high-frequency noise (> 500 Hz) on the high-voltage line. In the case of a wire short the maximum HV supply current set on the distributors, which cannot be greater than 0.7 mA, will flow through the 1 M $\Omega$  resistor for a period of 0.1 seconds, after which time the HV will be shut off. The capacitor is the same type as described in the signal hedgehog section. The final component is the 383  $\Omega$  resistor, which is in series with the tube matching its impedance.

As with the signal hedgehogs, there are 24 channels on each board, distributed in 3 rows of 8 channels each or in 4 rows of 6 channels each for the 3-layer and 4-layer chambers respectively. The layout is designed on two layers, without shielding layers, taking in account the minimum clearance of 3 mm between high-voltage and ground. The irregular design of some chamber Faraday cages plus the need for special HV hedgehogs that connect to the external HV source leads to a much



**Figure 10.** Schematic of one HV hedgehog channel.



**Figure 11.** A 3-layer barrel HV hedgehog board.

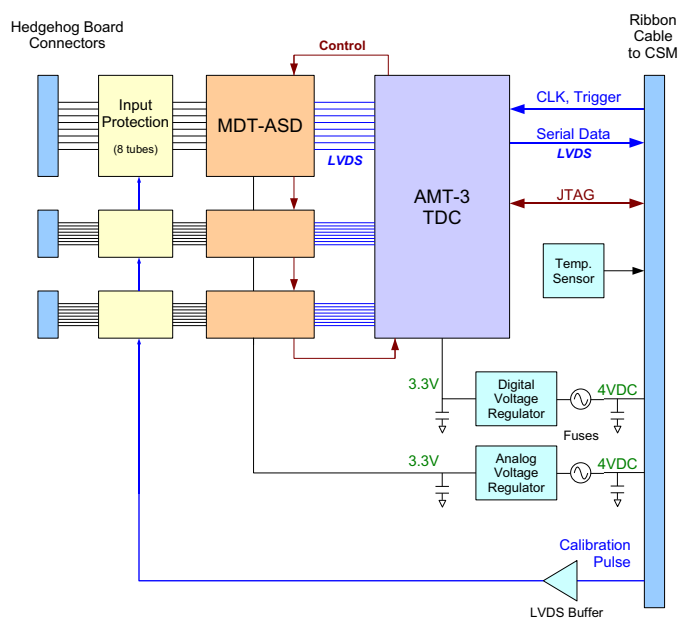
larger number of board designs than in the case of the signal hedgehogs. The total number of HV hedgehog types is 28: 22 for the barrel and 6 for the end-cap. A typical 3-layer HV hedgehog for the barrel MDTs is shown in figure 11.

The high-voltage lines coming from the external HV splitter box are connected to only one HV hedgehog for each multi-layer. This particular board has additional connectors installed: for the barrel chambers they are AMP two-position connectors, separated for high-voltage and ground, and for the end-cap they are Molex five-position connectors, with high-voltage and ground contacts on the same connector. In order to pass the high-voltage line through the full multi-layer, each high-voltage line on the hedgehogs is daisy-chained from board to board. In the barrel this is done using gilded jumpers. The end-cap HV hedgehogs are stepped due to the trapezoidal geometry of the chambers, and in this case chaining is done by means of wire jumpers connecting Molex multi-pin connectors on adjacent boards. Because of the high voltages present on the hedgehog boards, they are expected to operate in a relative humidity less than approximately 50%.

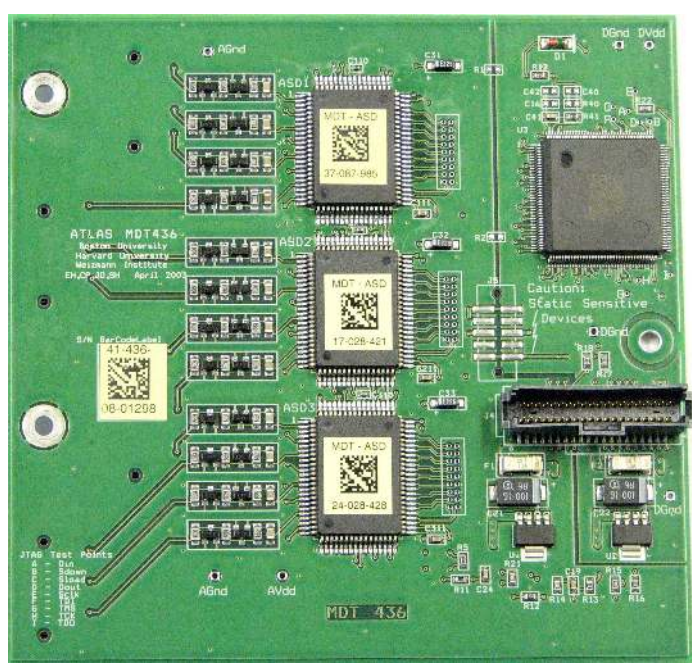
## 2.2 Front-end electronics - the mezzanine board

The mezzanine board carries the active electronics for 24 MDT channels and comes in different configurations for chambers with 3 and 4 tube layers. A block diagram of the mezzanine board is shown in figure 12 and a picture of a 3 tube layer board is shown in figure 13. Three MDT-ASD chips, one TDC chip, two voltage regulators, LVDS-drivers/receivers, a temperature sensor, and various other components are mounted on the board. The dimensions of the boards for 3 (4) tube layers are  $11.2 \times 9.3$  cm ( $11.2 \times 10.9$  cm).

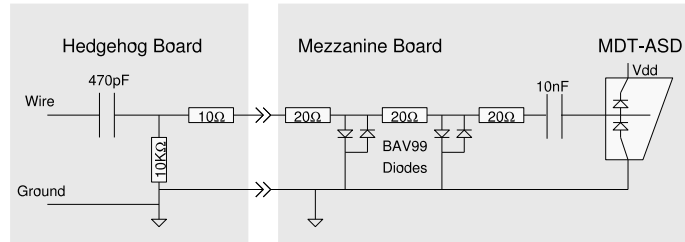




**Figure 12.** The mezzanine board contains three 8 channel ASD chips, a 24 channel time digitizer called the AMT, 3.3V power regulators, protection circuitry, connectors that accept the wire signals and a header for the cable to the readout logic.



**Figure 13.** A mezzanine board for use on a three tube layer MDT chamber. The input protection circuitry is on the left, the three ASD chips in the middle, and the AMT chip plus the CSM cable connector are on the right.



**Figure 14.** The input protection components on both the hedgehog board and the mezzanine board limit the pulse current into the amplifier.

The chamber input signals are carried in groups of eight from the signal hedgehog boards. Extensive protection against damage from HV discharges in the tubes is provided in several stages as shown figure 14. The hedgehog board has a  $10\ \Omega$  series through-hole  $1/4\ \text{W}$  resistor. It was found during testing that the inductance provided by the leads of the through-hole component was essential to limit the pulse current to the mezzanine board in the event of an HV breakdown. On the mezzanine board, there are two stages of series resistors and back-to-back diodes to ground. The  $20\ \Omega$  value of the series resistors was chosen as a compromise between increased series noise and pulse current reduction. Finally, the MDT-ASD chip itself contains integral protection diodes to limit input transients. With this protection scheme the MDT electronics were demonstrated to be robust against an indefinite number of full HV discharges.

Each ASD chip processes signals from eight MDT tubes, providing eight LVDS outputs to the TDC. These LVDS signals are also available on a small header on the mezzanine board for diagnostics. The TDC time-stamps the output pulses of the ASD using a clock and an encoded trigger, which are received serially on two LVDS pairs from the CSM. The output data and a strobe signal associated with these data are also carried on LVDS pairs between the TDC and CSM. Finally, a calibration pulse trigger signal is received from the CSM on an LVDS pair, and is buffered, and distributed to the ASDs by the TDC.

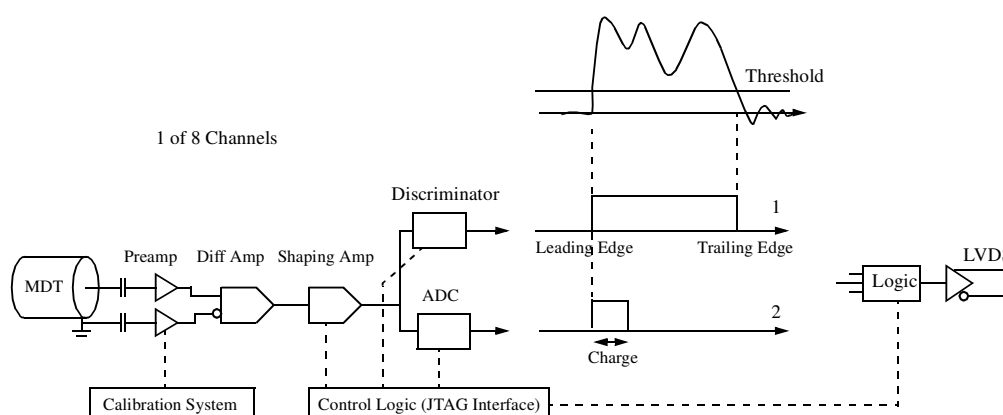
The programmable parameters for both the ASD and the TDC are initialized using the JTAG protocol. The three ASDs on each mezzanine board are connected in daisy-chain fashion, and are controlled by interface logic on the TDC. The TDC in turn is connected to a JTAG port controlled by the CSM.

A shielded ribbon cable with 20 twisted pairs connects the mezzanine board with the CSM transmitting the digital signals discussed above. A list of the cable lines is given in table 6. In addition to the digital data, four pairs of the cable are used to supply analog power to the mezzanine board and three separate pairs are used to for digital power. The cable also carries both voltage read lines and the signal from a TMP37 [27] linear temperature sensor on the mezzanine. These are digitized by ADCs on the CSM.

The analog and digital supply voltages  $AV_{dd_{in}}$  and  $DV_{dd_{in}}$  are supplied by a common source on the CSM. However, to minimize noise the corresponding grounds are kept separate, including separate ground planes for the digital and analog portions of the mezzanine board. Both analog and digital input power are each protected by a  $1.5\ \text{A}$  fuse and regulated at  $3.3\ \text{V}$  by an LP3964-3.3 linear voltage regulator [28]. The currents for the analog and digital supplies are  $0.27$  and  $0.13\ \text{A}$ , yielding a total consumption of  $1.6\ \text{W}$  at  $4\ \text{V}$  (for more detail on the power consumption see table 3 in section 1.3).

**Table 6.** Pin allocation of the mezzanine board. The resistance of the 40-wire cable is  $0.32 \Omega/\text{m}$  per wire. Cable lengths on most MDT chambers range from 0.33 m to 1.33 m. If CSMs are located outside the chamber (e.g. BIS, BEE) cable lengths run up to 5 m.

pin number		function	signal	destination
1, 3, 5, 7	2, 4, 6, 8	AVdd <sub>in</sub> (4 V); analog ground	DC	AVdd reg.
9	10	calibration strobe input to ASDs	LVDS	ASDs
11	12	temperature sensor; analog ground	DC	CSM
13	14	regulated analog volt. (3.3V); anlg. grd.	DC	CSM
15	16	regulated digital volt. (3.3V); dig. grd.	DC	CSM
17, 19, 21	18, 20, 22	DVdd <sub>in</sub> (4 V); digital ground	DC	DVdd reg.
23	24	master reset; digital ground	CMOS	AMT
25	26	serial data out from AMT	LVDS	CSM
27	28	system clock input to AMT	LVDS	AMT
29	30	encoded control input to AMT	LVDS	AMT
31	32	serial strobe out from AMT	LVDS	CSM
33	34	JTAG TMS	CMOS	AMT
35	36	JTAG TCK	CMOS	AMT
37	38	JTAG TDI	CMOS	AMT
39	40	JTAG TDO	CMOS	CSM



**Figure 15.** Block diagram of one ASD channel.

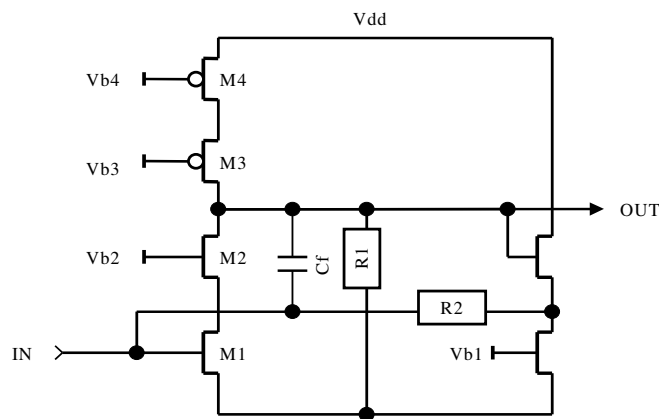
### 2.2.1 Amplifier Shaper Discriminator (MDT-ASD chip)

A block diagram of one of the eight channels in the MDT-ASD chip [29] is shown in figure 15 and its specifications are listed in table 7. Each channel consists of a differential input stage, a tail cancellation shaper, a discriminator, a gated integrator, output control logic and an LVDS output driver all running within a 3.3V supply.

The input stage is a pair of low noise cascode pre-amplifiers of moderately low input impedance ( $<100 \Omega$ ) for efficient charge collection from the relatively high impedance ( $383 \Omega$ ) MDTs. The

**Table 7.** ASD specifications.

Power supply	3.3 V
Pre-amplifier input impedance	100 $\Omega$
Pre-amplifier noise resistance	< 100 $\Omega$
Discriminator time walk	< 500 ps for the entire input signal range
Pre-amplifier peaking time	approximately 5 ns
Power consumption	30 mW per channel $\rightarrow$ 240 mW per chip
Channels per chip	8
Minimum pulse spacing of ASD output	10 ns



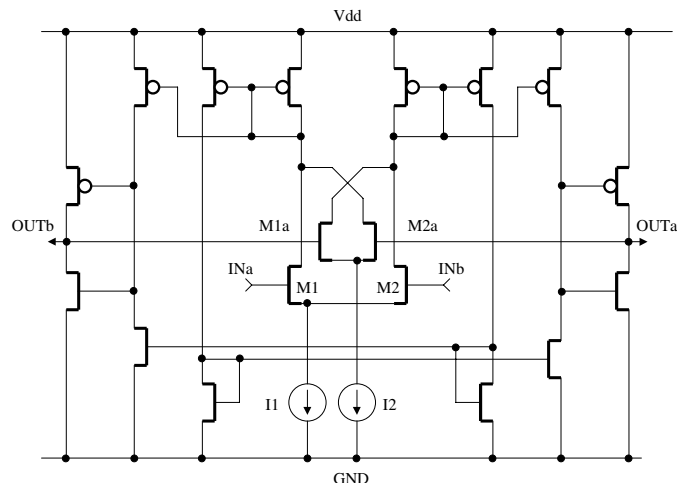
**Figure 16.** Cascode pre-amplifier schematic.

pre-amplifier shown in figure 16 is a low-noise design such that the noise of the system is dominated by the terminating resistor at the far end of the drift tube. The differential input provides high common-mode rejection of noise pick up at the input.

The tail cancellation shaper is a two-stage pole/zero network, which also provides the gain necessary at the discriminator input. Each pole/zero stage is characterized by a pole/zero ratio, which is fixed by design, and a single programmable time constant. Thus changes in drift gas composition can be accommodated within certain limits. In response to a delta function test pulse, the signal peaking time at the discriminator input is in the range of 10-12 ns.

The discriminator is a three-stage design with programmable hysteresis as shown in figure 17. The shaper output is AC-coupled onto the differential pair (M1, M2). Two current mirror "loops" provide differential outputs, which are converted to low-impedance outputs by inverters at OUTa and OUTb. Positive feedback is provided by pair (M1a, M2a) with a programmable current source (I2) which allows for adjustable hysteresis. This design provides fast switching and a time walk which is <500 ps over the dynamic range of the MDT signals.

The gated integrator is controlled by a one-shot which is initiated by the switching of the discriminator and covers the leading edge of the pulse. The charge contained in the leading edge is stored on a capacitor and then run down by the usual Wilkinson technique. The gate width is of



**Figure 17.** CMOS discriminator with programmable hysteresis.

order 8-45 ns and the rundown of order 100 ns to provide approximately seven bits of resolution. This time-encoded charge is used off-line as a correction for time slewing and enhances the leading-edge spatial resolution by about  $20 \mu\text{m}$ , as shown in figure 8.

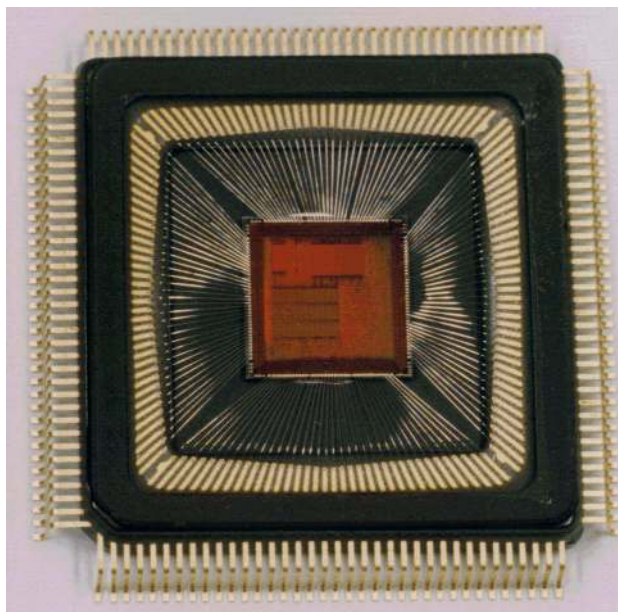
The output logic block shown in figure 15 provides two modes of operation. The first mode is time-over-threshold (TOT mode) where the output logic signal is forced high as long as the MDT shaped signal is above a fixed threshold. Ideally, this starts on arrival of the first few electrons at the anode wire and ends shortly after the last electrons arrive from the tube wall. In practice, the clumpiness of the primary ionization results in multiple crossings of the discriminator during this time. In the second mode of operation (ADC mode) the fixed current rundown of the charge on the capacitor of the Wilkinson integrator determines the width of the output pulse.

The criteria for selecting one of the two options are the following:

- At the start-up of the experiment when data rates are low, the leading and trailing edges (TOT mode) can be used. The correlation of the trailing edge and the bunch-crossing time is useful for checks on trigger matching and relative timing of different tubes.
- Once the system is understood, achieving optimal spatial resolution is the main goal. At this stage, ADC mode will be appropriate with leading-edge timing and the charge being read. At the nominal LHC luminosity this mode of operation will be used.

The programming of the ASD is done via a JTAG serial string that is passed from the CSM via the TDC chip. The following parameters can be adjusted: discriminator threshold and hysteresis, Wilkinson ADC gate width and discharge rate, dead-time, channel mode (active, held high, off), chip mode (TOT or ADC), calibration channel mask and calibration pulse height. More details on the setting of these parameters can be found in the ASD Users Manual [29].

This ASD chip was developed using the MOSIS fabrication service. The prototype chips were submitted to the *HP*  $1.2\mu\text{m}$  and *HP*  $0.5\mu\text{m}$  n-well processes. The latter process was used for the final device.



**Figure 18.** Photograph of the AMT-3 chip.

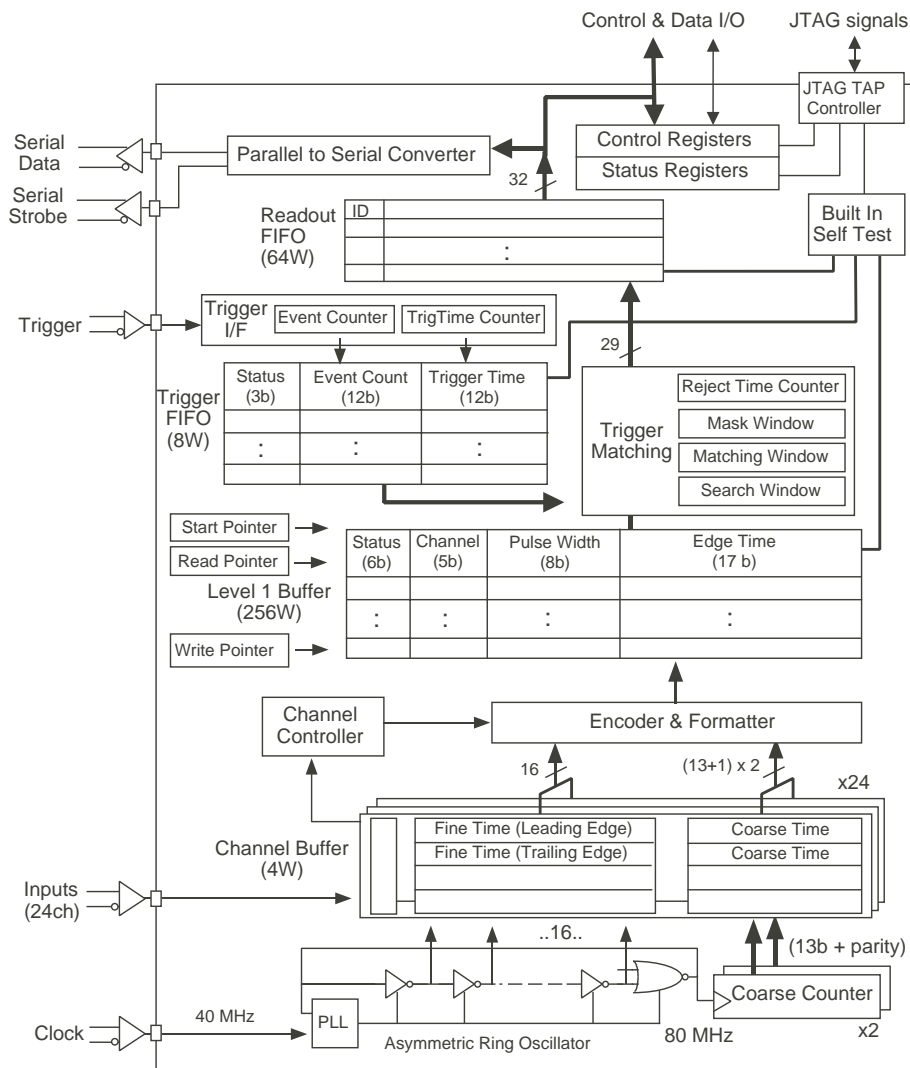
### 2.2.2 Time to Digital Converter (AMT-3 chip)

The AMT-3 (ATLAS Muon TDC) chip as shown in figure 18 was fabricated in the Toshiba 0.3 micron CMOS gate-array process (Toshiba TC220G). It performs the required time measurements on 24 channels coming from three ASD chips. Design requirements [30] and Production Readiness Review documents [31] are available for the AMT-3 as well as a detailed chip description and operating manuals [32–34]. Figure 19 shows a block diagram of the AMT-3 chip. The buffering scheme is entirely data driven to avoid large amounts of memory per channel. The AMT specifications are summarized in table 8.

The AMT has a PLL (Phase Locked Loop) circuit which generates an 80 MHz clock from the 40 MHz LHC clock. A voltage controlled oscillator (Asymmetric Ring Oscillator) in the PLL consists of 16 stages of variable delay elements. Gate delay variations as function of process parameters, temperature and supply voltage are stabilized with the PLL. Sixteen timing signal taps, with a delay of 0.78 ns per stage, are derived from the oscillator. Resolution of the time measurement is shown in figure 20 and is about 250 ps, which includes a digitization uncertainty of 226 ps.

Time measurements on a channel are stored in a channel buffer which is four words deep and capable of storing two leading and two trailing edges or four leading or trailing edges. At the output of the channel buffers, leading and trailing edges are paired and written to a common Level-1 (L1) buffer (256 words deep).

The Level-1 trigger information from the central trigger processor enters the AMT-3 via a trigger FIFO which is eight words deep to accommodate multiple triggers arriving within a short time interval. The AMT-3, being data-driven, collects all pulse edges as they arrive independent of its current trigger state. Trigger signals are required to arrive after all hits are collected and stored in the L1 buffers. To provide for flexible hit selection, the AMT-3 contains programmable registers that specify the window for hit selection relative to the trigger arrival time.



**Figure 19.** Block diagram of the AMT-3 chip.

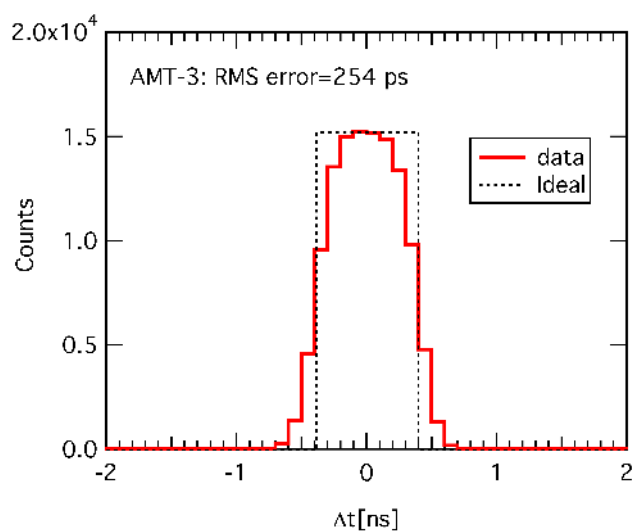
The association of hits stored in the L1 buffer to a given trigger is done via a matching function. The basic feature of this matching function is to search for hits within a trigger-specified time window. This time window is offset to begin at trigger-time and is adjusted to span the maximum drift time. The matching function can also look for hits in a time window preceding the matching window, which may be important for pattern recognition. The presence of any prior hits is signaled in a common output word which contains a flag bit for each channel. All time windows are programmable.

The matched data are stored in a readout FIFO, and are then transferred to the CSM using the serial data and strobe lines. Each serial data word has a one start bit, 32 data bits, one parity bit and two stop bits. The strobe line is either changed in each clock cycle, or changes according to the Data-Strobe (DS) protocol.

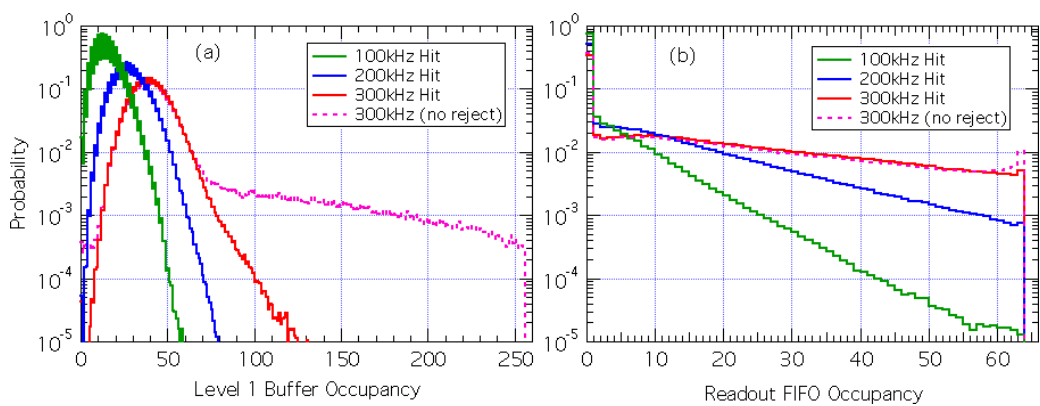
Initial setup and debugging are done using the JTAG protocol. There are 22 control and status registers, each with 12 bits. Many internal registers are also accessible via JTAG for debugging

**Table 8.** TDC Specifications.

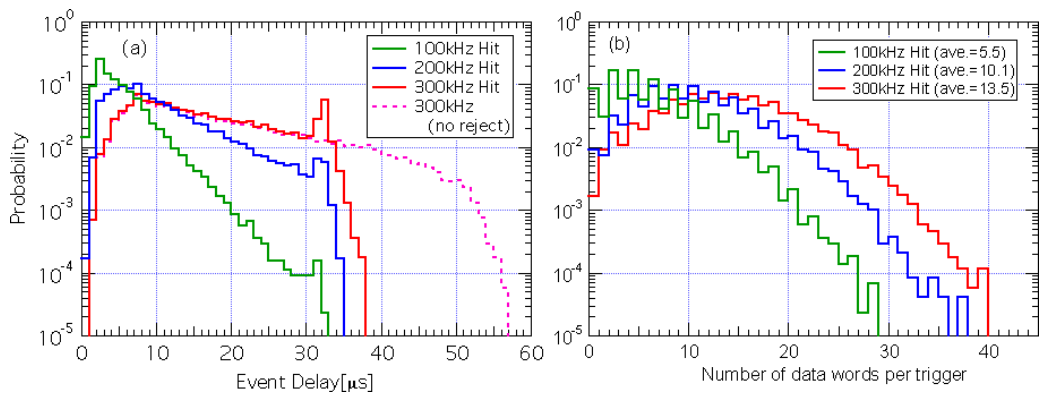
Technology	0.3 $\mu\text{m}$ CMOS Sea-of-Gate
Gate size	110 k gates used (300 k gates master)
Number of input channels	24
Signal input	LVDS (100 $\Omega$ termination)
Input clock frequency	40.08 MHz
Time bin size	0.78 ns/bit
Time resolution	250 ps RMS
Integral/differential non linearity	<80 ps RMS
Dynamic range	17 bits ( $\pm 50\mu\text{s}$ with trigger matching)
Minimum pulse width accepted	5 ns
Minimum time between pulses accepted	5 ns
Maximum rate where loss of data is negligible	400 kHz
Maximum trigger rate for negligible trigger loss	200 kHz
First-level buffer	256 words
Readout FIFO	64 words
Trigger FIFO	8 words
Serial output	10-80 Mbps, DS or Clock protocol
Parallel output	32 bits
Power supply	3.3 V
Power consumption	<15 mW/channel (<360 mW/chip)
Package	144 pin plastic QFP

**Figure 20.** Resolution of the AMT-3 chip.





**Figure 21.** Occupancy (words) of (a) the L1 buffer (256 words maximum) and (b) the readout FIFO (64 words maximum) for different MDT hit rates. The data have been simulated with a serial readout speed of 80 Mbits/sec and a trigger rate of 100 kHz. Old hits are removed from the L1 buffer when the readout FIFO becomes full. If this rejection feature is disabled, the occupancy reaches maximum L1 buffer size.



**Figure 22.** (a) Event delay (trigger to readout time) distribution and (b) number of data words (32 bits) per trigger for different MDT counting rates. The simulation conditions are the same as in the previous figure. The hit rejection feature reduces the maximum event delay to less than 40  $\mu$ sec. An average of 10 data words per AMT is expected at a hit rate of 200 kHz per tube.

purposes. Programming of the ASD chips is also done through the AMT-3 via the JTAG interface.

The AMT-3 architecture has been extensively simulated to investigate the possible loss of hits. A serial readout speed of 80 Mbits/sec was used along with a trigger rate of 100 kHz together with the standard output mode, namely each event includes a header and a trailer word plus a conditional mask word. Figure 21 shows the occupancy of the L1 buffer and the readout FIFO for different MDT count rates. The occupancy of the L1 buffer is reduced by enabling the rejection of old hits whenever a readout FIFO full condition occurs. This rejection feature is also important to avoid long event delays (trigger to readout time).

Figure 22 shows the event delay distribution and number of data words (32 bits) per trigger for different MDT count rates. The maximum delay is limited to less than 40  $\mu$ s with FIFO-full hit rejection enabled. The average number of data words is about ten at 200 kHz hit rate (which includes the 3 control words). The buffer becomes full for input rates greater than 200 kHz due to

the bandwidth limitation of the readout serial link. Data loss is about 0.7% and 5.3% for 200 kHz and 300 kHz hit rates respectively. This can be reduced by disabling the hit rejection feature, but this in turn increases the maximum event delay.

The AMT-3 architecture has also been simulated and tested to ensure that all hits within the programmed time window are appropriately digitized and sent to the CSM. If a buffer overflow does occur and one or more hits is lost, then a flag bit is set in the next TDC data word that is transmitted. The time elapsed between the previous good hit and a good hit with this flag set can be considered as a dead period for the TDC digitization.

The simulations described above were carried out using Verilog codes. The codes were initially written at the behavioral level, but eventually the tests were done with gate level codes corresponding to the actual AMT-3 chip. The same codes were also used in mass production testing to select good AMT-3 chips.

### 2.3 On-chamber multiplexer - Chamber Service Module (CSM)

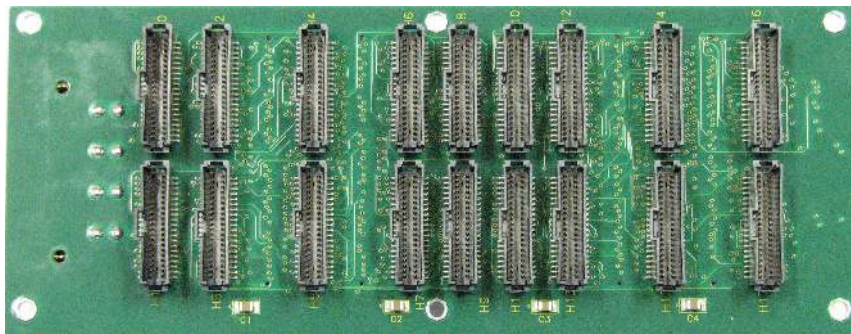
The on-chamber multiplexer known as the Chamber Service Module (CSM) is composed of a passive interconnect board and an active board which together have the following functions:

- Receiving the trigger, timing, and control signals from the TTC system.
- Delivering the TTC signals to all mezzanine boards.
- Multiplexing all serial data from the mezzanine boards to a single output stream.
- Delivering the output data stream to a gigabit fiber link connected to the MROD.
- Providing the ELMB monitoring function of voltage and temperature sensing.
- Routing the JTAG signals from the ELMB to the mezzanine boards.

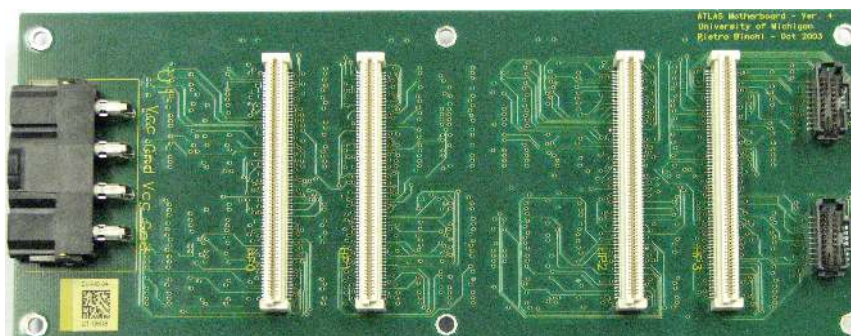
All connections to the active CSM board are routed through the passive board except the optical fiber connections from the TTC and to the MROD, which are made directly to the active board.

#### 2.3.1 The passive interconnect

The passive interconnect must provide for connection to the largest chambers which have eighteen mezzanine boards. These individual mezzanine boards are attached to the passive board via a high-density 40-pin twisted pair cable with 0.625 mm spacing. This cable delivers the supply voltage (nominally 4 V) to the analog and digital 3.3 V regulators on the mezzanine board, carries the 40.08 MHz crossing clock, the encoded commands to the board, receives the serial data from the AMT, and routes the sense lines from the mezzanine board voltages and temperature sensors to the analog multiplexer on the CSM, which is read out by the ELMB. Details of the signal allocation of the cable wires are given in table 6. The connections to the ELMB are opto-isolated and are provided by two ribbon cables with high-density 20-pin connectors mounted on the side of the interconnect board away from the chamber. This signal path provides for CSM initialization, conditions monitoring, and fault recovery. The passive board presents all signals to the active board, the actual CSM, via four high-density board to board connectors of 140 pins each. The interconnect board is shown in figure 23 and figure 24.



**Figure 23.** The passive interconnect board rear showing the eighteen mezzanine board connectors.

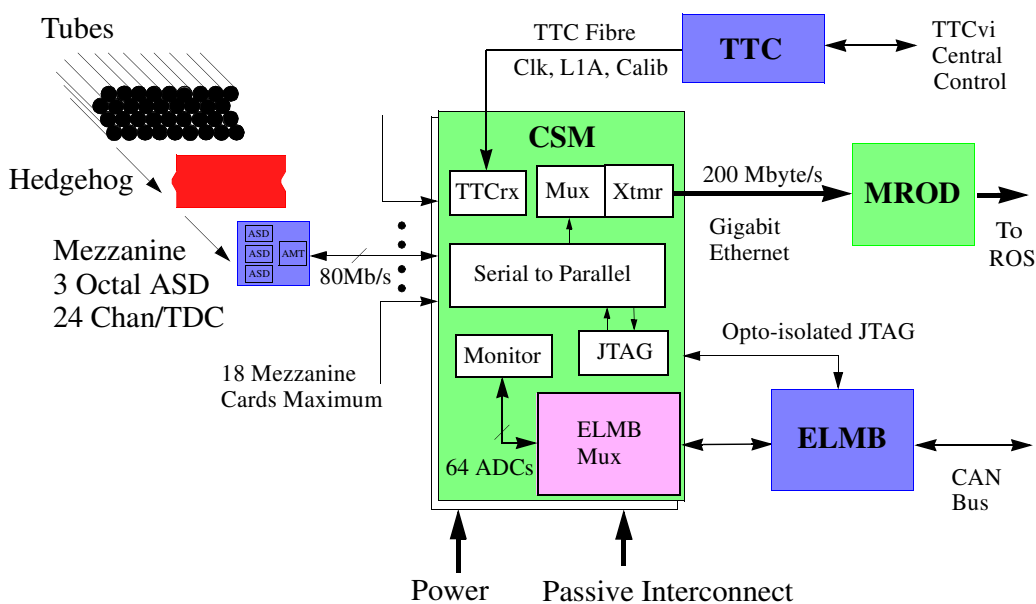


**Figure 24.** The passive interconnect board top showing the board to board connectors that route the mezzanine board signals to the active CSM. Power enters the passive board through the 4-pin connector at the left and is directed to the CSM and all mezzanine boards. The voltage supplied to the CSM is approximately 4 V, and an eighteen mezzanine board chamber draws about 8.3 A.

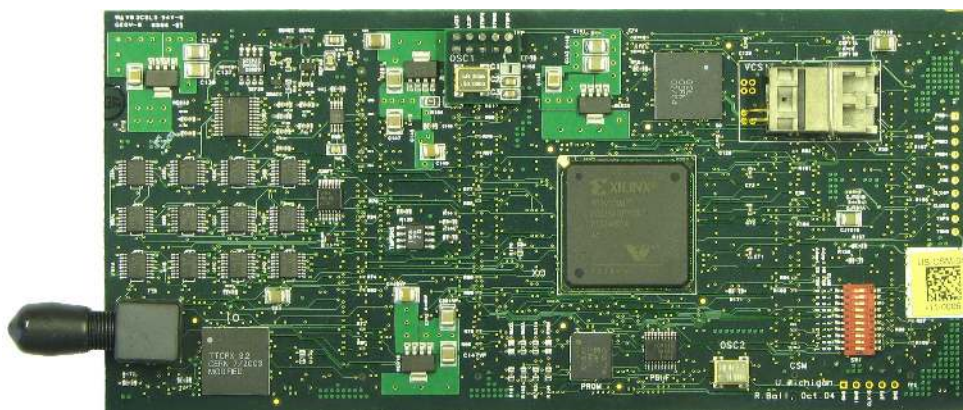
### 2.3.2 The active CSM multiplexer

The active CSM, represented in the block diagram of figure 25, incorporates:

- A medium-sized FPGA
- A TTC optical receiver and its TTCrx decoder chip [35]
- A gigabit optical encoder chip (GOL) [36]
- A VCSEL laser diode optical transmitter [37]
- Several voltage regulators
- 10 MHz and 50 MHz oscillator chips
- A PROM for FPGA configuration
- Several TTL fanout chips for JTAG control signals
- A 64-channel analog multiplexer to measure voltages and temperatures on the CSM and mezzanine boards



**Figure 25.** A block diagram of the on-chamber multiplexer showing its relationship to the mezzanine boards, ELMB, TTC, and MROD. Except for the TTC fiber and the fiber to the MROD all connections to the CSM are through the passive interconnect.



**Figure 26.** A photo of the CSM showing the TTC fiber connector at the left and the MROD fiber connector at the right. The medium sized Xilinx FPGA in the center provides the multiplex function and the cluster of small chips on the left constitutes the analog multiplexer for voltage and temperature monitoring.

- Opto-isolators to isolate the CSM ground from that of the ELMB.

A photo of the CSM board is shown in figure 26.

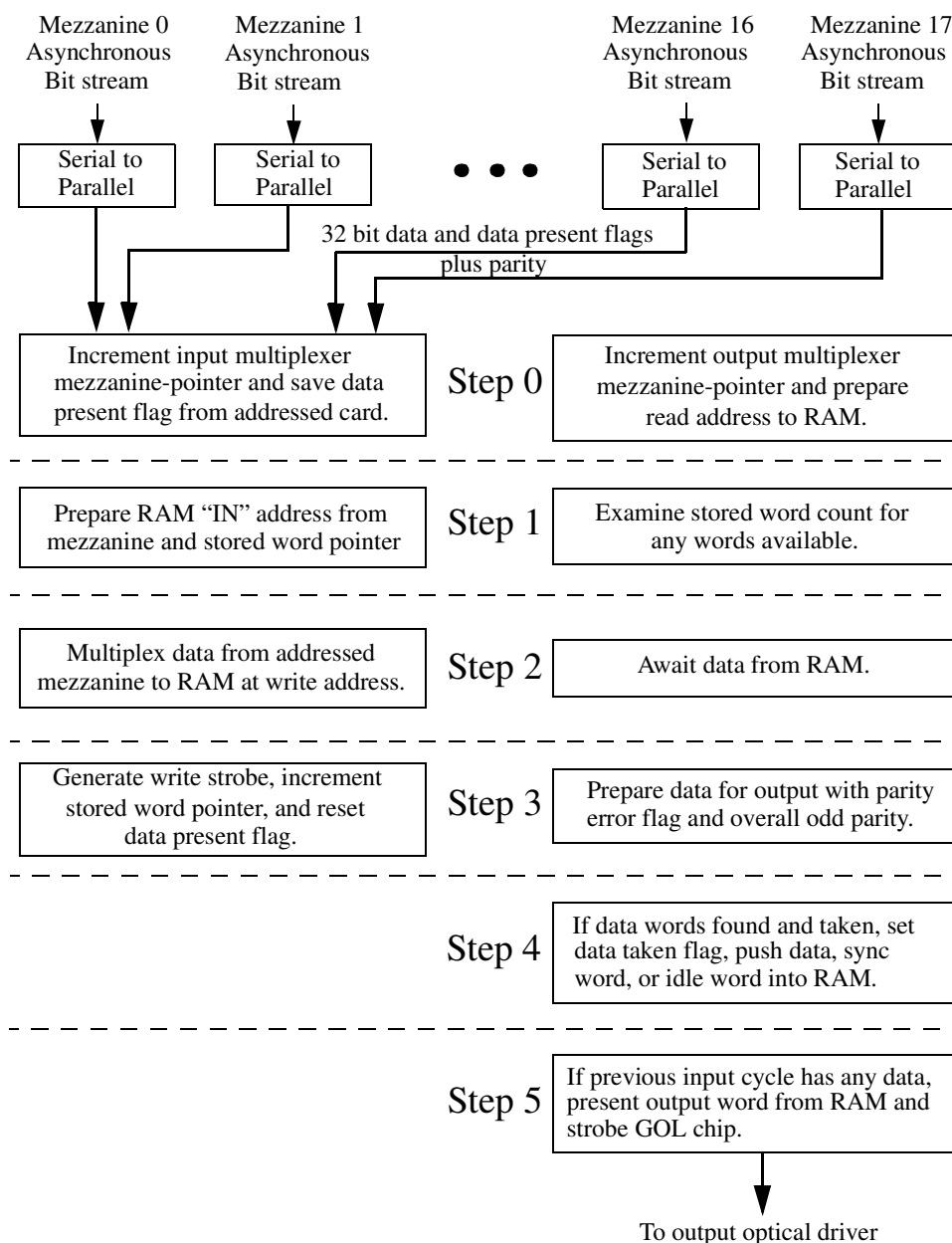
The active multiplexer has been implemented in a Virtex-II FPGA, coded in VerilogHDL, and simulated for various trigger and data rates [38]. The internal design and output bandwidth of the CSM has been arranged so that all data from up to eighteen mezzanine boards can be processed without data loss. The output bit rate of the AMT-3 operating at 80 MHz requires  $0.45 \mu\text{s}$  to transfer a data word plus parity, start, and stop bits. These words (eighteen maximum in 32 bit

format) are delivered to the MROD in eighteen time slots along with a synchronization word and two words of optical link idle codes. With the CSM to MROD link operating at a 50 MHz 32 bit word rate, these 21 words can be sent to the MROD in  $0.42 \mu\text{s}$ . With modest buffering, no data loss due to buffer overflow is possible. The trigger to readout latency is mostly due to the AMT-3 and serial link speed. However, the six pipeline processing steps of the CSM and the polling design of the output sequencing implies an additional contribution to the latency of approximately  $0.5 \mu\text{s}$ . Transmission delay in the approximately 100 m long optical fiber between the chamber-mounted CSM and the MROD in the electronics cavern will also add to the latency.

The CSM has two modes of operation, an asynchronous 40 MHz bit rate from the AMT coupled with a 25 MHz 32 bit word rate to the MROD or 80 MHz bit rate from the AMT with a 50 MHz 32 bit word rate to the MROD. In both cases no data loss is possible since the output rate can accommodate the sum of all eighteen (mezzanine boards) input rates with sufficient margin. A small add-on board with a 50 MHz crystal oscillator was added to the CSM to accomplish operation at the higher speed. (The board is labeled “OSC1” and can be seen at the upper edge of the photo in figure 26.) Normal operation will be at this higher rate. If a 40 MHz bit rate from mezzanine boards is sufficient to handle the data from chambers at large radius from the collision point, the 50 MHz frequency can be divided by 2 in the FPGA. Only the end-cap chambers have been fully outfitted with add-on boards and can operate at 50MHz. CSMs without the add-on board must operate at the lower readout speed. CSMs with the add-on board can operate at either speed.

The CSM accomplishes its tasks in six pipelined steps as illustrated in figure 27. In the first step, eighteen independent circuits sample the eighteen incoming bit streams from the mezzanine boards and perform the serial-to-parallel conversion. The asynchronous protocol requires a single start bit, 32 data bits, a parity bit, and 2 stop bits for each data word from the AMT. The CSM contains two polling loops, one examining the input from the 18 mezzanine cards and one sequencing through the 21 steps of output to the MROD. A dual-ported RAM buffers the information flow between these multiplexers which run at different speeds. The polling loops are not synchronized but the higher speed of data removal than entry guarantees that no pileup will occur in the RAM. If no data is available from a mezzanine, nothing is stored. The output loop operates as time division multiplexer and must fill each time slot of the 21 word sequence. Thus, when no AMT data word is available from a given mezzanine board, a dummy word with a unique identifier is sent. In order to sustain synchronization of this polling cycle, the CSM inserts one word per cycle with a second specific identifier that indicates the start of a polling cycle. At the end of the polling cycle, the CSM inserts two words of optical link synchronization codes. The presence of these words guarantees that the optical transmitter and receiver will be resynchronized automatically after each polling cycle should it lose synchronization at any time.

The parameters of the CSM are loaded via JTAG protocol in a series chain that includes the on-board PROM containing the FPGA code, the FPGA boundary scan and the CSM constants. Under control of the CSM the series may additionally include the GOL boundary scan and parameters, the TTCrx boundary scan, and the JTAG strings of up to eighteen Mezzanine boards [13]. The TTCrx chip does not permit its parameters to be included in the JTAG chain. To load the TTCrx with the needed setup constants, the data are included in the CSM parameters and sent to the TTCrx with the CSM emulating a PROM when viewed by the TTCrx. The GOL parameters used are the default settings, therefore the GOL need not be included in the JTAG chain. For “cold start” programming



**Figure 27.** The steps in the CSM pipeline for both input and output polling. A dual-ported RAM provides for data flow between these loops which operate at different speeds.

of the PROM or FPGA, the ELMB can force the JTAG loop to include only the PROM and FPGA prior to a new firmware download of the CSM. The ELMB can also force a reload of the FPGA from PROM for a “warm start” of the CSM.

One important initialization step for the CSM involves providing the CSM with the choice of clock phase to be used to sample the incoming data from each of up to eighteen mezzanine boards. The AMT chips transmit their serial data based on the clock signal provided by the CSM. Mezzanine boards reside electrically at the end of cables ranging from 0.3 m to 5 m. The return

phase from each AMT is thus influenced by the length of the connecting cable. To accommodate this variation, the CSM forms four clock phases (0, 90, 180, 270°) from the outgoing clock sent to all mezzanine boards. The appropriate phase must be selected for each mezzanine board (AMT). The CSM provides two means for the selection of the best phase. It can be instructed to dynamically sample the data from each mezzanine board and select the candidate phase to use or it can be instructed to use a specific phase for each of the eighteen mezzanine boards.

In the first case, the CSM sends a few internally generated triggers to the AMT and examines the data arriving from each AMT, flagging where data transitions appear in the intervals between the four clock phases. When the triggered events are all received by the CSM, the flags are examined. Most often only one flag is set and the selection of interval is obvious. Since the delay of the returning mezzanine data can be arbitrary, returning data sometimes appears in two adjacent intervals. In this case the later interval is selected. This selection is chosen since for the synchronous flip-flops of the FPGA, setup time is required but hold time is not. Once the latest (or only) interval where transitions are seen is determined, the clock edge 180 degrees after the starting point of the interval is selected.

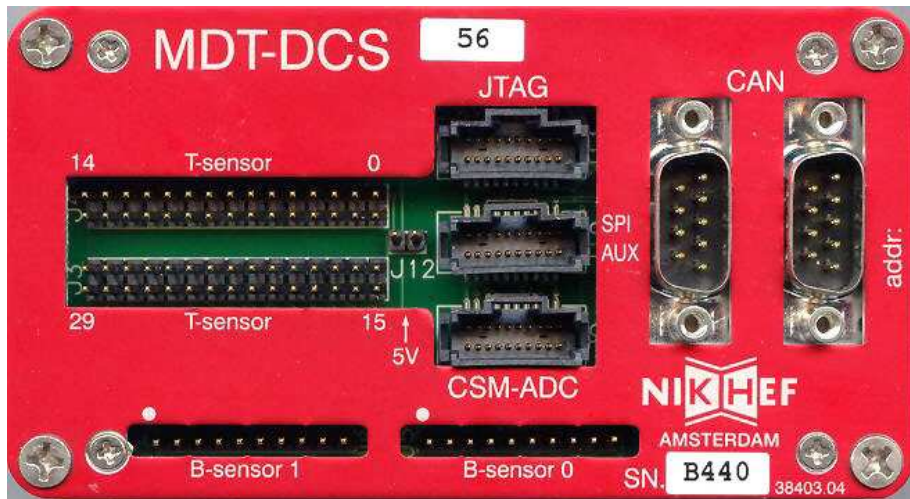
In the second case, the database is queried to provide the selection and the previously sampled and stored phase for each mezzanine board is transmitted to the CSM over JTAG. In all cases, the AMT is instructed to not send a clock with the data. This eliminates the returning data strobe as a source of crosstalk which might interfere with data sampling. Operation in the self synchronous mode is possible since the frequency of the AMT data is phase locked to the frequency of the clock signal provided by the CSM.

#### **2.4 Monitoring and control - Embedded Local Monitor Board (ELMB)**

Initialization, control, and conditions detection of the on-chamber electronics is handled by the Embedded Local Monitor Board (ELMB) [14]. An ELMB, plugged on a dedicated motherboard with connectors and installed in a metal enclosure is mounted on every MDT chamber. It is called MDT-DCS Module (MDM) and is pictured in figure 28. The ELMB processor is programmed with dedicated firmware as described in reference [13]. The unit provides initialization of the CSM by triggering the configuration load from an on-board PROM and by providing the parameter loading of the CSM and mezzanine cards via JTAG once the FPGA is programmed. The on-board PROM can be reloaded via JTAG if the need arises. The two ribbon cables connecting the ELMB to the CSM carry the JTAG signals together with other digital control signals. There are three encoded status bits presented to the ELMB by the CSM and four digital control bits input to the CSM. These four bits control the CSM reload from PROM, CSM reset, and JTAG loop control. Details of the JTAG instructions and registers are described in the CSM user manual [39].

To suppress noise pickup the active JTAG (TTL) signals are inhibited on the mezzanine cards during data taking. To accomplish this the JTAG chain within the CSM is configurable to include or exclude the mezzanine cards. The TTCrx and GOL chips can also be included or excluded from the chain although more for programming convenience than for noise reasons.

In addition, the CSM module contains a second dedicated 64 channel analog multiplexer for readout of the mezzanine card voltages and temperatures. This analog multiplexer is identical to the one of the ELMB. Some of these channels are also used to monitor the CSM voltages and temperatures. Readout through this multiplexer is controlled by the ELMB via an SPI bus [40]



**Figure 28.** The MDT-DCS module. It contains the ELMB processor, CANbus connectors, ribbon cable headers to connect to the CSM motherboard, and inputs from the chamber temperature and B-field sensors.

which uses five additional signal lines. The status bit interconnections between the ELMB and CSM provide for error monitoring within the CSM.

The DCS system via the ELMB monitors various mezzanine board and CSM voltages. These include mezzanine board digital and analog 3.3 V regulator outputs and the 3.3 V, 2.5 V, 1.8 V, and 1.5 V regulator outputs of the CSM. It also monitors temperature sensors on both the mezzanine board and the CSM.

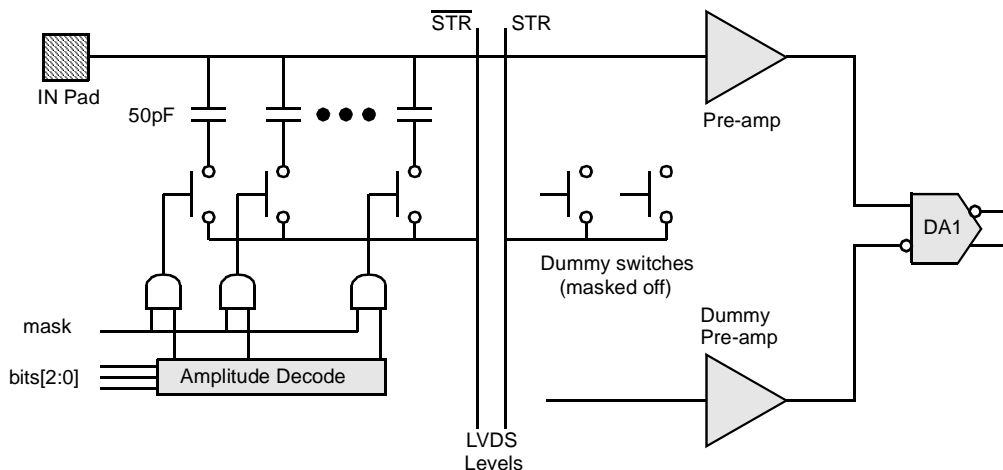
### 2.5 The calibration system

Time offsets between readout channels in the MDT system must be calibrated to better than 1 ns. For the 24 channels on a mezzanine board this can be accomplished by a combination of the TTCrx, CSM, and ASD chips. This is initiated through the TTC which provides a calibration signal together with a delayed Level-1 accept to the CSM. An LVDS signal is then routed to the ASD calibration circuits shown in figure 29, which results in calibration pulses being supplied to individual ASD inputs under the control of an 8 bit mask register. Each channel has 8 capacitors in multiples of 50 pF that couple the calibration pulse to the amplifier input. The amplitude decoder selects one of the capacitors and hence controls the magnitude of the injected charge. The channel mask and amplitude decoder bits are transmitted as part of the ASD JTAG string. This calibration procedure is also useful as an electronics system test.

### 3. On-chamber electronics support services and environmental factors

In this section the low and high-voltage systems associated with the on-chamber electronics components are described. This is followed by a discussion of radiation tolerance of the on-chamber electronics.





**Figure 29.** The MDT front-end electronics calibration system. A variable amplitude calibration pulse, derived from the signal labeled STR in the schematic, is introduced into selected ASD channels.

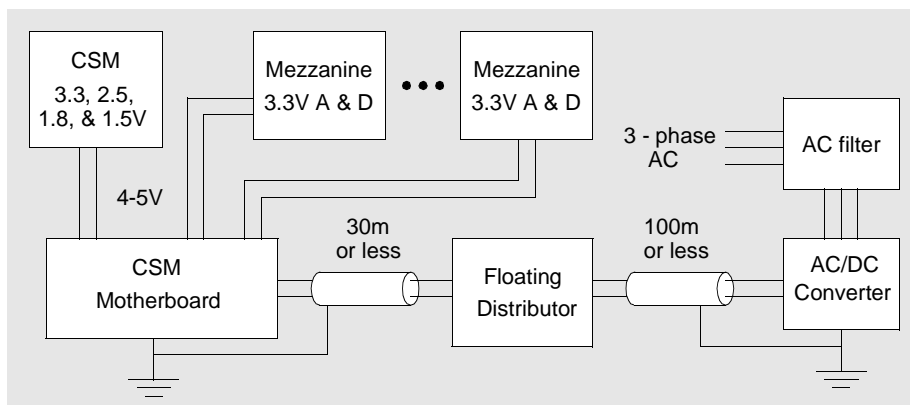
### 3.1 Low-voltage power

Low-voltage power is provided to the CSMs by distributors in electronics racks located on the galleries of the ATLAS cavern. The CSMs and mezzanine boards contain low-dropout linear voltage regulators which provide 3.3 V to the on-board electronics. The CSMs also incorporate 2.5 V, 1.8 V and 1.5 V power regulators. One distributor output supplies a pair of MDT chambers, consequently connecting their grounds, and is referenced to the chamber grounds at the CSMs. On each chamber the grounds of the regulators for the analog circuitry are connected to the Faraday cage at the mezzanine boards. The digital grounds are not attached to the analog grounds at the mezzanine boards but are referenced at the CSMs. This leads to ground differentials between analog and digital grounds of about 50 mV. The biggest MDT chamber, with 18 mezzanine boards serving 432 tubes, requires about 8.3 A, i.e. approximately 82 mW/tube at 4 V, excluding supply cable losses (see table 3).

The low-voltage supply chain shown in figure 30 is composed of three basic elements:

- DC/DC distributors, which have floating outputs and supply between 2 and 8 V and a maximum current per channel of 25 A.
- AC/DC converters, providing 48 V DC to the distributors from the 3- phase AC input. Each converter is composed of two 2.5 kW channels.
- AC filters, needed for correcting the power factor of the AC/DC converters. Each filter can serve two AC/DC converters via two 5 kW outputs.

The DC/DC distributors are remotely controlled and monitored. The distributors are exposed to magnetic field strengths of 200–1000 Gauss. This causes their power efficiency to be limited to about 70%. Because of the radiation levels in the cavern all DC/DC distributors have been certified for radiation tolerance according to the ATLAS rules [41]. The AC/DC converters and associated ADC filters are located in racks in an underground service area adjacent to the ATLAS cavern. The



**Figure 30.** Low-voltage DC power distribution. Three phase AC power is filtered and transmitted to AC/DC converters that output 48 VDC. The 48 V is then transmitted to DC/DC convertors called Distributors, that each provide approximately 5 V output to several chambers. At the chamber CSM a nominal value of 4 V is needed after resistive losses in the cables. From the motherboard, the unregulated but filtered 4V power plane provides input for CSM and mezzanine card regulators. The 3.3V analog and digital regulators on the mezzanine card are referenced to separate grounds. All voltages on the CSM are referenced to a common ground plane.

**Table 9.** Breakdown of the overall power consumption of the MDT system in kW. The power consumed at the MDT and lost in the cables is dissipated into the experimental hall, while the power supply overheads are evacuated by the cooling system of the racks.

Supply voltage type	LV/HV supply to MDT			48 V supply to the distributor				3-Phase pow. cons.
	MDT consumpt.	Cable loss	Overhead pow. supply	Total 48 V pow. cons.	Cable loss	Overhead 48V suppl.	Filter and AC/DC conv.	
Low (5 V)	29	4	14	47	6	4	7	64
High (3080 V)	1.5	0	0.5	2	0	9	1	12
<b>Total power</b>	30			49				76

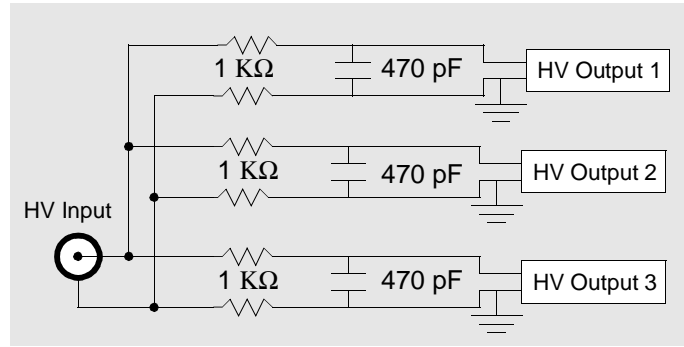
area is free from a significant magnetic field strength and screened from the radiation in the cavern. The efficiency of the AC/DC converters is close to 90%, not taking into account the internal current (“service current”) needed for proper operation, which is estimated to be about 20% of the total current.

About 10–15% of the power supplied is lost in the low-voltage cables ( $2 \times 8$  or  $2 \times 12$  mm<sup>2</sup> copper). The different contributions to the power dissipation are given in table 9.

All low-voltage power cables are shielded, the cable shields are grounded at the chambers to the CSMs. Separate insulated ground cables run from the chambers back to the racks containing the DC/DC distributors. The cables from the AC/DC converters to the DC/DC distributors are grounded on the AC/DC converter end. Finally, for safety, all the MDT chambers and their frames are attached to a large braided copper cable connected to the cavern ground.

### 3.2 High-voltage distribution

High-voltage and low-voltage power are generated in the same racks. The high-voltage chain [42] like the low-voltage chain is composed of AC filters, AC/DC converters and DC/DC distributors.



**Figure 31.** HV splitter section for 3-layer MDTs.

The nominal output of the high-voltage DC/DC distributors is 3080 V with a maximum current of 1 mA per channel. The contributions to the power dissipation from the high-voltage system are given in table 9.

One high-voltage distribution channel supplies one MDT multi-layer via a coaxial cable and is split at the detector into separate lines for the individual tube layers. This is done via a passive splitter circuit containing a low-pass filter to reject high frequency noise. The components of the splitter circuit shown in figure 31 are placed in a metallic box located close to the Faraday cage on the high-voltage side (opposite to the side with the readout electronics) of each chamber. The splitters have two identical sections, one for each multi-layer of a chamber. There are two types of splitters: one with one input and three outputs per section, which is used for the middle and outer MDTs. The second type has one input and 4 outputs per section, and is used for the inner MDTs. Each high-voltage line is filtered through a low-pass R-C filter of 1  $\mu$ s time constant.

The input and output high-voltage connectors are insulated from the splitter enclosure, which in most cases is attached to the chamber and its ground. In BIS and end-cap chambers the splitters are located off the chamber, and the enclosure is connected to the cavern ground. End-cap chambers have by construction a similar filter embedded into the Faraday cage which is in series to the splitter filter. The high-voltage cable shields, because of the floating outputs on the DC/DC distributors, are referred to the ground through the 1 k $\Omega$  resistors of the splitters. In the case of a wire short (“broken wire”) the HV supply channel will be automatically switched off after a period of 0.1 seconds making the complete multi-layer of 3 or 4 tube layers insensitive. By accessing the splitter box, the HV to the tube layer with the faulty tube can be disconnected, limiting the dead region to one tube layer. If the HV side of the chamber can be accessed, then the faulty tube alone can be disconnected from the HV bus on the hedgehog board.

Radiation tests of prototypes and pre-production DC/DC distributors have been carried out at the facilities in Louvain-la-Neuve, Casaccia and Uppsala [42]. Up to radiation levels of 14 krad (140 Gy),  $2 \times 10^{11}$  hadrons/cm<sup>2</sup> and  $2 \times 10^{12}$  neutrons/cm<sup>2</sup> (1 MeV equivalent) no malfunction was detected. Thus the requirements for radiation tolerance in the ATLAS cavern (see section 3.3.3) have been fulfilled.

**Table 10.** Irradiation doses and particle fluences in 10 years of LHC operation for the most important radiation types. The LHC is assumed to operate 1/3 of the time at the nominal luminosity ( $10^7$  seconds per year). Details of the three damage modes are given in the text. For the TID, the old unit *krad* is still used besides the official unit *Gray* (1 krad = 10 Gray).

		<b>TID</b> $\gamma$ 's <i>krad</i>	<b>NIEL</b> neutrons (1 MeV eq.) <i>units of <math>10^{11} \text{ cm}^{-2}</math></i>	<b>SEE</b> protons > 10MeV <i>units of <math>10^8 \text{ cm}^{-2}</math></i>
<b>Barrel</b>	center ( $ \eta  \approx 0$ )	0.18	0.4	1.1
	large z ( $ \eta  \approx 1$ )	0.22	0.6	2.2
<b>End-cap</b>	Small Wheel, large r	0.42	1.9	8.3
	Small Wheel, small r	2.0	10.3	23.1
	Big Wheel, large r	0.30	0.5	4.9
	Big Wheel, small r	2.0	0.9	11.4
	Outer Wheel, large r	0.15	0.4	0.9
	Outer Wheel, small r	0.26	0.6	0.9

### 3.3 Radiation tolerance of the front-end components

#### 3.3.1 Radiation levels in the MDT detector

The radiation in the ATLAS cavern is mainly caused by particles from the primary vertex interacting in the detector material or in the beam pipe. Particles at large angles (relative to the beam axis) face massive shielding in the calorimeters, in such a way that their contribution to the background in the cavern comes mainly from hadronic shower leakage and from particles escaping through the radial service ducts. In contrast, particles at shallow angles, hitting the beam pipe down-stream of the interaction point, are attenuated in a less efficient way, as the thickness of the forward shielding structure is limited by the available radial space. As a consequence, the energy spectra and particle rates in the cavern are quite non-uniform. In the forward region, around the end-cap toroid, the energy spectrum for neutrons and charged particles is harder and the overall particle rates (including  $\gamma$ 's) are considerably higher than in the barrel. Thus, MDT chambers at the inner edge of the Small and Big wheel (EI and EM-chambers) are exposed to up to 10 times higher  $\gamma$ -rates and up to 20 times higher neutron and proton rates than MDT chambers in the barrel. A detailed description of shielding strategies and simulated dose rates in ATLAS is given in ref. [43]. Irradiation doses and particle fluences at various MDT locations are listed in table 10 for the three radiation types known to be most harmful to electronic circuits. For the estimates of the total radiation doses it has been assumed that during ten years the collider is operated 1/3 of the time (corresponding to about  $10^7$  sec of operation per year) at the nominal luminosity of  $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ .

It should be noted that about 10% of MDT chambers are located in the regions of high background (“hot regions”) and their performance under radiation is a critical issue.

#### 3.3.2 Damage scenarios in electronics devices

The damage mechanisms to electronics, resulting from the different types of radiation depend

mainly on the technology of the electronic devices, but may also vary among devices of a given technology, depending on the exact choice of design and process parameters. Radiation tolerance may even vary between the production batches of a given commercial chip. Each type of component used on the MDT chambers has therefore undergone radiation tests with a dose corresponding to ten years of LHC operation.

The main damage is caused by the following types of radiation:

- Irradiation with  $\gamma$ 's: Most of the  $\gamma$ -background is created by nuclear capture of low energy neutrons, yielding  $\gamma$ -energies in the 1 MeV range. CMOS devices are most sensitive due to generation of local charges in the gate oxide. Typical failure modes are malfunction due to reduced speed and destruction because of large dark currents and subsequent overheating. The Total Ionising Dose (TID) due to  $\gamma$ -radiation during 10 years of operation ranges from 0.2–2 krad (2–20 Gray), depending on the location inside the detector.
- Neutrons in the MeV range: Energetic neutrons create permanent displacement of atoms in the silicon lattices resulting in a reduction of gain in bipolar transistors and in a reduction of light output in opto-electronic devices. This damage mode is known as Non-Ionising Energy Loss (NIEL). The dose associated with this effect is specified in terms of the fluence of 1 MeV neutrons. For ten years this quantity ranges from  $4 \times 10^{10}$  to  $10^{12}$  neutrons per  $\text{cm}^2$ .
- Energetic charged particles: Here protons play the most important role, as muons and pions are less frequent, while electrons are less penetrating and therefore less harmful. Protons above 10 MeV may generate sufficient ionisation in a single event to change the logic status of a memory cell, creating a Single Event Effect (SEE), possibly resulting in a Single Event Upset (SEU). SEEs are generally not caused by the proton's energy loss but by slow secondaries from the proton's interaction with a silicon nucleus. Ionisation from energy loss and from nuclear interactions have to be added to give the TID. The dose associated with this effect is specified in terms of the fluence of protons. For ten years this quantity ranges from  $10^8$  to  $2 \times 10^9$  protons/ $\text{cm}^2$ .
- Darkening of optical readout fibers due to  $\gamma$  radiation: The fibers used in the MDT system consist of germanium doped silica with no phosphorous content, and have been shown to have minimal transmission degradation after radiation doses of up to 100 krad.<sup>2</sup>

### 3.3.3 Levels of test doses and test results

The uncertainty of the simulated background levels is due to the error on the scattering cross-section at the primary vertex, estimated to be about a factor of 1.4 and to the error on the particle transport through the detector, which in turn is due to uncertainties on material composition, nuclear cross-sections and errors of the geometrical description. The error on the particle transport is estimated to be a factor of 2.5. The resulting total simulation error of 3.5 is considered a realistic estimate for the factor by which the radiation levels *observed* in the ATLAS cavern may well exceed the

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<sup>2</sup>Unfortunately a batch of radiation soft fibers was mistakenly installed on the EM chambers. We plan to replace these fibers during an early detector maintenance period.

**Table 11.** Radiation tolerance tests of CMOS components for the MDT frontend electronics. Tests marked "OK" have passed the requirements defined in reference [41]. The LP3964 circuit is a voltage regulator for 3.3 V, used on the mezzanine cards and on the CSM. The SN65LVDS179s are lvds drivers and receivers. AMTs and CSMs returned to normal operation after accelerated ageing, see text.

	TID		SEE	
	<i>krad</i>	<i>remark</i>	<i>prot./cm<sup>2</sup></i>	<i>remark</i>
ASD	300	OK	$4 \times 10^{13}$	$<1 \text{ SEU} / 10^{12}$
AMT	30	OK	$2 \times 10^{12}$	$1 \text{ SEU} / 10^{12}$
	45	leak. curr. incr.		
	70	no function		
CSM board with all components	30	curr. increase	$3 \times 10^9$	$1 \text{ SEU} / 10^7$
	45	funct. failure		
ELMB, SRAM ELMB, registers	14	OK	$10^{12}$	$1 \text{ SEU} / 10^9$
				$1 \text{ SEU} / 10^{11}$
LP3964	60	OK	does not apply	
SN 65LVDS179	300	OK	does not apply	

simulated ones. All electronic devices must therefore be tested up to the simulated value given in table 10 times the "safety factor" of 3.5.

For some device types the test dose must be incremented by additional factors. Thus, damage from TID in CMOS devices is known to show some dependance on the dose rate, low dose rates creating potentially more damage than the high dose rates used at the irradiation facilities, where a 10 year dose is usually applied in about one hour. The effect of the low dose rate can be simulated, however, by accelerated ageing, whereby the devices under test (DUT) are kept for one week at 100° C. The performance after this treatment is considered to correspond to the one after 10 years of LHC, i.e. at very low dose rate. If accelerated ageing was not applied, the uncertainty due to the dose rate effect would have to be accounted for by an additional safety factor of 5 [41].

As for commercial components where users have in general no control over production processes and reproducibility, an additional factor of 2–4 is assumed, as the device under test (DUT) may originate from a different production batch than those finally used in the experiment. For ASICs, where all devices usually come from the same production batch, this factor needs not to be applied.

The standard ATLAS procedure for testing the radiation tolerance of electronics is described in [41] and [44].

The radiation test results with  $\gamma$ 's and protons on the front-end electronics components of the MDT readout are presented in references [45, 46, 33, 47]. For the ELMB these results, also including neutrons, are described in [14, 48]. Table 11 gives a summary of the results. All listed components, except for the opto-couplers in the ELMB, are CMOS devices, for which the required test dose is obtained from the maximum expected TID (2 krad) multiplied by the simulation error 3.5 and the dose rate correction factor of 5, resulting in a test dose of 35 krad to be tolerated by the DUT.

The general result of these tests was that most DUTs start to draw excess current between 30 and 40 krad and fail to operate in the range 50 and 80 krad, a finding which is confirmed in other tests of CMOS electronics used in the muon spectrometer, cf. [49] and [50]. An exception is the ASD chip, which did not show any current increase or malfunction up to 300 krad when the test ended. The CMOS technology with which this chip was implemented (see section 2.2.1) was optimized for radiation tolerance [45, 46].

The CSM, showing current increase already at 30 krad, appears to have passed the test only with a narrow margin. However, accelerated ageing, as defined above, restored functionality and brought the current back to the pre-irradiation value. Consequently, the radiation tolerance of the CSM is assured, even in the detector regions with the highest radiation levels. Like for the CSM, the AMT devices returned to normal operation after accelerated ageing.

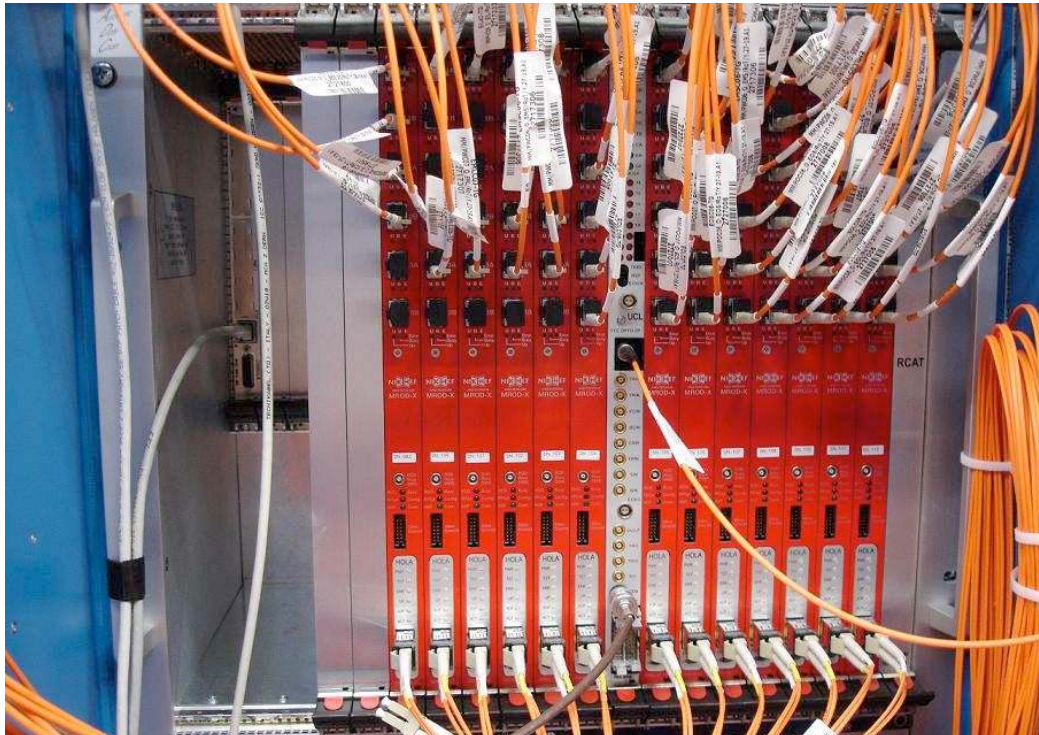
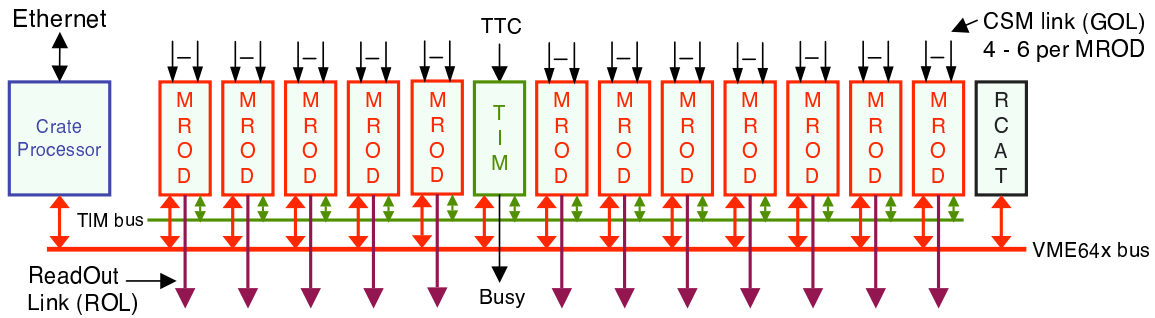
The SEE tests done with proton beams in the range of 70–230 MeV showed that SEUs are negligible for the ASD, AMT, ELMB and the commercial components. For the CSM the number of SEUs is well measurable and reproducible [47] and amounts to about 1 SEU/10<sup>7</sup> protons, which corresponds to about one SEU per  $5 \times 10^5$  seconds of LHC operation in the “hot regions” (at the tip of small and big wheel, cf. table 10) and to about 10<sup>7</sup> sec in the rest of the detector. It has been estimated that only about 1 in 90 SEUs in the FPGA may lead to a disruption of the DAQ, most of the SEUs affecting only data words or unused regions of the FPGA. In summary, only about one DAQ disruption in *one* of the 1118 CSMs is expected per hour, in which case a reload of the FPGA configuration from its local Flash-PROM would be necessary. (Flash-PROMs are known to be completely insensitive to SEUs). Triple modular redundancy (TMR) methods are prepared in order to push this failure rate even lower. Alternatively, a method called scrubbing can be applied, in which the FPGA configuration is permanently compared to its image in the Flash-PROM. If a discrepancy is detected, a correction can be made without interruption of the DAQ.

Tests with neutrons are generally not required for CMOS circuits. Yet, the AMTs and the LP3964 voltage regulators have been tested up to 10<sup>13</sup> neutrons cm<sup>-2</sup> without any observed malfunction. For the ELMB the current transfer ratio in the opto-couplers (Agilent, HCPL-0731) decreased by up to a factor of 10 after  $2 \times 10^{12}$  neutrons cm<sup>-2</sup> and 10<sup>12</sup> protons cm<sup>-2</sup>, but the ELMBs were still operating inside specifications [48].

## 4. Off-chamber electronics - MDT Read Out Driver (MROD)

### 4.1 Functionality

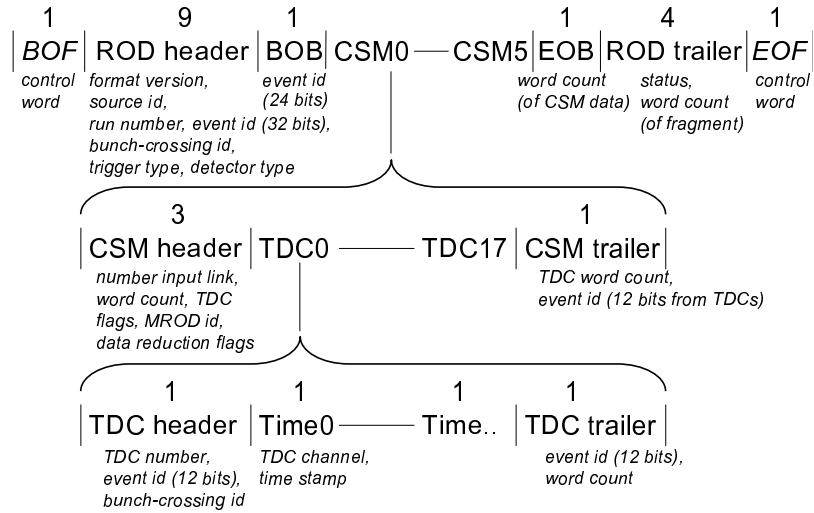
The main task of the MROD [15] is to receive the data streams from up to six CSMs, which in most cases together form a “tower”, i.e. the hits associated with the track of a single muon occur for a large fraction of the muons in the chambers outputting data to a single MROD. In this way the number of requests for MDT data generated by the Level-2 trigger for a muon “Region of Interest” is kept low (of the order of one). Information from the trigger, timing, and control (TTC) system is also received. Figure 32 contains an overview of the connectivity of the MRODs. The MROD builds event fragments from the incoming time division sequences sent by the CSMs, detects and reports errors and inconsistencies in the data, where possible initiates corrective action, collects statistics and allows to “spy” on the data. Moreover, data reduction schemes are implemented.



**Figure 32.** Overview of connectivity of MROD modules. Twelve (as shown in the drawing), in some case thirteen modules (as shown in the picture), reside in a VME crate, together with a crate processor, a module for receiving TTC system information and outputting the Busy signal (TIM) and a module for reloading the flash memories in the MRODs (RCAT). The CSMs are connected via the optical fibres at the top, the fibres at the bottom are the ReadOut Links connecting to the ROB. The fibre connecting to the middle of the TIM module is the TTC fibre, the coaxial cable connected at the bottom transports the BUSY signal. Sixteen crates house in total 204 MROD modules.

Event fragments are output via the Read-Out Link (ROL), which is an optical link using S-Link [51] protocol and connecting to a Read-Out Buffer (ROB), from where the data can be retrieved by the Trigger/DAQ system [5]. The MRODs are physically located in a different underground area (USA15) than the detector itself, shielded from the radiation in the detector cavern. The design of the MROD is therefore not constrained by requirements on radiation hardness. The length of the optical fibers connecting CSMs and MRODs is of the order of 100 m.



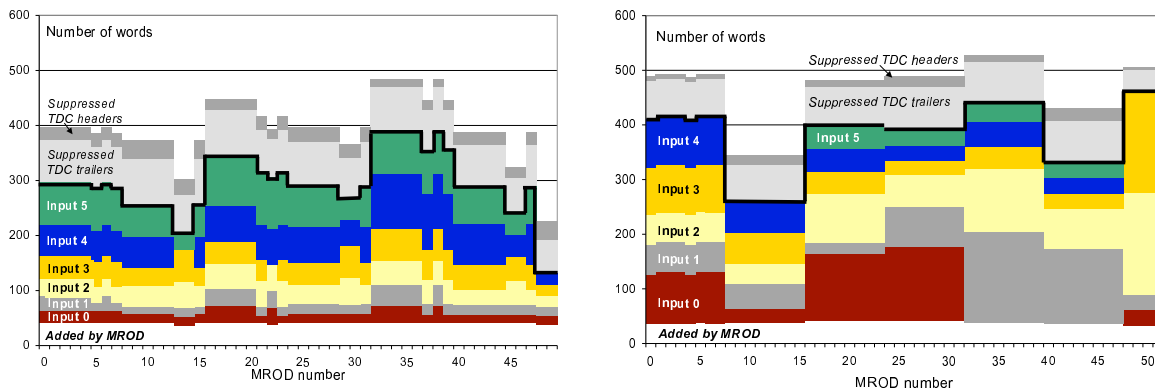


**Figure 33.** Organization of the data output by the MROD. The numbers specify the number of 32 bit words. The first and last word (BOF and EOF) are control words, which separate fragments and are not stored by the receiving ROB. Redundant information (event id’s, word counts) allows to check for errors.

The data sent by the CSM to the MROD over the optical fiber use Gigabit Ethernet protocol at the lowest level onto which 32 bit words are sent in a fixed length cycle of at maximum 21 words. As described in section 2.3.2, the first word is a cycle start word that has a fixed bit pattern, next follows for each TDC a single word with TDC data or in the case where no data is available, a placeholder word. The remaining two words are optical link words (IDLE words) to ensure link synchronization. Hence the length of the cycle is equal to the number of TDCs on a chamber (10–18) plus three words. The contents of the placeholder words are ignored by the MROD, the TDC data are stored and then assembled into event fragments, as described in section 4.2.1. The CSM output link (GOL [36]) either runs at a 1.6 Gbit/s or 0.8 Gbit/s net data rate (50 MHz or 25 MHz of 32 bit word transfers), see section 2.3.2. The MRODs automatically determine and set the correct clock frequencies under software control,

The event format for the MDT data is determined by the format of the output of the TDCs and the ATLAS ROD, and is described in detail in [52]. The format of the data output by the MROD can be visualized as consisting of three nested levels of “envelopes”, see figure 33. The lowest of the three levels is the TDC level. The next higher level is formed by the CSM level, whereas the highest level corresponds to a group of up to 6 chambers (i.e. MROD). Each envelope has the same basic structure: one or more header words followed by a number of data words and terminated with a trailer containing the word count for the envelope as a whole.

For the TDC and CSM levels, the respective trailers include a 12 bit event number. Envelopes may be empty, i.e. contain no data words. At each level the envelopes of the next lower level are fully included as data words in the envelope of the current level. The TDC envelopes are generated by the TDCs in the form of header and trailer words. In the absence of hits, a TDC sends an empty envelope for each Level-1 trigger to the CSM. Since the CSM is virtually transparent to the data, the CSM level envelope is generated by the MROD (MROD specific information is also added), as is the MROD level envelope. Empty TDC envelopes can be discarded by the MROD to reduce the



**Figure 34.** Estimates of the number of words per event and per input, for two words per hit, a background rate five times larger than the nominal rate and in the case where all TDC trailer words and TDC header words of empty envelopes are discarded. The plots are for the MRODs receiving data from the barrel chambers at one side of the interaction point (left) and from the chambers of one end-cap (right). The number of words added by the MROD is indicated, as well as the sum of the number of discarded TDC trailer words and TDC header words of empty envelopes. The thick lines indicate the average size of the fragments output by the MRODs. The correspondence between MROD number and MDT chamber type is given in reference [52].

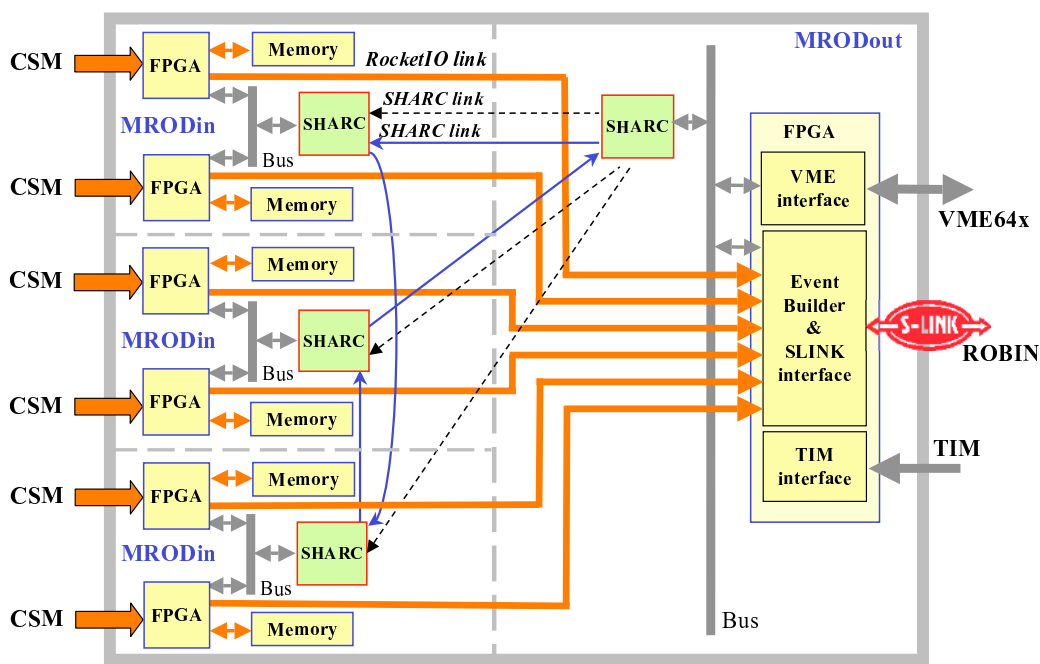
size of the event fragments output. The TDC trailers contain redundant information which can also be discarded by the MROD.

Figure 34 shows the estimated average number of words per event and per input if TDC trailer words of all envelopes as well as the header words of empty envelopes are discarded. The figure is for the case that two 32 bit words, i.e. two time stamps, one for the leading edge and the other for the trailing edge of the input signal (see section 2.2.2), are produced per wire hit and for a background rate five times higher than the nominal rate (see section 1.4), in combination with the maximum Level-1 trigger accept rate of 100 kHz. Only hits falling within a window of 750 ns after the time of the bunch crossing to which the Level-1 trigger corresponds or within a window of 100 ns before the time of that bunch crossing contribute. The latter hits only set a bit in the TDC mask word. The corresponding highest data rate is about 180 MByte/s or 1.5 Gbit/s.

## 4.2 Implementation

The MROD (figure 35 and figure 36) makes use of Xilinx Virtex-II Pro FPGAs [53] and of Analog Devices ADSP-21160 “SHARC” Digital Signal Processors (DSPs) [54]. Each FPGA has data links, eight RocketIO links, which each have a raw data rate of up to 3.125 Gbit/s. Each MRODin FPGA [55] connects with a RocketIO link (via an optical transceiver) to the CSM link and with a second RocketIO link to the MRODout FPGA [56]. A relatively simple approach with respect to fragment building is possible: the speed of the RocketIO links connecting MRODin and MRODout FPGAs is set equal to the speed of the MROD output link (1.6 Gb/s net data rate), so that fragment building in the MRODout FPGA basically consists of generating the correct envelope data words and of routing the output streams of the MRODin FPGAs one after the other to the MROD output link.

The SHARC DSPs run at 100 MHz and have an internal fast memory of 512 kByte and six half duplex data links. The links are used for fast point-to-point interconnections between the DSPs.



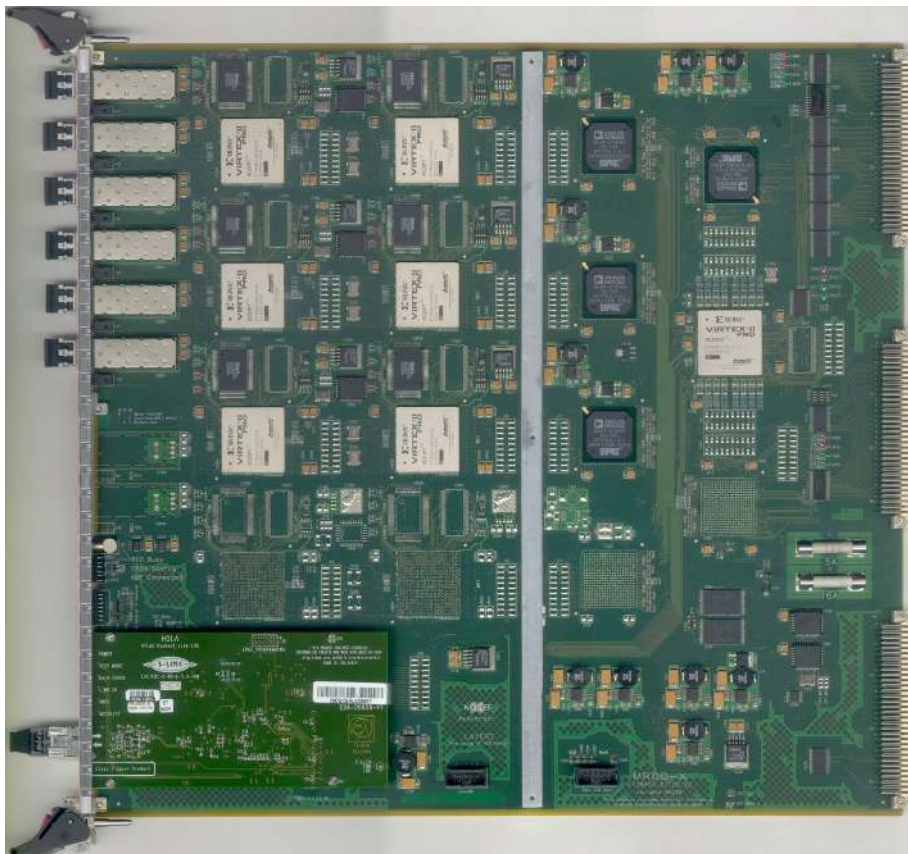
**Figure 35.** Schematic overview of the design of the MROD. Three identical “MRODin” sections are seen at the left, the “MRODout” section is at the right. Thick (orange) arrows running from left to right indicate the RocketIO links used for event fragment transfers. The dashed arrows indicate the SHARC links used to boot the MRODin SHARC DSPs. The thin (blue) arrows indicate the communication ring used to transfer messages between the SHARCs.

The maximum bandwidth per link is specified to be 100 MByte/s. However, for the MROD design it was found that reliable data transfers are only possible for link speed settings for which the bandwidth is a factor of two or more lower, i.e. the maximum bandwidth is 50 MByte/s. DMA controllers are associated with the links. Data transfers between the DSPs are automatically synchronized due to hardware handshaking across the links. The DSPs also have an external parallel bus with associated DMA controllers. The DSPs take care of initialization, control and error handling and can also be used to monitor the event data, as a programmable fraction of these data can be transferred to the DSPs [57].

The muon spectrometer is read out by 204 MROD modules. These are housed in 16 9U VME crates, with 12 or 13 modules per crate (see figure 32). Each crate has its own crate controller running a Linux operating system. Each crate also has a dedicated interface to the central Timing, Trigger and Control (TTC) system [10] of ATLAS and to the Busy logic in the form of a TTC Interface Module (TIM) [58]. The TTC signals received by the TIM are distributed to the MROD modules via a custom backplane. This also routes the busy signals from the MRODs to the TIM module. The MROD asserts its busy signal if internal congestion is detected, caused e.g. by assertion of the XOFF signal of the ROL by the ROB downstream of the MROD (see section 4.2.3).

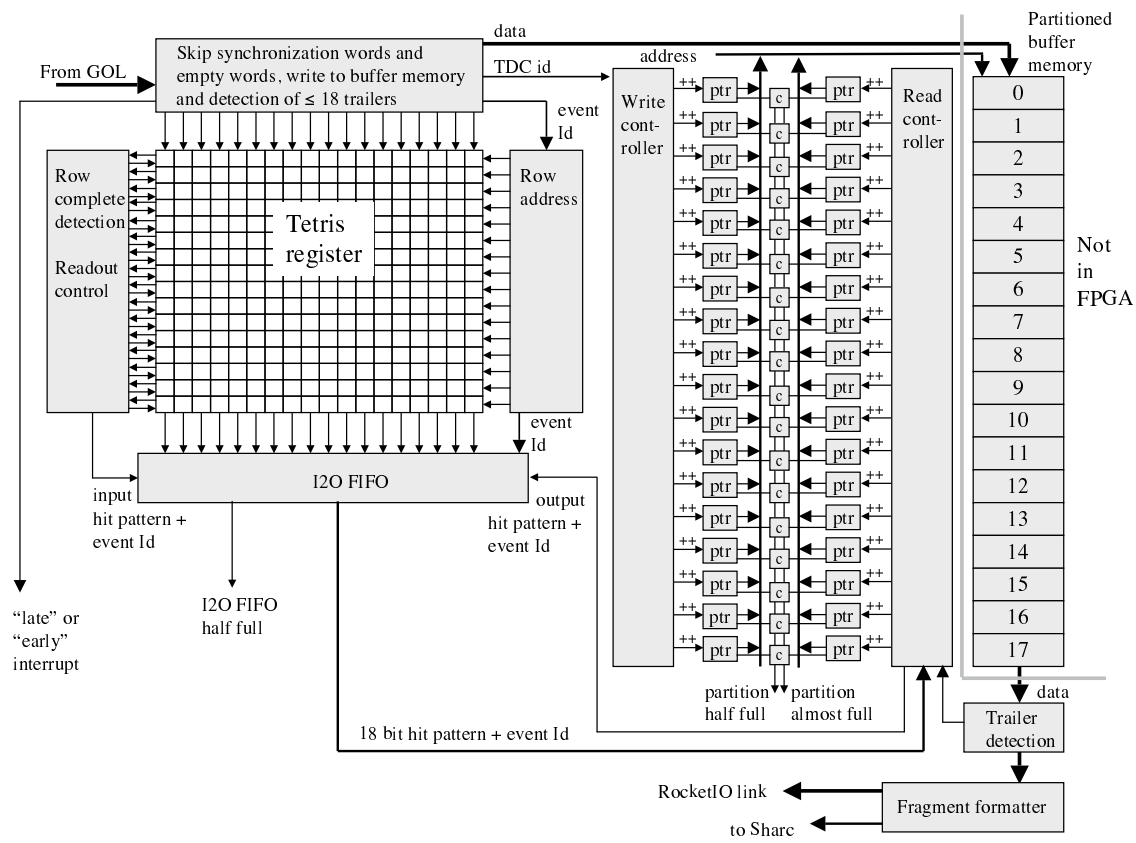
#### 4.2.1 The MRODin FPGA

The FPGAs of the MRODins (figure 37), clocked at 50 MHz, process the incoming data without any intervention of the MRODin DSP in the absence of errors. Each FPGA demultiplexes the CSM



**Figure 36.** The MROD board. Optical fibers from up to 6 CSMs are connected at the upper left. The metallic square integrated circuits are the FPGAs, those of the MRODin sections can clearly be seen at the upper and middle left, the MRODout FPGA is at the middle right. The large black square integrated circuits at the right of the reinforcer bar are the SHARC DSPs. In the lower part of the board an unassembled fourth MRODin section can be seen, as well as a location for a second MRODout SHARC. The daughterboard at the bottom left is the S-link source card to which the Read-Out Link is connected.

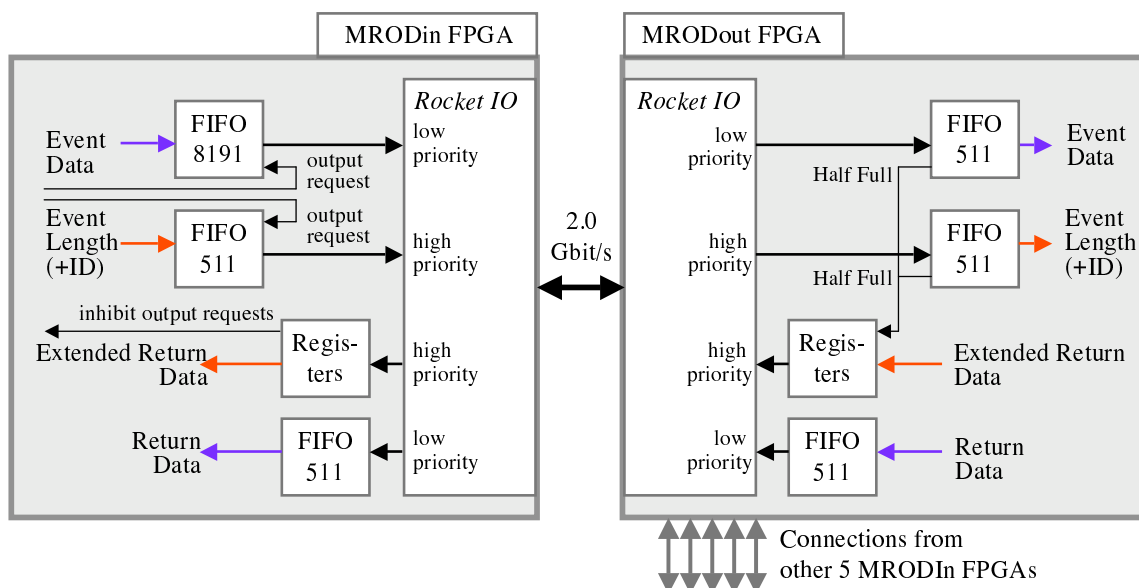
data and removes only placeholder words. For all other words, depending on the position of the word in the readout cycle, one of 18 registers (labeled with “ptr” in the figure) is selected to supply the address in the buffer memory to which the word is written. The buffer memory associated with the FPGA is a dual-port memory and consists of a “zero-bus turnaround” (ZBT) memory of 1 MByte, which can handle alternating read and write cycles without intermediate wait cycles, i.e. one write and one read cycle per 20 ns, corresponding to 200 MByte/s input and 200 MByte/s output bandwidth. Therefore uninterrupted streaming of data into the memory is always possible. The register contents is incremented each time a word is written to the buffer and is reset to its startup value after having been incremented 8191 times. In this way cyclic buffers of 8192 32 bit words are implemented in the buffer memory partitions. For a background rate five times larger than the nominal rate it is estimated that for TDCs handling the largest hit rates of the order of at least 500 events can be stored in these buffers. Under normal conditions the data is read from the buffer memory fast enough to prevent overwriting of data not yet read. Otherwise overwriting needs to be prevented by suppressing Level-1 triggers by means of the generation of a BUSY signal (see section 4.2.3).



**Figure 37.** Dataflow in the MRODin FPGA. Data arrives via the GOL (upper left) and is passed to the buffer memory after a filter and analysis step. The FPGA reads the data again from various partitions from the buffer memory once an event is complete, as detected with the help of the "Tetris" register. The data are passed, preceded by a header and followed by a trailer, via a RocketIO link to the MRODout (lower right).

The individual TDCs produce their data strictly time ordered event per event. However, the data streams of the different TDCs connected to a CSM are not necessarily in phase, while the event fragments to be output by the FPGA need to contain all data associated with the same event from all TDCs. A TDC trailer word flags that all data for the event (as indicated by the event number stored in the trailer) have been output by the TDC associated with the trailer word. In view of this the FPGA recognizes TDC trailer words "on the fly" and sets for each TDC trailer word received a bit in a two-dimensional bit array (in figure 37 labeled as "Tetris register"). The TDC number determines the column of the bit. The 4 least significant bits of the event number, extracted from the TDC trailer word, define its row.

An unexpected event number gives rise to an interrupt request for the DSP associated with the FPGA. Once all bits in a row (or a subset of the bits as defined by a mask) are set, the bit pattern, together with the lowest 12 bits of the event number is transferred into the "I2O FIFO". In case that not all trailers of up to 15 earlier events have been seen, the bit patterns corresponding to these events are transferred first to the I2O FIFO. Readout of the buffer memory is controlled by these bit patterns. The contents of each partition, indicated by the bit pattern, is read until a trailer word is encountered, incrementing for each read cycle the contents of the register supplying the address,



**Figure 38.** The RocketIO link between MRODin FPGA and MRODout FPGA and associated FIFOs.

with reset to the start value of the register contents after 8191 increments. Detection of the trailer word causes the start of the readout of the next partition. In this way a complete event fragment is built. Bits in a register control whether trailer words and/or empty TDC envelopes are skipped. A signal is generated if comparators (labeled with “c” in the figure) indicate for at least one partition that the cyclic buffer is more than half full or almost full. A bit mask controls which comparators are active, see also figure 40. Note that for this mechanism to work properly, it is crucial that each TDC sends at least the trailer word, even in cases when it has no data.

The MRODin FPGA checks for a number of error and exception conditions:

- parity errors on the TDC to CSM link (this parity is checked and errors are encoded in the data by the CSM, see section 2.3.2),
- link and/or parity errors on the CSM to MROD link,
- memory partition overflow,
- incorrect or too long event fragments from a TDC,
- absence of expected trailer words or corruption of trailer words, as mentioned above.

In case an error is detected, the FPGA may interrupt the DSP, which then reacts appropriately. For very serious conditions (too large event fragment, memory partition overflow, absence of data) the FPGA will independently decide to ignore (shut off) an individual TDC channel. This is flagged in one of the envelope words. Also in this case the DSP will be notified by means of an interrupt.

In the output stage of the FPGA the CSM level envelope is generated and the TDC data are enclosed to form the event fragment. The data can be output via a RocketIO link and/or a programmable fraction of the event fragments can be transferred to the internal memory of the MRODin DSP associated with the FPGA for monitoring purposes. Transfers to the DSP proceed

by way of DMA transfers, with handshaking between the FPGA and DSP. For each event fragment the FPGA passes one word, containing the length and the 12 bit event number of the event fragment, via a separate FIFO to the DSP. The availability of this “length word” indicates that all event data have been read from the buffer memory associated with the FPGA. Due to pipelined data handling, these data may not all have arrived yet in the DSP memory when the information in the FIFO becomes available. Transfers to the RocketIO link are processed likewise (figure 38).

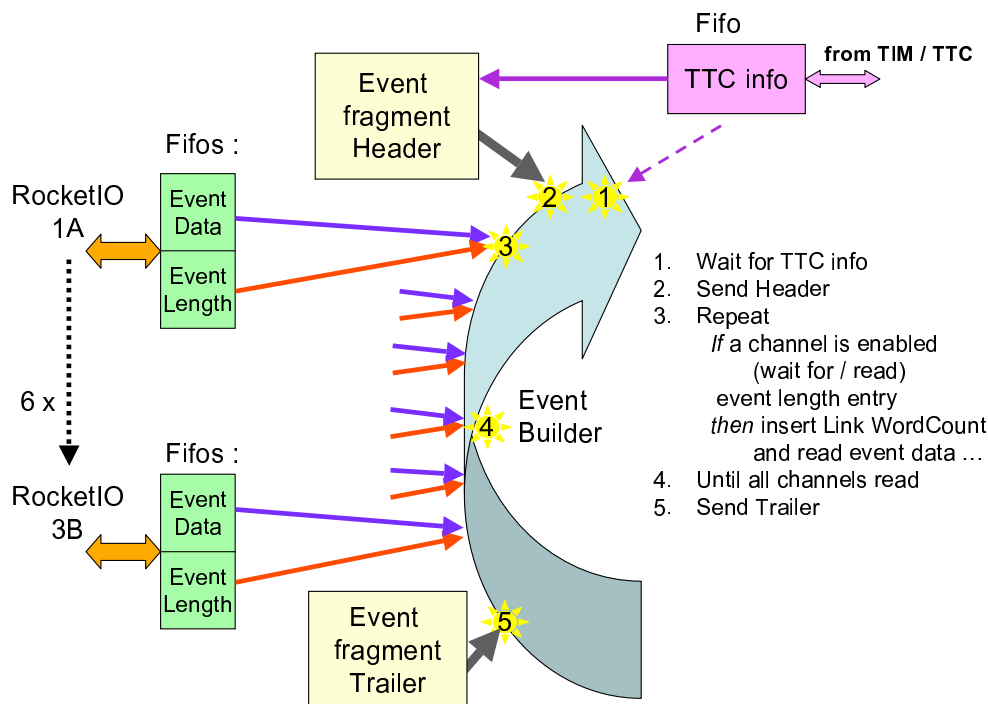
Event data readout from the buffer memory are stored in a 8191 words deep FIFO. After a fragment is stored, its length is known and stored, together with its event number, in a single word in a second FIFO of 511 words. This word is transmitted via the RocketIO Link as soon as possible and is preceded by a control word (available due to the use of 8B/10B coding), possibly interrupting the stream with the event data. The control word allows recognition in the MRODout FPGA of the arrival of this “length word”, which is stored again in a 511 words deep FIFO. The event data are stored in another 511 words deep FIFO. Activation of one or both of the half full flags of these FIFOs gives rise to the transfer of a word preceded again by a control word via the link from MRODout to MRODin FPGA. This results in an inhibit of the output requests for the FIFOs with event data and “length words”, i.e. of halting the data stream into the MRODout FPGA. Deactivation of the half full flags gives in the same way rise to removal of the inhibit signal. Support for passing data (“return data”) from MRODout to MRODin FPGA has been implemented, but is not used at present.

For each buffer memory partition the number of words between TDC header and trailer is truncated if larger than a programmable limit (default value: 96 words). Therefore, by appropriately choosing this limit a complete fragment can always be stored in the FIFO. This scheme assures that whenever a fragment length word is present in the FIFO at the receiving side of the RocketIO link, a complete event fragment is waiting to be read out from its corresponding FIFO.

Each MRODin FPGA contains a test generator that can be loaded with data by the SHARC DSP associated with the FPGA. It transfers data via an internal loopback connection to the GOL input, or via an external optical loopback fiber connecting to the (bi-directional) optical transceiver for the (uni-directional) GOL. The test generator can output the data loaded into it once or can be running in “circular mode”, in which the same event data is output repeatedly, while the 12 bit event numbers in TDC header and trailer words are incremented appropriately. This operation normally is triggered by the TTC system or by the trigger generator of the TIM module, but can also be free-running, and is enabled and disabled under software control by the SHARC DSP.

#### **4.2.2 The MRODout FPGA**

The FPGA of the MRODout interfaces to the VME bus, to the S-link interface and to the external bus interface of the MRODout SHARC DSP. For each event a header is passed to the 1024 words deep FIFO connecting to the output S-link, after which the event fragments transferred via the RocketIO links flow one after the other into the same FIFO (figure 39). At the same time the number of words in the event fragments is counted. Finally the word count is stored in the MROD trailer together with status and error information and output via the FIFO. In this way the building and output of a complete ROD event fragment is achieved. The error information in the MROD trailer consists of bits signaling whether a parity error has occurred (on one or more of the TDC-CSM links and on the GOL). It is also signaled whether a mismatch has been observed between



**Figure 39.** Overview of the event building mechanism in the MRODout FPGA.

the event id and bunch id stored in the TDC data and the event id and bunch id as received from the TTC (or as determined by the MROD (event id only) if used in test mode; the use of test mode is also signaled by a bit in the data).

The 50 MHz internal clocking of the MRODout FPGA and the reduced power dissipation with respect to 3.125 Gbit/s operation have led to a choice for the raw transfer speed of the RocketIO links of 2 Gbit/s (the net speed is 1.6 Gbit/s, due to the 8B/10B coding), i.e. equal to that of the output S-link. In practice, overhead in the MRODin has no effect, therefore the throughput of the MROD is approximately determined by the bandwidth of the output S-link (see section 4.3). The FIFOs associated with the RocketIO links increase throughput by reducing the likelihood of stalls of the data flow from RocketIO link into the output S-link. The FPGA also takes care of checks on error conditions, which again are handled by the DSP. A programmable fraction of the fragments output to the S-link can be transferred to the DSP for monitoring purposes, with the same mechanism as implemented in the MRODin FPGAs.

#### 4.2.3 The busy signal

Back-pressure exerted by the reception of an XOFF signal via the Read-Out link results in filling of the 1024 words deep FIFO associated with the link (figure 40). A full condition for this FIFO in turn results in filling of the FIFOs associated with the transmission of data via the RocketIO links between MRODin and MRODout FPGAs. An half full condition of the FIFOs for event data and “length words” at the receiving end results in filling up the 8191 and 511 words deep FIFOs (again event data and “length words” respectively) at the sending end. An almost full condition of these latter FIFOs in a MRODin FPGA results in halting the readout of the buffer memory associated with the FPGA. Still seven words can be stored in the FIFOs if the almost full condition is raised,



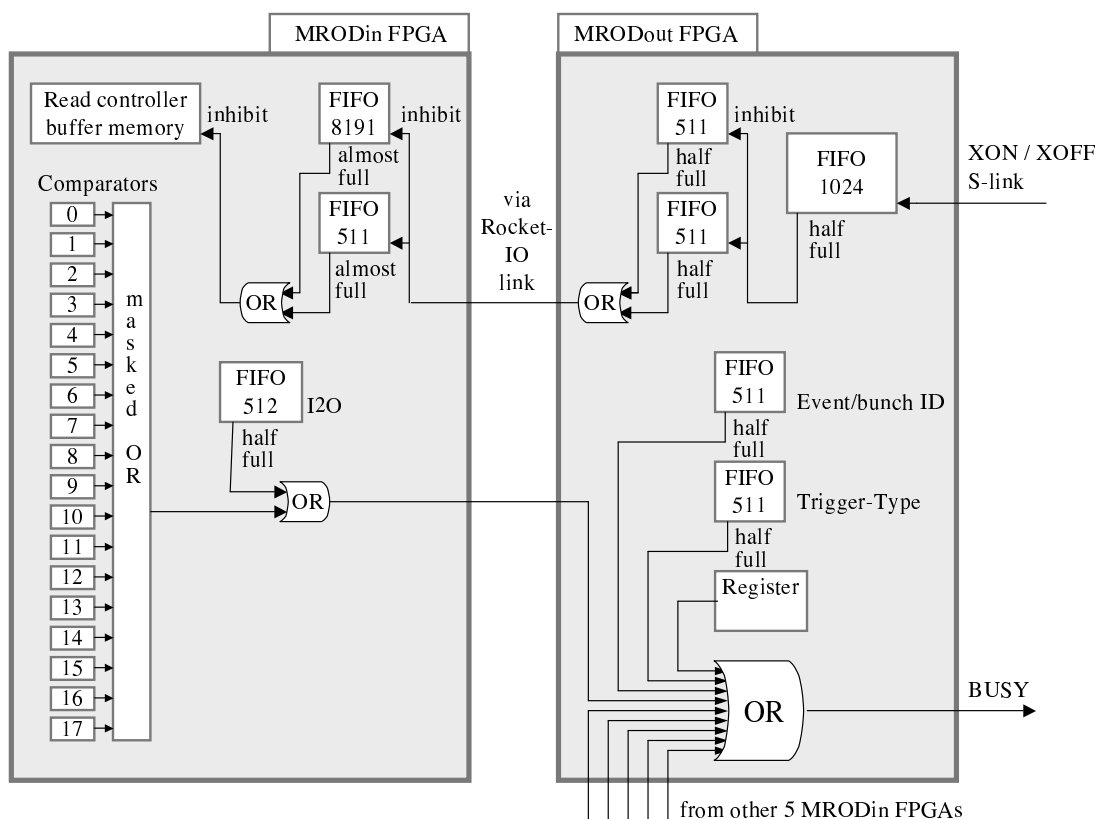


Figure 40. Busy signal generation.

so that the buffer memory readout pipeline can be emptied without loss of data. The partitions of the buffer memory will fill up once readout of the buffer memory is halted. A half full condition of any active partition is signalled by the comparators of read and write pointers associated with the partitions and will result in assertion of the BUSY signal which is passed to the Level-1 trigger system and should give rise to suppression of the Level-1 accepts. Other sources for assertion of the BUSY signal are the 512 word deep I2O FIFO of the MRODin becoming half full, the 511 words deep FIFOs used to receive TTC information in the MRODout FPGA becoming half full and a bit in a register that can be set under program control by the MRODout SHARC. The signal is available on a connector at the front panel and is passed to the TIM module via the dedicated backplane.

#### 4.2.4 Configuration of the FPGAs

The FPGAs are configured at power-on from on-board flash memories. The memories can be loaded via either a JTAG connection on the front panel or an addressable JTAG connection via the IEEE 1149.5 MTM bus [59] available in the VME64x P1 backplane. This latter connection is controlled by the crate processor, making remote reloading from the flash memories possible, with the help of a dedicated module, the Remote Configuration and Test (RCAT) module that connects to the MTM bus. The MROD modules are connected to the MTM bus via Addressable Scan Port (ASP) devices [60]. The address of each MROD is determined by the number of the

slot it is occupying. The RCAT module itself is driven by the crate processor via a USB port and a “Platform Cable USB” (USB compatible cable for in-circuit configuration and programming of Xilinx devices [61]). This cable is connected to the RCAT module with the help of the pass-through connections of the P2 backplane and of a simple board placed in the appropriate connector at the rear side of the backplane.

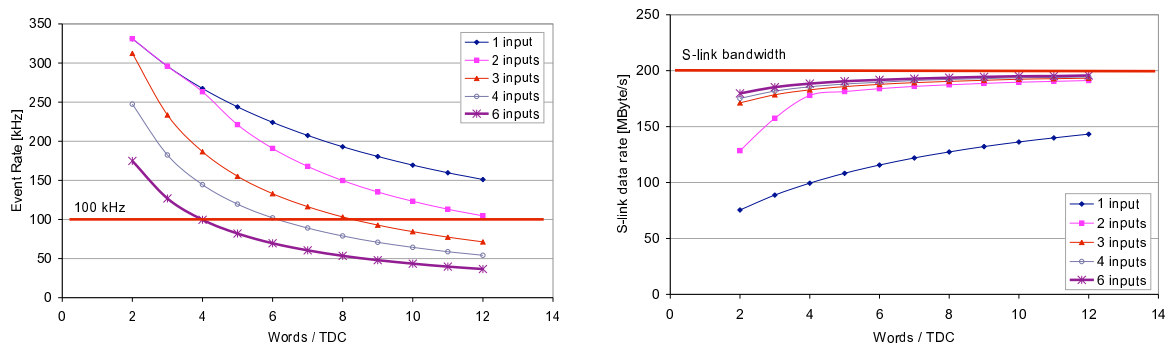
#### 4.2.5 Software environment

The MRODin DSPs are booted via the VME bus via their SHARC links (the dashed lines in figure 35). This is possible because the SHARC-link interfaces of the MRODout DSPs can be accessed directly from the VME bus. The MRODout DSP is booted via its internal memory, which is also accessible from the VME bus. The MRODs in a crate are under control of and communicating with the ROD Crate DAQ (RCD) software [62] running on the crate processor, which includes loader and communication functions. A communication mechanism has been developed and implemented which makes it possible to send messages to individually addressed DSPs, to broadcast messages to the DSPs as well as to send messages from any DSP to the RCD. The messages are transferred between the DSPs via SHARC links. Using these links a ring of interconnected DSPs is formed, via which data are always transmitted in one direction. The MRODout DSP communicates via its internal memory with the crate processor.

#### 4.2.6 Monitoring

A programmable fraction of the event fragments assembled by an MRODin FPGA can be transferred to the DSP connected to it. Likewise a programmable fraction of the event fragments built in the MRODout FPGA can be supplied to the MRODout DSP. In practice only the data from the MRODout FPGA are monitored. However, all four DSPs can still be involved in checking the data for correctness. This is achieved by transferring fragments via SHARC links to the MRODin DSPs. These are initially used to boot the MRODin DSPs, i.e. they are other links than those connecting the DSPs in an uni-directional ring network. The latter network is used to communicate results from monitoring to the MRODout DSP and subsequently to the crate processor via the VME bus.

The checking procedure consists of inspection of the event fragment structure as outlined in figure 33. The structure of each event fragment should be consistent with word counts in headers and trailers, while the event identifiers occurring in the various headers and trailers should be the same. Flags included in the data indicate which TDCs are read-out: changes in the settings of these flags should not occur during a run and are therefore also reported. The maximum event rate that can be handled by this checking procedure depends on the fragment size and on whether or not empty TDC envelopes and /or TDC trailers are discarded. This rate is not critical, as the data stream from the inputs of the MROD to its output during normal operation is not interrupted if the event length FIFO of the FPGA is not read out fast enough by the DSP. However, for debugging purposes the data stream can be halted, so that the processing speed by the DSP can limit the event rate. This mode of operation was used to measure the event rate that can be handled if all events are checked. The result was that under normal running conditions the four DSPs together can handle a rate of about 40 kHz, so checking about one in every three events would be feasible at the nominal maximum Level-1 accept rate of 100 kHz.



**Figure 41.** Maximum event rate and associated output bandwidth for the MROD as function of the number of words per TDC, with each active input receiving simulated data from 18 TDCs and for each TDC the same number of words.

### 4.3 Throughput tests

The throughput of the MROD has been measured with the help of the test data generators built in the MRODin FPGAs, see section 4.2.1. The test generators were triggered by a TIM and event data was transferred either via the senders of the bi-directional optical interfaces for the CSM links and via loopback fibers to the receivers of these interfaces (the CSM link itself is uni-directional, so the sender of the MROD optical interface is not used for normal operation), or via the internal loopback connection. The trigger generator in the TIM was throttled by means of the busy signal of the MROD.

The results of the measurements, presented in figure 41, show that handling of the event data in the MROD does not limit the rate, apart from an overhead caused by the MRODout FPGA: for each event, data can not be transmitted via the output link during  $18 + 2N$  clock cycles of 20 ns, where  $N$  is the number of active inputs. For 100 kHz event rate and  $N = 6$  this results in a maximum output bandwidth of about 190 instead of 200 MByte/s under the conditions of the test. The rate is limited by the overhead associated with the MRODin FPGA if only a single input link is used, and also for 2 or 3 words per TDC for two input links. In ATLAS at least four links per MROD are used and in this case the throughput is entirely determined by the bandwidth of the MROD output link and the overhead of  $18 + 2N$  clock cycles in the MRODout FPGA, as mentioned above.

## 5. System tests

When all system components were developed and tested, the performance of the complete readout chain had to be verified, operating one or more fully equipped chambers under conditions as close as possible to the ones in the final application. This was not possible in a single test setup, but the different performance aspects had to be tested in a number of complementary experimental arrangements.

The main performance parameters to be verified were:

- position resolution and noise behaviour
- high rate behaviour
- reliability of data transmission and operation
- certification of the JTAG based control via the DCS system

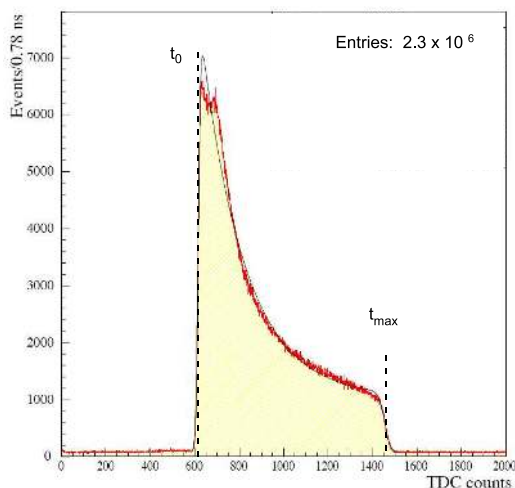
The corresponding tests were done with (a) cosmic ray setups at laboratories of the participating institutes, (b) in a high energy muon beam and (c) in a muon beam with accurate track definition in the presence of a powerful  $\gamma$ -source.

In the cosmic ray setups horizontally mounted MDT chambers are vertically stacked together with a scintillation counter telescope. For 3-layer chambers it is necessary to have multiple chambers in order to provide a position reference for the chamber under test, whereas a single 4-layer chamber can provide its own position reference. In high statistics runs with several million triggers (time scale of a day), wire position accuracies of about  $10\ \mu\text{m}$  could be achieved, allowing e.g. for the control of wire displacements away from the central position. This high accuracy of the position measurement required tight temperature control in the test area and optical control of chamber alignment. All chambers delivered to CERN were certified with this or similar methods. Comparison with wire position measurements obtained from X-ray imaging (“tomography”, see [63, 64]) showed good correlation for the wire displacement in a given chamber, confirming the high accuracy of the cosmic ray method. The noise measurements with and without HV applied to the chamber confirmed expected rates due to cosmic rays respectively inherent amplifier noise. Excessive noise of individual channels could in most cases be traced back to malfunction of the corresponding mezzanine card or to discharges in the tubes due to gas impurities. A general observation was that noise contributions from external sources (EMI) were negligible in the electrically quiet laboratory areas where the cosmic tests were performed. Details of the cosmic setups are described in [65].

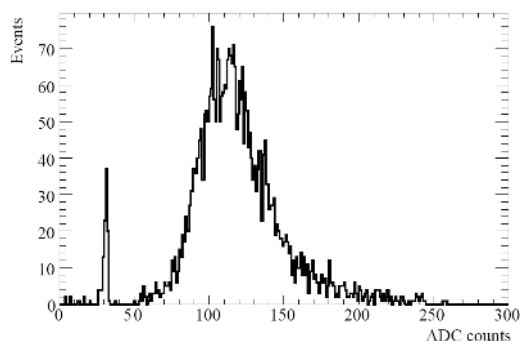
In the summer and fall of 2003 and 2004 six barrel and six end-cap chambers were tested in the high energy muon beam of the H8 test area at CERN. The readout chain included a prototype of the final MROD. Data were accumulated with a prototype version of the final DAQ system (“DAQ-1”). Unlike in the cosmic ray tests, the beam allowed for measurements with high hit rates in selected regions of the detector. Due to muon energies in the range 100–250 GeV, multiple scattering in chamber material did not play an important role. Chambers were aligned in pairs along the beam line, their relative location being monitored by a prototype of the final alignment system. The temperature in the ATLAS cavern varied by about 3–5° C between day and night.

The H8 tests confirmed resolution and noise measurements obtained earlier and allowed to test and improve operational control and readout stability at the system level. In addition a number of technical studies like resolution dependence on discriminator threshold and/or high voltage were done. The long term stability of “time zero”, i.e. the sum of all *constant* delays in the system due to cable length, circuit response etc. was verified to be better than one TDC count (cf. [66]). The correlation between temperature related displacements of the chambers, as observed with beam position measurements and optical alignment, was excellent and gave stable results during six months of operation. Detailed accounts of these tests are given in [67, 68].

To study the behaviour of MDT chambers at the high  $\gamma$ -background levels expected for the LHC, tests were done at the Gamma Irradiation Facility (GIF) at CERN. In this test facility  $\gamma$ -fluences are generated by a strong  $^{137}\text{Cs}$ -source ( $E_\gamma = 0.662\ \text{keV}$ ) in the presence of a 100 GeV muon beam. In order to measure the expected small track displacements of less than a few hundred microns, the position of the muon tracks was determined with a set of silicon detectors to an accuracy of about  $10\ \mu\text{m}$ . The degradation of position resolution due to space charges could thus be precisely measured and turned out to be in excellent agreement with simulation results. First



**Figure 42.** Drift time spectrum for tubes in a BML chamber as obtained in the H8 test of 2003.



**Figure 43.** Pulseheight spectrum from one tube in a BML chamber.

tests with a few tubes were reported in [9], while results on full chambers are presented in [19, 20]. At the nominal luminosity and the simulated background rate (including the safety factor 5 for simulation errors<sup>3</sup>) the average resolution of a MDT tube degrades from about 80 to 108  $\mu\text{m}$ , still inside the acceptable limits. The detailed resolution behaviour as a function of background hit rate is shown in figure 7.

Another consequence of high rates is the loss of hit efficiency due to the dead time of 750 ns (standard value), which enables background hits to mask subsequent muon hits. This leads to an efficiency reduction from 97% to 96% at nominal operating conditions and down to 91% at the high rates when the safety factor is applied.<sup>4</sup>

Reduction of the adjustable dead time to 200 ns improves the efficiency back to 97% for nominal conditions and to 95% with the safety factor of five. These improvements of efficiency, however, lead to an increase of data volume by up to about 50%. For the MDTs in the hottest region (cf. table 10) this brings the required bandwidth to about 50% of the available readout bandwidth.

To illustrate the performance of the system we show the two measurements which best characterize the performance of both an MDT chamber and its readout electronics, namely the distributions of the TDC values obtained with muon triggers and the corresponding ADC values. In figure 42 and 43 we show these distributions as obtained from a BML type chamber in the H8 test of 2003 [67]. The characteristics of the TDC plot is a steeply rising edge at  $t_0$  representing the muons which pass very close to the wire, and a broad distribution of hits extending to a less well defined  $t_{\text{max}}$  representing muons near the tube walls.

The distribution is peaked toward small values because of the non-uniform drift velocity in the Ar/CO<sub>2</sub> (93/7) gas mixture used in the chambers. The ADC plot shows a wide peak for the muon

<sup>3</sup>In addition to the simulation error of 3.5, discussed in section 3.3.3, there is a factor of 1.4, describing the uncertainty of the absorption process in the tube material and in the gas.

<sup>4</sup>The efficiency of a single layer of tubes is limited to about 97% because of the tube walls, the gap between adjacent tubes (“glue gap”) and the inefficiency of short track segments occurring when tracks pass very close to the wall.

hits which is well above the noise level.<sup>5</sup> Applying these ADC readings as a slewing correction to the drift time measurement leads to an improvement of the position resolution on the order of 20%, as shown in figure 8.

## 6. Conclusions

The MDT readout electronics system has been designed and constructed to achieve the high precision needed for the ATLAS muon spectrometer.

- The performance parameters of the system as well as its components have been thoroughly tested under realistic conditions and certified according to specifications.
- All MDT chambers in the ATLAS detector are now equipped with readout electronics and the full readout chain is operating reliably. The muon system is currently being commissioned using cosmic rays in the ATLAS cavern.
- Final conclusions on background rates, data volumes and long term radiation damage can only be drawn after the LHC accelerator has reached stable operating conditions at full luminosity.

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### A. MDT chamber specifications

Tables 12 and 13 summarize the parameters of mechanical structure and readout modularity for the chamber types in barrel and end-cap. More detailed information is available in reference [6]. The last two columns in the tables give the average chamber current (A) and the power consumption (kW) of all chambers, when chambers are operated at the nominal voltage of 4 V. The power dissipated in the supply cables is not included in these numbers.

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<sup>5</sup>The peak at 30 ADC counts is due to small noise pulses which fire the discriminator, but fail to trigger the Wilkinson ADC. This results in a default LVDS pulse width which digitizes to approximately 30 counts.

**Table 12.** Parameters of MDT barrel chambers. The direction along the beam is  $z$ , the azimuthal co-ordinate is  $\phi$ . Col. 5 gives the radial distance from the beam axis (mm). Most chamber types have subtypes with varying dimensions to fit between magnet coils, support structures etc. as is reflected in the number of mezzanine cards (col. 9). Dimensions given in col. 6 and 7 refer to the chamber subtype with the largest length along  $z$ . The BIS.8 and BEE have only one multi-layer. A BIS.7 and a BIS.8 as well as a pair of BEE chambers are served by one CSM each.

Chamb. type	Layer	No. of chamb.	Tube layers	Locat. in $R$	Length along $z$	Tube length	No. of CSMs	Mezz/ chamb.	Avg. curr.	Total power
BIS	inner	96	2 × 4	4550	1097	1671	96	10–12	5.2	2.0
BIS.7	inner	16	2 × 4	4550	1097	1671	8	10–12	5.4	0.35
BIS.8	inner	16	1 × 3	4620	496	851	8	2	1.8	0.12
BIL	inner	72	2 × 4	4949	1097	2671	72	8–12	5.4	1.6
BIM	inner	20	2 × 4	5373	1097	1536	20	12	5.9	0.47
BIR	inner	24	2 × 4	6056	1097	1536	24	8–12	5.2	0.50
BMS	middle	72	2 × 3	8095	1680	3071	72	8–14	5.7	1.65
BMF	middle	12	2 × 3	8095	2177	3071	12	12–18	7.2	0.35
BML	middle	94	2 × 3	7139	1697	3551	94	8–14	5.8	2.2
BEE	middle	32	1 × 4	4415	1457	912	16	8	4.2	0.54
BOS	outer	72	2 × 3	10569	2177	3773	72	12–18	8.1	2.3
BOF	outer	16	2 × 3	10675	2177	3773	16	10–18	6.7	0.43
BOG	outer	18	2 × 3	10675	1216	3771	18	10	5.1	0.36
BOL	outer	96	2 × 3	9500	2177	4961	96	12–18	7.4	2.8
Total barrel		656					624			15.7

**Table 13.** MDT chambers in the endcap. Col. 5 gives the location along  $z$  with respect to the interaction point, col. 6 the number of chambers radially mounted in a sector. The length along the radius of a sector shows some variation, the dimensions given in col. 7 (mm) refer to the largest chamber subtype. The shape of end-cap chambers is trapezoidal, and col. 8 gives the tube length at the outer side of the trapezoid of the largest chamber.

Chamb. type	Layer	No. of chamb.	Tube layers	Locat. in $ z $	No./ sect.	Radial dimens.	Max tube length	No. of CSMs	Mezz/ chamb.	Avg. curr.	Total power
EIS	inner	32	2 × 4	7261	2	1096	1546	32	12–14	6.3	0.80
EIL	inner	32	2 × 4	7675	2	1096	2311	32	16	7.5	0.96
EIL.4	inner	16	2 × 4	7641	2	1637	3071	16	14–18	7.5	0.48
EES	extra	32	2 × 3	10276	2	1216	2734	32	10–12	5.5	0.70
EEL	extra	30	2 × 3	11322	2	1216	4441	30	10–12	5.1	0.61
EMS	middle	80	2 × 3	13878	5	1937	3643	80	16	7.5	2.40
EML	middle	80	2 × 3	14294	5	1937	5746	80	14–16	7.3	2.35
EOS	outer	96	2 × 3	21820	6	1457	3985	96	12–14	6.3	2.41
EOL	outer	96	2 × 3	21404	6	1457	6241	96	12–14	6.1	2.36
Total end-cap		494						494			13.1
<b>Barrel + end-cap</b>		<b>1150</b>						<b>1118</b>			<b>28.8</b>

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