

FAST TRACK COMMUNICATION

Atom chip for BEC interferometry

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Abstract

We have fabricated and tested an atom chip that operates as a matter wave interferometer. In this communication we describe the fabrication of the chip by ion-beam milling of gold evaporated onto a silicon substrate. We present data on the quality of the wires, on the current density that can be reached in the wires and on the smoothness of the magnetic traps that are formed. We demonstrate the operation of the interferometer, showing that we can coherently split and recombine a Bose–Einstein condensate with good phase stability.

Atom chips are microfabricated devices that control electric, magnetic and optical fields in order to trap and manipulate cold atom clouds and Bose–Einstein condensates (BECs) [1–4]. Such devices have significant potential for applications in sensing, metrology and quantum information processing. Although BEC was first created on an atom chip 10 years ago [5], the fabrication of functional devices has posed significant technical challenges that have only recently been overcome. In particular, BEC interferometry on an atom chip has been demonstrated using static magnetic fields in combination with radio-frequency [6], optical [7] or microwave fields [8].

In this communication we report on the fabrication and initial testing of a working BEC interferometer. We have fabricated test batches of atom chips using a variety of techniques for depositing gold on silicon and for etching the required wire structures. After evaluating the quality of these, we settled on a fabrication method using electron beam evaporation of a gold layer followed by ion-beam milling to define the wires. We have used one of the atom chips fabricated in this way to make a BEC interferometer.

The atom chip that we have fabricated is shown in figure 1. Four parallel Z-shaped wires produce the necessary dc and rf

fields for trapping and manipulating BECs near the surface of the chip. The wires in the outer pair are 100 μm wide and have a separation of 300 μm (centre-to-centre). The inner wires are 50 μm wide with 85 μm separation. The central section of the wires along the z -axis, above which the BEC is produced, is 7 mm long. Two more wires are patterned onto the chip parallel to the ends of the Z-wires along the x -axis. These are used to provide additional axial trap depth and to adjust the field strength at the trap minimum.

In order to load this chip, cold ^{87}Rb atoms from a low-velocity intense source (LVIS) are first captured 4 mm from the surface in a magneto-optical trap (MOT) [9]. The gold surface serves as a mirror that reflects some of the laser cooling light, allowing the MOT to be formed close to the chip. The atoms are then passed to the magnetic trap, where the cloud is further cooled by forced evaporation using an rf field to eject the most energetic atoms. A BEC is formed at approximately 500 nK and this provides the coherent matter wave for our interferometer. The procedure is similar to that described in our previous publications [10].

Although atom chips are made using standard microfabrication techniques, the experimental requirements impose a number of unusual design constraints. In order to create magnetic traps with sufficient depth, the wires must be able to carry several amperes for a period of 10–20 s. At the same time they should be as small as possible to manipulate

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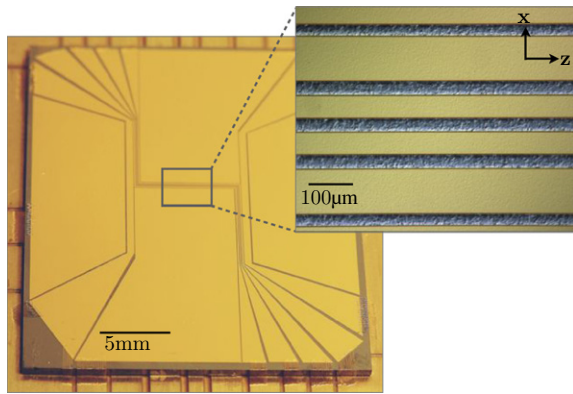


Figure 1. The atom chip used in our interference experiments. Four parallel Z-wires occupy the central region of the chip and there are two additional end wires. The surrounding gold pads form a mirror surface used in pre-cooling the atoms in a MOT. Inset: an optical microscope image of the centre of the chip showing the four parallel trapping wires (in gold). The silicon substrate can be seen in the gaps between the wires (in grey). The roughness of the silicon substrate is due to over-etching during the ion-beam milling.

the atoms on a small length scale. This means that they must be able to carry very large current densities. The wires must also be very smooth on length scales of up to several hundred microns in order to minimize transverse currents that lead to roughness of the magnetic trap and fragmentation of cold clouds (see below). Finally, in order to facilitate pre-cooling of the atoms in a MOT, the entire chip surface must have a mirror finish.

Gold is our material of choice since it has a low resistivity and high reflectivity at the relevant laser wavelength. We use a silicon substrate in order to take advantage of mature fabrication techniques that will allow for future integration of optical elements such as fibres, cavities, waveguides and pyramid MOTs into a single device [11–14]. Silicon has good thermal conductivity, but must be covered in a thin oxide layer to ensure that the wires are electrically isolated from the substrate.

The wires can be fabricated using standard lithographic techniques or by adapting thin film hybrid technology [4, 15]. High-quality wires have been made by applying a lift-off technique to an evaporated gold layer [16–18]. Evaporated gold has a good surface finish, and the lift-off technique gives the wires good edge definition when they are thin. However, the method is not well developed for films as thick as ours. Other groups have patterned a thin gold film photolithographically, then grown thick wires by electrochemical deposition [19–21]. Thicker wires can be fabricated using this technique, but the homogeneity of the gold and definition of the edges are not as good. In our previous work we have studied techniques for fabricating gold wires using sputtered and electrochemically deposited gold layers that are subsequently patterned by wet-etching or ion-beam milling [22]. We have also investigated growing wires by electrochemical deposition into a mould formed by a lithographically patterned photoresist [23]. In the light of all these studies, we have fabricated our BEC interferometer

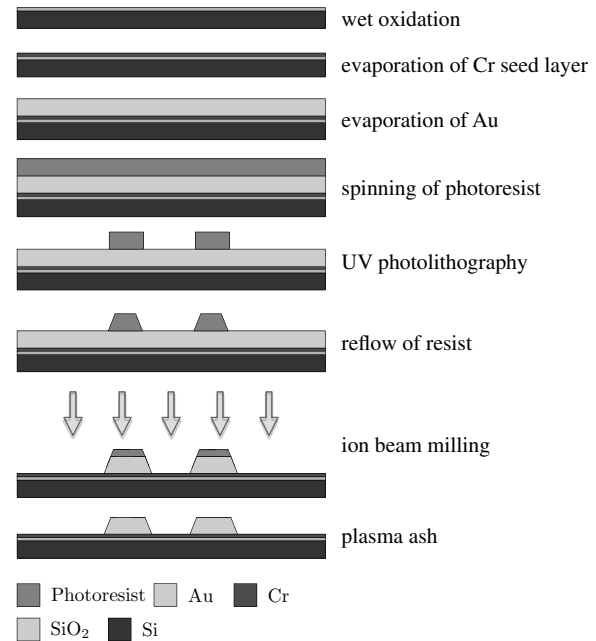


Figure 2. Fabrication process flow for electron beam evaporation of a thick gold film followed by ion-beam milling.

chip using a thick evaporated gold layer patterned by ion-beam milling.

We use a 4 inch p-doped [100] silicon wafer with a resistivity of 17–30 Ωcm to produce 16 atom chips. The wafer is cleaned using the standard Radio Corporation of America procedures and fuming nitric acid. It then undergoes wet oxidation to produce a 100 nm thick oxide layer, the first of several steps illustrated in figure 2. A 40 nm adhesion layer of chromium is then evaporated over the whole surface, followed by 3 μm of gold deposited in five steps of 600 nm to avoid overheating the evaporator. After cleaning in fuming nitric acid, a 2.2 μm thick layer of HPR504 photoresist is spun onto the gold at 500 rpm for 10 s, followed by 30 s at 1500 rpm. This is given a soft bake at 90°C for 120 s, then it is patterned by UV lithography using a Karl Suss MA8 machine for 9 s at 6.5 mW cm^{-2} . Finally, a hard bake is done for 30 min at 140°C so that the resist will be easier to remove after it has been subjected to ion-beam milling. This also causes the resist to develop sloping sides as it reflows a little.

Milling is done on an IONFAB 300+, with 388 V of beam voltage, 200 mA of current and 276 V of accelerating voltage. The wafer is cooled to a temperature of 21°C using helium and is milled for 50 min, resulting in a maximum cutting depth of 4.4 μm . The resist is quite hard to remove after exposure to the ions, despite the hard bake, so we use a plasma asher for this purpose run at 110°C with 600 W for 60 min. Once all the resist has been removed the wafer is cleaned in fuming nitric acid. The etch rate is not uniform across the wafer, resulting in over-etching in some places. Where the etch is too deep, the mill can go through the oxide layer and into the silicon substrate itself. In that case, re-deposited silicon on the side walls of the cut makes an electrical short to the wafer. This debris is removed by a 5 s buffered HF acid dip (7:1) followed

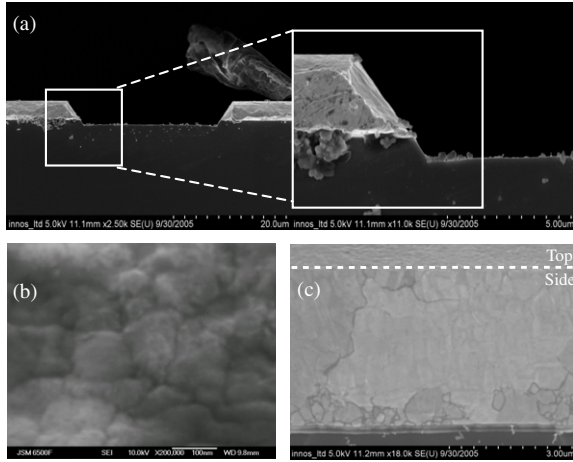


Figure 3. SEM images of the gold wires fabricated by e-beam evaporation followed by ion-beam milling. Image (a), wire cleaved through the middle to reveal sloping sides. (b) Top surface of the wire. (c) View facing the sloping side wall of the wire.

by a 5 min KOH etch. Finally, we use a diamond scribe to cleave the wafer into 16 separate atom chips 24 mm wide and 26 mm long.

Cleaving a chip through the middle allowed us to examine the cross-sectional profiles of the wires using a scanning electron microscope (SEM). Figure 3(a) shows the sloping side walls of the wire, transferred from the resist to the wire by erosion of the resist during the milling process. One also sees that the milling was too deep on this wire and penetrated into the silicon. Figure 3(b) shows an SEM image of the surface of one of the gold wires, which was found using an atomic force microscope to have 3 nm RMS roughness. Figure 3(c) shows an SEM image of the sloping side wall of one of the gold wires. Some grain structure is evident on the μm scale, but there is no sign of any layering due to the multi-stage evaporation. The surface and wire edge are smooth on the scale of this image.

The maximum usable current density in the chip wires follows from the temperature rise due to resistive power dissipation and is limited by thermal conduction. The insulating SiO_2 layer is the main barrier to heat flow. When current is turned on, the wire temperature rises rapidly over some microseconds until the drop across this layer saturates. Thereafter, the wire temperature rises more slowly, as determined by thermal conduction into the silicon substrate and on into the mounting structure, made of oxygen-free copper embedded in a Shapal-M (AlN) base plate, connected to an 8 inch stainless steel vacuum flange. The mounting structure acts as a heat sink.

The wires were tested by passing current through them and using the change in resistance to monitor the slow temperature rise. Taking an increase of 150°C (50% increase in resistivity) as a reasonable working upper limit, we measured maximum current densities of $8.8 \times 10^9 \text{ A m}^{-2}$ in the $50 \mu\text{m}$ wide wires and $6.1 \times 10^9 \text{ A m}^{-2}$ in the $100 \mu\text{m}$ wide wires with current pulses 10–20 s long and with the atom chip in vacuum.

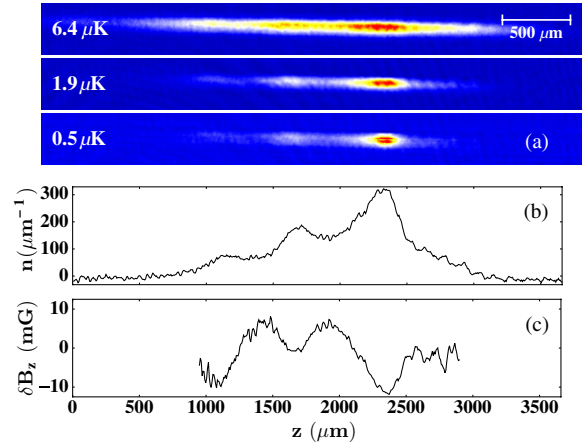


Figure 4. Cold atom studies of the chip. (a) Absorption images of successively colder clouds taken after turning off the trap and accelerating the clouds away from the chip for 3 ms. At $\sim 2\text{--}3 \mu\text{K}$ the cloud begins to sense roughness of the trapping potential, and the wing to the left becomes distinct from the main cloud. A BEC begins to form in the largest of these lumps at 500 nK . (b) Linear number density $n(z)$ of the $1.9 \mu\text{K}$ cloud. (c) Inferred deviation of trap from a smooth harmonic potential ($\omega_z = 2\pi \times 6.5 \text{ Hz}$), expressed as the magnetic field δB_z that causes it.

Atoms are loaded into the chip by passing them from the MOT to a magnetic trap at a height $y \simeq 150 \mu\text{m}$ above one of the wires. This is formed by passing 2 A through the wire, with a bias field of $B_x = 24.8 \text{ G}$. We then cool the atoms to the BEC transition by forced rf evaporation. The absorption images in figure 4(a) show the cloud at several temperatures near the end of the evaporation process. At $6 \mu\text{K}$ the cloud is roughly 1 mm long and exhibits an extended wing on the left-hand side. With further cooling down to $1.9 \mu\text{K}$ that wing becomes a clearly separate cloud, due to a subsidiary minimum in the axial potential. As described in [24], we can derive the variation of the potential from the density distribution of these atoms, shown in figure 4(b). The result is illustrated in figure 4(c). This roughness is due to transverse currents $\delta I_x(z)$, which generate fields $\delta B_z(z)$ parallel to the wire. Since the bottom of the trapping potential is set by $B_z(z)$, these fields make the trap rough [17, 21, 24, 25]. The angular variation of the current can be estimated from the ratio of the noise field to the main field, which is approximately $\pm 10^{-4}$. Since the variation takes place over typically $\pm 200 \mu\text{m}$, the centre of the wire need only deviate by 20 nm over this length to cause the effect that we see. It seems probable that this is due to slight variations in the edges of the wire, though it could also be due to minor defects in the homogeneity of the gold. It would be interesting to see if this could be improved by omitting the reflow of the resist to achieve better definition of the edges. The magnitude of the potential variation at this distance is similar to that seen in electroplated wires of similar dimensions and larger than that reported in evaporated wires patterned using a lift-off technique [17].

In order to split the matter wave with our atom chip, we alter the potential by adding near resonant rf fields as proposed by [26, 27] and demonstrated by [6, 28, 29]. The experimental arrangement is shown in figure 5(a). Two wires

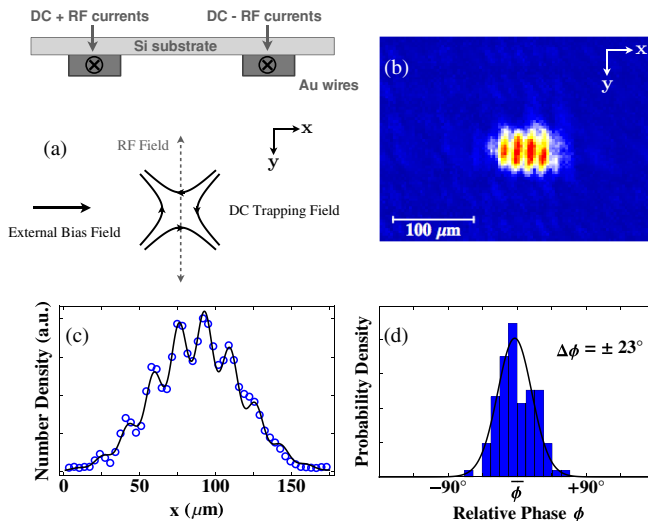


Figure 5. (a) Configuration of static and rf fields used to split the BEC coherently. (b) Absorption image of the atomic cloud showing interference fringes formed when the trapping potential is turned off and the two arms of the BEC interferometer are allowed to overlap in free fall. (c) The relative phase is obtained by fitting a modulated Gaussian (solid line) to a slice through the centre of the interference pattern. (d) Histogram of the relative phases extracted from 103 repetitions of the experiment. The solid line is a fit to the data using a normal distribution. The standard deviation is $\Delta\phi = \pm 23^\circ$.

carrying parallel dc currents form a 2D quadrupole with the help of the bias field. We evaporate to BEC in this trap and continue the evaporation until no discernible thermal atoms remain, at which point the BEC has $\sim 1.5 \times 10^4$ atoms and a chemical potential $\mu = h \times 3$ kHz. The addition of rf currents, 180° out of phase, generates a near-resonant rf field along y that splits the cigar-shaped cloud into two parallel clouds. The trap can be smoothly deformed from a single to a double well by ramping the intensity and/or frequency of the rf. A typical double well used in our interference experiments has a separation of $\sim 4 \mu\text{m}$ between the two trap minima and a barrier height of ~ 10 kHz.

After allowing the two parts to evolve separately for approximately 1 ms, we read out the relative phase between them by turning off the trapping potential and allowing them to overlap in free fall. We then take an absorption image of the density distribution, which exhibits interference fringes perpendicular to the splitting axis, as illustrated in figure 5(b). We analyse the pattern by fitting a modulated Gaussian $n(x) = g(x)(1 + \alpha \cos(\frac{2\pi x}{\Lambda} + \phi))$ to a slice through the centre, as shown in figure 5(c), to determine the relative phase ϕ . In figure 5(d) we plot a histogram of the phases extracted from 103 repetitions of the experiment. The standard deviation of these is $\pm 23^\circ$, indicating that the splitting produces a well-defined initial relative phase between the two arms of the interferometer, as is required for a useful measuring device. This phase spread is similar to that reported by Schumm *et al* [25] for similar experimental parameters and evolution time.

In conclusion, we have fabricated an atom chip by a process involving electron beam evaporation of a thick gold layer on a silicon substrate followed by ion-beam milling. The resulting wires are able to carry high-density dc and rf currents

and are sufficiently smooth and uniform to trap a cold atom cloud close to the surface of the chip. We have used one of these atom chips to make a working BEC interferometer with good phase stability.

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