Atom chips: Fabrication and thermal properties

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Neutral atoms can be trapped and manipulated with surface mounted microscopic current carrying and charged structures. We present a lithographic fabrication process for such atom chips based on evaporated metal films. The size limit of this process is below 1 μm. At room temperature, thin wires can carry current densities of more than 10^7 A/cm^2 and voltages of more than 500 V. Extensive test measurements for different substrates and metal thicknesses (up to 5 μm) are compared to models for the heating characteristics of the microscopic wires. Among the materials tested, we find that Si is the best suited substrate for atom chips. © *2004 American Institute of Physics*.
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Manipulation of neutral atoms using micro-structured surfaces (atom chips) has attracted much attention in recent years.[1] Atom chips promise to combine the merits of microfabrication and integration technologies with the power of atomic physics and quantum optics for robust manipulation of atomic quantum systems. Extreme and precise confinement in traps with large level spacing is possible (up to $\omega \sim 2\pi \times 1$ MHz and corresponding ground state sizes of ~10 nm). Neutral atoms have been trapped by currents flowing in microscopic wires fabricated on the atom chip surface,[2,3] manipulated by electric fields,[4] and even cooled to Bose–Einstein condensates.[5–7]

The demands on atom chips are high current densities to create steep traps, and small structure sizes to create complex potentials at a scale where tunneling and coupling between traps can become important. Exceptional high-quality fabrication is essential, since the smallest inhomogeneities in the bulk of the wire or the fabricated edges can lead to uncontrolled deviations of the current flow and therefore to disorder potentials in the magnetic guides and traps.[8–12]

The fabrication process preferred by groups working in the field is to grow thick wires from a thin patterned layer using electroplating,[13–15] which allow large currents for trapping and manipulating the atoms.

In contrast, we have chosen to pattern directly up to 5-μm tall evaporated high-quality layers of gold using a photolithographic lift-off technique (Fig. 1). Wires are defined by thin gaps in the evaporated gold surface. These μm sized gaps only produce an insignificant amount of stray light when the gold surface is used as a (nearly perfect) mirror for laser cooling and atom imaging. This technique was preferred because it results in high surface quality and very smooth structure edges.

In our process, the substrate (Si or GaAs covered with a SiO_2 insulation layer or sapphire) is prepared with an adhesion primer. To allow the evaporation of thick metal layers, we spin up to 5-μm-thick films of image reversal photoresist (AZ 5214E) onto the sample at low speed. The resist is then exposed to UV-light through an *e*-beam patterned mask. After developing the resist structure [Fig. 1(a)], a Ti adhesion layer (35 nm) and a thick Au layer (1–5 μm) are evaporated at a short distance from the source at a rate of 5–40 Å/s. To achieve good surface quality, care has to be taken in controlling the evaporation speed and substrate temperature. The gold covered resist structure is then removed in a lift-off procedure using acetone (if necessary in a warm ultrasonic bath) and isopropanol as solvents. A second gold layer can be added by repeating the above process. Some chips were covered with a thin protective insulation layer of Si_3N_4. Finally, the chips are cut or cleaved to the desired dimensions of 25×30 mm^2.

The resulting gold surfaces are smooth (grain sizes <80 nm) [Fig. 1(d)], and the wire edges are clearly defined. The surface quality depends on adhesion properties and the substrate smoothness. Semiconductor substrates (Si and GaAs) gave better results than sapphire samples.

An important characteristic of atom chips is how much current and voltage the microscopic wires can carry. The achievable confinement of the atoms depends on the maximal potential gradient, which scales with the achievable current density *j*.

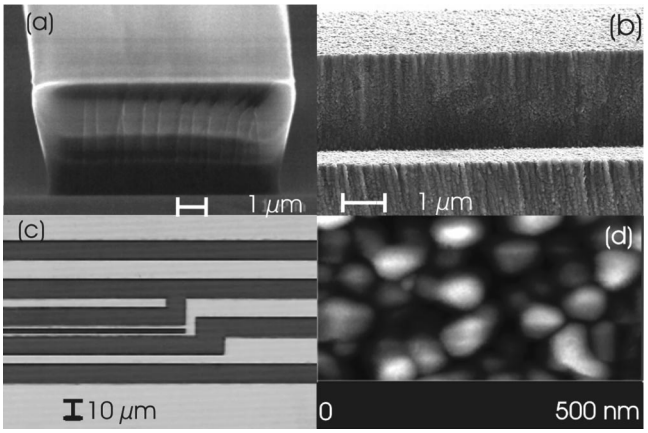

FIG. 1. Microscope images of chip details during and after the fabrication. (a) SEM picture of the resist structure. Its thickness is 4.5 μm, the undercut is 0.6 μm. (b) SEM image of a typical fabricated wire. (c) 1, 5, and 10-μm-wide gold wires on a fully fabricated chip. (d) AFM picture of the gold surface. The grain size is 50–80 nm.

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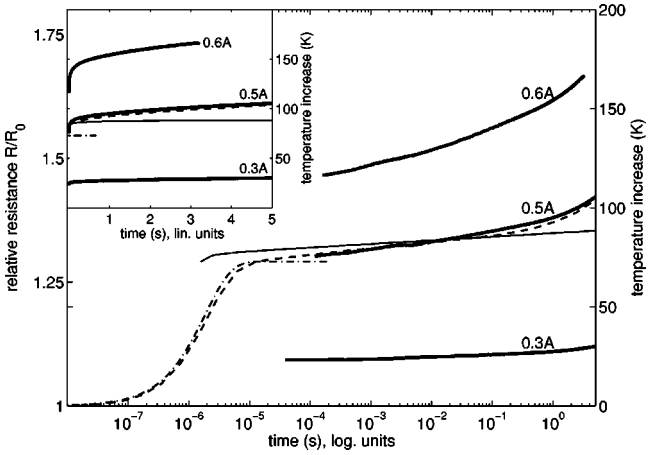

FIG. 2. Temperature evolution of a 5-μm-wide, 1.4-μm-tall wire mounted on a 700-μm-thick Si substrate with a 500 nm SiO_2 isolation layer. The thick solid curves show measured data for 0.6, 0.5, and 0.3 A current pulses. In one case (0.5 A) also the theoretical predictions (without fitting parameters) are shown. The initial fast temperature increase (thin dashed-dotted curve) occurs on a microsecond time scale. The analytical model for the heat transport through the substrate (thin solid curve) holds only as long as the approximation of a half space substrate is valid. A two-dimensional numerical model (dashed curve) accurately reproduces the measurements.

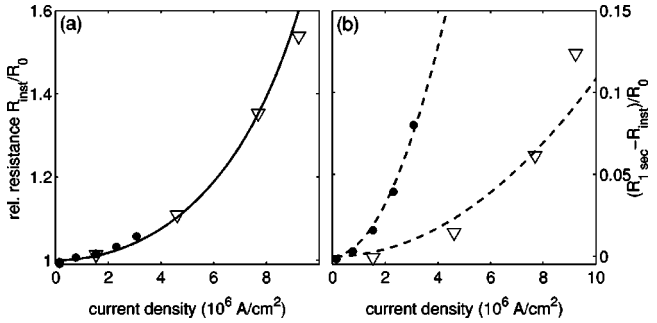

FIG. 3. Comparison of the measured heating of wires of different widths [5 μm (▽), 50 μm (●)] to the two models (solid and dashed lines; no fitting parameters used). (a) The fast heating process depends solely on the current density. (b) For the slow process, the wider wire exhibits a larger temperature increase at equal current density.

To evaluate the fabrication process and to collect comprehensive data for the operation of the atom chips and their limits, a series of test chips was built incorporating 2-mm-long wires with widths of 2, 5, 10, 50, and 100 μm and heights ranging from 1 to 5 μm on different substrates (Si with 20- or 500-nm-thick isolation layer, GaAs, and sapphire). The test chips were mounted on a simple sample holder, and the current and voltage characteristics were measured under moderate vacuum conditions (10^{-6} mbar).

Regarding charges, both semiconducting (Si) and insulating (sapphire) substrates tolerated voltages of >300 V (>500 V for sapphire) across a gap of 10 μm. This provides ample flexibility for manipulation of atoms in comparably deep potentials even at relatively large distances from the surface by means of electrostatic fields ($U_{\mathrm{el}} \sim k_B \times 100\ \mu$K at a surface distance of $\sim 50\ \mu$m).[4]

The current characteristics were measured by pushing a constant current through the wire and recording the voltage drop, which yields the resistance R of the wire. Depending on the wire dimensions, R ranges from 0.1 to 100 Ω. The experiments were carried out in a pulsed manner similar to the real atom chip experiments, allowing a cool down time (typically ~10 s) between the pulses. Usually, we arranged the length of the current pulses such that the resistance rose by less than 50%. This proved to be a safe procedure without damaging the wires. At stronger heating, the measurements were partly irreproducible (sometimes the wires were even destroyed).

The measurements show two time scales for the heating process (Fig. 2). Immediately after switching the current, the wires heat up on a microsecond time scale, seen as an increased resistance in our experiments. This initial jump, which was not resolved in our measurements (time resolution 100 μs), is followed by a slow rise of temperature, which was observed over the full duration of the current pulses (up to 10 s).

In order to gain insight into the relevant processes and parameters, we compared our data with a simple model for the heating of the substrate mounted wires. The heat created in a wire of height h and width w carrying a current density $j=I/wh$ is given by ohmic dissipation. Essentially, the heat is removed through heat conduction to the substrate, as thermal radiation is negligible for the observed temperatures. The temperature evolution of the wire is determined by the heat flow through the interface, which exhibits a thermal contact resistance (thermal conductance k), and the heat dissipation within the substrate, governed by the heat conductivity λ and heat capacity (per volume) C. This leads to two very different time scales for the heat removal:

The time scale of the first process (heat flow from the wire to the substrate through the isolation layer) is given by $\tau_{\mathrm{fast}}=C_W h/(k-hj^2\alpha\rho)$ where C_W is the heat capacity (per volume) of the wire, ρ its (cold) resistivity with a linearly approximated temperature coefficient α. For typical parameters of our chips, this time scale ($\sim 1\ \mu$s) is so short that the temperature difference between the wire and the substrate

$$\Delta T_f(t) = \frac{h\rho j^2}{k - hj^2\alpha\rho}(1 - e^{-t/\tau_{\mathrm{fast}}}) \tag{1}$$

saturates practically instantaneously, unless j exceeds the limit of $\sqrt{k/h\alpha\rho}$. In this case, an exponential rise of the temperature will lead to an almost instantaneous destruction of the wire.

Our model for the fast heating process quantitatively agrees with the data. While the initial temperature rise is independent of the wire width [Fig. 3(a)], it depends on the contact resistance to the substrate [Fig. 4(a)]. The latter effect can clearly be seen by comparing the data for two Si substrates with different insulation layers. A 500-nm-thick SiO_2 layer leads to stronger heating than a 20-nm-thick layer. In order to find the optimal substrate, the values for the thermal conductance k were obtained from fitting the model to our data ($k=6.5, 3.5, 2.6, 2.3\times 10^6 \mathrm{W/K\,m^2}$ for Si with 20 nm SiO_2, sapphire, Si with 500 nm SiO_2, and GaAs, respectively). The fitting is necessary, because k includes the conductance through the insulation layer and the contact resistances at the individual material interfaces. The best conductance was found for the Si substrate with the thin SiO_2 layer. The differences between the remaining data are mainly due to different wire heights. In our experiments Si substrates with thin isolation layers consistently exhibited the lowest fast heating of typically $\Delta T_f \sim 50$ K corresponding to ~20% resistance increase at $10^7\ \mathrm{A/cm^2}$.

In a two-dimensional model for the heat transport within the substrate, we assume a line-like heat source on the sur-

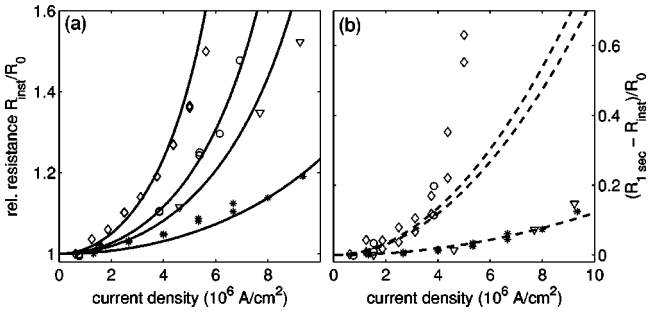

FIG. 4. Heating of 5-μm-wide Au wires fabricated on a commercial GaAs wafer (◇), sapphire without isolation layer (○), and Si substrates with a 500-nm (▽) and a 20-nm (*) thick isolation layers. The heights of the wires are 1.4 μm (Si), 2.6 μm (sapphire), and 3.2 μm (GaAs). (a) The prediction of the model for the fast process (solid lines) is compared to the wire resistances (in units of their respective cold resistance R_0) measured a few milliseconds after the beginning of a current pulse. The thermal contact resistance ($k \sim 10^6$ W/K m^2) was used as a fitting parameter. (b) Slow heating process data taken after 1 s of current flow. No fitting parameters were used to compare the model (dashed lines).

face of a half space substrate. The temperature increase $\Delta T_s(t)$ at this point is then given by the incomplete Γ function

$$\Delta T_s(t) = \frac{hw\rho j^2}{2\pi\lambda}\Gamma\left(0, \frac{Cw^2}{4\pi^2\lambda t}\right) \approx \frac{\rho I j}{2\pi\lambda}\ln\left(\frac{4\pi^2\lambda t}{Cw^2}\right). \qquad (2)$$

Here, the (small) temperature dependence of the resistivity is neglected.

For this slow heating process, the total heat dissipation becomes important. Hence, wider wires heat up faster than narrow ones for equal current density [Eq. (2) and Fig. 3(b)]. In addition, the heat transport in Si is faster than in the other tested materials due to its larger heat conductivity ($\lambda_{GaAs} \approx \lambda_{sapphire} \approx \lambda_{Si}/3$). Figure 4 shows that the thin wires (1.4 μm) mounted on Si heat up significantly less than the taller wires (~ 3 μm) fabricated on sapphire or GaAs. In the latter case, the simple model underestimates the temperature rise for large power dissipation as predicted by the numerical heat equation integration. The analytical model is only valid as long as the substrate can be treated as a heat sink. For a thin substrate (typically 700 μm) the heat transport out of the substrate has to be taken into account for longer times (typically after a few 100 ms). Then a two-dimensional numerical calculation accurately reproduces the data (Fig. 2).

To conclude, we have presented a method for fabricating atom chips with a lithographic lift-off process. With this process we produced wires that can tolerate high current densities of $>10^7$ A/cm^2. We have shown that the temperature evolution of surface mounted microwires agrees with a simple dissipation model. The optimal substrate has a large heat conductivity and capacity and is in good thermal contact with the wire. Si substrates with thin oxide layers showed the best thermal properties of the examined samples as well as good surface qualities. The described fabrication process leads to very accurate edge and bulk features, limited by the grain size of 50–80 nm. As a result, the disorder potentials have been observed to be sufficiently small not to fragment a cold thermal atomic cloud ($T=1$ μK) at a distance of <5 μm from the wire.[16]

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