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Atomic-scale ferroic HfO₂-ZrO₂ superlattice gate stack for advanced transistors

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37 With the scaling of lateral dimensions in advanced transistors, an increased gate capacitance
38 is desirable both to retain the control of the gate electrode over the channel and to reduce
39 the operating voltage¹. This led to the adoption of high- κ dielectric HfO₂ in the gate stack in
40 2008², which remains as the material of choice to date. Here, we report HfO₂-ZrO₂ super-
41 lattice heterostructures as a gate stack, stabilized with mixed ferroelectric-antiferroelectric
42 order, directly integrated onto Si transistors and scaled down to ~ 20 Å, the same gate ox-
43 ide thickness required for high performance transistors. The overall EOT (equivalent oxide
44 thickness) in metal-oxide-semiconductor capacitors is equivalent to ~ 6.5 Å effective SiO₂
45 thickness, which is, counterintuitively, even smaller than the interfacial SiO₂ thickness (8.0-
46 8.5 Å) itself. Such a low effective oxide thickness and the resulting large capacitance cannot
47 be achieved in conventional HfO₂-based high- κ dielectric gate stacks without scavenging the
48 interfacial SiO₂, which has adverse effects on the electron transport and gate leakage cur-
49 rent³. Accordingly, our gate stacks, which do not require such scavenging, provide substan-
50 tially lower leakage current and no mobility degradation. Therefore, our work demonstrates
51 that HfO₂-ZrO₂ multilayers with competing ferroelectric-antiferroelectric order, stabilized
52 in the 2 nm thickness regime, provides a new path towards advanced gate oxide stacks in
53 electronic devices beyond the conventional HfO₂-based high- κ dielectrics.

54 With the two-dimensional scaling of silicon field-effect transistors reaching fundamental lim-
55 its¹, new functional improvements to transistors⁴, as well as novel computing paradigms and verti-
56 cal device integration at the architecture-level⁵, are currently under intense study^{1,4,6}. Gate oxides
57 play a critical role in this endeavor, as it's a common performance booster for all devices, includ-
58 ing silicon², new channel materials with potential for higher performance^{7,8}, and even materials
59 suitable for three-dimensional integrated transistors^{9,10}. Indeed, the gate oxide transition from
60 SiO₂ to high- κ dielectric (DE) is considered a paradigm shift in computing technology. In this
61 context, ferroelectric oxides offer new functionalities¹¹ considered promising for energy-efficient
62 electronics^{4,9}. The advent of atomic layer deposition (ALD) grown ferroelectric doped-HfO₂¹²
63 has overcome much of the material compatibility issues that plague traditional perovskite-based
64 ferroelectric materials². In addition, considering ferroic order persists down to a thickness of 1 nm
65 in this system¹³⁻¹⁵ allows for integration of these oxides in the most aggressively-scaled devices in
66 which the state-of-the-art high- κ oxide thickness is less than 2 nm.

67 In an advanced silicon transistor, the gate oxide is a combination of two distinct layers. The
68 first is an interfacial SiO₂ formed with a self-limiting process, resulting in ~ 8.0 - 8.5 Å thickness¹⁶.
69 The next is the high- κ (HK) dielectric HfO₂ layer that is typically ~ 2 nm in thickness. Higher ca-
70 pacitance of this series combination is desirable to suppress short channel effects. The capacitance
71 is conventionally represented by effective oxide thickness (EOT), $EOT = t_{SiO_2} + t_{HK}/(\epsilon_{HK}/\epsilon_{SiO_2})$,
72 where lower EOT represents higher capacitance. Therefore, the EOT minimum value is limited
73 by the interfacial SiO₂ thickness. Indeed, even integrating HfO₂ as the high- κ layer, the EOT is
74 typically ~ 9 Å. To go below this value¹⁷, the semiconductor industry has implemented sophisti-
75 cated scavenging techniques^{16,18} to reduce the SiO₂ thickness after the full gate stack is formed.
76 Although this technique is very effective in scaling EOT, the thinner SiO₂ results in undesirable
77 leakage¹⁹ and mobility degradation^{2,16,20,21}.

78 In this work, we present an ultrathin HfO₂-ZrO₂ superlattice gate stack that exploits mixed
79 ferroelectric-antiferroelectric (FE-AFE) order (Fig. 1a,b). Our films demonstrate mixed ferroic
80 order down to 2 nm thickness – the same thickness of high- κ oxide used in advanced transis-

81 tors. Moreover, when integrated with silicon, it shows an overall EOT of $<6.5 \text{ \AA}$, despite the fact
82 that both transmission electron microscopy (TEM) and electrical characterization reveal 8.0-8.5
83 \AA interfacial SiO_2 thickness, as is typically expected. The larger capacitance than its constituent
84 layers is a signature of the charge boost stemming from the negative capacitance effect, possible
85 in materials with ferroic order¹¹. The EOT shows a clear dependence on the specific sequence and
86 layering, underlying atomic-level control of the gate oxide behavior. The fact that sub-8 \AA EOT
87 is achieved without any interfacial SiO_2 scavenging results in substantially lower leakage current
88 for the same EOT compared to benchmarks established by major semiconductor industries³. In
89 addition, no mobility degradation is observed as EOT is scaled with these $\text{HfO}_2\text{-ZrO}_2$ ferroic gate
90 stacks. Furthermore, large ON current ($> 1\text{mA}/\mu\text{m}$) obtained in $L_G = 90 \text{ nm}$ transistors indicate
91 that there is no adverse effect on the carrier velocity. Therefore, ultrathin $\text{HfO}_2\text{-ZrO}_2$ multilayers
92 exploiting ferroic order provide a new pathway toward energy-efficient gate stacks for advanced
93 transistors.

94 Thin films of $\text{HfO}_2\text{-ZrO}_2$ are grown using ALD in which the nanolaminate periodicity is
95 dictated by the sequence of Hf:Zr (4:12) ALD cycles before the Hf-Zr superstructure is repeated
96 various times (Figure 1c, Methods). After top metal deposition, the entire gate stack undergoes
97 a low-temperature post-metal anneal (200 C, 60s, N_2) which does not interfere with the $\text{HfO}_2\text{-}$
98 ZrO_2 multilayer structure, as various characterization techniques – synchrotron x-ray reflectivity
99 (XRR), layer-resolved electron energy loss spectroscopy (EELS) and angle-resolved X-ray photo-
100 electric spectroscopy (XPS) – confirm the expected Hf 4 \AA - Zr 12 \AA periodicity (Extended Data
101 Fig. 1). The underlying mixed ferroic order in these $\text{HfO}_2\text{-ZrO}_2$ heterostructure is established by
102 high-resolution transmission electron microscopy (TEM) (Fig. 1d, Extended Data Fig. 2e,f) and
103 in-plane grazing incidence diffraction (Fig. 1e and Extended Data Fig. 2a,b). Both techniques
104 indicate the presence of the tetragonal ($P4_2/nmc$, T^-) and orthorhombic ($Pca2_1$, O^-) phase, which
105 correspond to antiferroelectric and ferroelectric order in fluorite-structure films, respectively. Syn-
106 chrotron X-ray spectroscopy and optical spectroscopy further confirm the presence of inversion
107 symmetry breaking in the 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ heterostructure (Extended Data Fig. 2c,d).

108 Mixed-ferroic atomic-scale $\text{HfO}_2\text{-ZrO}_2$ multilayers were designed considering FE-AFE or-
109 der can tune the free energy landscape in a similar manner to the FE-DE model systems originally
110 studied for negative capacitance stabilization^{11,22} (Fig. 1a). From the free energy landscape pic-
111 ture within a Landau formalism (Methods), the competition between the negative curvature (i.e.
112 negative capacitance) of the FE and the positive curvature (i.e. positive capacitance) of the AFE
113 can flatten the overall energy landscape, thereby substantially increasing the system's susceptibil-
114 ity. To confirm the higher susceptibility in the mixed AFE-FE system directly, we have performed
115 capacitance-voltage (C - V) hysteresis loops in metal-insulator-metal (MIM) capacitor structures on
116 thicker films with the same superlattice periodicity (Fig. 2a). Besides features indicative of mixed
117 FE-AFE order, the total capacitance for the superlattice is larger than both conventional AFE ZrO_2
118 and FE Zr:HfO_2 of the same thickness (Fig. 2a), demonstrating enhanced susceptibility. To quan-
119 tify the permittivity, capacitance measurements were performed across the superlattice thickness
120 series. These measurements yield an extracted permittivity of ~ 52 (Fig. 2b, Methods), which is
121 larger than both FE orthorhombic Zr:HfO_2 and AFE tetragonal ZrO_2 values²³.

122 To further understand the ferroic evolution in these $\text{HfO}_2\text{-ZrO}_2$ superlattices, we performed
123 low temperature measurements where enhanced FE phase stabilization is expected. Indeed, temperature-
124 dependent C - V loops for thicker $\text{HfO}_2\text{-ZrO}_2$ multilayers demonstrate an evolution from mixed-
125 ferroic to FE-like hysteresis upon cooling slightly below room temperature (~ 240 K, Fig. 2c), con-
126 sistent with temperature-dependent X-ray spectroscopy indicating transition from mixed tetragonal-
127 orthorhombic phase to predominately orthorhombic structure at similar temperatures (Extended
128 Data Fig. 3). The capacitance decrease upon cooling as the system moves away from the highly-
129 susceptible mixed ferroic phase is consistent with previous work on negative capacitance in FE-DE
130 systems²² which establishes the energy landscape link between enhanced capacitance and suscep-
131 tibility near phase transitions. Notably, the intertwined FE-AFE phases within the superlattice and
132 resulting enhancement in susceptibility from the competition of FE and AFE phases is concep-
133 tually similar to negative stiffness composites of ferroelastics within a metal matrix^{24,25}, i.e. the
134 mechanical analog to negative capacitance.

135 Next, the superlattices were grown on Si substrates in metal-oxide-semiconductor (MOS)
136 capacitor structures. A self-limiting chemical oxide SiO_2 was grown first, resulting in $\sim 8.0\text{-}8.5$
137 \AA thickness³, following the standard practice in advanced Si devices (Methods). Next, a 20-cycle
138 thick multilayer was grown with ALD following the same stacking as before i.e. Hf:Zr:Hf 4:12:4.
139 Accumulation C - V curves of the superlattice stack results in significantly larger capacitance in
140 comparison to other conventional stacks – DE HfO_2 , AFE ZrO_2 , FE Zr:HfO₂ – of the same 20 \AA
141 thickness (Fig. 2d). Furthermore, the Hf:Zr:Hf 4:12:4 trilayer demonstrates enhanced capacitance
142 compared to a bilayer (Hf:Zr 8:12) and solid solution (Hf:Zr [2:3]₄) of the same thickness and
143 Hf:Zr composition (Fig. 2e). Notably, the composition in our films is close to where several previ-
144 ous reports have postulated a possible morphotropic phase boundary (MPB) in thicker HfO_2 - ZrO_2
145 solid solution films²⁶⁻³⁰. In our ultrathin HfO_2 - ZrO_2 multilayers, the negative free energy curva-
146 ture of the FE O-phase compensates the positive curvature of the AFE T-phase (Fig. 1a), leading
147 to a flattened energy landscape. Indeed, energy landscape flattening is the thermodynamic origin
148 of the MPB in the canonical perovskite ferroelectrics^{31,32}, in which multiple crystal symmetries
149 are nearly degenerate across a composition phase boundary³³. However, a critical distinction is
150 that here, the overall energy landscape flattening, and corresponding increase in capacitance, is
151 determined by the stacking of the atomic-scale HfO_2 - ZrO_2 layers, and not the volume fraction of
152 the constituent elements³⁴. For example, compared to HfO_2 - ZrO_2 solid solutions across a range of
153 typically-reported Zr-rich "MPB"-like compositions²⁶⁻³⁰, the HfO_2 - ZrO_2 multilayer demonstrates
154 larger capacitance (Extended Data Fig. 4). This indicates the enhanced capacitance in HfO_2 - ZrO_2
155 films is not simply driven by doping^{23,35}, but can instead be tuned by the configuration of the
156 multilayer structure (Extended Data Fig. 4, 5). In the ultrathin regime, surface energies become
157 a more dominant consideration for determining polymorphic phase stability^{36,37}; accordingly, the
158 importance of stacking is amplified. Overall, these capacitor studies suggest that the exact stack-
159 ing sequence plays a crucial role in stabilizing the fluorite-structure FE-AFE phase competition
160 that leads to enhanced capacitance, akin to previous reports in perovskite-based FE-DE superlat-
161 tices³⁸⁻⁴².

162 To quantify the observed capacitance, we have performed EOT simulations of MOS capac-

163 itors using the industry standard model Synopsys simulation platform (Methods). The Hf:Zr:Hf
164 4:12:4 trilayer stacks vary between 6.5-7.0 Å EOT (Fig. 2f), consistent over many measured ca-
165 pacitors. Notably, this EOT is smaller than the expected thickness of the interfacial SiO₂ layer
166 (8.0-8.5 Å), as mentioned above. To investigate further, we performed high-resolution TEM of
167 our gate stacks (Extended Data Fig. 6), which illustrates the SiO₂ thickness is indeed ~8.5 Å. To
168 supplement this physical characterization, we next implemented electrical characterization of the
169 interfacial layer via standard inverse capacitance vs thickness analysis of conventional dielectric
170 HfO₂ and Al₂O₃ thickness series grown on the same SiO₂ (Methods, Extended Data Fig. 6). All
171 thermal processing is kept exactly the same as the superlattice gate stack. The extracted HfO₂ and
172 Al₂O₃ permittivity – 19 and 9, respectively – is consistent with the typical dielectric phases of these
173 two materials. Therefore, one can reliably extract the SiO₂ layer thickness, yielding 8 Å (Extended
174 Data Fig. 6), consistent with the HR-TEM results and similar to previously studies established
175 by the semiconductor industry³. Moreover, the consistent interlayer thickness extracted from both
176 material systems indicates that neither Hf nor Al encroaches into the interfacial SiO₂ which would
177 reduce its thickness and/or increase its permittivity. This is consistent with the fact all our stacks
178 are processed at much lower temperature as compared to that needed for silicate formation⁴³. So
179 considering the interfacial layer thickness as 8 Å, the Hf:Zr:Hf 4:12:4 gate stack demonstrates an
180 overall EOT 1.0-1.5 Å lower than the constituent SiO₂ thickness. In other words, capacitance en-
181 hancement is observed in this 20 Å mixed ferroic gate oxide integrated on Si. Therefore, the mixed
182 FE-AFE order not only improves the permittivity of the multilayer stack itself, but also couples to
183 the SiO₂ in MOS capacitor structures, yielding improved overall capacitance.

184 The practical implication of this capacitance enhancement can be clearly seen in Fig. 3a,
185 which shows leakage current vs EOT behavior. The leakage current is measured at $V_G - V_{fb} = -1$
186 V, where V_{fb} is the flatband voltage of the semiconductor. All other data points on this plot are
187 taken from reported industrial gate stacks³. The leakage current for the Hf:Zr:Hf 4:12:4 stack is
188 substantially lower at the same EOT. Note that below 9 Å, the other gate stacks need sophisticated
189 scavenging techniques to reduce the thickness of the interfacial SiO₂³. On the other hand, we
190 can reach ~ 6.5 Å without any scavenging. This leads to the fact that the leakage current for our

191 stacks is lower (Fig. 3a). Notably, the scavenging the interfacial SiO₂ leads to a loss of mobility
 192 due to increase in remote phonon scattering. As it has been shown^{3,16}, the mobility drops off with
 193 a slope of $\sim 20 \text{ cm}^2/\text{V-s}$ per every \AA of scavenged SiO₂. To test how mobility is affected by
 194 the superlattice gate stack, we fabricated long channel bulk transistors with two different repeats
 195 of the superlattice, together with another sample that has thick (60 \AA) HfO₂ as the gate stack
 196 (Methods). To extract mobility, a careful fitting of the measured C - V from the transistor structures
 197 is performed. In addition, series resistance is modeled from the data and de-embedded to reveal
 198 the intrinsic behavior. Next, the mobility is extracted using the peak transconductance method
 199 (Methods, Extended Data Fig. 8). It is found that the mobility remains essentially the same for all
 200 three stacks despite the difference in materials and EOT (from 2 nm EOT for HfO₂ down to sub-8
 201 \AA for the superlattice gate stack). First, this shows that there is no fundamental change in electron
 202 transport due to the use of the superlattice gate stack compared to standard HfO₂. In addition,
 203 it shows that there is no penalty in mobility even below an EOT of 9 \AA where conventional gate
 204 stacks show a degradation due to the need for scavenging (Fig. 3b). Because the absolute value of
 205 mobility depends on the specific processing technique, mobility numbers have been normalized in
 206 Fig. 3b. This clearly shows the flat mobility-EOT behavior for the superlattice gate stack compared
 207 to the falling of trend for conventional gate stacks due to scavenging in the low EOT range.

208 To examine how the capacitance enhancement behaves at high frequency, radio frequency
 209 (RF) measurements were performed on the same long channel ($L_G = 1 \mu\text{m}$) devices (Methods,
 210 Extracted Data Fig. 9). This allows one to extract device parameters up to ~ 800 MHz for our
 211 devices (close to the cut-off frequency). Of particular interest is the transconductance (g_m) which
 212 is proportional to the product of capacitance and electron velocity (mobility). From Y -parameter
 213 measurements one can find AC transconductance as $Re(Y_{21}) = g_m + af^2$, where f is the frequency
 214 (Methods). This yields an AC transconductance as a function of applied gate voltage (V_G). This
 215 dependence is plotted together with DC transconductance ($\partial I_D/\partial V_G$ from DC I_D - V_G) (Fig. 3c).
 216 We find that DC and AC transconductance are similar with AC transconductance roughly 15%
 217 larger at the peak value. We hypothesize that this slightly large AC transconductance results from
 218 the fact that certain interface traps, which affect the DC behavior, cannot respond at frequencies

219 larger than 100 MHz, leading to better gate control. More importantly, these results show that the
220 capacitance enhancement is not limited to the low frequency regime^{44–46}.

221 Finally, to test the ON current capability, a $L_G = 90$ nm device was fabricated on a SOI
222 transistor with 18 nm SOI thickness and the superlattice gate stack. The transfer and output char-
223 acteristic of a typical transistor are shown in Fig. 3d,e. Note that the threshold voltage of this
224 device is 0.55 V which is consistent with the workfunction of W used as the gate metal. Because
225 of this, the transistors have been driven up to 1.6 V gate voltage so that an overdrive voltage (V_{ov}
226 $= V_G - V_T$) of ~ 1 V can be applied. It is found that at a drain voltage (V_D) and V_{ov} of 1 V, the
227 drain current exceeds 1 mA/ μ m. In addition, as shown in Fig. 3f, the measured extrinsic transcon-
228 ductance is ~ 1.1 mS/ μ m which gives an intrinsic transconductance of ~ 1.75 mS/ μ m (Methods,
229 Extended Data Fig. 10). These values of ON current and transconductance are substantially larger
230 than a conventional 90 nm transistor and is a result of the large capacitance provided by the super-
231 lattice gate stack and the fact that the low EOT resulting from the stack does not adversely affect
232 the electron transport.

233 With the superlattice gate stack demonstrated in integrated Si devices, we now come back to
234 the capacitance enhancement observed in this gate stack. We have already discussed how the mixed
235 FE-AFE order facilitates a flatter energy landscape where the negative curvature of the FE phase is
236 compensated by the positive curvature of the AFE phase (Fig. 1a). Notably when the mixed ferroic
237 oxide is grown on an SiO₂ interlayer, it can lead to similar compensation again. As we have seen
238 from thicker FE-AFE superlattice MIM capacitors, some hysteresis still remains, which manifests
239 at large voltages, indicative of a negative curvature regime still persisting in the superlattices. The
240 interfacial DE SiO₂ can flatten out that energy landscape even further, thus leading to enhanced
241 capacitance. This is similar to the negative capacitance and resultant capacitance enhancement
242 observed in FE-DE series combinations²². To supplement the C - V evidence of capacitance en-
243 hancement (Fig. 2f), pulsed electrical measurements of the superlattice gate stack MOS capacitors
244 – which can quantify the amount of stored charge as a function of voltage⁴⁷ (Methods) – demon-
245 strate larger stored charge than if just interfacial SiO₂ was sitting on top of Si, providing further

246 evidence of negative capacitance⁴⁷ in the gate stack (Extended Data Fig. 10). Note that previous
247 studies have shown that negative capacitance stabilization is favored under states of high suscep-
248 tibility^{39,40,48}. Here, the competing ferroic order in HfO₂-ZrO₂ multilayers substantially increases
249 its susceptibility and is thus expected to facilitate negative capacitance behavior when placed on
250 top of the interfacial SiO₂.

251 Capacitance enhancement has been demonstrated in single-crystalline, perovskite-structure
252 ferroelectric-dielectric superlattices by many groups³⁸⁻⁴¹. This work demonstrates that the same
253 enhancement is possible in HfO₂-ZrO₂ fluorite-structure superlattices exhibiting mixed ferroelectric-
254 antiferroelectric order in films as thin as just ~ 2 nm. The ability to control ferroic order in
255 such ultrathin films is of critical importance for advanced electronic devices considering previous
256 studies have shown that negative capacitance can be stabilized under states of high susceptibil-
257 ity^{39,40}. Furthermore, this work establishes the critical role of atomic-layer stacking – as opposed
258 to conventional doping techniques^{23,35} – in controlling the ferroic phase space and permittivity of
259 fluorite-structure oxides down to ultrathin limits, leveraging its unique size effects^{13-15,49} and rich
260 antiferroelectric-ferroelectric polymorphs^{36,50}. When this mixed phase HfO₂-ZrO₂ multilayer is
261 integrated on Si, the gate stack exhibits a capacitance enhancement, lowering the EOT below the
262 thickness of SiO₂ itself, which would not be possible with a conventional dielectric. Notably, the
263 lowest EOT achieved (6.5 Å) for the gate stack and interfacial SiO₂ together is lower than that
264 used in the most advanced Si transistors today. Therefore, this work demonstrates that harnessing
265 atomic-scale layering in ultrathin HfO₂-ZrO₂ ferroic gate oxides presents a promising materials de-
266 sign platform for future Si transistors beyond conventional high- κ dielectrics³ which have enabled
267 the semiconductor industry over the past two decades.

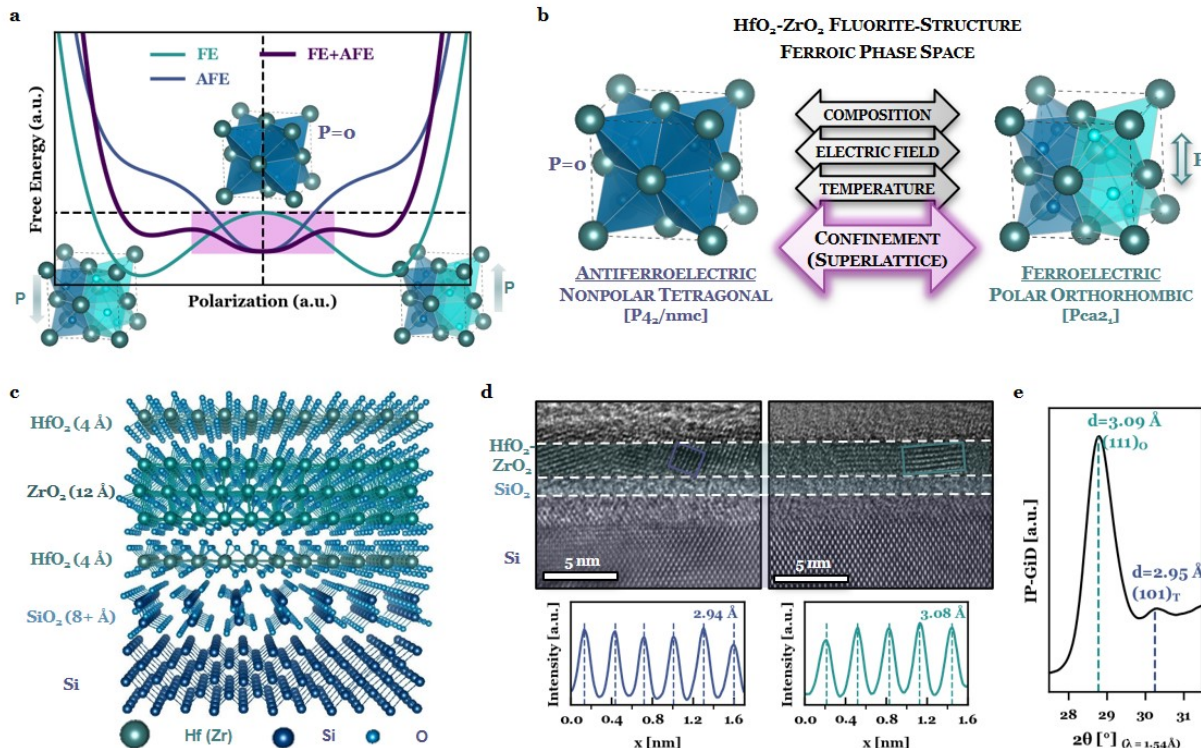
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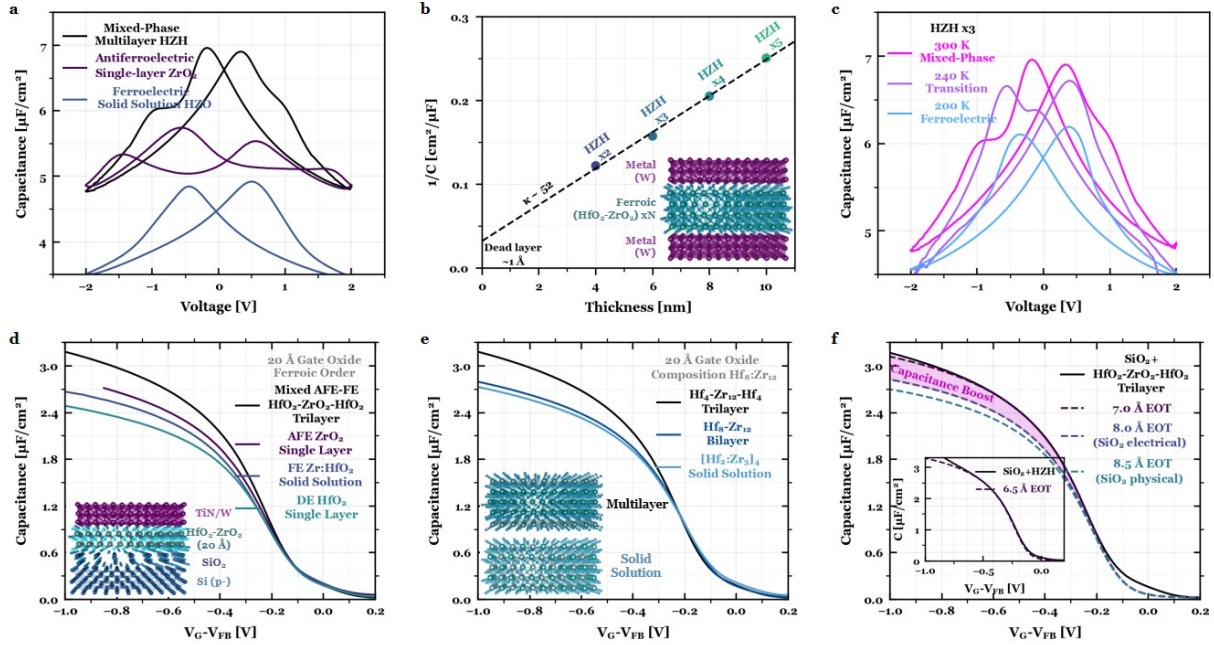
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379

380 **Fig. 1. Atomic-scale design of negative capacitance in ultrathin HfO₂-ZrO₂.** (a) Phenomeno-
 381 logical model of negative capacitance (NC) in a mixed ferroic system. Landau free energy land-
 382 scapes for a FE, AFE, and mixed FE-AFE system (Methods). Mixed FE-AFE phase competition
 383 should suppress polarization⁴⁸ and enhance electric susceptibility^{22,40} via proximity to a phase
 384 boundary, and flattens the energy landscape, desirable traits for NC stabilization. The stable en-
 385 ergy minimum of the composite free energy landscape, corresponding to the negative curvature
 386 (NC) regime of the ferroelectric energy landscape, is highlighted. (b) Engineering ferroic phase
 387 competition in the HfO₂-ZrO₂ fluorite-structure system. Beyond the conventionally-studied tuning
 388 parameters – composition, electric field, temperature^{23,35} – here we introduce dimensional confine-
 389 ment via superlattice layering to tailor ferroic phase competition at the atomic-scale. (c) Schematic
 390 of the HfO₂-ZrO₂ fluorite-structure multilayer on Si; the heterostructures maintain distinct layers
 391 (i.e. not solid solution alloys) based on EELS, XRR, and depth-resolved XPS (Extended Data Fig.
 392 1). The role of the layering on the underlying ferroic order and capacitance is studied by electrical

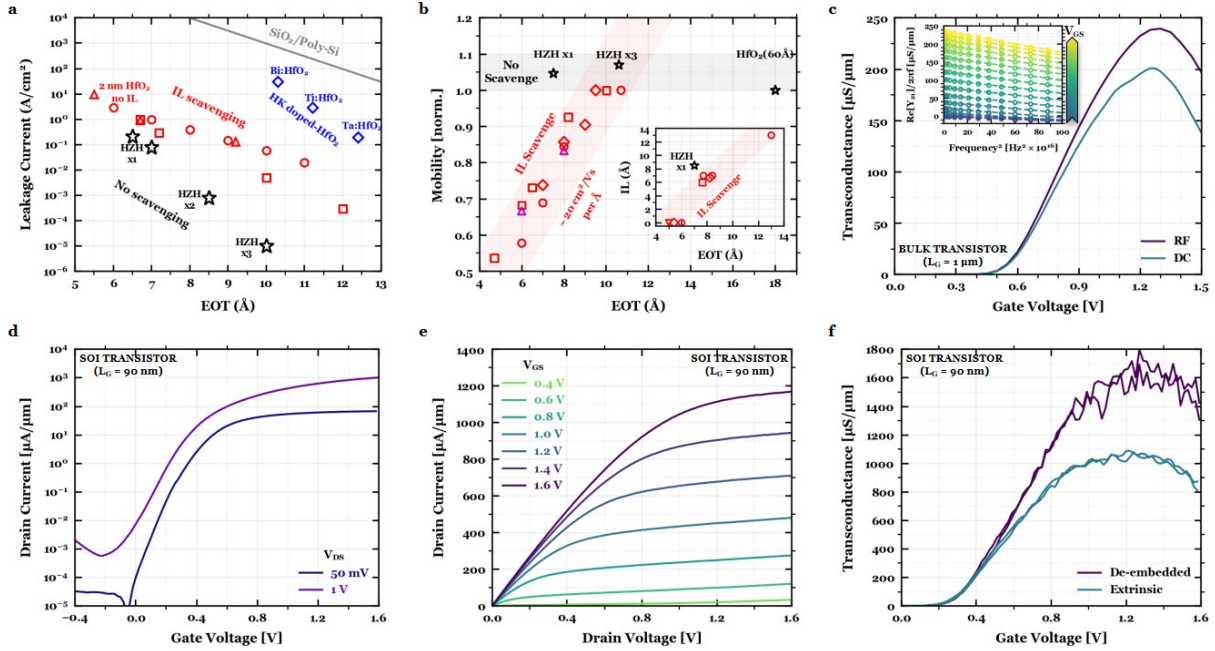
393 measurements as a function of $\text{HfO}_2\text{-ZrO}_2$ stacking structure and annealing temperature (Extended
394 Data Fig. 4 and 5, respectively). **(d)** HR-TEM image of the atomic-scale $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer
395 (top) and extracted d -lattice spacings (bottom) corresponding to the fluorite-structure AFE tetrago-
396 nal ($P4_2/nmc$, red) and FE orthorhombic ($Pca2_1$, blue) phases, respectively. The layer delineations
397 are approximate, as the $\text{HfO}_2\text{-ZrO}_2$ and SiO_2 interlayer thicknesses are more rigorously deter-
398 mined by XRR and TEM analysis (Extended Data Fig. 1 and 6, respectively). Note imaging the
399 crystallinity of the $\text{HfO}_2\text{-ZrO}_2$ layers requires mistilt with respect to the Si lattice (Methods). **(e)**
400 Synchrotron IP-GiD demonstrating the presence of both the AFE T -phase $(101)_t$ and FE O -phase
401 $(111)_o$ reflections whose d -lattice spacings are consistent with those extracted from TEM. Detailed
402 indexing to higher-order reflections for structural identification of the ferroic phases is provided
403 by wide-angle synchrotron diffraction (Extended Data Fig. 2a). Further evidence of inversion
404 symmetry breaking is provided by second harmonic generation and synchrotron linear dichroism
405 (Extended Data Fig. 2c,d). Additionally, the evolution between these two ferroic phases are also
406 studied as a function of temperature (Extended Data Fig. 3).



407

408 **Fig. 2. Enhanced capacitance in ultrathin $\text{HfO}_2\text{-ZrO}_2$ mixed-ferroic heterostructures.** (a)
 409 MIM C - V hysteresis loops for a mixed FE-AFE $\text{HfO}_2\text{-ZrO}_2$ multilayer demonstrating higher ca-
 410 pacitance compared against its AFE (ZrO_2) and FE (Zr:HfO_2) counterparts of the same thickness.
 411 (b) Inverse capacitance versus thickness of the MIM $\text{HfO}_2\text{-ZrO}_2$ multilayers up to 5 superlattice
 412 repeats (10 nm), with an extracted permittivity of 52 (Methods), extremely large for HfO_2 -based
 413 oxides. (c) MIM C - V hysteresis loops for $\text{HfO}_2\text{-ZrO}_2$ multilayers of the same periodicity demon-
 414 strating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room
 415 temperature. The proximity to the temperature-dependent phase transition (Extended Data Fig.
 416 3) suggests the $\text{HfO}_2\text{-ZrO}_2$ heterostructures lies near its maximum electric susceptibility position,
 417 ideal for negative capacitance stabilization^{40,48}. (d) MOS accumulation C - V of $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$
 418 trilayer compared to AFE ZrO_2 , FE Zr:HfO_2 , and DE HfO_2 , all of the same thickness (20 Å), indi-
 419 cating mixed-ferroic behavior is optimal for enhancing capacitance rather than purely FE or AFE
 420 behavior. (e) Accumulation C - V of the $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer compared to bilayer and solid so-
 421 lutions films of the same thickness (ALD cycles) and composition (Hf:Zr cycles). Inset: Schematic
 422 of multilayer (Hf and Zr cations vertically separated) versus solid solution (Hf and Zr cations inter-

423 mixed). These results suggest the capacitance enhancement in multilayer films is not simply driven
424 by Hf:Zr composition^{23,35}, but instead the atomic-scale stacking (Extended Data Fig. 4, 5). **(f)** Ac-
425 cumulation C - V curves for a 2 nm HfO₂-ZrO₂-HfO₂ trilayer grown on sub-nm SiO₂ fit to effective
426 oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation C -
427 V of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of
428 SiO₂ demonstrates lower EOT than the thickness of SiO₂ interlayer alone, carefully extracted via
429 physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence
430 of capacitance enhancement. Furthermore, these 2 nm ferroic gate stacks demonstrate amplified
431 charge from pulsed I - V measurements relative to the SiO₂ interlayer (Extended Data Fig. 10).
432 Notably, this 2 nm HfO₂-ZrO₂ multilayer on sub-nm SiO₂ provides the most scaled demonstration
433 of charge and capacitance enhancement at the capacitor-level (Extended Data Fig. 10).



434

435 **Fig. 3. Device performance benefits utilizing ultrathin mixed-ferroic HfO₂-ZrO₂ gate stacks.**

436 **(a)** Leakage-effective oxide thickness (J_G -EOT) scaling of the multilayer gate stacks (black) bench-
 437 marked against reported HKMG literature³, including interlayer-scavenged 2 nm HfO₂ (red), high-
 438 κ doped HfO₂ (blue), and SiO₂/poly-Si (gray). The leakage is the lowest reported for a 6.5-7.0 Å
 439 EOT MOS capacitor on silicon³, due to the EOT reduction without requiring interlayer SiO₂ thick-
 440 ness reduction. **(b)** Normalized mobility versus EOT scaling of the multilayer gate stacks (black)
 441 benchmarked against reported HKMG literature³, including interlayer-scavenged 2 nm HfO₂ (red)
 442 and hybrid silicate-scavenged interlayer (magenta). For EOT scaling in conventional HKMG sys-
 443 tems, the SiO₂ interlayer has to be reduced to lower EOT, which leads to degraded mobility³. In
 444 this case, enhanced capacitance in HfO₂-ZrO₂ multilayers achieves scaled EOT without having
 445 to thin the SiO₂ interlayer; therefore, mobility is not degraded. Inset: SiO₂ interlayer thickness
 446 versus EOT scaling comparing the 7.0 Å EOT HfO₂-ZrO₂-HfO₂ trilayer against notable HKMG
 447 literature which employ interlayer scavenging to reduce EOT³. This scatter plot highlights the un-
 448 derlying reason for the enhanced leakage-EOT and mobility-EOT behavior in the ultrathin trilayer
 449 gate stacks: low EOT without reduced SiO₂ interlayer thickness. **(c)** Transconductance (g_m) versus

450 gate voltage (V_G) for long-channel bulk transistors ($L_G = 1 \mu\text{m}$) obtained from both DC (derivative
451 of I_D - V_G) and RF ($\text{Re}[Y_{21}]$) measurements (Methods) at $V_{DS} = 1 \text{ V}$. Inset: De-embedded $\text{Re}[Y_{21}]$
452 (open circles) as a function of squared frequency at different DC V_{GS} bias points extrapolated to
453 the zero frequency limit (dotted lines) to extract the RF g_m (Extended Data Fig. 8). The high-
454 frequency measurements help suppress defect contributions which would otherwise dampen the
455 intrinsic g_m . **(d, e, f)** DC I - V transfer characteristics (I_D - V_G , d), DC output characteristics (I_D - V_D ,
456 e), and DC transconductance (g_m - V_G , f) for short-channel ($L_G = 90 \text{ nm}$) SOI transistors. Notably,
457 the maximum on-current and g_m at $V_{DS} = 1 \text{ V}$ exceeds $1 \text{ mA}/\mu\text{m}$ and $1 \text{ mS}/\mu\text{m}$. DC mobility
458 and transconductance values are carefully extracted after de-embedding the series resistance from
459 double-swept I - V measurements (Extended Data Fig. 7 and 9, respectively).

460 **Methods**

461 **Gate stack**

462 **Gate oxide** Thin films of $\text{HfO}_2\text{-ZrO}_2$ were grown by atomic layer deposition (ALD) in a
463 Fiji Ultratech/Cambridge Nanotech tool (U.C. Berkeley) at 270°C in which tetrakis (ethylmethy-
464 lamino) hafnium and tetrakis (ethylmethylamino) zirconium precursors are heated to 75°C and
465 water vapor is used as the oxidant. For metal-ferroelectric-insulator-semiconductor (MFIS) capac-
466 itor structures, sub-nm chemically-grown SiO_2 on lightly-doped Si (10^{15} cm^{-3}) was prepared by
467 the standard clean (SC-1) solution (5:1:1 $\text{H}_2\text{O}:\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$ at 80°C for 10 minutes) after the Si
468 wafer was cleaned in Piranha (120°C for 10 minutes) to remove organics and HF (50:1 $\text{H}_2\text{O}:\text{HF}$
469 at room temperature for 30 s) to remove any native oxide. Subsequently, $\text{HfO}_2\text{-ZrO}_2$ multilayers
470 are deposited at 270°C by ALD. After ALD deposition, post-deposition annealing (PDA) was per-
471 formed at 175°C (20 min, forming gas N_2/H_2 background) to help cure the SiO_2 -oxide interface.
472 For confirmation and reproducibility, $\text{HfO}_2\text{-ZrO}_2$ multilayers of the same ALD cycling were also
473 deposited at MIT Lincoln Laboratory (MIT LL); after ALD deposition, PDA was performed at
474 250°C (1 min, N_2 background).

475 **Gate metal** For UC Berkeley capacitors, the first layer of the gate metal, TiN, is deposited
476 by ALD (250°C , 20 cycles, 15 \AA) in N_2 and H_2 plasma. Subsequently, W is deposited by sputtering
477 (room temperature, 60 nm). For MIT LL capacitors, the gate metal, TiN, is deposited by PVD
478 (room temperature).

479 **Annealing** The entire gate stack undergoes a low-temperature post-metal anneal (200 C ,
480 1 min, N_2) to cure interface defects. This low temperature does not interfere with the $\text{HfO}_2\text{-}$
481 ZrO_2 multilayer structure, as confirmed by various characterization techniques (Extended Data
482 Fig. 1), and maintains the mixed ferroic behavior, as high-temperature annealing would induce
483 purely ferroelectric behavior (Extended Data Fig. 5). X-ray diffraction and TEM confirm the

484 presence of crystalline ultrathin films despite the low deposition temperature, afforded by the low
485 crystallization temperature of ZrO_2 ⁵¹. In fact, non-post-annealed ALD-grown ZrO_2 has previously
486 demonstrated crystallization into the ferroelectric orthorhombic phase on Si⁵².

487 **Device fabrication**

488 **MOS and MIM capacitors, Bare Structures** For MOS capacitor structures, after gate
489 stack deposition, top electrodes are defined by photolithography and dry etching. For bare struc-
490 tures (structural studies), the top metal is removed by chemical etching to expose the gate oxide
491 surface. For metal-insulator-metal (MIM) capacitors, W is deposited by sputtering (room temper-
492 ature, 30 nm) on a lightly-doped Si substrate as the bottom metal electrode. After ferroic film
493 deposition by ALD, 60 nm of W is deposited by sputtering. The top electrodes are then again
494 defined by photolithography and dry etching.

495 **Bulk transistors** The n-type bulk transistors were fabricated by a non-self-aligned gate-
496 last process on bulk silicon wafers (10^{17} cm^{-3}) with local oxidation of silicon (LOCOS) as device
497 isolation technique. First, a 10 nm of SiO_2 thermal oxide and a 30 nm of low-pressure chemical
498 vapor deposition (LPCVD) Si_3N_4 were grown on the Si substrates. After the active region was
499 defined by photolithography and $\text{Si}_3\text{N}_4/\text{SiO}_2$ etching, dry oxidation was performed to form the
500 LOCOS isolation. Next, the source/drain regions were defined by photolithography and ion im-
501 plantation with an ion dose of $3 \times 10^{15} \text{ ions/cm}^2$. The dopants were then activated by a rapid thermal
502 anneal (RTA) at 900°C for 7 min in N_2 ambient. The gate stacks with the sub-nm chemically-grown
503 SiO_2 , 2 nm $\text{HfO}_2\text{-ZrO}_2$ heterostructure, and 100 nm of sputtered W gate were then deposited. Af-
504 ter the gate fingers (from 500 nm to $50 \mu\text{m}$) were patterned by photolithography and etched by
505 inductively-coupled plasma (ICP) metal etching, the 400 nm thick interlayer dielectric (ILD) SiO_2
506 was deposited using plasma-enhanced CVD (PECVD). Last, after the contact hole opening, the
507 Ti/TiN contact metal was deposited by sputtering, defined by photolithography, and then etched by
508 ICP metal etching.

509 **Short-channel SOI Transistors** The n-type short-channel transistors were fabricated by a
510 non-self-aligned gate-last process on SOI substrates with a gate length (L_G) down to 90 nm. First,
511 the device layer was thinned down to 20 nm and the active regions were defined by photolithogra-
512 phy with expose regions etched slightly into the buried oxide. The hydrogen silsequioxane (HSQ)
513 negative resist were written by e-beam lithography as a hard mask for the ion implantation with a
514 dose of 5×10^{15} ions/cm². The dopant activation was conducted in an RTA at 900°C for 15 seconds
515 in N₂ ambient. The gate stacks with the sub-nm chemically-grown SiO₂, 2 nm HfO₂-ZrO₂ het-
516 erostructure, 1.5 nm of PEALD TiN, and 100 nm of sputtered W were sequentially deposited. The
517 gate region (250 nm) was then patterned by photolithography. Like the back-end process for the
518 bulk transistors, a 400 nm of ILD and a sputtered Ti/TiN contact metal were deposited and defined
519 by photolithography and ICP etching.

520 **Microscopy**

521 **Transmission electron microscopy** Electron microscopy was performed at the National
522 Center for Electron Microscopy (NCEM) facility of the Molecular Foundry at Lawrence Berkeley
523 National Laboratory (LBNL). The high-resolution bright field TEM images of HfO₂-ZrO₂ thin
524 films were performed by FEI ThemIS 60-300 microscope with image aberration corrector operated
525 at 300 kV (Fig. 1d, Extended Data Fig. 2e,f). To prepare cross-sectional TEM samples of HfO₂-
526 ZrO₂ thin films, mechanical polishing was employed by using an Allied High Tech Multiprep at
527 a 0.5° wedge to thin down the total thickness of samples down to 10 μm. Later, Ar ion milling
528 of the Gatan Precision Ion Milling System was utilized to make an electron-transparent sample,
529 starting from 4 keV down to 200 eV as final cleaning energy. For high-resolution imaging, in order
530 to capture the crystallinity of the HfO₂-ZrO₂ layers, the zone axis alignment required varying
531 degrees of mistilt with respect to the Si lattice, explaining the slightly obscured Si atomic columns
532 (Fig. 1d, Extended Data Fig. 2e,f).

533 The local interplanar d -spacing in the ultrathin HfO₂-ZrO₂ films (Extended Data Fig. 2e,f)
534 was measured by DigitalMicrograph software using its line profile plus integration width analy-

535 sis. For the 2 nm HfO₂-ZrO₂-HfO₂ multilayer film, the extracted interplanar lattice spacings were
536 averaged over multiple lattice periodicities and confirmed across various local regions of the film
537 (Extended Data Fig. 2e,f). The SiO₂ interlayer thickness from low-magnification wide field-of-
538 view (FoV) imaging was determined by the same method (Extended Data Fig. 6a). In particular,
539 the intensity line scan from the wide FoV image (Extended Data Fig. 6a) is obtained from averag-
540 ing across the entire FoV specified by the teal-colored box (~ 150 nm). Next, the inflection points
541 of the intensity peak were used as the criteria to set the boundaries of the SiO₂ interlayer (Extended
542 Data Fig. 6a). This methodology was also utilized to determine the boundaries of the HfO₂-ZrO₂
543 layers from the EELS spectrum (Extended Data Fig. 1c). Regarding the wide FoV cross-sectional
544 TEM (Extended Data Fig. 6a), both the low atomic weight and lack of crystallinity of the SiO₂
545 layer contribute to its weak scattering (bright color), which aids in the visual delineation of the
546 layer boundaries and the thickness extraction from the corresponding averaged intensity line scan.

547 **Optical microscopy** Second harmonic generation (SHG) measurements (Extended Data
548 Fig. 2d) were performed with a Ti:sapphire femtosecond laser (Tsunami, Spectra Physics, $\lambda \sim 800$
549 nm, frequency ~ 80 MHz). The linearly polarized femtosecond laser beam was focused through
550 50X objective lens (NA ~ 0.42) which results in a focal spot size of $2 \mu\text{m}$. The generated SHG
551 signal was collected through the same objective lens and separated from the fundamental beam by
552 the harmonic separator. After passing through the optical bandpass filter, the SHG signals were
553 registered to the photon multiplier tube (PMT) without a polarizer. The fundamental beam was
554 mechanically chopped, and the signal collected by the PMT was filtered by a lock-in amplifier
555 to reduce the background noise. For SHG spatial mapping, a two-axis piezo stage was utilized
556 and the coordinate was synchronized with the PMT signal. The SHG intensity was obtained by
557 averaging the mapping signals across a $100 \mu\text{m} \times 100 \mu\text{m}$ sample area.

558 **X-ray characterization**

559 **X-ray reflectivity** Synchrotron X-ray reflectivity (XRR) – performed at Sector 33-BM-C
560 beamline of the Advanced Photon Source, Argonne National Laboratory and at Beamline 2-1 of the
561 Stanford Synchrotron Radiation Lightsource, SLAC National Accelerator Laboratory – confirmed
562 the thickness of HfO₂-ZrO₂ heterostructures (Extended Data Fig. 1b). The overall thickness of
563 the HfO₂-ZrO₂ heterostructures is consistent with the growth rate ($\sim 1 \text{ \AA/cycle}$) of ALD-grown
564 Zr:HfO₂ as demonstrated in our previous work¹³. Furthermore, the presence of irregularly spaced
565 fringes in the thicker HfO₂-ZrO₂ heterostructures suggests the presence of well-separated HfO₂-
566 ZrO₂ layers, i.e. not a solid solution. This is confirmed by XRR fitting (Extended Data Fig. 1b)
567 performed with the python package GenX⁵³ which considers factors such as density, roughness,
568 and thickness.

569 **Grazing incidence diffraction: in-plane** Synchrotron in-plane grazing-incidence diffrac-
570 tion (GID) (Fig. 1e and Extended Data Fig. 2a) was performed at Sector 33-ID-D beamline of
571 the Advanced Photon Source, Argonne National Laboratory. A Pilatus-II 100K Area Detector
572 mounted on the del-arm was used to collect diffraction signal with a grazing incidence geometry.
573 The region-of-interest on the detector was set such that the ring-like signal was fully integrated. In-
574 plane GID was collected by sweeping the in-plane angle ν (8-50°) with a fixed out-of-plane grazing
575 angle δ ($\delta = 0.9^\circ$); the corrected Bragg angle (2θ) over which the data is plotted and indexed is de-
576 termined from the relationship $\cos 2\theta = \cos \nu \cdot \cos \delta$ set by the geometry of the diffractometer.
577 The X-ray source was fixed at 16 keV ($\lambda = 0.775 \text{ \AA}$). In-plane diffraction yields more diffraction
578 peaks with better defined width, likely due to the preferred orientation and disc-shape domains in
579 the film. Therefore, in-plane GID enables clear indexing to the ferroelectric orthorhombic (Pca2₁)
580 and antiferroelectric tetragonal (P4₂/nmc) fluorite structure in the ultrathin HfO₂-ZrO₂ films, as
581 the presence of many reflections from the in-plane GID spectra (Fig. 1e, Extended Data Fig. 2a)
582 allow for clear distinction from other nonpolar fluorite-structure polymorphs. Such diffraction
583 spectra would be otherwise prohibited in typical out-of-plane geometry due to the lack of vertical
584 diffraction planes and the large linewidth inherent to ultrathin films.

585 **Two-dimensional diffraction** Two-dimensional reciprocal space maps (Extended Data Fig.
586 2b) were measured at Beamline 11-3 of the Stanford Synchrotron Radiation Lightsource, SLAC
587 National Accelerator Laboratory. Rayonix MX225 CCD area detector collected diffraction flux in
588 grazing incidence ($< 0.20^\circ$) geometry; the X-ray source (50 microns vertical x 150 microns hor-
589 izontal beam size) was fixed at 12.7 keV. The sample-detector work distance was set to 80 mm
590 to enable detection of a wide region of reciprocal space (Q -range 0.2 to 5 \AA^{-1}) at the expense of
591 reciprocal space resolution, set by the pixel size. The two-dimensional diffraction scans – in which
592 a wide portion of the entire reciprocal space was collected simultaneously, rather than at discrete
593 regions in Q_x - Q_y space – were averaged over data collection time and for repeated scans. These
594 measurement features, in tandem with the high X-ray flux afforded by the synchrotron source, en-
595 abled sufficient diffraction signal detection and contrast in films just two nanometers in thickness.
596 Data analysis was performed Nika, an Igor Pro package for correction, calibration and reduction of
597 two-dimensional areal maps into one-dimensional data⁵⁴. Two-dimensional reciprocal space maps
598 on bare HfO_2 - ZrO_2 heterostructures confirm the presence of crystalline ultrathin films despite the
599 low deposition temperature, afforded by the low crystallization temperature of ZrO_2 on Si ⁵¹.

600 **Ferrioic phase identification from diffraction** For fluorite-structure thin films, the main
601 phases to consider are the dielectric monoclinic ($\text{P}2_1/\text{c}$), antiferroelectric tetragonal ($\text{P}4_2/\text{nmc}$),
602 and ferroelectric orthorhombic ($\text{Pca}2_1$) phases. Various diffraction reflections from the wide-angle
603 IP-GiD spectra enable indexing to the orthorhombic $\text{Pca}2_1$ phase. Lattice parameters (a , b , c)
604 – determined via Bragg’s law from the d_{200} family of reflections – are self-consistently checked
605 against the (111) lattice spacing $\frac{1}{d_{111}^2} = \frac{1}{a^2} + \frac{1}{b^2} + \frac{1}{c^2}$ as well as other higher-order reflections present
606 in the in-plane diffraction spectra (Extended Data Fig. 2a). For example, the lattice parameters
607 extracted from the {200} peaks were $a = 5.36 \text{ \AA}$, $b = 5.23 \text{ \AA}$, and $c = 5.47 \text{ \AA}$. This corresponds to a
608 d_{211} lattice spacing of 2.209 \AA , which agrees well with the lattice spacing (2.205 \AA) obtained from
609 Bragg’s law based on the peak position (Extended Data Fig. 2a)

610 The monoclinic phase was ruled out due to a lack of two {111} peaks in the diffraction spec-
611 tra and the $(111)_o$ and $(101)_t$ reflections being significantly offset from its expected peak position

612 in the monoclinic phase. With regards to the indexing of tetragonal (101)_t peak (Extended Data
613 Fig. 2a), it is always reported that the tetragonal (101)_t reflection has a smaller *d*-spacing⁵⁵ in
614 thicker HfO₂-based films²⁸, and is therefore expected to be present at a higher angle compared to
615 the orthorhombic (111)_o reflection, which is the case in the indexed diffraction spectra (Extended
616 Data Fig. 2a) based on the self-consistent indexing methodology outlined above provides.

617 In terms of extracting the phase fraction of the tetragonal and orthorhombic phases, while
618 Rietveld refinement has been applied to grazing incidence x-ray diffraction of thick (10 nm)
619 Zr:HfO₂⁵⁶ to determine the orthorhombic phase fraction, that methodology cannot be applied in
620 the ultrathin regime, as the films are highly oriented, as opposed to fully polycrystalline (Extended
621 Data Fig. 2b), which is a requirement to apply Rietveld refinement.

622 **X-ray absorption spectroscopy** Hard and soft synchrotron X-ray spectroscopy (Extended
623 Data Fig. 2c) was measured at beamline 4-ID-D of the Advanced Photon Source, Argonne Na-
624 tional Laboratory and Beamline 4.0.2. of the Advanced Light Source, Lawrence Berkeley National
625 Laboratory, respectively. Spectroscopy measurements were taken at the oxygen *K*-edge (520-550
626 eV), zirconium *M*_{3,2}-edge (325-355 eV), hafnium *M*₃-edge (2090-2150 eV), and zirconium *L*_{3,2}-
627 edge (2200-2350 eV). X-rays were incident at 20° off grazing. XAS (XLD) was obtained from the
628 average (difference) of horizontal and vertical linearly polarized X-rays. To eliminate systematic
629 artifacts in the signal that drift with time, spectra measured at ALS were captured with the order
630 of polarization rotation reversed (e.g., horizontal, vertical, vertical, and horizontal) in successive
631 scans, in which an elliptically polarizing undulator tuned the polarization and photon energy of the
632 synchrotron X-ray source⁵⁷. Spectra measured at ALS were recorded under total electron yield
633 (TEY) mode⁵⁷ from room temperature down to 100 K. Spectra measured at APS were recorded
634 under various modes: total electron yield (TEY), fluorescence yield (FY), and reflectivity (REF).

635 **Ferroic phase identification from spectroscopy** X-ray spectroscopy provides various sig-
636 natures to distinguish the competing ferroelectric orthorhombic (Pca2₁) and antiferroelectric tetrag-

637 onal ($P4_2/nmc$) phase. Simulated XAS spectra at the oxygen K -edge (Extended Data Fig. 3d) for
638 ZrO_2 in the various fluorite-structure polymorphs (orthorhombic $Pca2_1$ and tetragonal $P4_2/nmc$)
639 were computed through the Materials Project⁵⁸ open-source database for XAS spectrum⁵⁹. The
640 T -phase ($P4_2/nmc$) nonpolar distortion (D_{4h} , 4-fold prismatic symmetry) from regular tetrahe-
641 dral (T_d , full tetrahedral symmetry) fluorite-structure symmetry does not split the degenerate e -
642 bands ($d_{x^2-y^2}$, $d_{3z^2-r^2}$), as confirmed by experiment⁶⁰ and the aforementioned XAS simulations¹³.
643 Meanwhile, the O -phase ($Pca2_1$) polar rhombic pyramidal distortion (C_{2v} , 2-fold pyramidal sym-
644 metry) does split the e -manifold based on crystal field symmetry, providing a spectroscopic means
645 to distinguish the T - and O -phases. The additional spectroscopic feature present between the
646 main e - and t_2 - absorption features due to orthorhombic symmetry-lowering distortion is illus-
647 trated by its crystal field diagram (Extended Data Fig. 3b). This provides a spectroscopic finger-
648 print for phase identification beyond diffraction which can often be ambiguous due to the nearly
649 identical T - and O -phase lattice parameters. For the 2 nm HfO_2 - ZrO_2 - HfO_2 trilayer, the exper-
650 imental O K -edge XAS spectra demonstrates tetrahedral and rhombic splitting features closely
651 matching the polar O -phase ($Pca2_1$) emerge slightly below room temperature, indicative of the
652 mixed tetragonal-orthorhombic to orthorhombic phase transition upon cooling. This temperature-
653 dependent tetragonal-orthorhombic structural evolution is expected for fluorite-structure thin films⁶¹
654 and is consistent with temperature-dependent capacitance measurements (Extended Data Fig. 3f).
655 Further XAS phase identification details are provided in previous work on ultrathin $Zr:HfO_2$
656 films¹³.

657 **X-ray photoelectron spectroscopy** Angle-resolved photoelectron spectroscopy (ARPES)
658 was performed using a Phi Versaprobe III at the Stanford Nano Shared Facilities (Extended Data
659 Fig. 1d). A monochromated aluminum source was used to give a photon energy of 1486.6 eV. Data
660 was fit and analyzed using CasaXPS. Angle-dependent XPS at various incident grazing angles
661 enabled depth-resolved composition analysis to help confirm the HfO_2 - ZrO_2 multilayer structure.

662 **Dielectric measurements**

663 **Metal-oxide-semiconductor (MOS) capacitance** Capacitance-voltage (C - V) measurements
664 were performed using a commercial Semiconductor Device Analyzer (Agilent B1500) with a
665 multi-frequency capacitance measuring unit (MFCMU). 19 micron W tips (d.c.P-HTR 154-001,
666 FormFactor) made electrical contact within a commercial probe station (Cascade Microtech); volt-
667 age was applied to the W top electrode and the lightly-doped Si bottom electrode was grounded.
668 To eliminate contributions from series and parasitic resistances, frequency-dependent C - V mea-
669 surements were performed. In particular, C - V data was analyzed at two frequencies (100-500 kHz
670 regime) to allow for the extraction of accurate frequency-independent C - V via a three-element
671 circuit model consisting of the capacitor and the parasitic series and parallel resistors⁶². The
672 frequency-independent capacitance is given by

$$C = \frac{f_1^2 C_1 (1 + D_1^2) - f_2^2 C_2 (1 + D_2^2)}{f_1^2 - f_2^2} \quad (1)$$

673 where C_i and D_i refer to the measured capacitance in parallel mode (C_p - R_p) and dissipation values
674 at frequency f_i . The dissipation factor is given by $D = -\cot \theta$, where θ is the phase. In order to
675 maximize the accuracy of this method, it is important the the dissipation factors are small ($\ll 1$) at
676 the frequencies chosen; therefore, high frequencies were selected.

677 **Permittivity extraction** The permittivity of Al_2O_3 and HfO_2 dielectric layers was ex-
678 tracted from thickness-dependent MOS C - V measurements on lightly-doped p substrates (Ex-
679 tended Data Fig. 6). In the accumulation region of the MOS C - V measurements, the MOS ca-
680 pacitor can be modeled as three capacitors (Al_2O_3 or HfO_2 dielectric layer, SiO_2 interlayer, and Si
681 space charge layer) in series using the following equation,

$$\frac{1}{C} = \frac{1}{\epsilon_0 \epsilon_{H\kappa}} t_{H\kappa} + \frac{1}{\epsilon_0 \epsilon_{\text{SiO}_2}} \left[t_{\text{SiO}_2}^{\text{phys}} + t_{\text{CL}} \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{Si}}} \right], \quad (2)$$

682 where $t_{H\kappa}$ is the thickness of the high- κ (Al_2O_3 or HfO_2) layer, $t_{\text{SiO}_2}^{\text{phys}}$ is the physical SiO_2 thickness,
683 and t_{CL} is the charge layer thickness in silicon. The physical SiO_2 thickness is constant across all
684 of the thickness series (Al_2O_3 and HfO_2 single layers). Additionally, the capacitance values were
685 extracted at various values of fixed charge ($Q = 0$ to $-3 \mu\text{C}/\text{cm}^2$) which ensures that the charge-
686 layer thickness is constant across all thicknesses and in the accumulation region. Therefore, from

Equation 2, the inverse capacitance at a fixed charge as a function of film thickness should result in a line and the permittivity can be extracted from the slope. This yielded extracted permittivities of 9 and 19 for the Al₂O₃ and HfO₂ thickness series, respectively, as expected for these systems. Note that for the HfO₂ thickness series, thicknesses of 6 nm and higher were used to ensure HfO₂ stabilizes in the dielectric monoclinic phase ($\kappa \sim 18$)³⁶.

Similarly, the permittivity of the HfO₂-ZrO₂ heterostructures was extracted from thickness-dependent MIM *C-V* measurements (Fig. 2b). The inverse capacitance is a linear function of the film thickness, and the permittivity can be extracted from the slope.

Electrical interlayer thickness extraction The thickness of the SiO₂ interlayer was determined not only by TEM (Extended Data Fig. 6a), but also electrically via *C-V* measurements of both dielectric HfO₂ and Al₂O₃ thickness series on SiO₂-buffered Si (Extended Data Fig. 6f). From Equation 2, the inverse capacitance at a fixed charge as a function of dielectric thickness should result in a line and the capacitance-equivalent thickness (CET) of the SiO₂ interlayer and Si charge layer can be extracted from the y-intercept. By extracting the CET at different charge values, the *Q-V* relation of the SiO₂ interlayer and Si charge layer can be calculated through the following equation

$$V - V_{fb} = \int_0^Q \frac{t_{SiO_2}^{phys} + t_{CL} \frac{\epsilon_{SiO_2}}{\epsilon_{Si}}}{\epsilon_0 \epsilon_{SiO_2}} dQ, \quad (3)$$

where V_{fb} is the flatband voltage (Extended Data Fig. 6b,d). To confirm this methodology, another method for determining the *Q-V* relation of the SiO₂ interlayer and Si charge layer was extracted from the *Q-V* relations of both the dielectric HfO₂ and Al₂O₃ thickness series. At a fixed charge, the corresponding voltage values of each thickness were fit to a line and the y-intercept corresponds to the voltage value for the SiO₂ interlayer and Si charge layer *Q-V* relation (Extended Data Fig. 6c,e). As expected, both methods lead to the same extracted *Q-V* relation (Extended Data Fig. 6c,e), corresponding to 8 Å EOT (Extended Data Fig. 6f) – close to the SiO₂ physical thickness of 8.5 Å obtained via TEM (Extended Data Fig. 6a) – based on simulated TCAD *Q-V* relations of different SiO₂ thicknesses on lightly-doped Si.

712 **Hysteretic C - V measurements** Capacitance-voltage (C - V) measurements on MIM capac-
713 itors were performed using a commercial Semiconductor Device Analyzer (Agilent B1500) with
714 a multi-frequency capacitance measuring unit. 19 micron W tips (d.c.P-HTR 154-001, FormFac-
715 tor) made electrical contact within a commercial probe station (Cascade Microtech); voltage was
716 applied to the W top electrode and the W bottom electrode was grounded.

717 **Electrical characterization**

718 **Bechmarking to HKMG literature** In Figure 3a, the leakage-effective oxide thickness
719 (J_G -EOT) scaling of negative capacitance multilayer gate stack benchmarked against reported
720 HKMG literature includes references taken from interlayer-scavenged 2 nm HfO₂^{16,18,63} (red),
721 high- κ doped HfO₂¹⁸ (blue), and SiO₂/poly-Si³ (gray). In Figure 3b, the normalized mobility ver-
722 sus EOT scaling of the negative capacitance multilayer gate stack benchmarked against reported
723 HKMG literature includes references taken from interlayer-scavenged 2 nm HfO₂^{16,18,64} (red) and
724 hybrid silicate-scavenged interlayer¹⁶ (magenta). In the Figure 3b inset, the SiO₂ interlayer thick-
725 ness versus EOT scaling scatter plot considers the 7.0 Å EOT HfO₂-ZrO₂-HfO₂ trilayer to HKMG
726 references which employ interlayer scavenging to reduce EOT^{16,18,63,65}.

727 **Transistor transfer and output characteristics** Transistor I_d - V_g and I_d - V_d characteriza-
728 tion of short-channel and long-channel transistors were performed using a commercial Semicon-
729 ductor Device Analyzer (Agilent B1500). 19 micron W tips (d.c.P-HTR 154-001, FormFactor)
730 made electrical contact within a commercial probe station (Cascade Microtech); voltage was ap-
731 plied to the gate and drain contacts, while the source and Si substrate were grounded.

732 **Mobility extraction** The low-field transistor mobility is calculated based on the channel
733 resistance (R_{ch}) and inversion sheet charge density (Q_{inv}), which are extracted respectively from
734 transfer characteristics ($I_D - V_{GS}$) and from the gate-to-channel capacitance-voltage ($C_{gc} - V_{GS}$)
735 measurements. Given the the device aspect ratio of channel length (L) and channel width (W), we

736 have

$$R_{ch}(V_{GS}) = \frac{L}{W} \times \frac{1}{\mu_{eff}(V_{GS})Q_{inv}(V_{GS})} \quad (4)$$

737 Firstly, the channel resistance is extracted at 50 mV drain-to-source bias (V_{DS}) by subtracting the
738 parasitic resistance (R_p) from the measured drain-to-source resistance (R_{DS}).

$$R_{DS}(V_{GS}) = \frac{V_{DS}}{I_D(V_{GS})} = R_{ch}(V_{GS}) + R_p \quad (5)$$

739 where R_p is ascribed to the resistance of the source and the drain contacts and the n+ extension
740 regions that are extrinsic to the channel region. When the overdrive voltage ($V_{ov} = V_{GS} - V_t$,
741 where V_t is the threshold voltage) is sufficiently large, R_{ch} is known to be inversely proportional to
742 V_{ov} according to 4. Therefore, R_p can be extracted using a linear extrapolation of the $R_{DS} - 1/V_{ov}$
743 relationship (Extended Data Fig. 7e), which is derived from the $I_D - V_{GS}$ from which the threshold
744 voltage (V_t) can be characterized with the max- g_m method. Secondly, the $C_{gc} - V_{GS}$ of a large
745 ($W=L=50\mu m$) device (Extended Data Fig. 7a) is integrated and normalized to the channel area
746 ($A=2500\mu m^2$) to estimate the inversion charge.

$$Q_{inv}(V_{GS}) \approx \int_{-\infty}^{V_{GS}} \frac{C_{gc}(v_{gs})}{A} dv_{gs} \quad (6)$$

747 The large device dimensions minimizes the parasitic capacitance contribution to ensure C_{gc} is
748 representative of the inversion electron responses. Finally, we combine the above characterizations
749 to obtain the effective mobility using Equation 4 (Extended Data Fig. 7f).

750 **Transconductance extraction** The measured transconductance ($g_m = \partial I_D / \partial V_{GS}$) and the
751 output conductance ($g_{ds} = \partial I_D / \partial V_{DS}$) are affected by the series resistance on the source (R_S) and
752 the drain sides (R_D), as they reduce the voltage drops on the channel region,

$$V_{GSi} = V_{GS} - I_D R_S \quad (7)$$

$$V_{DSi} = V_{DS} - I_D (R_S + R_D) \quad (8)$$

753 where V_{GSi} and V_{DSi} are the gate-to-source and the drain-to-source voltages intrinsic to the chan-
754 nel, respectively. $R_S \approx R_D \approx R_p/2$ because the transistor is symmetric.

755 R_p can be extracted from the $R_{DS} - 1/V_{ov}$ relationships as discussed in the "Mobility Ex-
756 traction" Methods section (Extended Data Fig. 9b). Besides, devices with different gate length
757 (L_g) series are fabricated on the Silicon-On-Insulator (SOI) wafer, which enables another extrac-
758 tion method with $R_{SD} - L_g$ relations. At low V_D and a given V_{ov} , Q_{inv} and μ_{eff} are unchanged
759 across different L_g if short-channel effect is not significant, making R_{ch} proportional to the channel
760 length. Such condition is confirmed by the consistency of V_t across measured L_g (Extended Data
761 Fig. 9a). Therefore, the L_g offset as well as the R_p can be found at the intersect of the linear rela-
762 tions of the $R_{SD} - L_g$ with different V_{ov} (Extended Data Fig. 9c). The two R_p extraction methods
763 yield consistent results.

764 The following equation is solved to extract the intrinsic $g_{mi} = \partial I_D / \partial V_{GSi}$ and $g_{dsi} =$
765 $\partial I_D / \partial V_{DSi}$ without the degradation due to R_S and R_D .

$$\begin{pmatrix} 1 - g_m R_S & -g_m (R_S + R_D) \\ -g_{ds} R_S & 1 - g_{ds} (R_S + R_D) \end{pmatrix} \begin{pmatrix} g_{mi} \\ g_{dsi} \end{pmatrix} = \begin{pmatrix} g_m \\ g_{ds} \end{pmatrix} \quad (9)$$

766 where g_m and g_{ds} are measured, and $R_S \approx R_D \approx R_p/2$ from the above discussed characterizations.
767 Using this methodology, the intrinsic g_{mi} and intrinsic g_{dsi} are extracted (Fig. 3f, Extended Data
768 Fig. 9d,e).

769 **RF measurements** Scattering-parameters (S parameters) for $L_G = 1 \mu\text{m}$ bulk transistors
770 (henceforth referred to as the device under test, DUT) at various DC biases as well as open and
771 short structures (Extended Data Fig. 8a) are measured using a Keysight E8361C Network An-
772 alyzer in conjunction with a Keysight 4155C Semiconductor Parameter Analyzer. The devices
773 were measured using low contact resistance Infinity Series probes. To calibrate the measurement
774 setup, a line-reflect-reflect-match (LRRM) calibration was performed with a Cascade Microtech
775 Impedance Standard. Following calibration, S -parameters were measured for each of the DUT,
776 open, and short structures. These measured S -parameters were converted to admittance param-
777 eters (Y -parameters), Y_{DUT} , Y_{open} , and Y_{short} . In order to remove the effects of parasitic shunt
778 parasitic pad capacitance and series pad resistance and inductance of the DUT, the following de-
779 embedding process was followed. First, to decouple the effect of shunt parasitic capacitances, the

780 Y parameters of the open structure (Y_{open}) are subtracted from the Y parameters of the DUT and
 781 short structure, and then are converted to impedance parameters (Z parameters):

$$Z_1 = (Y_{DUT} - Y_{open})^{-1} \quad (10)$$

$$Z_2 = (Y_{short} - Y_{open})^{-1} \quad (11)$$

782 Next, to decouple the effect of series pad resistance and inductance of DUT, Z_2 is subtracted from
 783 Z_1 and the resulting difference is converted back to admittance parameters, Y_{corr} :

$$Y_{corr} = (Z_1 - Z_2)^{-1} \quad (12)$$

784 Y_{corr} represents the de-embedded admittance parameters of the DUT. This de-embedding proce-
 785 dure is schematically represented in Extended Data Fig. 8a.

786 To extract the total gate capacitance (C_{gg}) and transconductance (g_m) from the de-embedded
 787 admittance parameters, a small-signal model of the transistor was assumed (Extended Data Fig.
 788 8b). Under this small-signal model, the Y -parameters can be written in terms model parameters
 789 and frequency (assuming $R_s = R_d = 0$, $C_{gg} = C_{gs} + C_{gd}$, and $4\pi^2 C_{gg}^2 R_g^2 f^2 \ll 1$)

$$Y_{11} = 4\pi^2 C_{gg}^2 R_g f^2 + 2\pi f C_{gg} j \quad (13)$$

$$Y_{12} = -4\pi^2 C_{gd} C_{gg} R_g f^2 - 2\pi f C_{gd} j \quad (14)$$

$$Y_{21} = g_m - 4\pi^2 C_{gd} C_{gg} R_g f^2 + 2\pi f (C_{gd} + g_m R_g C_{gg}) j \quad (15)$$

$$Y_{22} = g_{ds} + 4\pi^2 C_{gd} R_g (C_{gd} + C_{gg} g_m R_g) f^2 + 2\pi f (C_{ds} + C_{gd} + C_{gd} g_m R_g) j. \quad (16)$$

790 The transconductance (g_m) can therefore be extracted at a fixed DC bias via the following relation
 791 (Fig. 3c, Extended Data Fig. 9c).

$$g_m = \text{Re}(Y_{21}) \Big|_{f^2=0} \quad (17)$$

792 **Charge boost measurements** Pulsed charge-voltage measurements (Extended Data Fig.
 793 10) were conducted on p- Si/SiO₂/HfO₂-ZrO₂ (2 nm)/TiN/W capacitor structures to extract the
 794 energy landscape of the ferroic HfO₂-ZrO₂ heterostructure, following the measurement scheme

795 detailed in previous works^{47, 66-68}. The capacitor structures were connected to an Agilent 81150A
796 Pulse Function Arbitrary Noise Generator and the current and voltage was measured through an
797 InfiniiVision DSOX3024A oscilloscope with a 50 Ω and 1 M Ω input impedance, respectively.
798 Short voltage pulses (500 ns) with increasing amplitudes were applied to the capacitor (Extended
799 Data Fig. 10c). From the integration of the measured discharging current, a charge vs voltage
800 relationship was extracted (Extended Data Fig. 10d). The voltage was calculated by $\max(V - IR)$,
801 where V is the applied voltage pulse, I is the measured current, and R is a combination of the
802 oscilloscope resistance (50 Ω) and parasitic resistances associated with the setup and lightly-doped
803 substrate (220 Ω). Fast voltage pulses were applied in order to minimize charge injection into
804 the ferroelectric-dielectric interface, which could mask the observation of the negative capacitance
805 regime^{47, 67}. Additionally, short voltage pulses help prevent electrical breakdown of the SiO₂ layer.
806 In order to determine the $P-E_F$ relation of the 2 nm HfO₂-ZrO₂ heterostructure, the electric field
807 across the ferroic HfO₂-ZrO₂ heterostructure was calculated by subtracting the voltage across the
808 series capacitance of the SiO₂ interlayer and Si charge layer (V_D) at a fixed charge value,

$$E = \frac{1}{t} (V - V_D), \quad (18)$$

809 where t is the thickness of the HfO₂-ZrO₂ heterostructure. The $Q-V$ relation of the series ca-
810 pacitance of the SiO₂ interlayer and Si charge layer was determined via thickness-dependent $C-V$
811 measurements of Al₂O₃ and HfO₂ (Extended Data Fig. 6, Methods, Electrical interlayer thickness
812 extraction), which corresponded to 8 Å SiO₂ on lightly-doped Si. The charge boost due to neg-
813 ative capacitance was calculated by integrating the difference between the $Q-V$ relations of the 2
814 nm HfO₂-ZrO₂ heterostructure and the series combination of the SiO₂ interlayer and the Si charge
815 layer (Extended Data Fig. 10e).

816 **Modeling**

817 **Landau phenomenology of antiferroelectric-ferroelectric system** The qualitative en-
818 ergy landscape for a mixed ferroelectric-antiferroelectric material (Fig. 1a) was calculated by
819 assuming a series combination of antiferroelectric and ferroelectric layers connected to a voltage

820 source V_s . The energy landscape potentials were calculated via the Landau-Ginzburg-Devonshire
 821 (LGD) formalism (without strain coupling)⁶⁹⁻⁷¹:

$$U_{FE} = (\alpha_{FE}P^2 + \beta_{FE}P^4 + \gamma_{FE}P^6 - E_{FE}P)t_{FE} \quad (19)$$

$$U_{AFE} = (\alpha_{AFE}(P_a^2 + P_b^2) + \delta_{AFE}P_aP_b + \beta_{AFE}(P_a^4 + P_b^4) \\ + \gamma_{AFE}(P_a^6 + P_b^6) - E_{AFE}(P_a + P_b))t_{AFE} \quad (20)$$

822 For the antiferroelectric layer, the energy landscape assumes two sublattices (P_a, P_b) with sponta-
 823 neous, antiparallel dipoles. In order to express the AFE energy landscape in terms of total polar-
 824 ization, a change of variables was performed ($P = P_a + P_b, A = P_a - P_b$). The antiferroelectric
 825 profile therefore becomes,

$$U_{AFE} = t_{AFE}\left(\frac{1}{2}\alpha_{AFE,p}P^2 + \frac{1}{2}\alpha_{AFE,n}A^2 + \frac{\beta_{AFE}}{8}(P^4 + 6A^2P^2 + A^4) \quad (21) \\ + \frac{\gamma_{AFE}}{32}(P^6 + A^6 + 15P^2A^2(A^2 + P^2)) - E_{AFE}P\right).$$

826 The system is also constrained by electrical boundary conditions at the antiferroelectric/ferroelectric
 827 interface ($\epsilon_0 E_{AFE} + P_{AFE} = \epsilon_0 E_{FE} + P_{FE}$) and that the voltage across both layers must sum up
 828 to V_g ($V_g = E_{FE}t_{FE} + E_{AFE}t_{AFE}$). With these constraints, the combined energy profile is given
 829 by:

$$U_{AFE+FE} = t_{AFE}\left(\frac{1}{2}\alpha_{AFE,p}P_{AFE}^2 + \frac{1}{2}\alpha_{AFE,n}A_{AFE}^2 + \frac{\beta_{AFE}}{8}(P_{AFE}^4 + 6A_{AFE}^2P_{AFE}^2 + A_{AFE}^4) \quad (22) \\ + \frac{\gamma_{AFE}}{32}(P_{AFE}^6 + A_{AFE}^6 + 15P_{AFE}^2A_{AFE}^2(A_{AFE}^2 + P_{AFE}^2))\right) \\ + (\alpha_{FE}P_{FE}^2 + \beta_{FE}P_{FE}^4 + \gamma_{FE}P_{FE}^6)t_{FE} - V_g \frac{P_{FE}t_{FE} + P_{AFE}t_{AFE}}{t_{FE} + t_{AFE}} \\ + \frac{t_{AFE}t_{FE}(P_{AFE} - P_{FE})^2}{\epsilon_0(t_{FE} + t_{AFE})}$$

830 In order to further simplify this expression, we note that the last term represents the electrostatic
 831 energy arising from polarization mismatch at the AFE-FE interface. In general, such mismatch
 832 is quite costly, resulting in nearly uniform polarization across all layers. Therefore, we apply
 833 the approximation ($P_{AFE} = P_{FE} = P$), which sets the last term to 0. Furthermore, in order to
 834 express U as just a function of P , we can generate another constraint by noting that in equilibrium,

835 $\nabla U_A = 0$, resulting in the constraint,

$$0 = A^2 \left(\frac{\beta_{AFE}}{2} + \frac{\gamma_{AFE}}{32} (6A^2 + 60P^2) \right) = -\alpha_{AFE_n} - \frac{3}{2}\beta_{AFE}P^2 - \frac{15}{16}\gamma_{AFE}P^4 \quad (23)$$

836 This constraint allows for the determination of A for any value of P , which allows us to determine
837 U as a function of P (Fig. 1a).

838 **Technology computer-aided design simulations** The measured C - V curves are calibrated
839 to Sentaurus Technology computer-aided design simulations (TCAD) device simulator which solves
840 the electrostatics, electron and hole transports, and the quantum confinement effect self-consistently⁷².
841 MOS capacitors with $1 \times 10^{15} \text{cm}^{-3}$ p-type substrate doping and $L = 50 \mu\text{m}$ planar MOSFET with
842 $2 \times 10^{17} \text{cm}^{-3}$ p-type substrate doping are simulated with finite-element method. The equivalent
843 oxide thickness (EOT) and the metal work function (ϕ_m) are the only two parameters that are fit
844 to the MOS capacitor measurement results, yet the slope of the accumulation capacitance can be
845 successfully captured by the model (Fig. 2f, Extended Data Fig. 6). Similarly, both components
846 (gate-to-channel and gate-to-body) of the MOSFET split C - V are captured by the TCAD model
847 with appropriate EOT, ϕ_m , and an Si/SiO₂ interface state density of $2 \times 10^{12} \text{cm}^{-2} \text{eV}^{-1}$ (Extended
848 Data Fig. 7a).

849 **Atomic-scale HfO₂-ZrO₂ mixed-ferroic heterostructure**

850 **Thickness limits and atomic-scale heterostructures** Recent perspectives on HfO₂-based
851 ferroelectricity for device applications^{9, 73-76} posed the technological challenges stemming from
852 thickness limit concerns of HfO₂-based ferroelectricity, and thereby, negative capacitance. The
853 use of short-period superlattices i.e. nanolaminates is common in the high- κ field to enhance
854 permittivity⁷⁷⁻⁸¹; in particular, rutile-structure TiO₂ is often paired with fluorite-structure HfO₂
855 and/or ZrO₂ in DRAM capacitors⁸². Recently, fluorite-structure nanolaminates were employed to
856 tune the ferroelectric behavior of HfO₂-ZrO₂ films⁸³⁻⁸⁵. However, all of these works have studied
857 nanolaminates with thick periodicity, going as thin as 10 ALD cycles ($\sim 1.1 \text{ nm}$) per superlattice
858 sub-layer⁸³. In this work, we scale down to a much thinner thickness limit while still maintaining

859 physical separation of the individual layers (Extended Data Fig. 1). The reasoning behind using
860 a short-period superlattice structure to scale down the ferroic behavior of $\text{HfO}_2\text{-ZrO}_2$ rather than
861 simply thinning down a solid solution stems from the notorious thickness-dependent ferroelectric
862 behavior in Zr:HfO_2 at fixed composition^{35, 61, 86}. Here, the use of nanolaminated structures can
863 help provide thickness-independent scaling of ferroic order, as has been previously demonstrated
864 to overcome the upper thickness limit of HfO_2 -based ferroelectricity⁸⁵. The persistence of high
865 capacitance for these 2 nm films is notable considering other high- κ dielectric systems suffer from
866 significant permittivity degradation in the thin film (sub-10 nm) regime, particularly TiO_2 - and
867 SrTiO_3 -based oxides^{82, 87}. Sustaining the mixed ferroic order underlying negative capacitance to
868 the 2 nm regime is extremely relevant for advanced technology nodes⁸⁸ which budget only ~ 2 nm
869 for the oxide layer.

870 **Iso-structural polycrystalline multilayer** Previous attempts to heterostructure ferroelec-
871 tric Zr:HfO_2 with dielectric Al_2O_3 ^{47, 67, 68} failed to demonstrate capacitance enhancement, which
872 was attributed to the fixed charges at the ferroelectric-dielectric interface. These charges can screen
873 the ferroelectric polarization, pushing the stable point of the energy well to one the minimum
874 points, and thereby preventing stabilization of negative capacitance regime via depolarization fields
875 from the dielectric. Here, the use of iso-structural $\text{HfO}_2\text{-ZrO}_2$ to serve as both the nonpolar (an-
876 tiferroelectric) and polar (ferroelectric) layers, and leveraging the high (low) onset crystallization
877 temperature of HfO_2 (ZrO_2) on Si^{51} , enables interfaces with diminished defects, allowing for the
878 polar layer to experience the depolarization fields and stabilize in the "forbidden" NC regime. Re-
879 garding the polycrystalline nature of the ultrathin multilayers, it has been experimentally³⁹ and
880 theoretically⁸⁹ established that negative capacitance can be stabilized in the presence of ferroelec-
881 tric domains, as recently reviewed⁷⁵.

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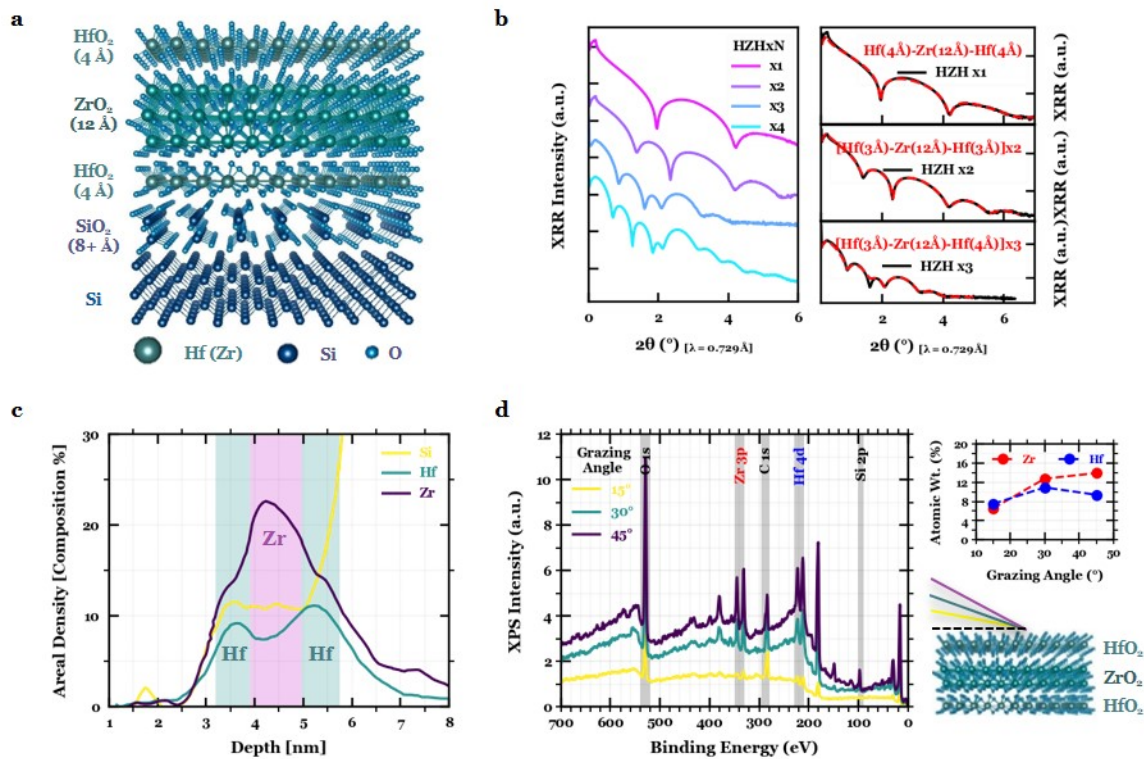
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985 **Author contributions** S.S.C. and S.S. designed the research. S.S.C. performed design, synthesis and
986 optimization of the superlattice oxide heterostructure and its ferroic characterization. C.-H.H. and N.S.
987 performed capacitor fabrication. C.-H.H. helped with optimization of annealing treatments. S.S.C. and
988 N.S. performed capacitor measurements and analysis. L.-C.W. fabricated the transistors and performed DC
989 characterization. S.-L.H. performed TEM. S.S.C. and S.-L.H. performed TEM analysis. Y.H.L. performed
990 all simulations include EOT estimation, series resistance determination and mobility and transconductance
991 analysis. M.S.J., J.G. and W.L. contributed to RF electrical measurements and analysis. D.W.K. initiated
992 the gate oxide synthesis. D.W.K. and J.B. developed the initial processes for transistor fabrication. M.M.,
993 R.R., C.S., D.P., G.P., M.C., B.T. contributed to capacitor fabrication and characterization at MIT LL. Y.R.
994 performed second harmonic generation. S.V. performed X-ray photoelectron spectroscopy. S.S.C. and C.-
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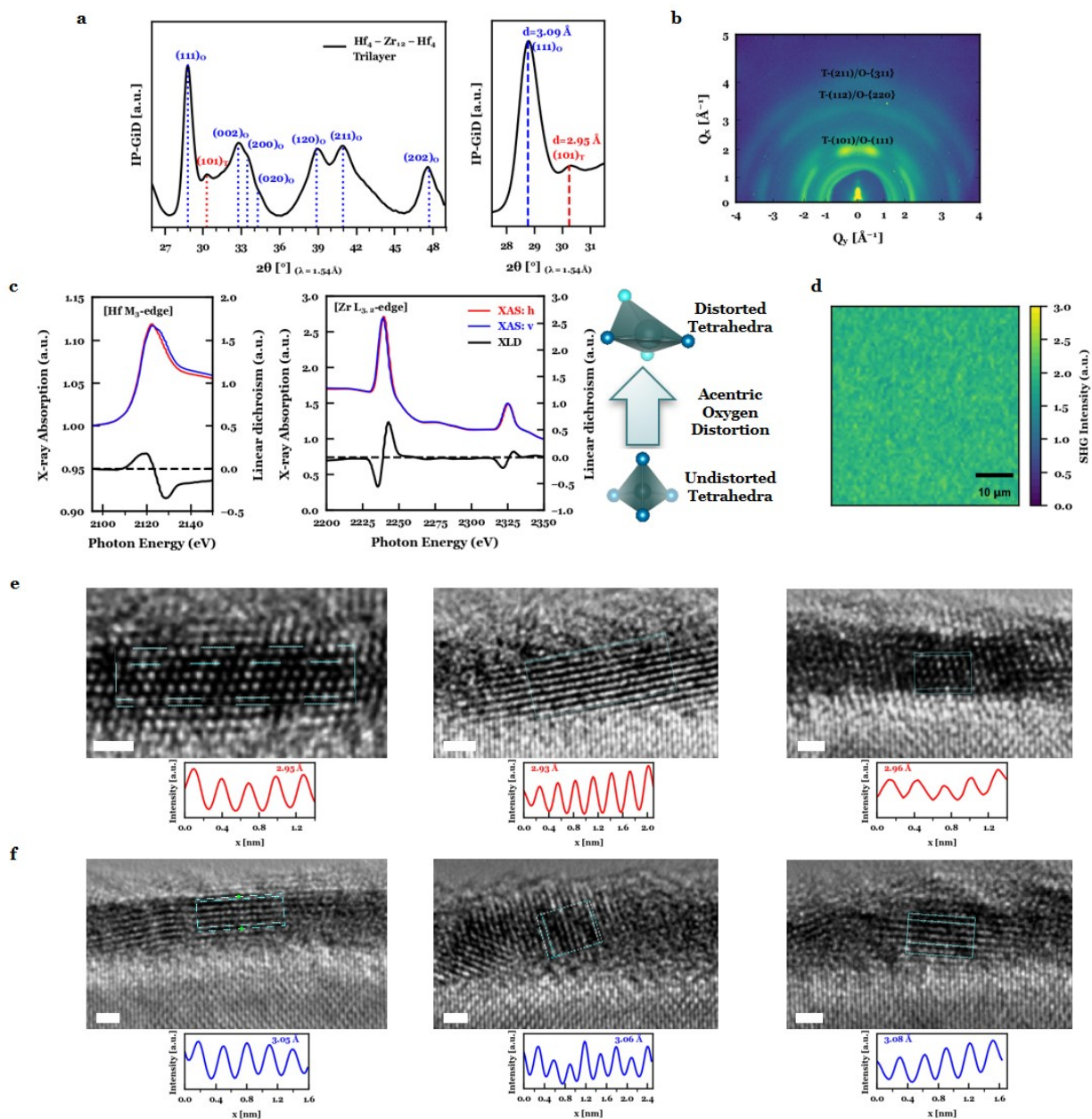
1000 **Competing interests** The authors declare that they have no competing financial interests.

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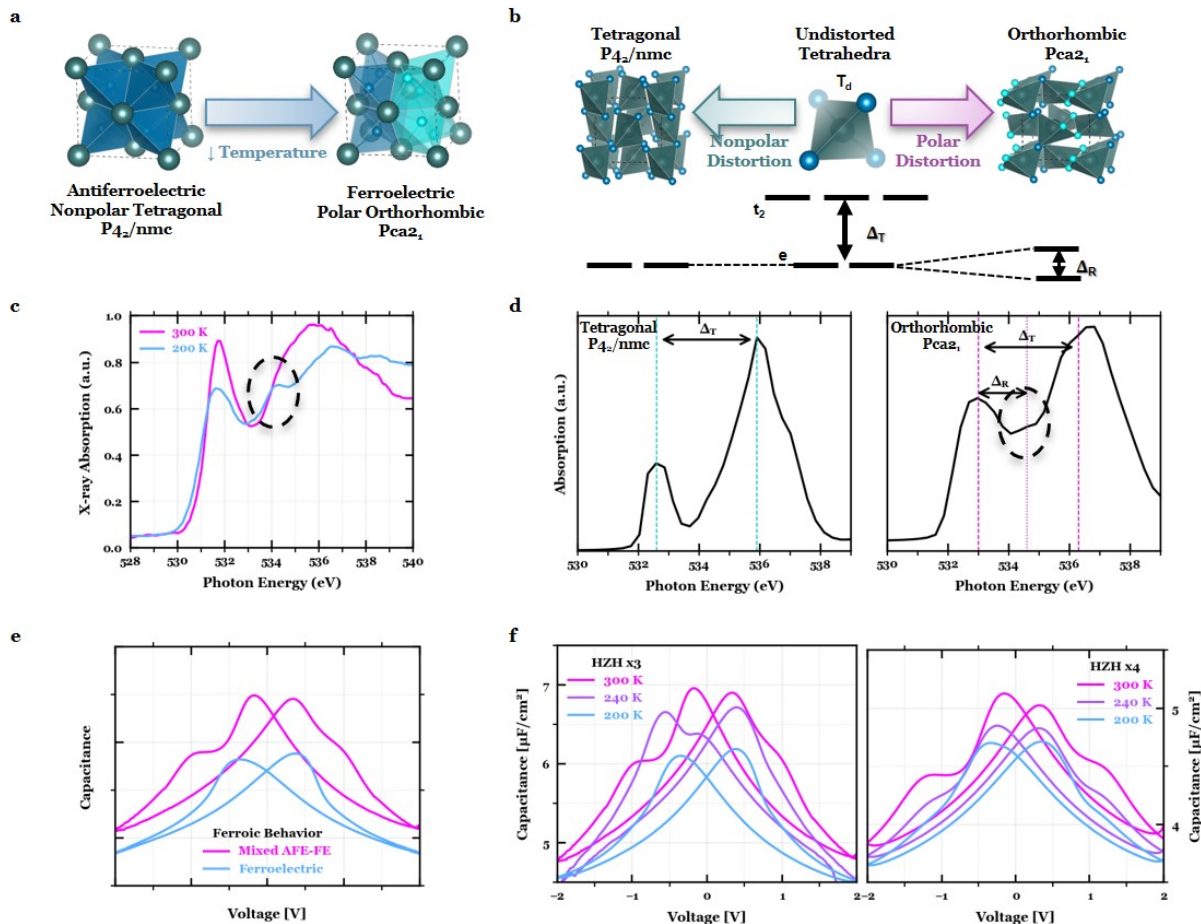
1004 **Extended Data Fig. 1. Atomic-scale multilayer structure.** (a) Schematic of the HfO₂-ZrO₂
 1005 multilayer structure on SiO₂-buffered Si. (b) Synchrotron x-ray reflectivity (XRR) of thicker HfO₂-
 1006 ZrO₂ heterostructures (left) repeated with the same periodicity as the thinner trilayer structure;
 1007 XRR fitting (right) demonstrates the presence of well-separated HfO₂-ZrO₂ layers, i.e. not a solid-
 1008 solution, for three different multilayer repeats of fixed periodicity, all approximately following
 1009 the expected 4 Å - 12 Å - 4 Å HfO₂-ZrO₂-HfO₂ structure. (c) Layer-resolved electron energy
 1010 loss spectroscopy (EELS) of the 2 nm HfO₂-ZrO₂-HfO₂ trilayer, demonstrating clear separation of
 1011 HfO₂-ZrO₂ layers. The exact layer thicknesses are extracted from XRR, which spans a wider sam-
 1012 ple footprint, rather than the local EELS measurement in which the apparent width increase can be
 1013 due to beam spreading and local thickness variation. (d) Angle-resolved X-ray photoelectric spec-
 1014 troscopy (XPS) of the 2 nm HfO₂-ZrO₂-HfO₂ trilayer (left) and the extracted atomic composition
 1015 (right). The presence of increasing Zr-content as the grazing angle increases is expected from the
 1016 multilayer structure in which Zr-content increases after the surface Hf-rich layer.



1017

1018 **Extended Data Fig. 2. Ferroic phase insights from structural characterization.** (a) (left)
 1019 In-plane synchrotron grazing-incidence diffraction (IP-GID) of a bare 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ tri-
 1020 layer indexed to the tetragonal $P4_2/nmc$ and orthorhombic $Pca2_1$ phases and (right) zoom-in of
 1021 the spectrum about the orthorhombic $(111)_o$ and tetragonal $(101)_t$ reflections, confirming the co-

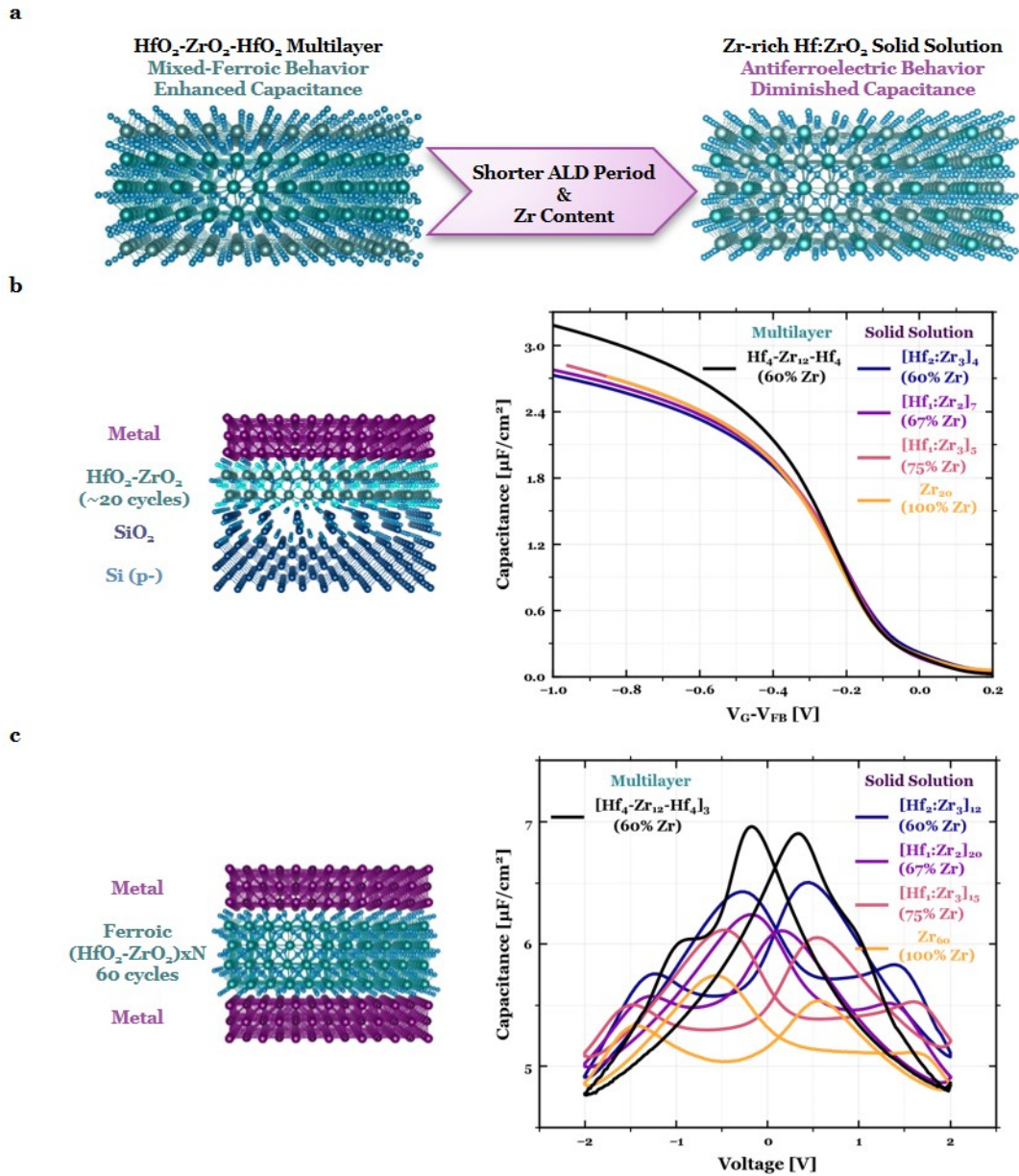
1022 existing structural polymorphs in the 2 nm film. These two peaks were differentiated via self-
1023 consistent indexing of the entire spectrum, in which interplanar lattice spacings – determined from
1024 the $\{200\}_o$ family of reflections – closely match the d -spacings for all other reflections – $(111)_o$,
1025 $(120)_o$, $(211)_o$, $(202)_o$ – determined by Bragg’s law (Methods). **(b)** Two-dimensional reciprocal
1026 space map of the bare 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer, indexed by integrating the diffraction spec-
1027 trum. The lack of fully polycrystalline rings illustrates that the 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer is
1028 highly-oriented, consistent with TEM imaging. **(c)** Synchrotron spectroscopy (XAS) of the bare 2
1029 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer at the (left) Hf M_{3-} and (center) Zr $L_{3,2}$ -edges: (right) the presence
1030 of linear dichroism (orbital polarization) provides further evidence of symmetry-breaking in these
1031 oriented thin films. **(d)** Second harmonic generation (SHG) mapped across the bare 2 nm $\text{HfO}_2\text{-}$
1032 $\text{ZrO}_2\text{-HfO}_2$ trilayer; the presence of SHG intensity confirms broken inversion symmetry in these
1033 ultrathin ferroic films. **(e, f)** Additional cross-sectional TEM providing complementary evidence of
1034 the (e) tetragonal $P4_2/nmc$ and (f) orthorhombic $Pca2_1$ phases, in which the extracted $(101)_t$ lattice
1035 spacing ($\sim 2.95 \text{ \AA}$) and $(111)_o$ lattice spacing ($\sim 3.08 \text{ \AA}$) extracted from IP-GID are consistent
1036 with the average lattice spacings extracted from the periodicity of the TEM-imaged planes. The
1037 white scale bars in all of the TEM images represent 1 nm.



1038

1039 **Extended Data Fig. 3. Ferroic phase insights: proximity to temperature-dependent phase**
 1040 **transition.** (a) Schematic of temperature-dependent antiferroelectric-ferroelectric phase evolu-
 1041 tion in fluorite-structure oxides. At lower temperatures, the higher symmetry tetragonal phase is
 1042 expected to transition to the lower symmetry orthorhombic phase. (b) Schematic crystal field split-
 1043 ting diagram for fluorite-structure polymorphs; symmetry-induced e-splitting provides a spectro-
 1044 scopic signature for the polar *O*-phase (Methods). (c) Temperature-dependent XAS at the oxygen
 1045 *K*-edge for a 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ bare film demonstrating clearer spectroscopic signatures of
 1046 the ferroelectric *O*-phase emerge slightly below room temperature. (d) Simulated oxygen *K*-edge
 1047 XAS spectra (Materials Project) for the respective *O*- and *T*-phases. XAS provides spectroscopic
 1048 signatures to distinguish between the *O*- and *T*- phases (difficult to resolve from GI-XRD). (e)

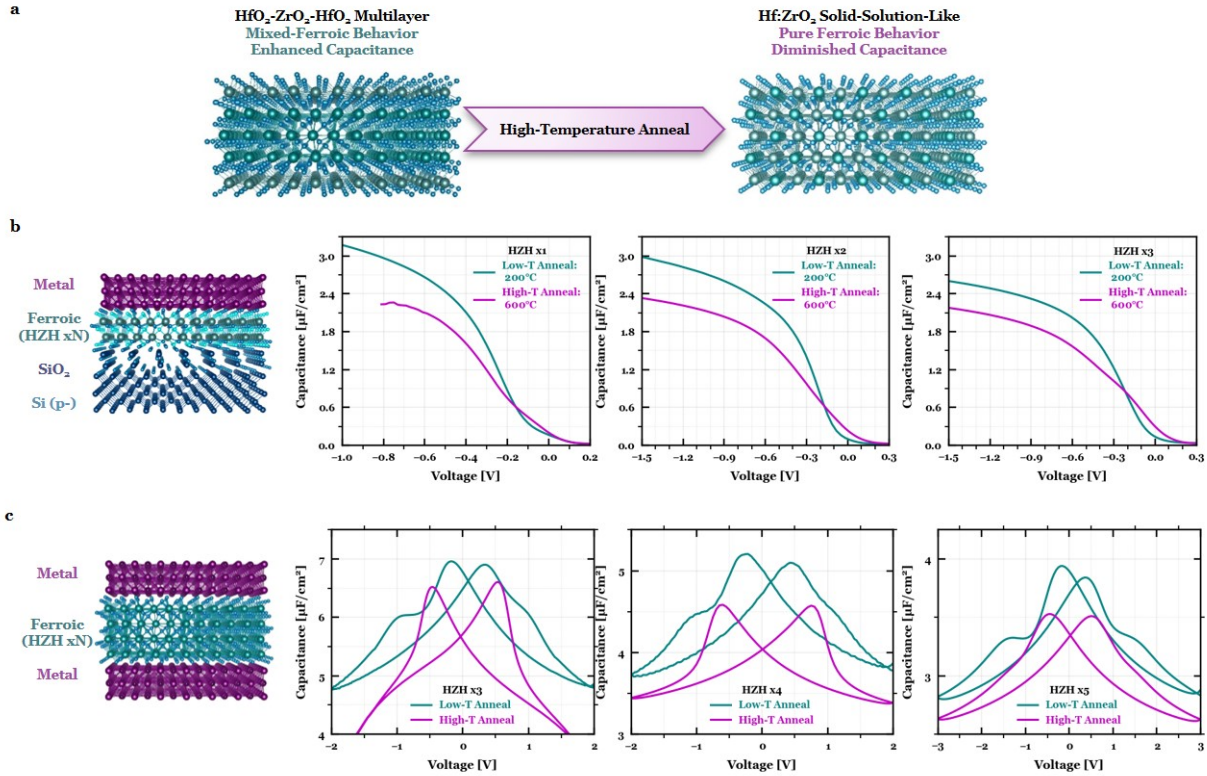
1049 Prototypical C - V behavior for mixed antiferroelectric-ferroelectric (shoulder-like features in addi-
1050 tion to the characteristic butterfly-like shape) and ferroelectric films (just butterfly-like) in MIM
1051 capacitor structures. (f) Temperature-dependent C - V for thicker HfO_2 - ZrO_2 multilayers of the
1052 same periodicity (in MIM capacitor structure) demonstrating an evolution from mixed-ferroic to
1053 ferroelectric-like hysteresis upon cooling slightly below room temperature. Thinner HfO_2 - ZrO_2
1054 multilayers films suffer from leakage-limitations, preventing such hysteretic C - V measurements.
1055 The thicker HfO_2 - ZrO_2 multilayers of the same periodicity – annealed at the same low-temperature
1056 condition to maintain the multilayer structure – demonstrate a similar mixed ferroic to ferroelectric
1057 phase transition slightly below room temperature as the thinner 2 nm multilayer (c).



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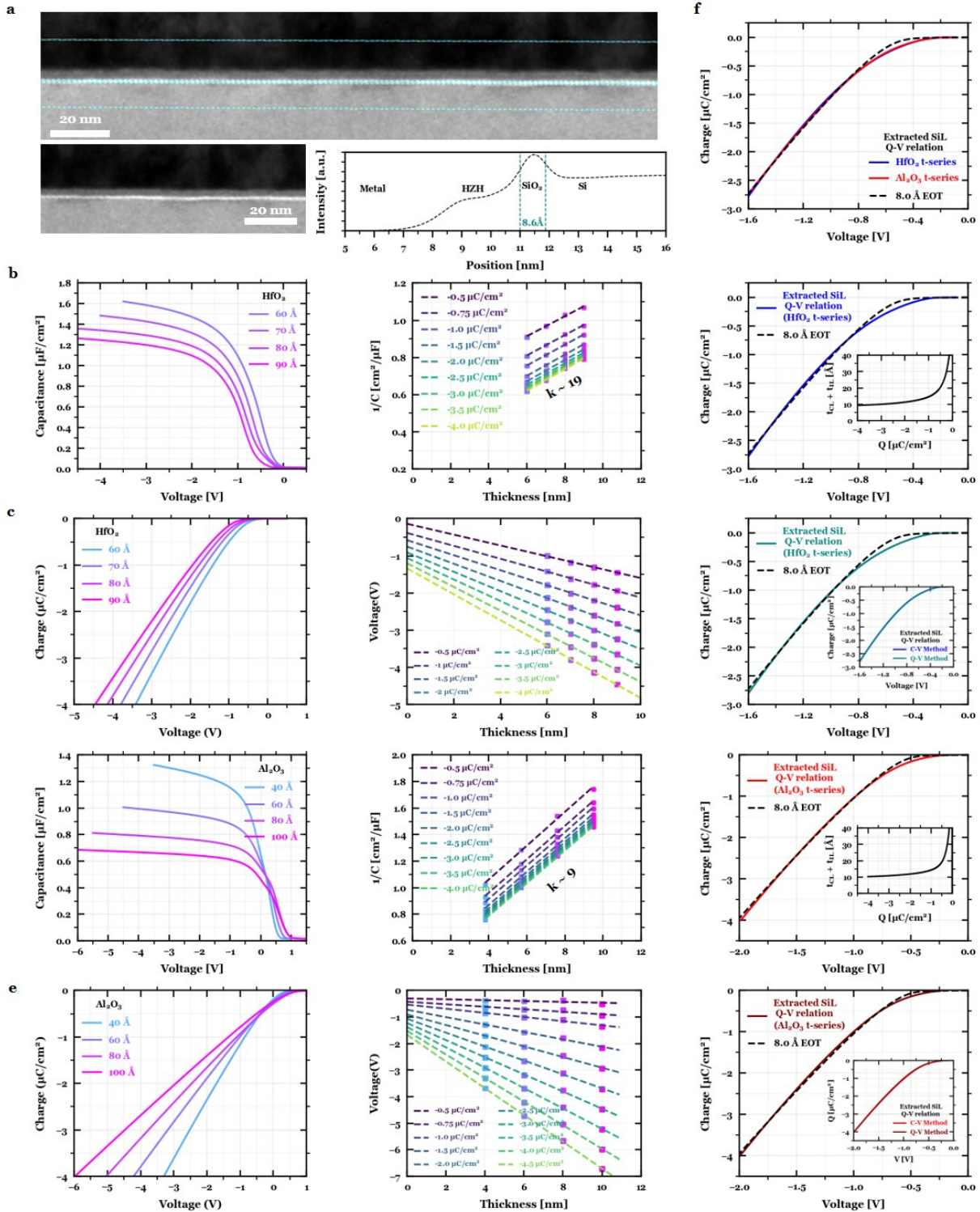
1059 **Extended Data Fig. 4. Solid solutions versus superlattice structure: Role of ALD period and**
 1060 **Zr-content.** (a) Schematic of HfO₂-ZrO₂ multilayer and Zr-rich Hf:ZrO₂ solid solution films.
 1061 With shorter ALD periods, the mixed FE-AFE multilayer structure transitions towards a Hf:ZrO₂
 1062 solid-solution with AFE-like behavior. In the solid solution state, the loss of the mixed ferroic order
 1063 yields diminished capacitance due to the lack of mixed-ferroic-induced capacitance enhancement

1064 (Fig. 1a). (b) MOS accumulation $C-V$ of the $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer (60% Zr) compared to
1065 solid solutions films of the same thickness (2 nm) and composition (60% Zr), as well as solid
1066 solutions films of the same thickness and higher Zr-composition (67%-100% Zr). (c) MIM $C-V$
1067 hysteresis loops of the $\text{HfO}_2\text{-ZrO}_2$ superlattice (60% Zr) compared to solid solutions films of the
1068 same thickness (6 nm) and composition (60% Zr), as well as solid solutions films of the same
1069 thickness and higher Zr-composition (67%-100% Zr). Hf:ZrO_2 solid solution films with higher Zr
1070 content (60%-75%) is around the range attributed to the "MPB" in thicker Hf:ZrO_2 alloys^{26-30,90}.
1071 These results indicate the capacitance enhancement in multilayer films is not simply driven by Zr-
1072 content^{23,35,61,86}, but instead the atomic-scale stacking, as the solid solution films with sub-atomic
1073 superlattice period do not demonstrate the same mixed ferroic behavior and enhanced capacitance
1074 as the superlattices.



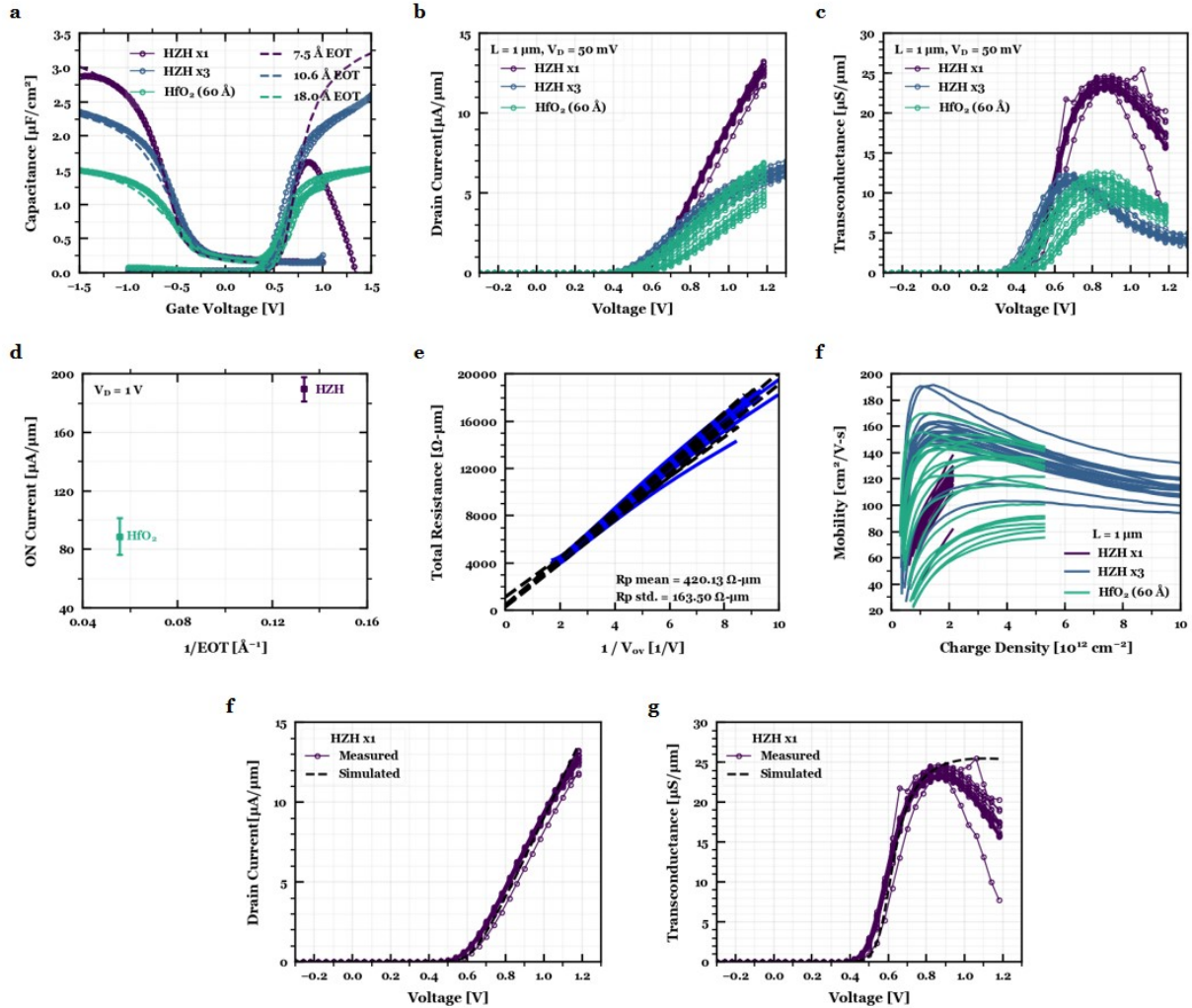
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1076 **Extended Data Fig. 5. Solid solutions versus superlattice structure: Role of annealing tem-**
 1077 **perature.** (a) Schematic of HfO₂-ZrO₂ multilayer and Hf:ZrO₂ solid solution films. Under a
 1078 high-temperature anneal, the multilayer structure transitions towards a Hf:ZrO₂ solid-solution-like
 1079 structure demonstrating more FE-like behavior. The solid solution state yields diminished capaci-
 1080 tance due to the lack of both the higher-permittivity AFE phase and the mixed-ferroic-induced
 1081 capacitance enhancement (Fig. 1a). (b) Comparison of MOS capacitor accumulation C-V char-
 1082 acteristics in HfO₂-ZrO₂ multilayers, where the superstructure was repeated (left) 1, (center) 2, or
 1083 (right) 3 times, under both low- and high-temperature anneals. (c) Comparison of mixed-ferroic
 1084 behavior in low-temperature treated MIM HfO₂-ZrO₂ multilayers versus FE behavior in in the
 1085 same multilayers annealed at high temperatures, where the superstructure was repeated (left) 3,
 1086 (center) 4, or (right) 5 times. In all instances, the high-temperature anneal (> 500°C) results in di-
 1087 minished accumulation capacitance compared to the low-temperature anneals, as the multilayered
 1088 mixed-ferroic films presumably transition to more FE-like solid-solution alloys.



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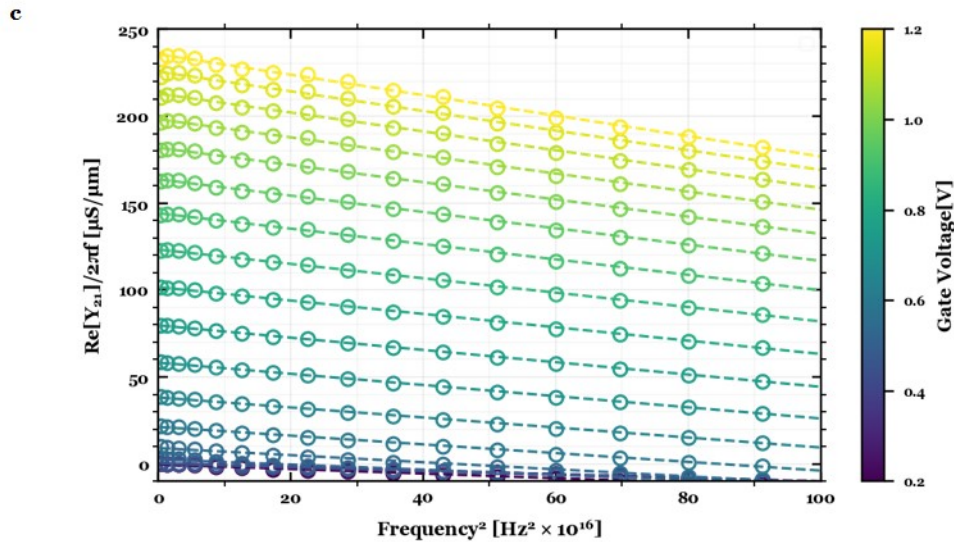
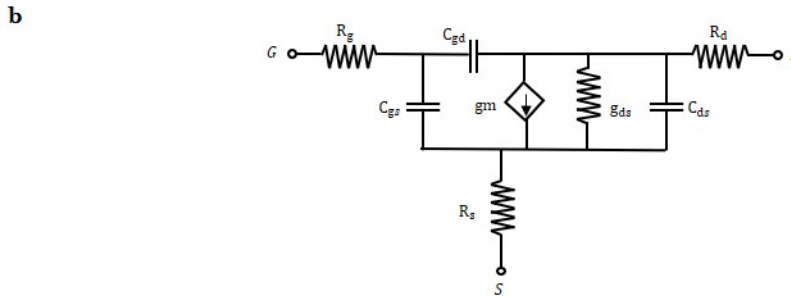
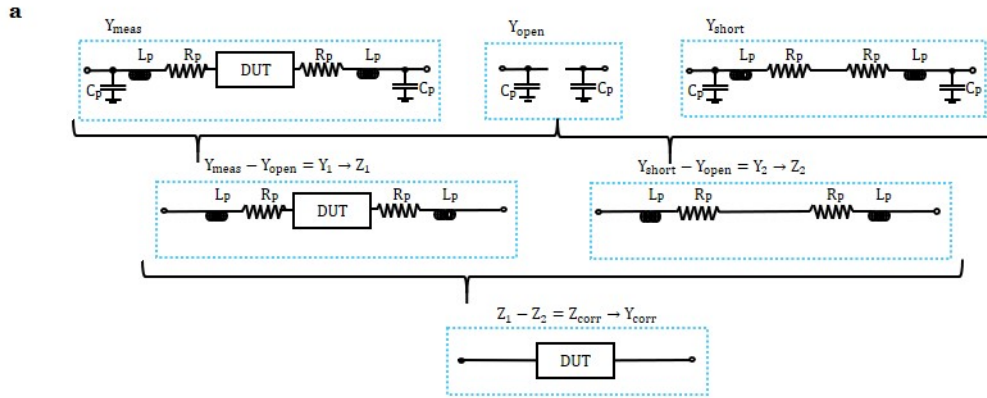
1090 **Extended Data Fig. 6. SiO₂ interlayer thickness.** (a) Wide field-of-view cross-sectional TEM
1091 images of the HfO₂-ZrO₂ multilayer structure and its corresponding intensity line scan (bottom
1092 right) averaged across the entire field-of-view (FoV) of the top cross-sectional image (~ 150 nm),
1093 specified by the teal-colored box. Note the vertical teal-colored lines in the intensity line scan cor-
1094 respond to the inner teal-colored box in the wide-FoV image, which delineate the SiO₂ interlayer
1095 boundaries. The bottom cross-sectional TEM image is provided to highlight the thin SiO₂ inter-
1096 layer (white region) without obfuscation by the teal-colored box. A physical SiO₂ thickness of 8.6
1097 Å is extracted from analysis of the averaged intensity line scan of the wide FoV TEM (Methods).
1098 (b), (d) *C-V* measurements of HfO₂ (b) and Al₂O₃ (d) thickness series in MOS capacitor struc-
1099 tures (left), extracted inverse capacitance versus thickness at various values of charge (center), and
1100 extracted *Q-V* relation Si charge layer and SiO₂ interlayer (SiL) (right), which fits to TCAD sim-
1101 ulations for 8.0 Å SiO₂. The SiL *Q-V* relation was found by integrating the extracted capacitance
1102 equivalent thickness of SiL versus charge (right, inset). This electrical interlayer thickness (8.0 Å)
1103 is slightly less the physical thickness determined by TEM (8.6 Å). As a sanity check, the extracted
1104 permittivity from this methodology for HfO₂ and Al₂O₃ corresponds to 18 and 9, respectively, as
1105 is expected (Methods, Permittivity Extraction). (c), (e) *Q-V* curves of HfO₂ (c) and Al₂O₃ (e)
1106 thickness series obtained from integrating MOS *C-V* measurements (left), extracted voltage vs
1107 thickness at various values of charge (center), and extracted *Q-V* relation of SiL (right). The SiL
1108 *Q-V* relation is consistent with the *Q-V* relation extracted from the *C-V* data (inset). (f) Consis-
1109 tency in the SiL *Q-V* relation extracted from the *C-V* data from both the HfO₂ and Al₂O₃ thickness
1110 series, which both fit to an SiO₂ interlayer thickness of 8.0 Å.



1111

1112 **Extended Data Fig. 7. Mobility extraction.** (a) Split C - V curves obtained for multilayer HfO_2 -
 1113 ZrO_2 gate stacks (repeated 1 and 3 times i.e. HZHx1 and HZHx3) and 60 Å HfO_2 dielectric
 1114 control (Hf-60) from $L_G = 50 \mu\text{m}$ bulk transistors at 10 kHz. These C - V curves were fit to EOT
 1115 simulations of 7.5 Å, 10.6 Å, and 18 Å for HZHx1, HZHx3, and Hf-60, respectively. From the
 1116 off-state accumulation C - V , a doping level of $N_a = 2 \times 10^{17} \text{cm}^{-3}$ was extracted and from the slope
 1117 of the inversion C - V , the interface trap density was found to be $D_{it} = 3 \times 10^{12} \text{eV}^{-1} \text{cm}^{-2}$. (b, c)
 1118 I_D - V_G (b) and g_m - V_G (c) transfer characteristics for $L_G = 1 \mu\text{m}$ bulk transistors at $V_{DS} = 50 \text{mV}$
 1119 for multiple devices per sample. (d) ON current-capacitance (plotted as I_{ON} -1/EOT) comparison

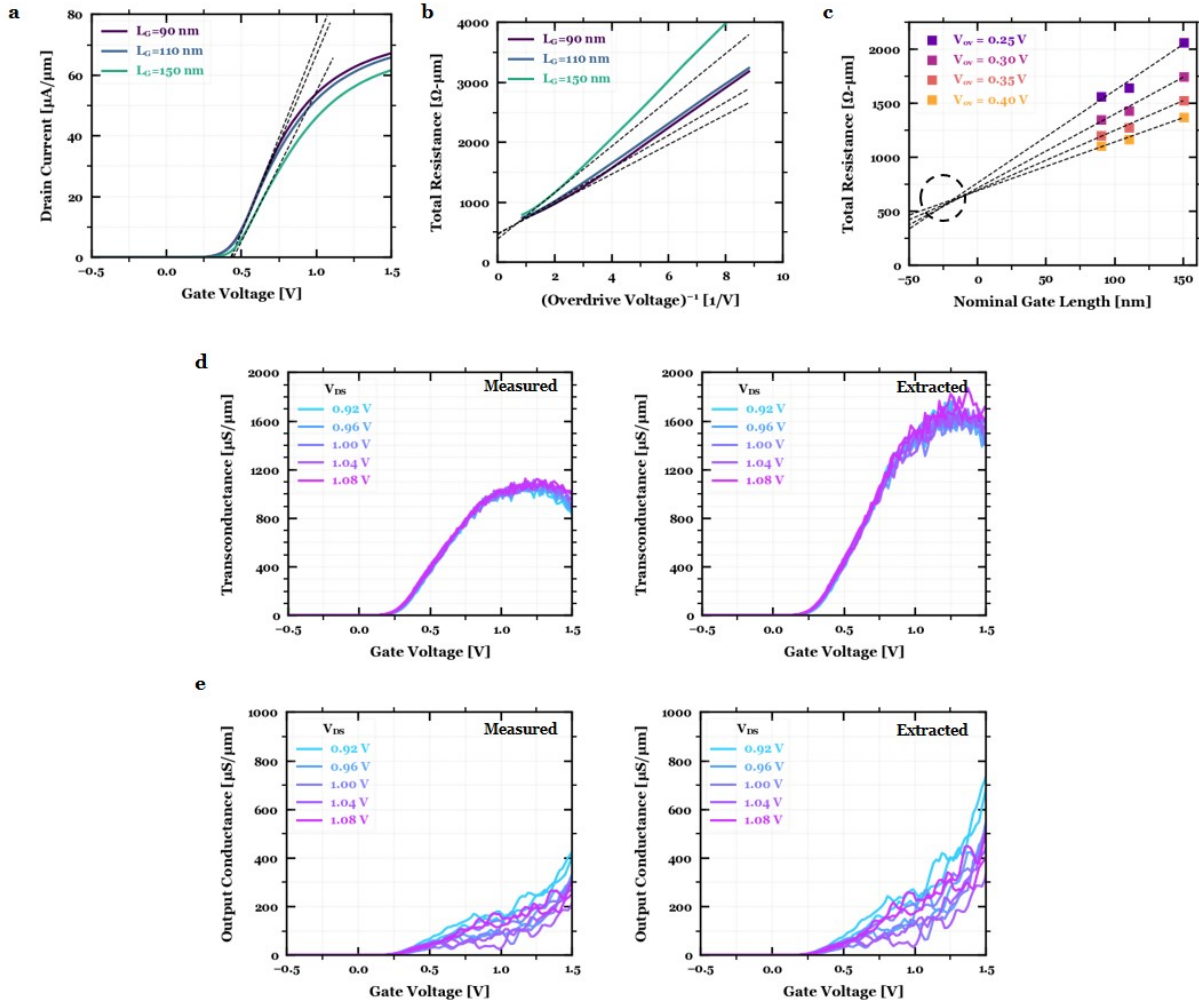
1120 of the HZH multilayer gate stack versus the HfO₂ dielectric control for L_G = 0.5 μm devices. Here,
1121 the ON-current is defined as I_D at V_D = 1 V with an overdrive voltage V_{ov} = 0.5 V. The error bars
1122 represent 1 standard deviation of the ON-current measured from 20 different devices. As expected,
1123 the ON current increases as the inverse-EOT (proportional to the gate capacitance) increases. **(e)**
1124 Series resistance extraction from 1/V_{ov} method for V_{ov} = V_{gs} - V_t = 0.3 V to 0.5 V for L_G = 1
1125 μm devices. The threshold voltage was extracted from the maximum g_m method. **(f)** Extracted
1126 mobility as a function of inversion sheet charge density. The effective mobility was taken to be
1127 the average maximum mobility across multiple L_G = 1 μm devices. **(g, h)** Transfer I_D-V_G (g) and
1128 g_m (h) data fit to a constant mobility model based on the extracted effectively mobility in (f). A
1129 summary of the EOT-mobility trend from the various samples is provided in Figure 3b.



1130

1131 **Extended Data Fig. 8. RF device characterization.** (a) De-embedding procedure for extracting
 1132 corrected admittance parameters (Y_{corr}) by decoupling parasitic shunt capacitance and series resis-
 1133 tance and inductance by measuring scattering parameters for the device under test (DUT) as well
 1134 as open and short structures. More details can be found in the Methods. (b) Small-signal model for

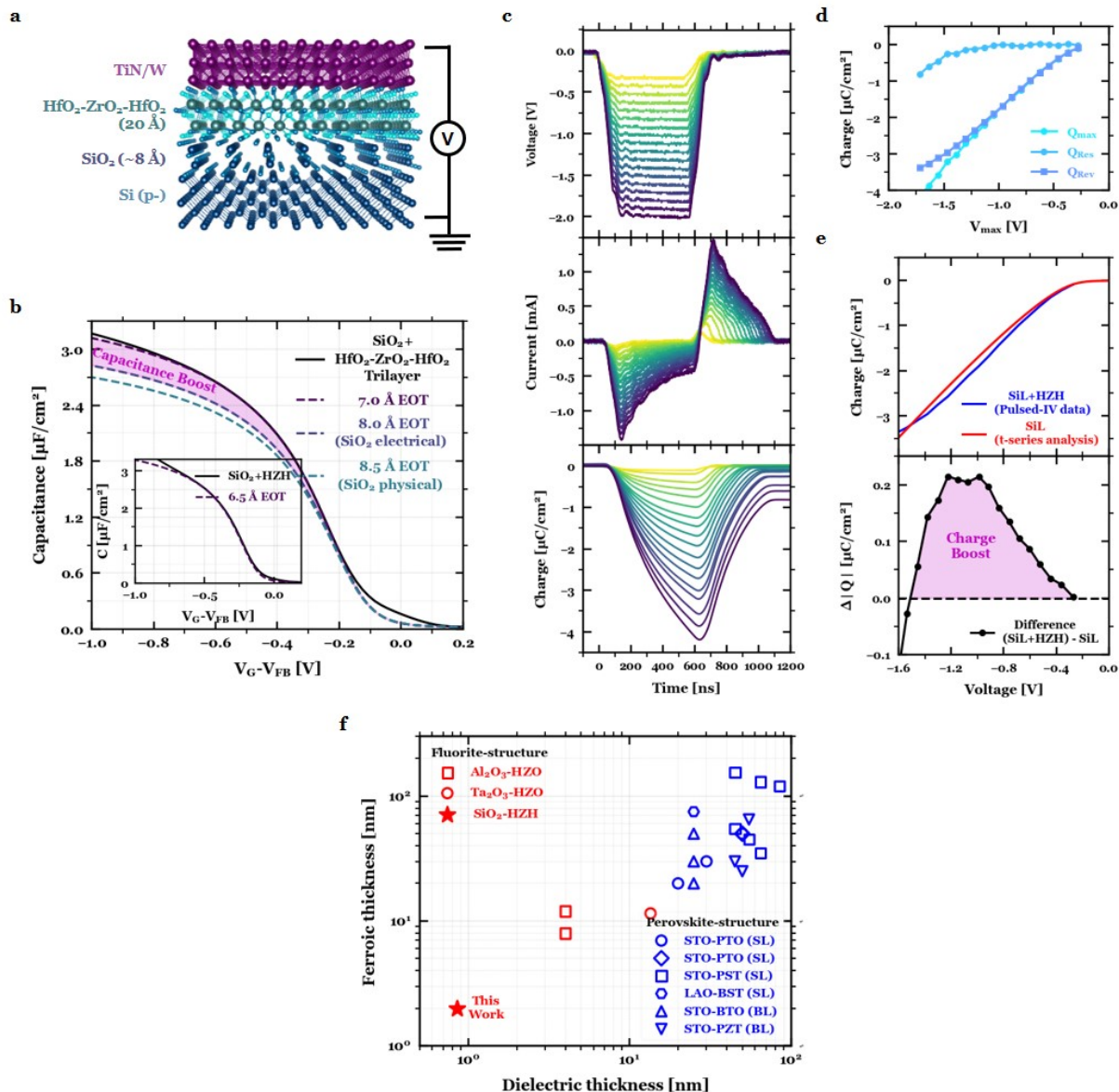
1135 transistor used to extract transconductance (g_m) and total gate capacitance ($C_{gg} = C_{gs} + C_{gd}$). **(c)**
1136 De-embedded $\frac{Re[Y_{21}]}{2\pi f}$ (open circles) as a function of squared frequency at different DC V_{GS} bias
1137 points extrapolated to the zero frequency limit (dotted lines) to extract the RF g_m . All data shown
1138 was extracted from bulk transistors ($L_G = 1 \mu\text{m}$) integrating the 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ ferroic
1139 gate stack.



1140

1141 **Extended Data Fig. 9. Transconductance extraction.** (a) Threshold voltage extraction by
 1142 linear extrapolation for various channel lengths. All channel lengths give nearly constant V_T (\sim
 1143 0.42 V), satisfying the assumption for the line resistance method. (b) Source/drain series resistance
 1144 extracted using the $1/V_{ov}$ method (Methods). By performing a linear interpolation of the total
 1145 resistance for $V_{ov} = 0.5\text{-}0.6$ V, the extracted series resistance is ~ 500 $\Omega\text{-}\mu\text{m}$. (c) Source/drain
 1146 series resistance extracted using the line resistance method (Methods). The trend is considered
 1147 down to $L_G = 90$ nm, which intersects at $\sim 500\text{-}600$ $\Omega\text{-}\mu\text{m}$ – consistent with the $1/V_{ov}$ method–
 1148 with an L_G offset of ~ 50 nm. (d), (e) Measured (left) and extracted (right) transconductance (d)

1149 and output conductance (e) versus V_G for $V_{DS} = 0.9-1.1$ V, assuming $R_s = R_d = 250 \Omega\text{-}\mu\text{m}$ for
1150 $L_G = 90$ nm. The de-embedding of intrinsic g_m and g_{ds} from extrinsic G_m and G_{ds} is described in
1151 the Methods. All data shown was measured on SOI short-channel transistors integrating the 2 nm
1152 $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ ferroic gate stack.



1153

1154 **Extended Data Fig. 10. Capacitance and charge enhancement.** (a) MOS schematic of the
 1155 20 Å $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ mixed ferroic trilayer sample on lightly-doped Si (10^{15} cm^{-3}) considered
 1156 for the following accumulation C - V and pulsed I - V measurements. (b) Accumulation C - V curves
 1157 for the 2 nm $\text{HfO}_2\text{-ZrO}_2\text{-HfO}_2$ trilayer grown on sub-nm SiO_2 fit to effective oxide thickness
 1158 (EOT) simulations (Methods). Inset: Externally verified MOS accumulation C - V of the same tri-
 1159 layer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO_2 demonstrates

1160 lower EOT than the thickness of SiO₂ interlayer alone, carefully extracted via physical (8.5 Å)
1161 and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance
1162 enhancement. **(c)** The applied voltage pulse (top), the measured current response (center) and the
1163 integrated charge (bottom) as a function of time for 2 nm HfO₂-ZrO₂-HfO₂ trilayer in MOS capac-
1164 itors. **(d)** The maximum charge Q_{max} , the residual charge Q_{res} , and their difference, Q_{rev} , derived
1165 from the charge vs time curve for each of the voltage pulses (Methods). **(e)** The reversible charge
1166 of the MOS layer (top) compared against the extracted charge of the Si charge layer plus SiO₂
1167 interlayer (SiL) derived electrically (Extended Data Fig. 5f). The charge boost (bottom) present
1168 in the total MOS structure (SiL plus HZH capacitors) compared to just the SiL is a signature of
1169 negative capacitance, as previously demonstrated in metal-ferroelectric-insulator-metal (MFIM)
1170 structures^{47,67}. **(f)** Scatter plot of reported ferroelectric-dielectric systems demonstrating nega-
1171 tive capacitance at the capacitor level via capacitance (C - V measurements) or charge (pulsed I - V
1172 measurements) enhancement. The plot considers fluorite-structure bilayers^{47,67} (red), perovskite-
1173 structure bilayers^{22,91} (blue, BL), and perovskite-structure superlattices³⁸⁻⁴¹ (blue, SL). This work
1174 employing sub-nm SiO₂ interlayer and 2 nm HfO₂-ZrO₂ multilayer on silicon (black, star) provides
1175 the most scaled demonstration of negative capacitance, as supported by enhanced capacitance from
1176 C - V measurements (b) and amplified charge from pulsed I - V measurements (e) relative to the SiO₂
1177 dielectric interlayer.

Figures

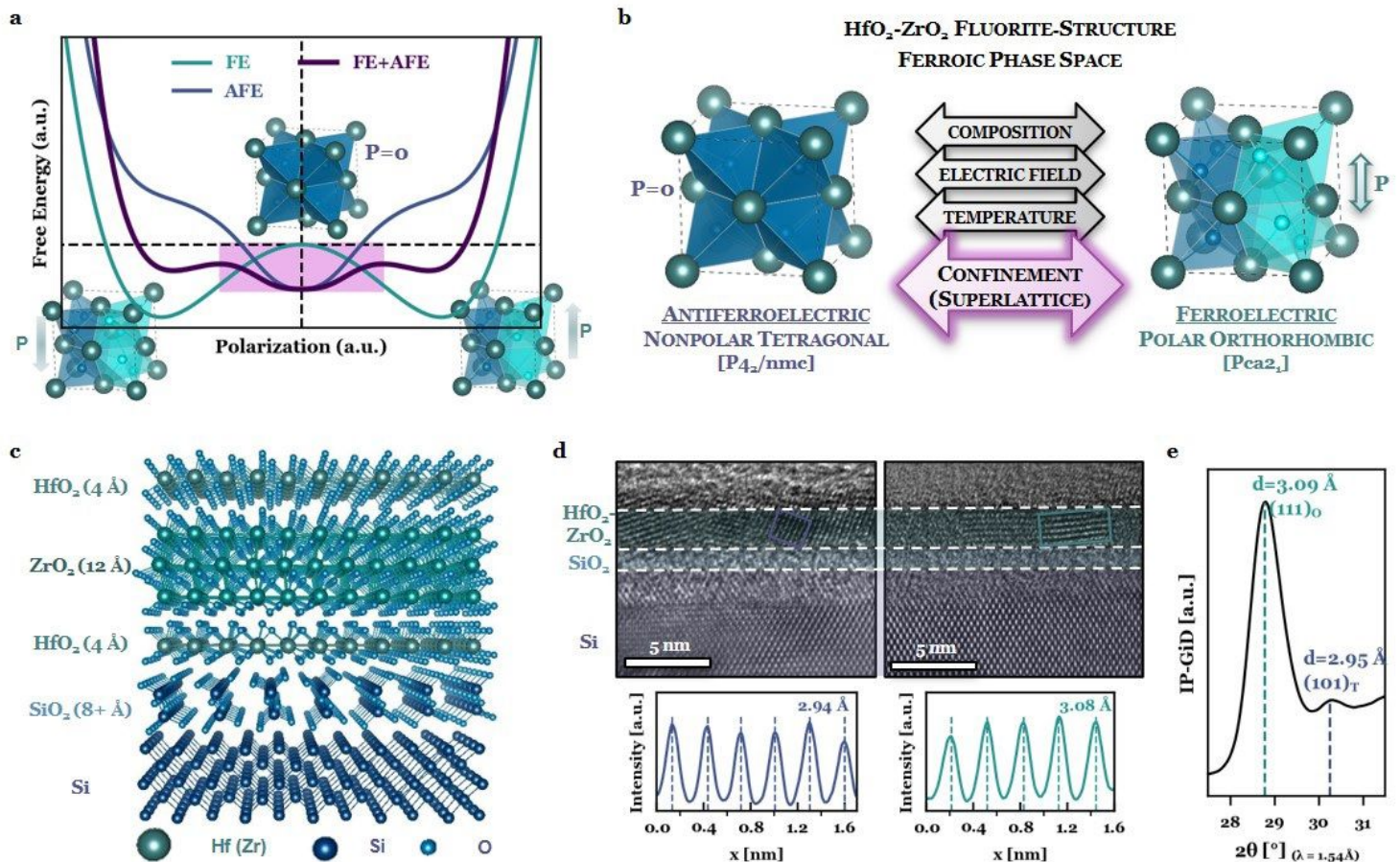


Figure 1

Atomic-scale design of negative capacitance in ultrathin HfO₂-ZrO₂. (a) Phenomenological model of negative capacitance (NC) in a mixed ferroic system. Landau free energy landscapes for a FE, AFE, and mixed FE-AFE system (Methods). Mixed FE-AFE phase competition should suppress polarization⁴⁸ and enhance electric susceptibility^{22,40} via proximity to a phase⁴ boundary, and flattens the energy landscape, desirable traits for NC stabilization. The stable energy minimum of the composite free energy landscape, corresponding to the negative curvature (NC) regime of the ferroelectric energy landscape, is highlighted. (b) Engineering ferroic phase competition in the HfO₂-ZrO₂ fluorite-structure system. Beyond the conventionally-studied tuning parameters – composition, electric field, temperature^{23,35} – here we introduce dimensional confinement via superlattice layering to tailor ferroic phase competition at the atomic-scale. (c) Schematic of the HfO₂-ZrO₂ fluorite-structure multilayer on Si; the heterostructures maintain distinct layers (i.e. not solid solution alloys) based on EELS, XRR, and depth-resolved XPS (Extended Data Fig. 1). The role of the layering on the underlying ferroic order and capacitance is studied by electrical measurements as a function of HfO₂-ZrO₂ stacking structure and annealing temperature (Extended Data Fig. 4 and 5, respectively). (d) HR-TEM image of the atomic-scale HfO₂-ZrO₂-HfO₂ trilayer (top) and extracted d-lattice spacings (bottom) corresponding to the fluorite-structure AFE

tetragonal (P42/nmc, red) and FE orthorhombic (Pca21, blue) phases, respectively. The layer delineations are approximate, as the HfO₂-ZrO₂ and SiO₂ interlayer thicknesses are more rigorously determined by XRR and TEM analysis (Extended Data Fig. 1 and 6, respectively). Note imaging the crystallinity of the HfO₂-ZrO₂ layers requires mistilt with respect to the Si lattice (Methods). (e) Synchrotron IP-GiD demonstrating the presence of both the AFE T-phase (101) and FE O-phase (111) reflections whose d-lattice spacings are consistent with those extracted from TEM. Detailed indexing to higher-order reflections for structural identification of the ferroic phases is provided by wide-angle synchrotron diffraction (Extended Data Fig. 2a). Further evidence of inversion symmetry breaking is provided by second harmonic generation and synchrotron linear dichroism (Extended Data Fig. 2c,d). Additionally, the evolution between these two ferroic phases are also studied as a function of temperature (Extended Data Fig. 3).

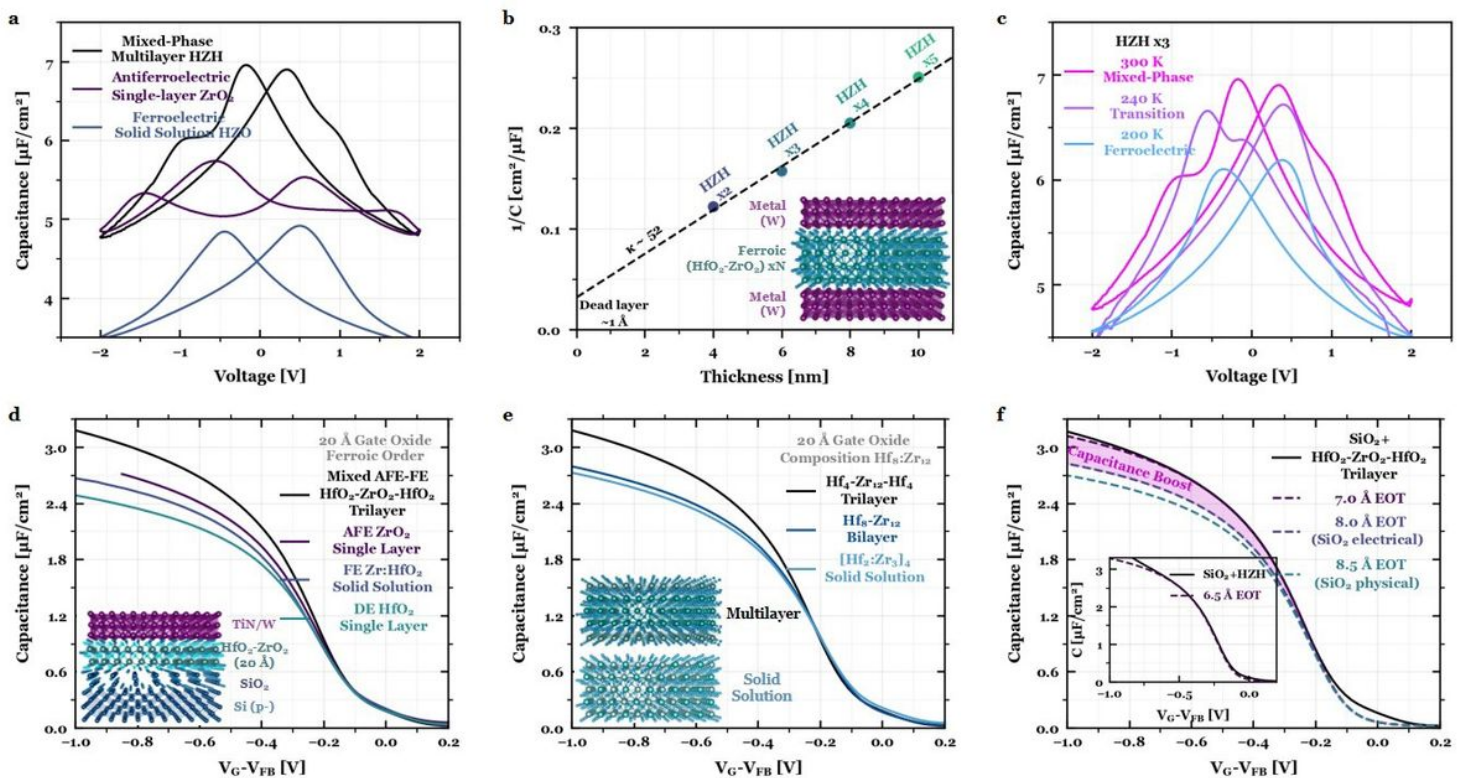


Figure 2

Enhanced capacitance in ultrathin HfO₂-ZrO₂ mixed-ferroic heterostructures. (a) MIM C-V hysteresis loops for a mixed FE-AFE HfO₂-ZrO₂ multilayer demonstrating higher capacitance compared against its AFE (ZrO₂) and FE (Zr:HfO₂) counterparts of the same thickness. (b) Inverse capacitance versus thickness of the MIM HfO₂-ZrO₂ multilayers up to 5 superlattice repeats (10 nm), with an extracted permittivity of 52 (Methods), extremely large for HfO₂-based oxides. (c) MIM C-V hysteresis loops for HfO₂-ZrO₂ multilayers of the same periodicity demonstrating an evolution from mixed-ferroic to FE-like hysteresis upon cooling slightly below room temperature. The proximity to the temperature-dependent phase transition (Extended Data Fig. 3) suggests the HfO₂-ZrO₂ heterostructures lies near its maximum electric susceptibility position, ideal for negative capacitance stabilization^{40,48}. (d) MOS accumulation

C-V of HfO₂-ZrO₂-HfO₂ trilayer compared to AFE ZrO₂, FE Zr:HfO₂, and DE HfO₂, all of the same thickness (20 Å), indicating mixed-ferroic behavior is optimal for enhancing capacitance rather than purely FE or AFE behavior. (e) Accumulation C-V of the HfO₂-ZrO₂-HfO₂ trilayer compared to bilayer and solid solutions films of the same thickness (ALD cycles) and composition (Hf:Zr cycles). Inset: Schematic of multilayer (Hf and Zr cations vertically separated) versus solid solution (Hf and Zr cations inter-mixed). These results suggest the capacitance enhancement in multilayer films is not simply driven by Hf:Zr composition^{23,35}, but instead the atomic-scale stacking (Extended Data Fig. 4, 5). (f) Accumulation C-V curves for a 2 nm HfO₂-ZrO₂-HfO₂ trilayer grown on sub-nm SiO₂ fit to effective oxide thickness (EOT) simulations (Methods). Inset: Externally verified MOS accumulation C V of the same trilayer stack (Methods), demonstrating 6.5 Å EOT. The 2 nm trilayer on top of SiO₂ demonstrates lower EOT than the thickness of SiO₂ interlayer alone, carefully extracted via physical (8.5 Å) and electrical (8.0 Å) methodologies (Extended Data Fig. 6), providing evidence of capacitance enhancement. Furthermore, these 2 nm ferroic gate stacks demonstrate amplified charge from pulsed I-V measurements relative to the SiO₂ interlayer (Extended Data Fig. 10). Notably, this 2 nm HfO₂-ZrO₂ multilayer on sub-nm SiO₂ provides the most scaled demonstration of charge and capacitance enhancement at the capacitor-level (Extended Data Fig. 10).

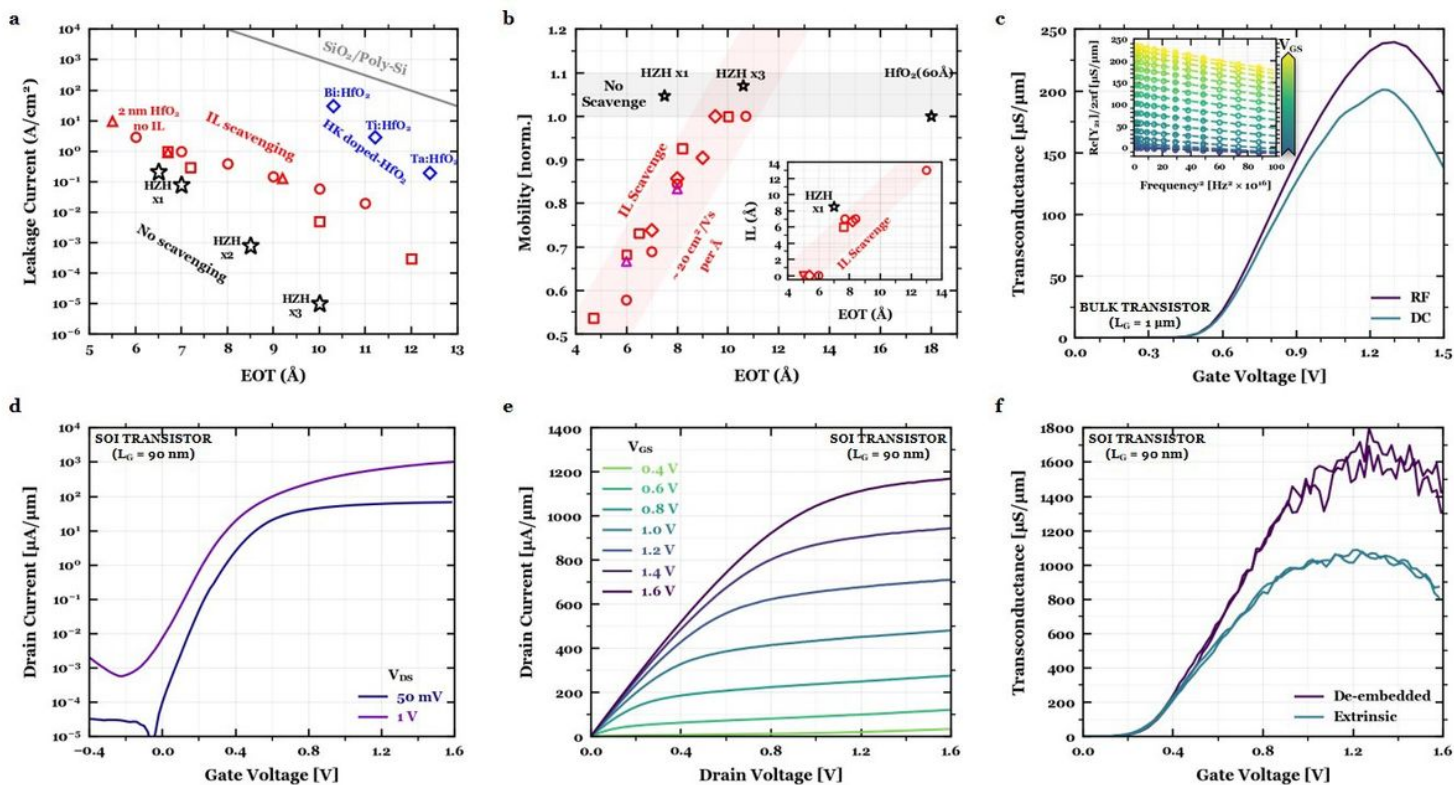


Figure 3

Device performance benefits utilizing ultrathin mixed-ferroic HfO₂-ZrO₂ gate stacks. (a) Leakage-effective oxide thickness (JG-EOT) scaling of the multilayer gate stacks (black) bench marked against reported HKMG literature³, including interlayer-scavenged 2 nm HfO₂ (red), high-doped HfO₂ (blue), and SiO₂/poly-Si (gray). The leakage is the lowest reported for a 6.5-7.0 Å EOTMOS capacitor on silicon³, due

to the EOT reduction without requiring interlayer SiO₂ thickness reduction. (b) Normalized mobility versus EOT scaling of the multilayer gate stacks (black) benchmarked against reported HKMG literature³, including interlayer-scavenged 2 nm HfO₂ (red) and hybrid silicate-scavenged interlayer (magenta). For EOT scaling in conventional HKMG systems, the SiO₂ interlayer has to be reduced to lower EOT, which leads to degraded mobility³. In this case, enhanced capacitance in HfO₂-ZrO₂ multilayers achieves scaled EOT without having to thin the SiO₂ interlayer; therefore, mobility is not degraded. Inset: SiO₂ interlayer thickness versus EOT scaling comparing the 7.0 Å EOT HfO₂-ZrO₂-HfO₂ trilayer against notable HKMG literature which employ interlayer scavenging to reduce EOT³. This scatter plot highlights the underlying reason for the enhanced leakage-EOT and mobility-EOT behavior in the ultrathin trilayer gate stacks: low EOT without reduced SiO₂ interlayer thickness. (c) Transconductance (gm) versus gate voltage (VG) 450 for long-channel bulk transistors (LG = 1 μm) obtained from both DC (derivative of ID-VG) and RF (Re[Y₂₁]) measurements (Methods) at VDS = 1 V. Inset: De-embedded Re[Y₂₁] (open circles) as a function of squared frequency at different DC VGS bias points extrapolated to the zero frequency limit (dotted lines) to extract the RF gm (Extended Data Fig. 8). The high frequency measurements help suppress defect contributions which would otherwise dampen the intrinsic gm. (d, e, f) DC I-V transfer characteristics (ID-VG, d), DC output characteristics (ID-VD, e), and DC transconductance (gm-VG, f) for short-channel (LG = 90 nm) SOI transistors. Notably, the maximum on-current and gm at VDS = 1 V exceeds 1 mA/μm and 1 mS/μm. DC mobility and transconductance values are carefully extracted after de-embedding the series resistance from double-swept I-V measurements (Extended Data Fig. 7 and 9, respectively).