Atomically abrupt and unpinned $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces: Experiment and simulation

Eun Ji Kim,[1,a)] Evgueni Chagarov,[2] Joël Cagnon,[3] Yu Yuan,[4] Andrew C. Kummel,[2] Peter M. Asbeck,[4] Susanne Stemmer,[3] Krishna C. Saraswat,[1,5] and Paul C. McIntyre[1,b)]
[1]*Department of Materials Science and Engineering, Stanford University, Stanford, California 94305, USA*
[2]*Department of Chemistry and Biochemistry, University of California, San Diego, California 92093, USA*
[3]*Department of Materials, University of California, Santa Barbara, California 93106, USA*
[4]*Department of Electrical and Computer Engineering, University of California, San Diego, California 92093, USA*
[5]*Department of Electrical Engineering, Stanford University, Stanford, California 94305, USA*

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III-V semiconductor field effect transistors require an insulator/channel interface with a low density of electrically active defects and a minimal interface dipole to avoid Fermi level pinning. We demonstrate that an atomically abrupt and unpinned interface can be formed between an $In_{0.53}Ga_{0.47}As$ (100) channel and an Al_2O_3 dielectric layer grown by atomic layer deposition (ALD) when oxidation of the substrate surface is prevented before and during oxide deposition. X-ray photoelectron spectra and electron microscopy indicate that *in situ* desorption of a protective As_2 layer on the $In_{0.53}Ga_{0.47}As$ $(100)-4\times2$ surface followed by ALD of Al_2O_3 produced an atomically abrupt interface without Fermi level pinning. Temperature-dependent and frequency-dependent capacitance-voltage and conductance-voltage analysis of the resulting $Pt/Al_2O_3/InGaAs$ capacitors are consistent with movement of the Fermi level through the InGaAs band gap. Moreover, the nearly ideal flat band voltages observed for gate metals of widely varying work function indicate a small oxide/semiconductor interface dipole. Density functional theory calculations of the electronic structure of an ideal amorphous $Al_2O_3/InGaAs$ (100) interface predict a weak perturbation of the InGaAs electronic structure if its oxidation is avoided, consistent with experiment. © *2009 American Institute of Physics*. [doi:10.1063/1.3266006]

I. INTRODUCTION

The physical origins of electrically active defects in insulator/III-V structures remain poorly understood; however, recent research has prompted renewed interest in this subject.[1,2] A serious problem for metal-oxide semiconductor (MOS) device applications of III-V materials is the difficulty of achieving electrically passive interfaces with deposited or grown gate insulators. Previous research on GaAs oxidation, for example, indicates that less than 1% of a monolayer of chemisorbed O_2 can pin the Fermi level at the semiconductor surface,[3] preventing proper device operation. Several different methods have been explored to prepare III-V channel MOS devices with low interface defect densities, including removal of native oxides[4–8] and deposition of a passivating molecular monolayer[9] prior to gate dielectric deposition. However, these approaches may not avoid the unintentional oxidation of the substrate surface, or, if they do, the effect may be strongly dependent on the substrate surface reconstruction. Therefore, suppressing oxidation of the III-V surface prior to and during gate dielectric deposition may be essential to achieving transistor performance that is superior to that of silicon in nanoscale devices.[10]

In this study, we demonstrate a method of protecting the $In_{0.53}Ga_{0.47}As$ (100) channel from oxidation and contamination during exposure to air. An As_2 capping layer deposited at the end of epitaxial growth of the channel was thermally desorbed *in situ* in an atomic layer deposition (ALD) reactor prior to Al_2O_3 gate dielectric deposition. By preventing subcutaneous oxidation of the channel surface, we obtained unpinned $Al_2O_3/In_{0.53}Ga_{0.47}As$ interfaces that exhibit near-ideal flat band voltages, consistent with a minimal interface dipole. Photoelectron spectra and both capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) data indicate that the ALD-Al_2O_3 gate insulator does not significantly perturb the local electronic structure near the channel interface. These results are consistent with *ab initio* simulations of an ideal amorphous $Al_2O_3/InGaAs$ interface for which subcutaneous oxidation of the substrate is avoided.

II. EXPERIMENTAL METHODS

$In_{0.53}Ga_{0.47}As$ $(100)-4\times2$ channel substrates (185 nm thick, Si doped at 1×10^{17} cm^{-3} and grown on S-doped InP with a doping concentration of $6-15\times10^{18}$ cm^{-3}, IntelliEpi) capped with an 80-nm-thick As_2 layer were loaded into a load-locked, warm-wall ALD reactor. Throughout the As_2 decapping process, forming gas (5% H_2/95% Ar) flowed over the sample in the ALD reactor at 1 Torr pressure. The sample stage temperature was increased slowly from room temperature (RT) to 460 °C. After As_2 decapping for 15 min, the stage temperature was decreased to RT, and *in situ* x-ray photoelectron spectroscopy (XPS)[11] measurements

[a)]Electronic mail: eunjikim@berkeley.edu.
[b)]Electronic mail: pcm1@stanford.edu.

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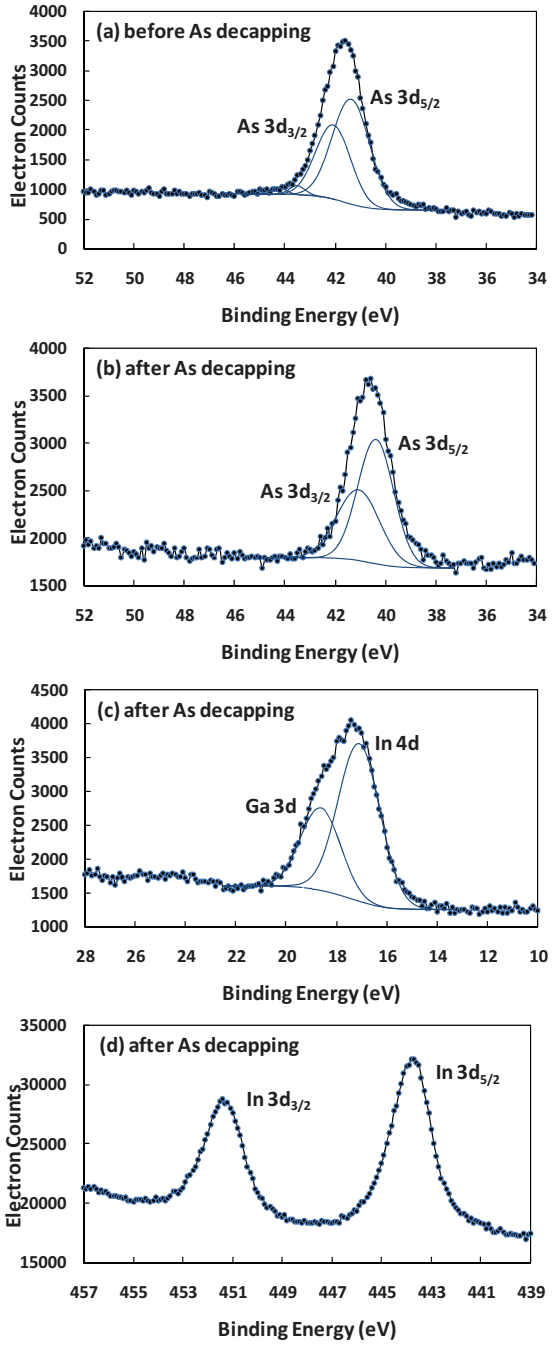

FIG. 1. (Color online) As 3*d* core spectra of (a) As-capped $In_{0.53}Ga_{0.47}As$ and (b) As-decapped $In_{0.53}Ga_{0.47}As$. (c) Ga 3*d* and In 4*d* and (d) In 3*d* core spectra of $In_{0.53}Ga_{0.47}As$ after As decapping. [The spectra were measured by the *in situ* XPS system equipped with a nonchromatic spectrometer using Al($k\alpha$) radiation and with a base pressure in the mid-10^{-6} Torr range, which produced an apparent degradation of resolution.]

confirmed the As $3d_{5/2}$ peak shift from As–As metallic bonding (41.6 eV) to As–Ga and As–In bonding (40.9 eV) and no evidence of oxide formation on the As-decapped surface (Fig. 1).[12–14] The *in situ* XPS system is equipped with a nonchromatic spectrometer using Al($k\alpha$) radiation and is built into the ALD reactor with a base pressure in the mid-10^{-6} Torr range. The measurement system collects photoelectrons using a differentially pumped electron collection system, capable of monitoring the real-time surface composition at millitorr pressures.[11] The stage temperature was increased to 270 °C for Al_2O_3 deposition. The base pressure of the ALD chamber was $\sim 10^{-7}$ Torr and the chamber pressure was 0.8 Torr during the deposition. The trimethylaluminum (TMA) and H_2O precursors were held at RT. During each cycle of the ALD process, TMA was pulsed for 1 s, followed by a 5 s evacuation interval, 45 s forming gas purge, and 5 s evacuation, and then H_2O was pulsed for 1 s, followed by 5 s evacuation interval, 60 s forming gas purge, and 1 s evacuation. A platinum gate electrode of 50 nm thickness and a composite back contact layer of 50 nm Ti and 150 nm Au (Ti on InP) were deposited through shadow masks for front and back contacts to the Al_2O_3/InGaAs capacitors, respectively, by RT e-beam evaporation.

The *C-V* measurements were performed in a shielded probe station. The gate bias applied to the capacitors increased from −1 (inversion) to 2 V (accumulation) and decreased back to −1 V with a dc voltage step of 0.1 V (1 s wait time) and an ac modulation of 10 mV. The diameter of the measured circular capacitors is 100 μm. *C-V* measurements were initially done at 10, 100, and 800 kHz and were performed again on the sample capacitor at multiple frequencies from 5 to 800 kHz. Current-voltage (*I-V*) measurements were performed at RT with a voltage step of 0.1 V (3 s wait time). The measured gate leakage current density was lower than 1×10^{-8} A/cm^2 at $V_{fb} \pm 1$ V. *C-V* measurements were performed using a HP4284A precision *LCR* meter. *I-V* measurements were made using a Keithley 230 programmable voltage source and a Keithley 6512 programmable electrometer.

Ex situ XPS measurements were performed to detect any changes in bonding at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface after 10 cycles of ALD. The *ex situ* XPS system is equipped with a SSI S-Probe Monochromatized XPS spectrometer, which uses Al($K\alpha$) radiation, with a base pressure in the mid-10^{-10} Torr range and is capable of angle-resolved XPS (ARXPS) measurements.

Cross-section transmission electron microscopy (TEM) samples were prepared by standard techniques including mechanical polishing using diamond lapping films followed by 2.8–0.8 kV argon ion milling using a Model 1000 ion mill (E. A. Fischione Instruments, Export, Pennsylvania). Before inserting samples into the TEM, they were plasma cleaned with a 25/75% O_2/Ar mixture. High resolution transmission electron microscopy (HRTEM) and atomic-number sensitive high-angle annular dark-field (HAADF) (*Z* contrast) imaging in scanning TEM (STEM) were performed using a field-emission transmission microscope operating at 300 kV (FEI Titan 80–300 TEM/STEM) equipped with a Fischione annular dark-field detector Model 3000 (E. A. Fischione Instruments, Export, Pennsylvania).

III. SIMULATION METHODS

The simulated *C-V* curves were computed, with no adjustable parameters, for a structure of InGaAs (doped *n*-type with Nd=10^{17} cm^{-3}) and Al_2O_3 (assuming a relative dielectric constant of 8, and thickness of 4.6 nm) with no interface states or dipoles. The computation accounts for the density of states (DOS) in the InGaAs conduction and valence bands,

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TABLE I. Nearest neighbor distribution of our classical a-Al_2O_3 sample versus classical sample of Ref. 17. Cutoff radius-2.2 Å.

Nearest neighbor distribution	O(2)	O(3)	O(4)	Al(3)	Al(4)	Al(5)	Al(6)
Our sample	18%	79%	3%	0.0%	75%	23%	2.0%
Ref. 17	20%	78%	2%	0.3%	76%	22%	1.7%

and Fermi–Dirac statistics. In order to properly represent the capacitance in the accumulation region, nonparabolicity of the conduction band was taken into account, using a simplified dispersion relation relating energy relative to the conduction band to wave vector k according to $\varepsilon(1+\alpha\varepsilon)=\hbar^2k^2/2m^*$. Here α is a nonparabolicity parameter taken to be 1.22 eV^{-1}, and m^* is the effective mass at the bottom of the band, taken to be 0.041. An electron affinity of 4.51 eV was used, together with the effective gate metal work functions of Ref. 15. The computation does not account for possible quantum mechanical effects, which we have been separately verified to be small over the gate bias range shown.

In atomistic simulations of the α-Al_2O_3/InGaAs system, the most realistic amorphous aluminum oxide (α-Al_2O_3) sample was generated by classical annealing at low ($\sim$0.9 g/cm^3) density at 5000 K for 250 ps, rescaling to the normal classical a-Al_2O_3 density of 3.20 g/cm^3 and annealing at 5000 K for 400 ps, constant-rate cooling to RT for 100 ps and thermally equilibrating at RT for 120 ps.[16] The sizes of the classical a-Al_2O_3 samples are $\sim 17.05\times 8.52\times 8.74$ Å. The classical simulations were performed at constant volume. Constant-volume annealing was employed instead of constant-pressure annealing for several reasons: (a) the properties of the classical amorphous sample are primarily determined by the amorphization which happens during cooling stage at much lower temperature than 5000 K; (b) the main purpose of the high-temperature annealing at 5000 K is to provide good intermixing of the melt so the usage of NVT ensemble does not have significant negative effects on the final sample properties, and (c) the use of NVT instead of NPT ensembles helps to avoid unphysical sample volume oscillations during 5000 K annealing. Subsequently, the classical amorphous sample was homogenously rescaled from the classical (3.20 g/cm^3) to the density functional theory (DFT) density (3.26 g/cm^3) and DFT-molecular dynamics (DFT-MD) annealed in NVT ensemble at 1400 K for 1000 fs with 1 fs time step, cooled to 0 K for 200 fs, and relaxed below the 0.01 eV/Å force tolerance level. The classical-MD and DFT-MD stages used the same sample which was rescaled from classical to DFT density.

The a-Al_2O_3 sample has 120 atoms, keeping correct stoichiometry at the classical and DFT-MD stages of amorphous sample generation, and sizes of $\sim 16.95\times 8.47\times 8.69$ Å after rescaling to DFT density. The a-Al_2O_3 sample quality was verified via radial-distribution function main peak positions and full widths at half maximum, average nearest neighbor numbers, nearest neighbor distributions, calculated neutron scattering static structural factor, and DFT calculated band gap, showing good correlation to simulated and experimental reference properties.[17–21] Table I presents the coordination distribution of the classical-MD annealed a-Al_2O_3 sample versus the reference classical sample distribution, demonstrating excellent correlation.[17] The classical-DFT MD annealed a-Al_2O_3 sample exhibits defect-free band gap of $\sim$3.7 eV, agreeing well with a previously reported calculated band gaps of 3.77 (Ref. 19) and 3.8 eV.[20] The DFT-MD annealed oxide sample was cleaved in the X-Y plane parallel to the interface and periodic boundary conditions were truncated by adding $\sim$12 Å of vacuum over the samples. The cleavage planes were chosen to provide a roughly equal number of metal and oxygen atoms at the bottom surface.

The oxide sample was not relaxed after surface cleavage prior to stacking on $In_{0.5}Ga_{0.5}As$ $(100)-4\times 2$ in order to provide a chemically reactive surface with dangling bonds for contact with $In_{0.5}Ga_{0.5}As$ $(100)-4\times 2$. Conversely, the upper surface of the oxide was passivated by H atoms having $\sim$12 Å of vacuum to avoid spurious interactions through periodic boundary conditions (PBC). The $In_{0.5}Ga_{0.5}As$ $(100)-4\times 2$ surface reconstruction has nonplanar row/trough topography. To match its profile, a groove of approximately 7.5×1.7 Å was cut out of the classical-DFT MD generated a-Al_2O_3 sample in its final equilibrium state prior to stacking to the InGaAs substrate (Fig. 2). After the groove cut, the a-Al_2O_3 sample has 105 atoms maintaining correct stoichiometry. This study employed a model with one oxide/semiconductor interface and a vacuum layer. The presence of a vacuum layer over the oxide allows relaxation of the interfacial oxide-semiconductor height and of possible residual stresses in the amorphous sample induced by bonding to the semiconductor. The one-interface design (with vacuum layer) is a widely used and well-proven design for DFT simulations of oxide-semiconductor stacks. The one-interface design was successfully applied by Puthenkovilakam *et al.*[22] for simulations of ZrO_2/Si and $ZrSiO_2/Si$ stacks, by Monaghan *et al.*[23] for simulations of Hf silicates on Si, by Hakala *et al.*[24] for simulations of HfO_2 on Si, by Gavartin and Shluger[25] for simulations of $HfO_2/SiO_2/Si$ stacks, by Chagarov and Kummel[20,26] for simulations of a-Al_2O_3/Ge, a-ZrO_2/Ge interfaces, and by other authors.

To compensate for spurious electric fields induced by PBC for this type of system, a dipole correction was applied.[27–29] After oxide/semiconductor stacking, the $In_{0.5}Ga_{0.5}As$ slab was fixed in space while the oxide was partially relaxed for $\sim$20–30 conjugate-gradient relaxation steps. After this initial partial relaxation, the $In_{0.5}Ga_{0.5}As$ atoms were unfixed except for the three bottom layers and the whole system was annealed at 800 K for 1000 fs with 1.0 fs time step in NVT ensemble, cooled to 0 K for 200 fs, and finally relaxed below a 0.05 eV/Å force tolerance level (Fig. 2). The a-Al_2O_3/InGaAs stack (Fig. 8) had several dangling bonds (unpassivated states) at the a-Al_2O_3/vacuum interface (upper oxide surface), which formed states in the band-gap region of the total DOS. To locate these pinning states, the band-decomposed charge density corresponding to the band gap pinning energy interval was visualized in 3D. The pinning states were localized at the undercoordinated Al atoms having two bonds to O's and one to H. In amorphous bulk a-Al_2O_3, Al has predominantly four bonds to O. It is noted that the electronic structure of the vacuum/oxide interface is

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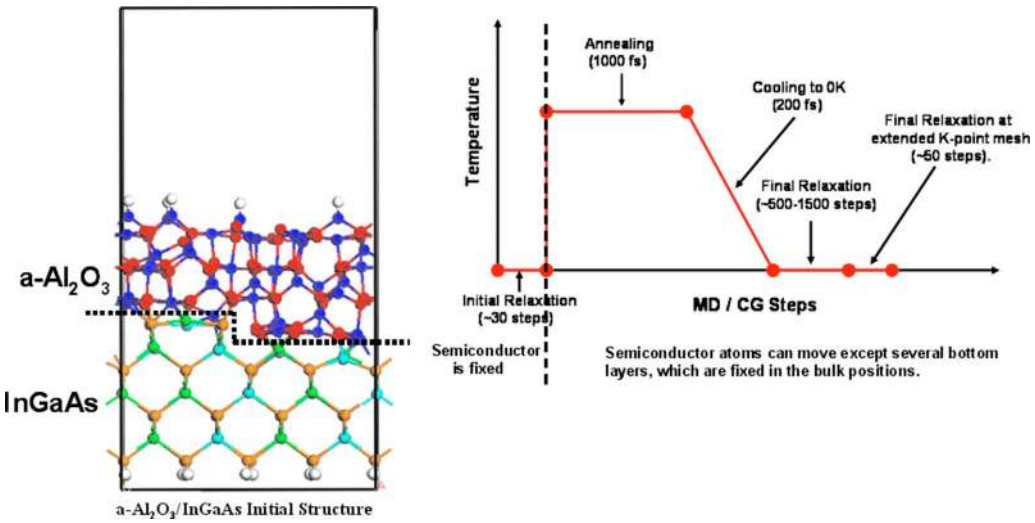

FIG. 2. (Color online) DFT-MD annealing of the amorphous oxide interface. Left panel shows the initial structure: the oxide bulk is placed on the clean semiconductor surface; right panel shows DFT-MD annealing sequence: (1) initial relaxation—oxide is allowed to partially relax at 0 K but semiconductor is frozen, (2) annealing—oxide and most of semiconductor are annealed at 800 K, (3) cooling/relaxation—stack is cooled and relaxed, and (4) final relaxation with an extended *K*-point set to obtain improved electronic structure.

not important in practical devices since the oxide would have a gate metal on the top surface. To fix the problem of Al undercoordination at the oxide/vacuum interface, eight OH groups have been added so that every Al at the oxide/vacuum interface was bonded to at least four O atoms. To avoid significant interface deformation, these eight OH groups have been added in two steps: four OH's were added and the whole system was relaxed; afterward, four more OH's were added and the system was again relaxed. This led to *a*-Al_2O_3/InGaAs interface without significant changes in interfacial geometry, but passivated the upper oxide-vacuum interface and moved the Fermi level to the middle of the band-gap region.

The lattice mismatch between crystalline Al_2O_3 and InGaAs is not relevant for the present simulations which use an amorphous Al_2O_3 sample specially generated/molded to perfectly match in its final equilibrium state the InGaAs substrate surface area. After amorphous sample generation, the absence of internal hydrostatic pressure in the sample was verified. One of the main advantages of amorphous samples is that they can be prepared for particular substrate area and do not require oxide compression/elongation to match the substrate area. As an additional check, the *a*-Al_2O_3/InGaAs stack was annealed and relaxed in the supercell geometry with two interfaces and no vacuum layer. This system developed an interface structure very similar to the one-interface design including a vacuum layer.

All DFT simulations were performed with the Vienna *ab-initio* simulation package (VASP) (Refs. 27 and 28) using projector augmented-wave (PAW) pseudopotentials (PP) (Refs. 30 and 31) and the Perdew–Burke–Ernzerhof (PBE) exchange-correlation functional.[32,33] The choice of PBE functional and PAW PP was validated by parametrization runs demonstrating good reproducibility of experimental lattice constants, bulk moduli, and formation energies for bulk crystalline Al_2O_3, Al, InAs, and GaAs. Classical MD simulations were performed by a large-scale atomic/molecular massively parallel simulator (LAMMPS),[34] expanded by a well-tested empirical potential for Al_2O_3.[35] The DFT initial relaxation, annealing, cooling, and final relaxation of the oxide/semiconductor stack were performed with a two irreducible *K*-point mesh to obtain acceptable computational efficiency. After the final relaxation, the *K*-point set was expanded to a $2\times4\times1$ mesh, and the system was tuned by another relaxation run to improve the electronic structure.

IV. EXPERIMENTAL RESULTS

A. An oxide-free interface

Figure 3 shows Ga 3*d*, As 3*d*, In 3*d*, and In 4*d* core level spectra of the $In_{0.53}Ga_{0.47}As$ surface after 10 cycles of Al_2O_3 ALD. The thickness of the Al_2O_3 layer was estimated to be 0.9 nm by ARXPS, thin enough for photoelectrons to escape through the Al_2O_3 layer and provide information on bonding across the underlying $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. The group III and As core level spectra in Fig. 3 are consistent with the features observed from clean $In_{0.53}Ga_{0.47}As$ (100),[12–14] indicating that the substrate surface remains oxide-free to the detection limit of XPS (in this case $<1/10$ of a monolayer) throughout As decapping and subsequent TMA/H_2O ALD processes.

The HRTEM image in Fig. 4 of the ALD-Al_2O_3/As-decapped $In_{0.53}Ga_{0.47}As$ sample shows that the interface between the Al_2O_3 and $In_{0.53}Ga_{0.47}As$ is atomically abrupt. This is confirmed by the inset HAADF image, which indicates that the As-capping layer was completely removed without detectable oxidation of the $In_{0.53}Ga_{0.47}As$. The ALD-grown Al_2O_3 layer is amorphous, as expected for an alumina film deposited at such a low temperature.

The absence of a detectable interfacial oxide at the Al_2O_3/InGaAs interface after ALD-Al_2O_3 deposition indicates that the combination of (1) As capping to prevent native oxide formation prior to ALD, and (2) a TMA-first Al_2O_3 deposition process performed on the *in situ* As-

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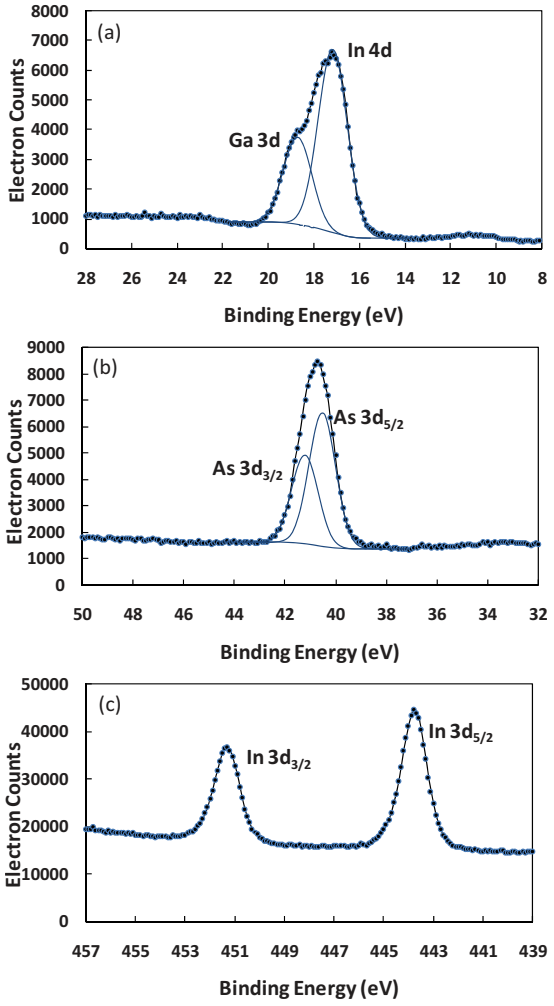

FIG. 3. (Color online) (a) Ga 3*d* and In 4*d*, (b) As 3*d*, and (c) In 3*d* core spectra of $In_{0.53}Ga_{0.47}As$ after 10 cycles of ALD-Al_2O_3. The As-decapped $In_{0.53}Ga_{0.47}As$ surface remains oxide-free during ALD.

decapped substrate suppresses its surface oxidation. A detailed study of the effects of ALD processing conditions on stability of As-decapped InGaAs surface will be the subject of another publication. However, the results of that study suggest that the TMA precursor adsorbs in a facile manner directly on the As-decapped surface, forming a dense and well-ordered layer that resists subsequent oxidation of the underlying InGaAs substrate.

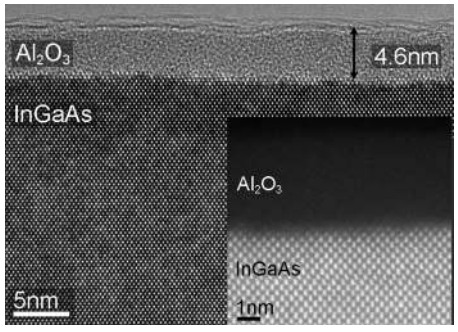

FIG. 4. HRTEM micrograph showing the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. The inset shows a HAADF image of the interface. Because of the strong atomic number contrast in HAADF, the Al_2O_3 layer appears much darker than the $In_{0.53}Ga_{0.47}As$. The absence of any interface layer with brighter contrast shows that the interface is atomically abrupt and free of native oxides of the semiconductor.

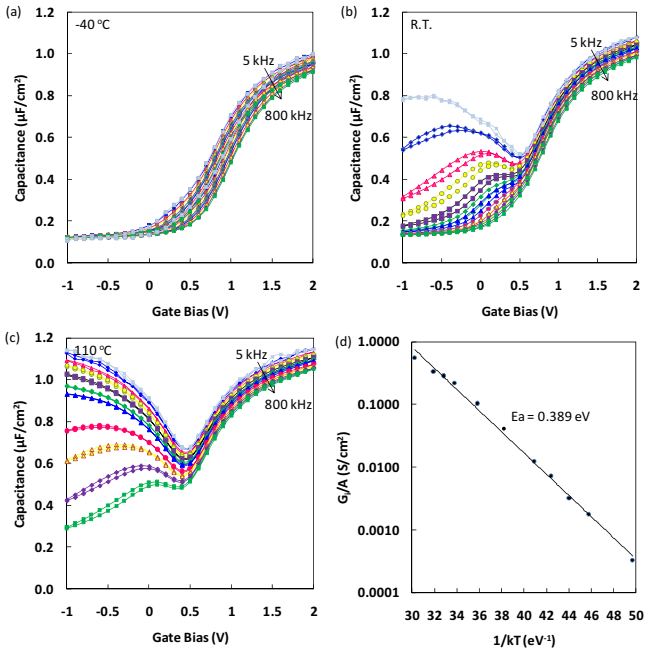

FIG. 5. (Color online) *C-V* characteristics of $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$ at (a) −40 °C, (b) RT, and (c) 110 °C under various frequencies of 5 kHz (■), 10 kHz (♦), 20 kHz (▲), 30 kHz (●), 50 kHz (■), 80 kHz (♦), 100 kHz (▲), 200 kHz (●), 300 kHz (▲), 500 kHz (♦), and 800 kHz (■). (d) Arrhenius plot of inversion specific conductance in $Pt/Al_2O_3/In_{0.53}Ga_{0.47}As$.

B. An unpinned interface

Figures 5(a)–5(c) show the *C-V* characteristics of a representative $Pt/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ capacitor measured in the frequency range 5–800 kHz at −40, RT, and 110 °C. The *C-V* curves exhibit hysteresis less than 40 mV and relatively small frequency dispersion in accumulation compared to previous reports of ALD-Al_2O_3/InGaAs devices prepared without a protective capping layer to prevent native oxide formation.[36,37] The inversion layer conductance was suppressed at −40 °C, whereas strong inversion was achieved at 110 °C, as shown in Figs. 5(a)–5(c).

The inversion specific conductance closely fits an Arrhenius temperature dependence with an activation energy of ~0.39 eV, as shown in Fig. 5(d). The conductance G_i is calculated from the measured capacitance and conductance in strong inversion and measured maximum capacitance in accumulation at a frequency of 5 kHz.[38,39] The activation energy (E_a) determined from the slope of Fig. 5(d) is close to half of $In_{0.53}Ga_{0.47}As$ band gap. This is the expected inversion behavior when the minority carrier concentration is controlled by recombination/generation at defects producing midgap states either in the semiconductor channel or at the oxide/semiconductor interface.

To examine whether a sufficiently high density of midgap interface states exists to pin the Fermi energy in the gap, the Berglund integral[39] was used to calculate the semiconductor surface potential change as a function of gate bias (Fig. 6). The *C-V* data collected at 110 °C and 5 kHz measurement frequency, which exhibit the strongest inversion

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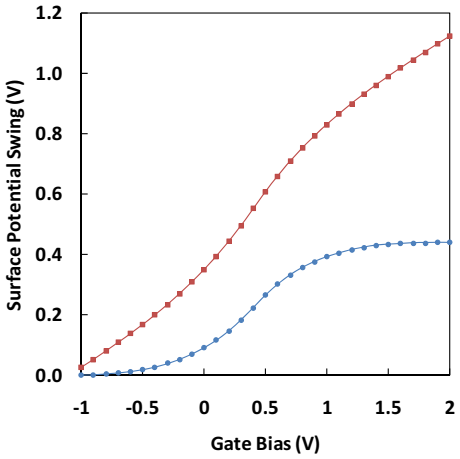

FIG. 6. (Color online) Surface potential swing of a Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$ capacitor estimated assuming the oxide capacitance is ideal (k=8, from Pt/Al_2O_3/Si) (■), and assuming the oxide capacitance is the measured accumulation capacitance at 5 kHz at 110 °C (●).

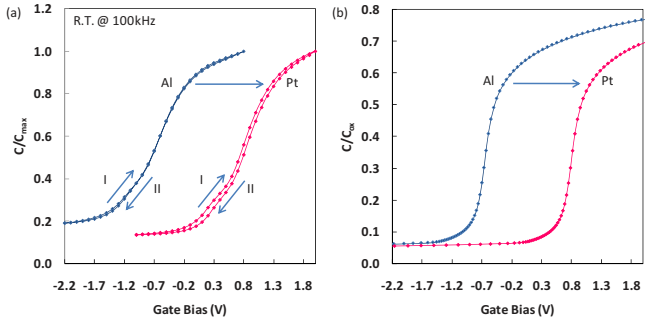

FIG. 7. (Color online) (a) C-V curves of Al-gated and Pt-gated $Al_2O_3/In_{0.53}Ga_{0.47}As$ capacitors measured at 100 kHz at room temperature. C-V measurements were performed from inversion to accumulation (I) and accumulation to inversion (II) and normalized by the maximum capacitance in accumulation (C_{max}). (b) Simulated C-V curves of ideal Al-gated and Pt-gated $Al_2O_3/In_{0.53}Ga_{0.47}As$ capacitors assuming C_{ox} from the ALD-Al_2O_3 dielectric constant (8) measured using Pt/ALD-Al_2O_3/SiO_2/Si capacitors and D_{it}=0.

response, were integrated. Because there is some uncertainty in the oxide capacitance (C_{ox}), two curves are shown, corresponding to different assumed values for C_{ox}. The red curve is calculated using C_{ox} from the dielectric thickness (4.6 nm) and the ALD-Al_2O_3 dielectric constant (8) measured using Pt/ALD-Al_2O_3/SiO_2/Si capacitors and the blue curve is calculated assuming C_{ox} is equal to the measured capacitance in accumulation. These curves set upper and lower bounds on the surface potential change. The band-gap potential difference of $In_{0.53}Ga_{0.47}As$, 0.71 V at 110 °C,[40] is within these bounds. It is significant that the lower bound of the surface potential change exceeds one half of the band-gap potential, which is inconsistent with the presence of a very high density of midgap interface states required for Fermi level pinning at midgap. This suggests that recombination/generation events that control the conductance in inversion occur primarily at defects in the III-V channel rather than at interface states. This result is also in keeping with the absence of a strong capacitance peak in depletion, as shown in Figs. 5(a)–5(c).

A key finding apparent in Fig. 5 is the temperature independence of the frequency dispersion of the accumulation capacitance, which is inconsistent with filling and emptying of relatively slow interface states.[41] Instead, these data are consistent with tunneling of carriers into near-interface defects, border traps,[42,43] in the a-Al_2O_3 layer. Details of the border trap response and approaches to passivate the associated defects in the ALD-Al_2O_3 dielectric will be the subject of another publication.[44]

The measured and simulated flat band voltage (V_{fb}) shifts in C-V curves for Pt and Al gate metals are identical, 1.4 V, consistent with the reported work function difference of these metals on Al_2O_3.[15] The C-V curves are shown in Fig. 7. Observation of a near-ideal flat band voltage for both Pt-electroded and Al-electroded capacitors indicates the absence of a significant interface dipole between the Al_2O_3 layer and the InGaAs channel. In contrast, a large and positive flat band voltage shift is typically observed for Al_2O_3 dielectrics deposited on SiO_2/Si substrates.[45]

V. *AB INITIO* CALCULATION RESULTS

A realistic amorphous oxide sample was generated using a hybrid classical-DFT MD "melt-and-quench" approach. The amorphous oxide was bonded to the In/Ga-rich $In_{0.5}Ga_{0.5}As$ (100)−4×2 reconstruction, the same surface expected to be prepared by experimentally decapping of the wafers to leave a group III rich reconstruction. The resulting predicted a-$Al_2O_3/In_{0.5}Ga_{0.5}As$ (100)−4×2 interface does not exhibit intermixing and has no As–O bonds. The final structure has polar As–Al bonds and In/Ga–O bonds of opposite dipole direction. There is only a small displacement of InGaAs interface atoms and little InGaAs lattice distortion relative to the atomic position in the InGaAs prior to oxide bonding as shown in Fig. 8. Three typical causes of midgap states are As–O bond formation, interface mixing, and disruption of the substrate lattice to form new dangling bonds;[46] the DFT model of the ideal a-$Al_2O_3/In_{0.5}Ga_{0.5}As$ (100)−4×2 interface shows the absence of all three of these phenomena.

To provide a closer comparison to experiments, the Bader charges[47,48] of the interface shown in Fig. 8 were calculated. Relative to the $In_{0.5}Ga_{0.5}As$ (100)−4×2 surface atoms, the As atoms bonded to Al gain ~0.4|e|, the In and Ga bonded to one O atom lose ~0.3|e|, while In bonded to two O atoms lose ~0.7|e|. These results show weakly polar bond formation and no ionic bonding. Relative to bulk atoms, the As bonded to Al have excessive charge of ~0.26|e|, the In bonded to one O atom are depleted by ~0.18|e|, the In bonded to two O are depleted by ~0.40|e|, and the Ga bonded to one O are depleted by ~0.08|e|. Interfacial semiconductor atoms are predicted to have near bulklike charge consistent with the XPS and CV results (Figs. 3 and 7). The projected DOS was calculated for the interface region and the semiconductor region just below the interface which would correspond to the channel shown in Fig. 8. For a-Al_2O_3/InGaAs, the Fermi level is positioned in the middle of the band-gap region. Consistent with the unpinned interface observed in electrical measurements, the band gap for the ideal a-$Al_2O_3/In_{0.5}Ga_{0.5}As$ (100)−4×2 interface is equal to the band gap of the clean surface, and the band gaps of the interface region and bulklike channel region overlap.

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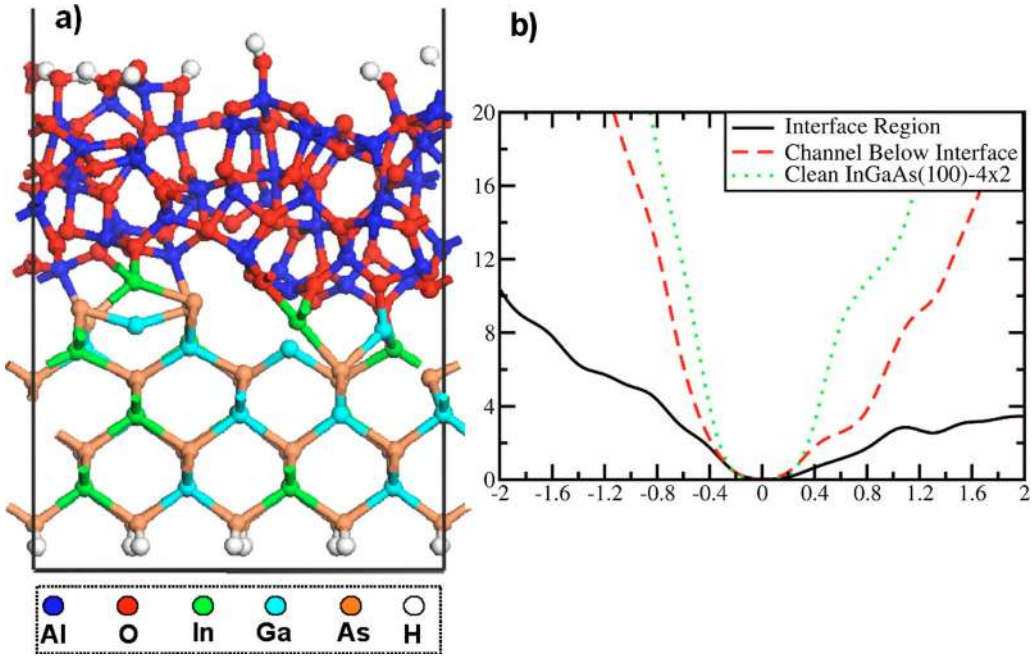

FIG. 8. (Color online) DFT-MD model of a-$Al_2O_3/In_{0.5}Ga_{0.5}As(100)-4\times2$ after 800 K anneal. (a) Annealed and relaxed structure of the a-$Al_2O_3/In_{0.5}Ga_{0.5}As(100)-4\times2$ interface (with eight OH passivating groups at the vacuum interface). (b) Projected DOS for the interface and InGaAs channel below the interface showing no midgap states. DOS for the clean $In_{0.5}Ga_{0.5}As(100)-4\times2$ surface as a reference.

VI. CONCLUSIONS

Arsenic (As_2) capping to prevent oxidation of $In_{0.53}Ga_{0.47}As$ followed by *in situ* As_2 desorption prior to ALD-Al_2O_3 deposition avoided detectable oxidation of the III-V channel, as indicated by *in-situ* and *ex situ* XPS and by chemically sensitive STEM cross-sectional images. Electrical measurements of MOS capacitors prepared on the As-decapped $In_{0.53}Ga_{0.47}As$ (100) substrate exhibited temperature-dependent and frequency-dependent capacitance and conductance behavior that is consistent with an interface at which the Fermi level is unpinned. The observed flat band voltages for capacitors with Pt and Al electrodes indicate a minimal interfacial dipole and the ability to control majority and minority carrier concentrations in the channel using the gate work function. These results are consistent with the predictions of DFT calculations for an ideal a-$Al_2O_3/In_{0.53}Ga_{0.47}As$ $(100)-4\times2$ interface formed by a melt-and-quench simulation procedure. Both experimental results and *ab initio* electronic structure simulations indicated that, by reducing the perturbation of the local electronic structure of the InGaAs surface, ALD-Al_2O_3 growth on an As-decapped channel offers a route to chemically abrupt and electrically passive oxide/III-V interfaces.

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