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Augmented Fractional-order Reset Control: Application in Precision Mechatronics

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***Abstract*—Linear control such as PID possesses fundamental limitations, seen through the Waterbed effect. Reset control has been found to be able to overcome these limitations, while still maintaining the simplicity and ease of use of PID control due to its compatibility with the loop shaping method. However, the resetting action also gives rise to higher order harmonics that hinders consistent realization of the aforementioned expected improvement. In this paper, a fractional-order augmented state analogue of the reset integrator is investigated. This analogue is composed of a series of augmented states that each possesses unique reset values, providing the same first order harmonic behavior but reduced higher order harmonics magnitude compared to the reset integrator. The optimal number of augmented states along with the corresponding tuning values are investigated. To validate the improvement, the reset integrator and the optimal fractional order analogue are tuned to equally improve disturbance rejection of a high precision 1 DOF positioning stage while maintaining the stability level, with both designed to overcome linear control. From simulation and experimental results, it was found that the novel fractional-order augmented state analogue gives rise to disturbance rejection performance that is closer to the desired and expected improvement, compared to using the traditional reset integrator.**

***Index Terms*—Reset Control, Motion control, Fractional Calculus, Fractional Order Control**

I. Introduction

PID control scheme has become the most used controller in many industries even if it is new or high-tech [1], [2] due to robustness and ease of use through the loop-shaping method. However, being inherently linear, it suffers from fundamental limitations, which are the waterbed effect and Bode's gain phase relation [3], [4]. Reset control is a nonlinear control technique which has gained increasing attention due to its compatibility with frequency domain techniques for design and analysis, which are popular within industry.

In reset control, the states of the controller are reset when a predefined condition is satisfied. The first reset element introduced was a Clegg Integrator (CI) in 1958 [5], which is an integrator whose state is reset to zero when the input is zero. Using a pseudo-linear frequency response description of nonlinear filters called Describing Function (DF) [6], the frequency response of the CI is obtained, which reveals a similar gain behaviour as the linear integrator but with only -38° phase lag. This is advantageous since this violates Bode's gain phase relationship, allowing improved performance without sacrificing stability. The idea of reset has also been extended to elements such as First Order Reset Element (FORE) [7], [8] and Second order Reset Element (SORE) [9]. These elements have been successfully applied to satisfy various objectives such as phase lag reduction [10], broadband phase compensation [11], improving servomotor performance [12], and improvement of mid frequency disturbance rejection [13].

Frequency response of reset controllers can be approximated using the aforementioned DF method [6]. However, since it is an approximation, the advantages described previously are not always seen in practice. This is because the higher order harmonics present in the output of the nonlinear reset controllers are not considered by the DF method. These higher order harmonics are analyzed in open loop through HOSIDF method [14] and recently in closed loop [15]. There exists a need to reduce the higher order harmonics such that the output is dominated by the first harmonic, which makes the benefit of reset control predicted by the DF consistently realizable. This paper presents a novel augmented analogue for the reset integrator with the aim of obtaining the same first harmonic behavior while reducing the higher order harmonics.

The paper is structured as follows. Section II of this paper will introduce reset control. Section III examines the fractional order augmented state reset integrator and the benefits it possesses over the traditional reset integrator. Section IV gives an illustrative example of the benefits of using the augmented state reset integrator through simulation and experimental validation of disturbance rejection on a precision positioning

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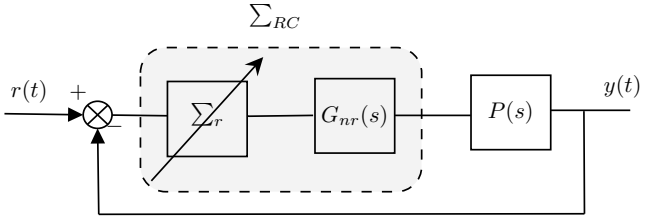


Fig. 1: Block diagram of a reset controller RC with a plant P.

system. Conclusions and possible future work are outlined in section V.

II. Reset Control

A. Definition

A single-input single-output (SISO) reset controller (denoted Σ_{RC}) is defined as

$$\Sigma_{RC} := \begin{cases} \dot{x}(t) = A_r x(t) + B_r e(t) & \text{if } e(t) \neq 0 \\ x(t^+) = A_\rho x(t) & \text{if } e(t) = 0 \\ u(t) = C_r x(t) + D_r e(t) \end{cases} \quad (1)$$

where $x(t)$ are the states, and A_r, B_r, C_r and D_r are the matrices corresponding to state-space representation. These are referred to as the base linear system of the controller. $e(t)$ and $u(t)$ are the input and output of the controller respectively. A_ρ is a diagonal matrix that dictates the after-reset values of the states.

Theorem 1. *[16] The reset controller defined by* (1) *with a sinusoidal input has a $\frac{2\pi}{\omega}$ periodic solution that is globally asymptotically stable for all $\omega > 0$ if and only if*

$$|\lambda(A_\rho e^{\Delta})| < 1 \quad (2)$$

where $\Delta \in \mathbb{R} > 0$. This theorem consequently constraints each member of the diagonal of A_ρ to be between -1 and 1.

B. Reset Systems Stability

Fig. 1 shows a reset controller Σ_{RC} with a plant P. As shown in the figue, the reset controller can be decomposed into a reset part Σ_r and a non reset part G_{nr}. Let n_r and n_{nr} therefore denote the number of reset and non reset states of Σ_{RC} respectively.

Theorem 2. *[17] The reset control system depicted in Fig. (1) is quadratically stable if and only if the H_β condition holds, i.e. there exists a $\beta \in \mathbb{R}^{n_r}$ and a positive definite matrix $P_r \in \mathbb{R}^{n_r \times n_r}$ such that the transfer function*

$$Z_\beta(s) := \begin{bmatrix} \beta C_p & 0_{n_r \times n_{nr}} & P_r \end{bmatrix} (sI - A_{cl})^{-1} \begin{bmatrix} 0_{n_p} \\ 0_{n_{nr} \times n_r} \\ I_{n_r} \end{bmatrix} \quad (3)$$

is strictly positive real. And

$$A_\rho^T P_\rho A_\rho - P_\rho \leq 0. \quad (4)$$

Here A_{cl} is the closed loop A matrix of Fig. 1 defined as:

$$A_{cl} = \begin{bmatrix} A_p & B_p C_{RC} \\ -B_{RC} C_p & A_{RC} \end{bmatrix}$$

in which (A_p, B_p, C_p) are the state space matrices of Σ_p, and (A_{RC}, B_{RC}, C_{RC}) are the state space matrices of Σ_{RC}.

C. Describing function

Describing Function (DF) is a pseudo-linear approximation of the frequency response of nonlinear elements like reset controllers. Since it only considers the first harmonic of the output, expected experimental results based on loop shaping are not seen [11]. Reference [6] developed the concept of higher order sinusoidal input describing function (HOSIDF), which is further developed by [14] specifically for reset elements. The HOSIDF formula for reset elements is as shown:

$$\begin{aligned} H_n(\omega) &= \begin{cases} C_r(j\omega I - A_r)^{-1}(I + j\Theta(\omega))B_r + D_r, & n = 1 \\ C_r(j\omega n I - A_r)^{-1} j\Theta(\omega) B_r, & \text{odd } n > 2 \\ 0, & \text{even } n \geq 2 \end{cases} \\ \Theta(\omega) &= -\frac{2\omega^2}{\pi}\Delta(\omega)[\Gamma(\omega) - \Lambda^{-1}(\omega)] \\ \Lambda(\omega) &= \omega^2 I + {A_r}^2 \\ \Delta(\omega) &= I + e^{\frac{\pi}{\omega}A_r} \\ \Delta_\rho(\omega) &= I + A_\rho e^{\frac{\pi}{\omega}A_r} \\ \Gamma(\omega) &= \Delta_\rho^{-1}(\omega) A_\rho \Delta(\omega) \Lambda^{-1}(\omega) \end{aligned} \quad (5)$$

where $H_n(\omega)$ is the n^{th} harmonic describing function for sinusoidal input with frequency of ω. The DF is therefore a special case of HOSIDF with $n = 1$.

III. Augmented Fractional-order State Reset Integrator

Fractional calculus generalizes integration and differentiation to real or complex number powers. There exist multiple accepted definitions of fractional differentiation. The notation $D^\alpha x(t)$, $k \in [0, 1]$ in this paper will refer to the Caputo definition defined in [18].

A. Augmented system of fractional order reset integrator

A fractional order reset integrator is defined as:

$$\begin{aligned} D^\alpha x(t) &= e(t) \\ x(t^+) &= \gamma x(t) \\ u(t) &= x(t) \end{aligned} \quad (6)$$

where $\alpha \in [0, 1]$.

The fractional order integrator is implemented through the CRONE approximation [19] with its poles being reset, defined by:

$$s^\alpha \overset{\gamma}{\approx} P \prod_{m=1}^{N} \frac{1 + \frac{s}{\omega_{z,m}}}{1 + \frac{s}{\omega_{p,m}}} \overset{A_\rho}{} \quad (7)$$

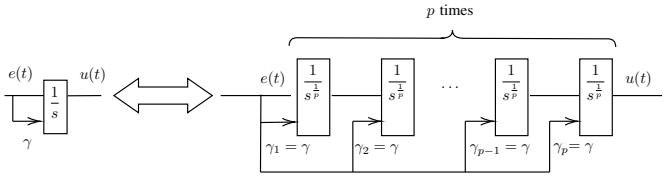


Fig. 2: Illustration of equivalence between cascade of fractional order integrators and an integer reset integrator. The arrows indicate that the reset of each element is with respect to the input to the cascade i.e. $e(t)$

with

$$\omega_{z,m} = \omega_l \left(\frac{\omega_n}{\omega_l}\right)^{\frac{2m-1-\alpha}{2N}}$$
$$\omega_{p,m} = \omega_1 \left(\frac{\omega_h}{\omega_l}\right)^{\frac{2m-1+\alpha}{2N}}$$

where $\alpha \in (0,1)$, N is the number of real stable poles and real minimum phase zeros, $[\omega_l, \omega_h]$ is the frequency range where the approximation is valid, and P is a parameter to tune the gain of the approximation. A_ρ is a reset matrix that corresponds to the reset of the fractional order integrator γ.

B. Augmented system of integer order reset integrator

The integer-order state reset integrator is obtained by setting $k = 1$ in (6). The augmented fractional order form of this case is given by:

$$\begin{aligned} D^q \chi(t) &= \mathbf{A}\mathcal{X}(t) + \mathbf{B}e(t) \\ \mathcal{X}\left(t^+\right) &= \mathbf{A}_\rho \mathcal{X}(t) \\ u(t) &= \mathbf{C}\mathcal{X}(t) \end{aligned} \tag{8}$$

where,

$$\mathbf{A} = \begin{bmatrix} \mathbf{0} & \boldsymbol{I} \\ \mathbf{0} & \mathbf{0} \end{bmatrix}, \quad \mathbf{A}_\rho = \gamma \boldsymbol{I}$$
$$\mathbf{B} = \begin{bmatrix} 0 \\ \vdots \\ 1 \end{bmatrix}, \mathbf{C} = \begin{bmatrix} 1 & \dots & 0 \end{bmatrix}$$

Here $\mathcal{X} = [x_1, x_2 \dots x_p]^T$ is a vector of the augmented states and $p = \frac{1}{q}$, where $p \in \mathbb{Z}^+$.

C. Equivalence of cascaded fractional order reset integrators with augmented integer order reset integrator

Remark 1. *Consider Fig. 2. The cascade of p fractional order reset integrators in series is equivalent to the augmented form of an integer reset integrator with $q = \frac{1}{p}$.*

Proof. Consider the k^{th} fractional order reset integrator, with $1 \le k \le p$. The state space representation becomes:

$$\begin{aligned} D^{1/p} x_k(t) &= e_k(t) \\ x_k(t^+) &= \gamma_k x_k(t) \\ u_k(t) &= x_k(t) \end{aligned} \tag{9}$$

With $e_1(t) = e(t)$, $e_k = u_{k-1}$ and $u_p(t) = u(t)$, the combined state space of the cascade is simplified to:

$$D^{1/p} \begin{bmatrix} x_1(t) \\ \vdots \\ x_p(t) \end{bmatrix} = \begin{bmatrix} \mathbf{0} & \mathbf{0} \\ \boldsymbol{I} & \mathbf{0} \end{bmatrix} \begin{bmatrix} x_1(t) \\ \vdots \\ x_p(t) \end{bmatrix} + \begin{bmatrix} 1 \\ \vdots \\ 0 \end{bmatrix} e(t) \tag{10}$$
$$u(t) = \begin{bmatrix} 0 & \dots & 1 \end{bmatrix} \begin{bmatrix} x_1(t) \\ \vdots \\ x_p(t) \end{bmatrix}$$

where $x_2 = x_1/D^{1/p}$, $x_3 = x_2/D^{1/p}$, $\dots$, $x_p = x_{p-1}/D^{1/p}$.

Reverse the ordering of the state vector above such that x_p becomes in the first entry. With $q = 1/p$ and $\mathbf{A}_\rho = \gamma \boldsymbol{I}$, this results in state space that is equal to (8). Therefore equivalence is proven and the augmented system is a valid replacement of the integer-order reset integrator.

□

Remark 2. *[20] Let the reset control system Σ_{RC} in Fig. 1 be composed of firstly a reset element Σ_r followed by a linear element G_{nr}. The higher order harmonics gain of Σ_{RC} is smaller than Σ_r if G_{nr} is a linear lag element:*

$$|H_n(j\omega)|_{\Sigma_{RC}} \le |H_n(j\omega)|_{\Sigma_r}, \quad \textit{odd } n > 1 \tag{11}$$

Remark 3. *Consider a reset integrator with reset value γ. With $-1 < \gamma \le 1$, the following relation holds:*

$$-90^\circ \le \angle H_1(j\omega) < 0^\circ \tag{12}$$

where -90° corresponds to $\gamma = 1$ (linear integrator) and 0° corresponds to $\gamma = -1$.

Remark 3 also holds for the fractional order reset integrator of (6), with the lower limit changed to $-90k^\circ$.
Equation (10) is the analogue to the reset integrator if $\gamma_k = \gamma, \forall\, k$. It therefore follows that not only the first but also higher order harmonics are similar. However, it is desired to reduce the higher order harmonics while maintaining the first order harmonic behavior. Considering Remarks 2 and 3, this could be achieved through a combination of $\gamma_1, \dots, \gamma_p$ that does not necessarily satisfy the aforementioned restriction on γ_k. More specificly, from Remark 2, there could be an advantage in making later fractional integrators more linear. Therefore, the goal of this paper is to design $\gamma_1, ..., \gamma_p$ such that the first harmonic is the same as that of the reset integrator while simultaneously possessing lower higher order harmonic gain.

This goal is casted in an optimization problem as shown:

$$\min_{\gamma_{Aug}=[\gamma_1,\gamma_2,\dots,\gamma_p]} |H_n(\gamma_{Aug}, j\omega)|_{Aug} \tag{13}$$
$$\forall \text{ odd } n > 1\,, \forall \omega \in [\omega_l, \omega_h]$$

subject to

$$|H_1(\gamma_{Aug}, j\omega)|_{Aug} = |H_1(\gamma, j\omega)|_{\text{RI}}$$
$$\angle H_1(\gamma_{Aug}, j\omega)_{Aug} = \angle H_1(\gamma, j\omega)_{\text{RI}}$$

where Aug refers to the fractional order analogue of the reset integrator and RI stands for Reset Integrator. For simplicity, the optimization will be run for $p = 2$, 3 and 4 and the reductions

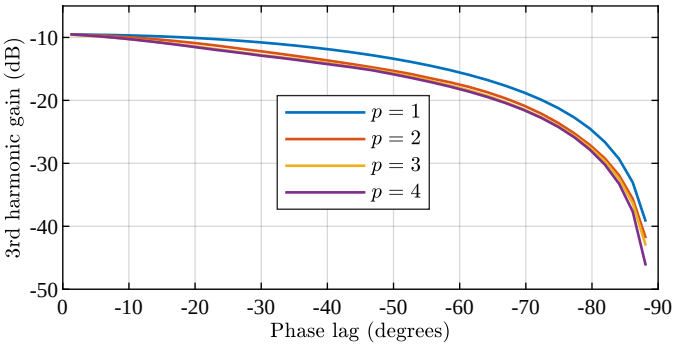


Fig. 3: 3rd order harmonic gain at $\omega = 100$ rad/s of various p values, for different provided phase lag.

in higher order harmonics magnitude will be compared. In addition, non-zero values of γ for RI will also be considered.

D. Results

Table I shows the third order harmonic gain for different reset values of the reset integrator and its respective augmented fractional order analogue for $p = 2$, 3 and 4. Instead of the different reset values, by utilizing Remark 3, the horizontal axis of Fig. 3 alternatively shows the phase lag that the reset integrator provides which is matched by the novel augmented fractional order analogue. Table I shows the reset values of the augmented states for each value of p and the optimal reset values. Some observations:

- For all p and phase lag values, the integrator nearing the end of the cascade is more linear than those nearing the start, which satisfies Remark 2.
- As the required phase lag decreases, the reset value of the integrators near the end of the cascade is not fully linear. Considering Remark 2, this indicates that the starting integrators cannot provide all the required phase lag reduction, and thus the integrators near the end provide some support in this regard.
- There is more reduction of the third order harmonic for larger phase lag. Thus there exists a tradeoff between obtaining larger reduced phase lag advantage and the corresponding third harmonic gain reduction.
- The further reduction in third harmonic gain by going from $p = 2$ to $p = 3$ or $p = 4$ is insignificant compared to reduction from the original reset integrator to $p = 2$ case. Therefore it is recommended to use $p = 2$ in implementation.

E. Non-Zero Higher Order Harmonic Phase

In this subsection it will be shown how the non-zero higher order harmonics phase of the augmented fractional-order state analogue could be of benefit.

The time domain output of a reset element given a sinusoidal input $\sin(\omega t)$ is:

$$u(t) = \sum_{n=1}^{\infty} A_n \sin(n\omega t + \phi_n), \text{ odd } n \geq 1 \qquad (14)$$

TABLE I: Reset values and 3rd harmonic gain at $\omega = 100$ rad/s of each augmented state for various p values, the subscripts for the various γ correspond to Fig. 2.

Reset Integrator		
γ	Equivalent phase lag (°)	3rd harmonic gain (dB)
-0.8	-5.00	-9.57
-0.4	-18.60	-10.00
0	-38.15	-11.63
0.4	-61.38	-15.94
0.8	-81.95	-26.62

Augmented analogue, $p = 2$				
γ	Equivalent phase lag (°)	γ_2	γ_1	3rd harmonic gain (dB)
-0.8	-5.00	-0.98	-0.74	-9.71
-0.4	-18.60	-0.98	-0.11	-10.83
0	-38.15	-0.97	0.66	-13.56
0.4	-61.38	-0.38	1.00	-18.44
0.8	-81.95	0.59	1.00	-29.32

Augmented analogue, $p = 3$					
γ	Equivalent phase lag (°)	γ_3	γ_2	γ_1	3rd harmonic gain (dB)
-0.8	-5.00	-0.97	-0.97	-0.66	-9.80
-0.4	-18.60	-0.95	-0.95	0.27	-11.25
0	-38.15	-0.75	-0.71	1.00	-13.72
0.4	-61.38	-0.6	0.48	1.00	-18.55
0.8	-81.95	0.35	1.00	1.00	-29.68

Augmented analogue, $p = 4$						
γ	Equivalent phase lag (°)	γ_4	γ_3	γ_2	γ_1	3rd harmonic gain (dB)
-0.8	-5.00	-0.94	-0.92	-0.87	-0.64	-9.81
-0.4	-18.60	-0.95	-0.92	-0.87	0.53	-11.34
0	-38.15	-0.97	-0.82	0.18	1.00	-13.73
0.4	-61.38	-0.43	-0.23	1.00	1.00	-18.60
0.8	-81.95	0.16	1.00	1.00	1.00	-30.20

The above emphasizes that not only the gain but the higher order harmonics phase also influence the output of the reset element.

To investigate this, the RMS difference between the time domain response of the reset integrators and the ideal response is computed, where the ideal response is the response of the reset integrator with all the higher order harmonic gains eliminated. Fig. 4 shows this RMS difference for different values of the higher order harmonics phase. At -48.5° there exists a minimum of the RMS difference. The reset integrator however, has zero higher order harmonics phase and so this minimum cannot be achieved.

In contrast, the augmented fractional-order state analogue has a negative higher order harmonics phase. For instance the third harmonic phase is shown in Fig. 5 for $p = 2$. Therefore in addition to lower higher order harmonics gain, the augmented fractional-order state analogue also possesses a beneficial higher order harmonics phase behavior.

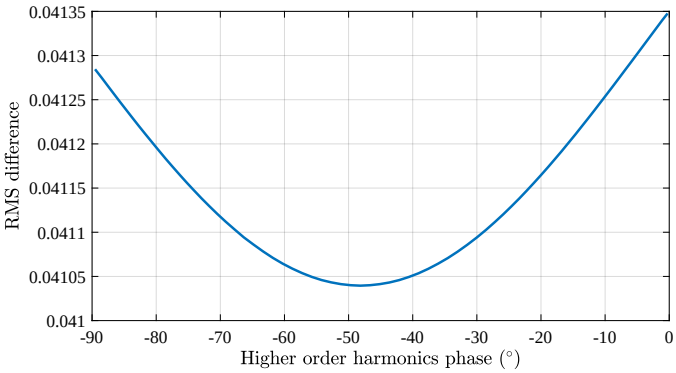


Fig. 4: Higher order harmonics phase vs. RMS error of reset integrator with $\gamma = 0$.

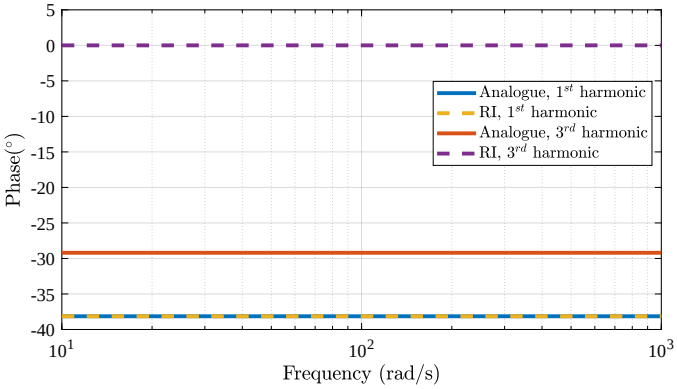


Fig. 5: Phase plot of 1st and 3rd harmonic of the RI vs. augmented fractional-order analogue.

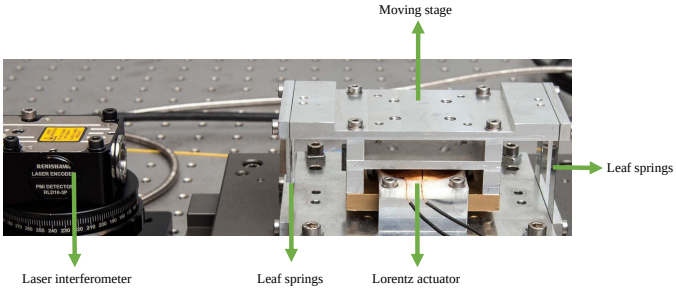


Fig. 6: The custom-designed precision stage used for experiments.

IV. Illustrative Example

For validation in performance improvement of a system that utilizes the augmented fractional state analogue, four controllers are designed and studied in simulation and in practice. This section compares results of disturbance rejection performance between a parallel PID (termed PI+D) and three other parallel PID respectively in series with a linear integrator, Clegg Integrator and augmented fractional state analogue of the Clegg Integrator with $p = 2$.

1) Plant: The plant use for this validation is a flexure-guided stage actuated by a Lorentz actuator as shown in Fig. 6, with Fig. 7 describing its identified frequency response and additionally a fitted second order transfer function. The position of the plant is sensed using a laser interferometer with 10nm resolution, with the sampling period of 100μs.
The fitted transfer function is:

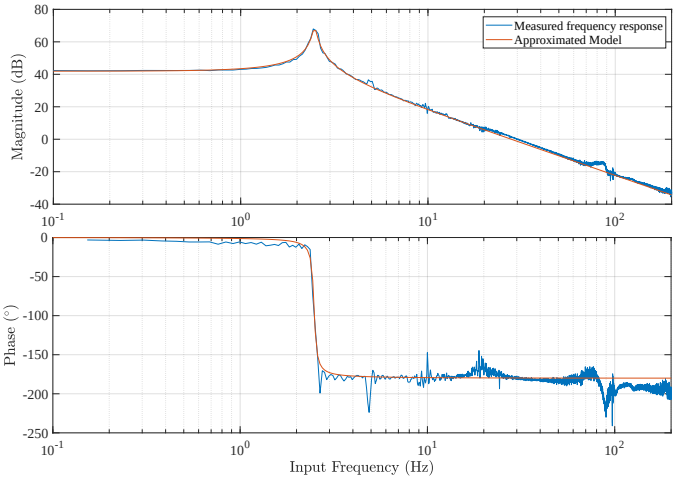
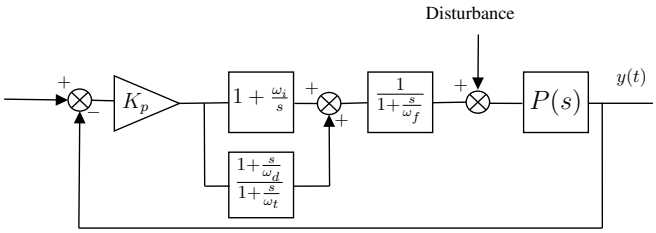


Fig. 7: Identified frequency response of the stage.

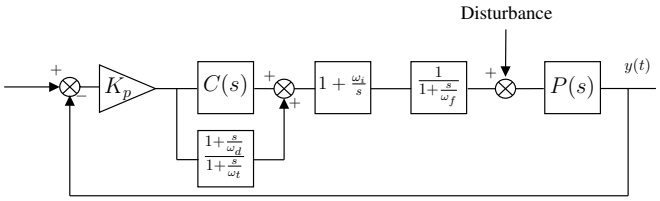
$$G(s) = \frac{3.038e4}{s^2 + 0.7413s + 243.3} \tag{15}$$

2) Control Strategy: Four sets of controllers are designed with a bandwidth of 100 Hz: a parallel PID controller (PI+D), a parallel PID with an extra tamed integrator ((PI+D)PI), a parallel PID with an extra tamed Clegg Integrator ((PCI+D)PI), and a parallel PID with an extra tamed augmented fractional order analogue of Clegg Integrator ((PCI_{Aug}+D)PI). Fig. 8 depicts the details of these controllers. As shown in Fig. 9, the (PI+D)PI controller is capable of outperforming PI+D in terms increased gain at low frequencies resulting in better disturbance rejection, however with the tradeoff of phase margin reduction. Considering the reduced phase lag advantage of a Clegg Integrator, it is surmised that the (PCI+D)PI controller could be tuned to have less phase margin reduction while still maintaining the gain behavior of (PI+D)PI, which is indeed the case as shown in yellow and blue in Fig. 9. To verify this result, Fig. 10 shows simulation result of disturbance rejection performance to 1 Hz disturbance input. Contrary to expected performance from Fig. 9, the simulation plot shows (PCI+D)PI performing far worse compared to (PI+D)PI; this is because Fig. 9 shows only the first order harmonic.

To reduce the effects of the higher order harmonics, the augmented fractional-order analogue replaces the Clegg Integrator (giving the controller (PCI_{Aug}+D)PI), with tuned open loop performance shown in purple in Fig. 9. The simulation result is also shown in purple in Fig. 10. From these figures it is observed that the phase margin of (PCI+D)PI is still maintained, while the jump size in Fig. 10 reduced in magnitude, making the maximum amplitude of the response now closer to (PI+D)PI.



(a) PI+D



$$C(s) = 1 + \frac{\omega_i}{s} \Longrightarrow (PI + D)PI$$

$$C(s) = 1 + \frac{\omega_i}{s}\overset{\gamma=0}{\not}{} \Longrightarrow (PCI + D)PI$$

$$C(s) = 1 + \frac{\omega_i}{s}\overset{\gamma_{CI_{Aug}}=[-0.97,0.66]}{\not}{} \Longrightarrow (PCI_{Aug} + D)PI$$

(b) Control schemes used for the adapted PI+D controllers

Fig. 8: Control scheme definitions for validation. Disturbance refers to an applied sinusoidal disturbance input.

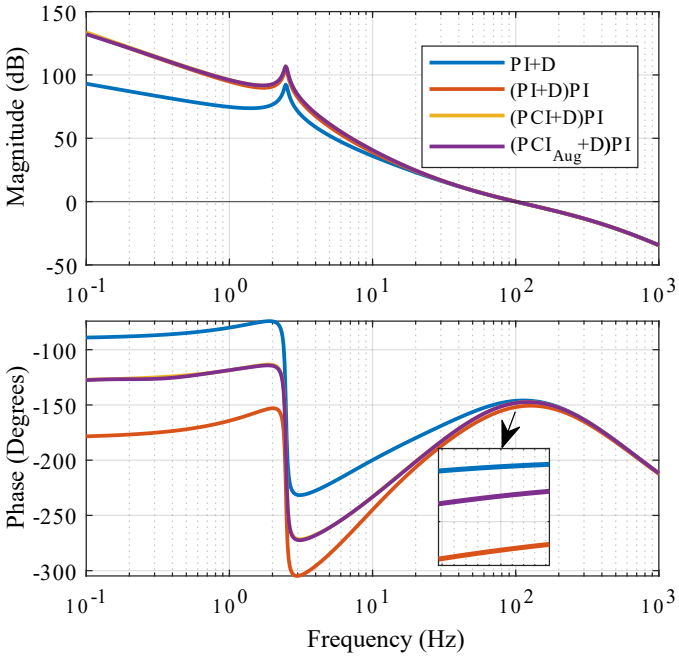


Fig. 9: Open loop frequency response of control scheme in Fig. 8. The gain and phase response of (PCI+D)PI (yellow) is below that of (PCI$_{Aug}$+D)PI (purple).

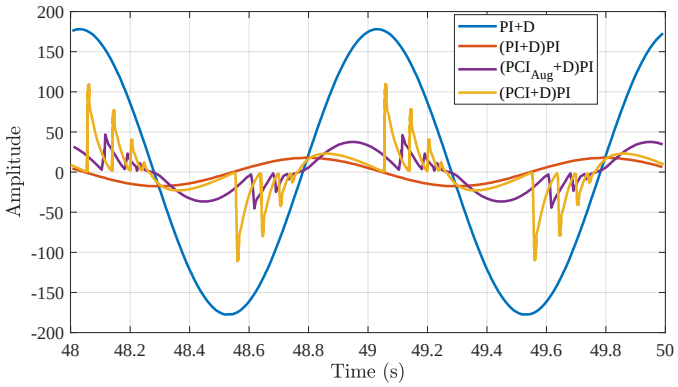


Fig. 10: Response of control scheme in Fig. 8 to a 1 Hz disturbance, using each of the four different extra controllers.

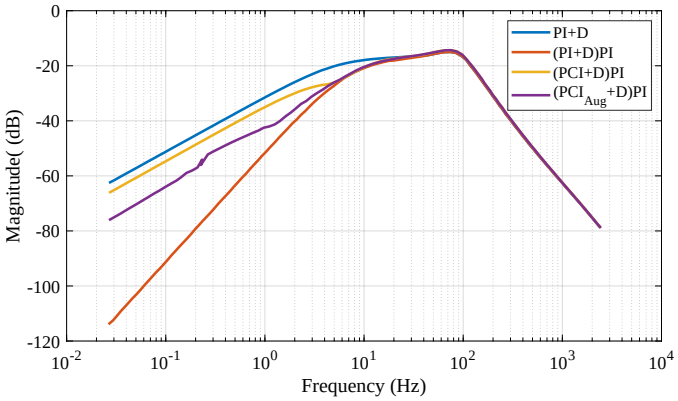


Fig. 11: Process sensitivity plot based on (16).

To see whether this improvement exists over a range of frequencies, a process sensitivity function is constructed. To capture the higher order harmonics in the process sensitivity function plot for the controllers with reset elements, a new process sensitivity function is defined as:

$$S(\omega) = \frac{max(|e(t)|)}{|D|} \quad \text{for } t \geq t_{ss} \tag{16}$$

where t_{ss} is the time it takes for the response to become steady state and periodic, $y(t)$ is the output and D is the amplitude of the sinusoidal disturbance input. This function is found by simulating the closed loop system with a disturbance input for increasing, closely spaced ω. The plot is shown in Fig. 11. Here it is seen that compared to (PCI+D)PI, (PCI$_{Aug}$+D)PI's performance is closer to (PI+D)PI up to approximately 4 Hz, from which the performance of all the reset controllers are now able to match (PI+D)PI.

It is also noted that the higher stability level of the (PCI+D)PI and the (PCI$_{Aug}$+D)PI compared to (PI+D)PI and PI+D, which was implied by their higher phase margin from Fig. 9, was also taken by utilizing the Descibing Function. This therefore means that the true stability level may not be the same as what the DF predicted in this figure. To check that the higher stability level indeed truly exist, the peak of the step response is examined, with a lower overshoot indicating higher

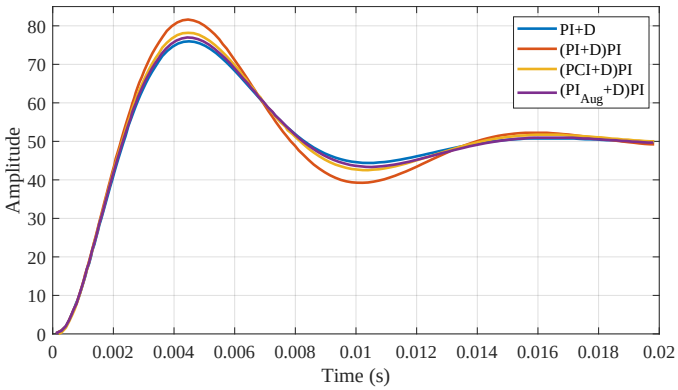


Fig. 12: Step response of each controller.

TABLE II: Experiment results. Disturbance sinusoidal input amplitude is 6528 (10 nm) and step input size is 1000 (10 nm).

Sin Dist.	$\max(\lvert y(t)\rvert)$			
Hz	PI+D	(PI+D)PI	(PCI+D)PI	(PCI$_{Aug}$+D)PI
0.1	21	3	14	13
0.2	32	3	25	20
0.3	56	4	37	35
0.4	74	5	49	40
0.5	93	7	61	46
0.6	110	8	72	62
0.7	127	12	84	69
0.8	146	14	96	78
0.9	163	13	107	85
1	178	19	116	89
2	341	68	206	146
3	476	137	263	250
4	582	216	296	290
Step Dist.	$\max(\lvert y(t)\rvert)$			
1000	1492	1611	1515	1516

stability. This is shown in Fig. 12. This confirms that a higher stability level has indeed been achieved.

3) Stability Check Using H_β condition: To further confirm the stability of the fractional order analogue, the H_β condition described in Section II is also applied on the control scheme of Fig. 8. Solving the condition using a YALMIP Sedumi solver [21], a positive definite matrix P_r was indeed found, further confirming that the fractional order analogue is indeed stable.

V. Experiment Results

To validate the closed loop simulation results, an experiment is conducted. Disturbances of selected frequencies are chosen, and the amplitude of the plant response are recorded. To check the stability level, a step input is also applied.

Table II shows the maximum error of the plant controlled by each of the four different controllers at steady state. It is seen that the trend in the simulation result is confirmed, with the (PCI$_{Aug}$+D)PI outperforming (PCI+D)PI and PI+D in the frequency region predicted by the simulation in Fig. 11. In addition, the step response of the (PCI+D)PI and the (PCI$_{Aug}$+D)PI also exhibit a similar overshoot value, indicating that the increased stability level predicted by simulation is also seen in experiment.

VI. Conclusion

Reset controller is a subset of nonlinear controllers that overcomes the fundamental limitations of linear controllers, while still retaining the advantage of linear controllers in that the loop shaping method is applicable through the Describing Function method. However, the Describing Function does not take into account higher order harmonics, which makes the actual output of the reset controlled system sometimes deviate from that predicted using the Describing Function. It is then desired to minimize the role of these higher order harmonics on influencing the output.

Augmented fractional-order reset integrator analogue is a promising method in achieving this goal. By resetting the fractional states of the reset integrator to determined optimal values, it has been shown that there is a higher order harmonics reduction that may not seem huge in open-loop, however results in significant closed loop performance improvement. A recommendation was then made as to the reset values of the fractional states required for a particular tolerable phase lag. Furthermore, the non-zero higher order harmonics phase that the augmented fractional-order reset integrator analogue possess was shown to be promising in further improving the output of the reset integrator.

For future work, it is recommended to develop a tuning rule for the state space representation of the augmented fractional-order analogue such that the higher order harmonics phase can be manipulated to obtain the optimal reduction in the RMS difference discussed in Section III-E, while still maintaining reduced higher order harmonic gains. A final recommendation is to also investigate resetting the fractional elements with respect to their own respective inputs as opposed to the error; there may be aspects of the intermediate signals that could bring about more higher order harmonic reductions.

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