

Automatic Fault Extraction and Simulation of Layout Realistic Faults for Integrated Analogue Circuits

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Abstract - A comprehensive tool has been implemented for the comparison of different test preparation techniques and target faults. It comprises of the realistic fault characterisation program LIFT that can extract sets of various faults from a given analogue or mixed-signal circuit layout and the automatic analogue fault simulation program AnaFAULT which can handle arbitrary catastrophic and parametric faults. For a fabricated integrated VCO circuit the capabilities of the tool are demonstrated and simulation results are presented.

I. INTRODUCTION

Analogue and in particular mixed-signal testing has become key for high quality manufacturing. For an early and rapid development of appropriate and dependable tests a Computer-Aided Test (CAT) capability must be provided along with the CAD support. Such a CAT tool should feature components for fault simulation and for the generation of fault lists. Both are required to assess the performance of a chosen test as well as to judge a particular analogue Design-for-Testability (DFT) measure, or Built-In Self-Test like the HBIST approach [19]. This paper introduces an implemented CAT system which links the realistic fault characterisation tool LIFT [29] and the automatic analogue fault simulator AnaFAULT [24].

LIFT extracts faults from a given layout and generates a list of realistic and relevant faults. This list represents the interface to AnaFAULT, which can handle faults extracted by LIFT. By this link, the new tool allows a more comprehensive fault simulation. On the one hand the faults are more realistic resulting in a higher relevance of the results and on the other hand the overall time consumption for the fault simulation decreases significantly compared with the

assumption of the complete set of possible faults taken from the schematic.

After the introduction and the state-of-the-art, the application procedure of the universal CAT tool within the

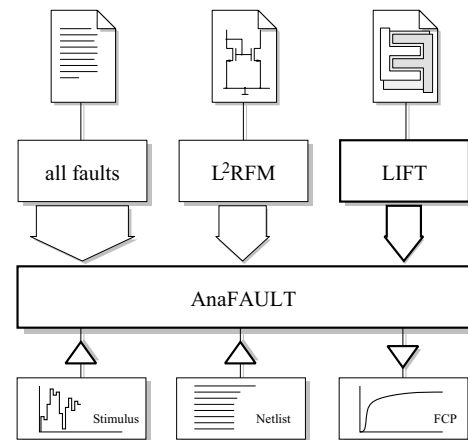


Fig. 1 Analogue fault simulation from concept and schematic to layout. The arrows width represents the size of the fault lists.

design process is described. Chapters IV and V are dealing with the tools LIFT and AnaFAULT, respectively. Some results for a CMOS VCO are presented in section VI.

II. STATE-OF-THE-ART

From reliability investigations a wide range of physical failures are known, e.g. reported in [1] [7] [8]. For the fault simulation, their electrical failure modes can be either represented by the catastrophic or 'hard' fault model or the parameter deviation or 'soft' fault model [5] [3]. The latter can be introduced by special commands [13] or by Monte Carlo analysis methods [2]. But, analogue circuit simulators lack the capability to alter the topology of a circuit in its textual or stored matrix representation required for the

hard fault modeling. Consequently this task has been tackled in previous work for the development of fault models [22], the fault recognition from AC and DC measurements [6] and for ISPICE's AC and DC fault simulation capabilities with different simulation models for hard faults [30] [31] [12]. In view of previous work and due to new requirements, AnaFAULT has been developed since 1988 [15] [14] [4] [11] [24]. Recently it was improved for parallel execution in a workstation cluster environment [21].

Faults to be simulated are read from a fault list. By default this list may initially comprise the complete set of possible single hard faults on each component of the circuit [20]. It can either be updated prior to the final layout using "*Local Layout Realistic Faults Mapping*", *L²RFM* [18] or, as described here, at the end of the design process by the "*Global Layout Realistic Faults Mapping*", *GLRFM* performed by LIFT (Fig. 1). The pioneering work for obtaining global realistic faults from the final circuit layout [25] is referred to as "*Inductive Fault Analysis*", *IFA*. Based on random spot defects introduced on the layout according to statistics, defects large enough to modify the circuit topology such that an electrical failure is caused, are identified and translated into realistic faults [16]. In contrast to the *L²RFM* technique, this analysis additionally takes into account global short conditions and single defects causing global multiple open faults. Recently, another methodology of realistic fault extraction was developed [27], based on concurrent circuit and fault extraction. Similar to [25], defect statistics analysis is used to evaluate the probability $P(f_j) = p_j$ of occurrence of each fault, f_j . This methodology, together with a set of tools, previously was used to investigate the testability of digital circuits by analysing the estimated testability of realistic faults according to the fault topology [23]. In this work, the fault extraction procedure is used to identify (and rank) the most likely realistic faults in analogue integrated circuits.

III. APPLICATION AND PROCEDURE

At the beginning of the design process the conception of the circuit is chosen. The compliance with the given specifications are verified by hand calculation and network simulations. But the development of appropriate tests is very time consuming and the test quality can neither be

assessed nor guaranteed without CAT support. Furthermore, self-tests for mixed-signal circuits require advanced methods to judge the performance. The CAT system described here supports the development of tests providing detailed reports, clearly arranged overview tables and comprehensive fault coverage plots. For hard faults, an initial fault list can be constructed from the schematic that comprises the complete set of possible hard faults irrespective whether or not the assumptions are realistic. A reduction of this initial list can be accomplished prior to the final layout employing *L²RFM* [18], or, after the final layout is available, by employing *GLRFM*. AnaFAULT performs an automatic fault simulation with the actual set of faults using a given stimulus that has to be checked and computes the required fault coverage. Depending on the result the stimulus can be refined. Currently the system does not generate the stimulus by itself, this will be a topic of future work.

IV. REALISTIC FAULT EXTRACTION TOOL LIFT

Realistic faults describe physical defects, induced during IC manufacturing [26]. Defect statistics are characterised by the defect densities, associated with the different failure

Layer(s)	Failure	Relative Density
Diffusion	open	$\alpha_d = 0.01$
	short	$\beta_d = 1.00$
Polysilicon	open	$\alpha_p = 0.25$
	short	$\beta_p = 1.25$
Metal_1	open	$\alpha_{m1} = 0.01$
	short	$\beta_{m1} = 1.0$
Metal_2	open	$\alpha_{m2} = 0.02$
	short	$\beta_{m2} = 1.50$
Al/diff.contacts	open	$\alpha_{cd} = 0.66$
m1/poly contacts	open	$\alpha_{cp} = 0.67$
vias	open	$\alpha_{cv} = 0.8$

Tab. 1 Likely physical failure modes in a digital CMOS process and typical failure densities

mechanisms, and, for each mechanism, by its probability density function of the defect size. Each process line and process step exhibits specific defect densities. For a positive photoresist-based lithography, bridging faults are dominant (typical for CMOS process lines). In Tab. 1, the assumed failure mechanisms and their relative defect

densities (normalised to the metal 1 short defect density) are shown. These values are also used for the example (section VI). A typical value for the metal 1 short density is 1 defect/cm² [9]. In most cases, the beta/alpha ratio is around 100, which justifies the importance given to bridging faults. The probability density function p_j , for each failure mechanism, describes the probability of occurrence of defects, as a function of their size [10]. Typically, a circle or square shape is assumed. As can be seen, the IC layout and linewidths and spacing between adjacent lines strongly influences the fault set, as well as the probability of occurrence of each fault. Geometrical design rules for each technology are determined in such a way that in the target process line acceptable yields are obtained.

In LIFT, each fault originates from a single failure. A file (default, or user defined), contains the assumed likely

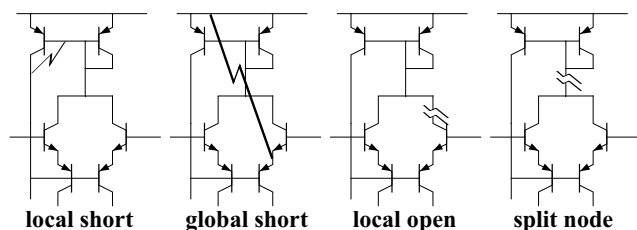


Fig. 2 Fault types supported

failure modes, and their likelihood of occurrence, is provided, for the p_j evaluations. The fault extraction procedure is carried out simultaneously with the transistor-level circuit extraction [29]. For each identified realistic failure, a critical area evaluation [28] is performed. The probability of each fault is computed as a function of the critical areas associated with a particular failure. Finally, by layout inspection and probability evaluation, the realistic fault set is extracted, characterised by faults $f_1, \dots, f_j, \dots, f_N$, each one associated with its probability of occurrence, $p_1, \dots, p_j, \dots, p_N$. In practice, p_j is in the order of 10^{-7} down to 10^{-9} . This weighted fault list is used to evaluate the effectiveness of the test previously derived using e.g. L²RFM.

V. AUTOMATIC FAULT SIMULATOR ANAFAULT

ANAFault is a complete tool that is flexible in terms of fault models, easy to use through a user interface and uses ELDO by Anacad as the kernel simulator [2]. The fault

injection algorithm has been proven to work with standard SPICE [17] netlists. Basically, the procedure is as follows: After the execution of the nominal simulation, the automatic analogue fault simulation is performed in a repetitive cycle of three main phases. Namely, the preprocessing of the original input file, the call of the kernel simulator and a post-processing phase that compares results and generates statistics. Results are presented in tabular form or in form of fault coverage plots displaying the progress of the fault coverage versus time or frequency simulated. The faults that may be introduced are shown in Fig. 2. Beside the local fault attributed to single elements, global faults like global shorts and split nodes are supported. The latter modes split nodes of order n into two new nodes of order $k < n$ and $n - k$. There is no restriction for the simulation models used as long as they can be described in the kernel simulators' language. The fault list obtained from LIFT is merged into the configuration file during the setup procedure.

VI. EXPERIMENTAL RESULTS

The tool has been used for the fault simulation of various circuits. In the following some results for a voltage controlled oscillator, VCO depicted in Fig. 3 will be presented. It comprises 26 transistors and has been fabricated in a single poly, double metal CMOS technology. From the schematic 78 possible single open faults can be assumed

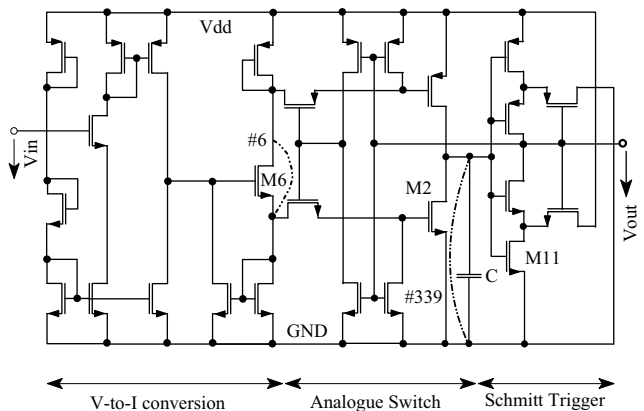


Fig. 3 Voltage controlled oscillator with some example faults

on the transistors and one open fault on the capacitor. The number of shorts is less than the number of opens, since on six transistors a gate-drain short configuration has been de-

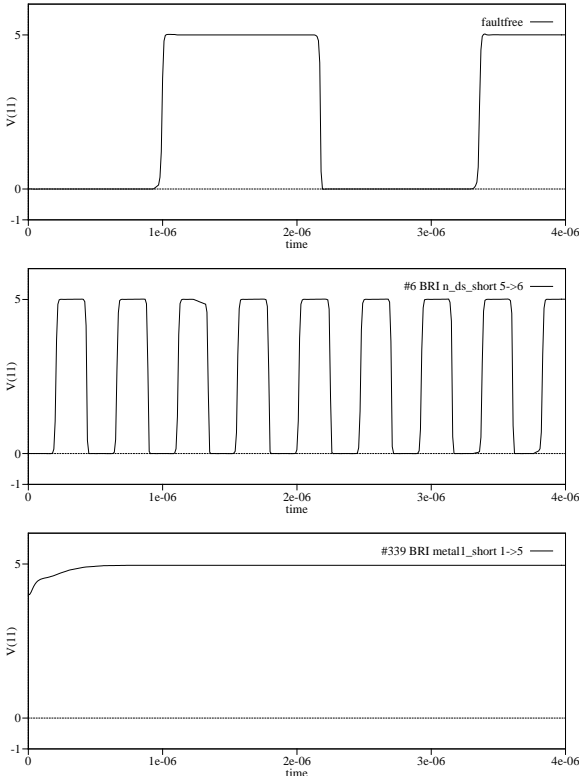


Fig. 4 Three examples for faults extracted by LIFT and simulated with AnaFAULT

signed. Thus, the number of shorts is 73, including the short on the capacitor. LIFT extracted 70 different failures: 55 bridging, 8 line opens and 7 transistor stuck open faults. Compared with the complete set of possible faults from the schematic this is a reduction in the number of faults by 53%. Note, that not only the number of faults decreased, but also the nature and impact on the circuit behaviour is quite different.

For the reduced fault set a 400 step transient fault simulation was performed by AnaFAULT. An explicit test stimulus was not required and the VCO control voltage was held constant. After the activation of the supply voltage the simulation started. Faults were either modeled by the source model or by the resistor model [19] [30] [31] (short: $.01\mu\Omega$, open: $100M\Omega$) yielding nearly identical fault coverage plots. Examples of output waveforms for different bridging faults are shown in Fig. 4. The top waveform depicts the fault-free oscillation. As can be seen there are short faults that change the frequency of oscillation (#6 BRI) whereas others cause a constant high or low output signal. Note, that at the first glance an increased oscillation

would be attributed to some kind of soft rather than to a hard fault. The fault coverage plot is depicted in Fig. 5. It shows, that all faults are detected after approximately 55% of the overall test time. After 25% of test time the fault coverage almost reaches 100%. The protocol files showed that the source model simulations required a simulation time 43% longer than the simulation time for the resistor model (4383 sec./3068 sec.). Note, that for each fault only one additional resistor is added [30]. The determination of appropriate resistor values required for the resistor model are subject of fault modeling by process monitoring and can become critical.

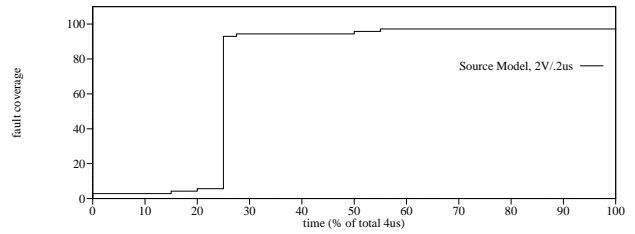


Fig. 5 Fault coverage plot by AnaFAULT using a tolerance of 2V for the amplitude and $0.2\mu s$ for the time

To demonstrate the effect of the choice of different resistor values, the value for the resistor bridging the drain of the Schmitt trigger transistor M11 to ground was ranged between $1k\Omega$ and $10^{-8}\Omega$. In Fig. 6 the results for the values 1, 21 and 41Ω of the shorting resistor R are shown. Set to $1k\Omega$ the waveform is only slightly affected (compared with the fault-free waveform in Fig. 4). Decreasing the value of R makes the impact more visible in the output waveform. After the value of R is set to 1Ω the oscillation stops after one cycle. This shows that the circuit itself strongly influences the optimal resistor value that has to be used to model a fault at the respective location.

From the simulations it further turned out, that the

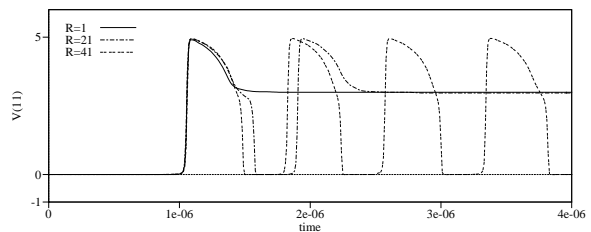


Fig. 6 Three different values for the resistor shorting M11

detection of particular faults is impacted by their locations.

Some faults are easily detectable whereas others are only visible under certain load conditions or depend on the frequency of the stimulus.

VII. SUMMARY

A comprehensive and demonstrable CAT environment has been introduced which comprises the automatic analog fault simulator AnaFAULT and the automatic fault extraction tool LIFT. Inductive fault analysis based on given defect statistics as well as simultaneous circuit and fault extraction are used by LIFT to map defects to electrical failure modes. These are converted to fault models and finally fault simulation models by AnaFAULT. The tool offers a variety of representations of the simulation results supporting the design and test engineer with valuable information for the development of tests, DFT measures and Built-In Self-Test.

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