Automatic Linearity and Frequency Response Tests With Built-in Pattern Generator and Analyzer

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***Abstract*—We present a built-in self-test (BIST) approach based on a direct digital synthesizer (DDS) for functionality testing of analog circuitry in mixed-signal systems. A main contribution of this paper is the BIST-based hardware implementation and measurement of amplifier linearity (IP3) and frequency response, including both phase and gain. The approach has been implemented in Verilog and synthesized into a field-programmable gate array (FPGA), where it was used for functional testing of an actual device under test (DUT) and compared to simulation results.**

***Index Terms*—Analog integrated circuits, built-in self-test (BIST), frequency response, inter-modulation, linearity, mixed-signal systems, VLSI testing.**

I. Introduction

Analog functionality testing in a high-speed radio-frequency integrated circuit (RFIC) is a time consuming and costly process based on the current methodology of manual-analog testing. It is becoming a substantial barrier to continued RFIC cost reductions because of the additional complexities required by new standards—including multiband compatibility, higher linearity, lower bit-error rate, and longer battery life. Typical test costs, as a percentage of the manufacturing cost, are commonly low for digital application-specific integrated circuits (ASICs). However, the RFIC test cost can be as high as 50% of the total cost, depending on the complexity of the functionality to be tested. The overall cost of an RF system consists of manufacturing, testing (wafer sort and final testing), and packaging. The dc wafer test for RFICs is mainly digital, using cheap testers to prune away defective devices. Typically, in this test flow, the RF circuitry is bypassed due to the high cost of RF testers. Unfortunately, RF functional faults cannot be tested until the chip is packaged, resulting in a significant loss since RFIC packaging can represent 30% of the overall cost. Current test practices are expensive because of, among other reasons, the required tester infrastructure, long test times, cumbersome test preparation, lack of appropriate defect and fault models, and lack of standardized tests.

It is, therefore, highly desirable to automate the analog testing process with low cost, built-in test circuitry. Analog test features built into the RF and baseband ASICs could provide not only analog test capability, but also an efficient technique for calibrating and compensating analog circuitry that is sensitive to temperature, supply voltage, and process variations. Built-in self-test (BIST) and design for testability (DFT) of analog circuits are important and necessary to produce highly reliable mixed-signal systems. Due to the constant increase of analog circuit speed and density, the nature of analog faults, and the embedding of analog functions within large digital systems, the detection and isolation of faults in these circuits is becoming more difficult. At the operating frequencies beyond a few GHz, analog IC testing requires tester electronics close to the device under test, or even better, directly built on-chip. Hence, BIST and other forms of embedded analog testing will come to market in just a matter of time [1].

A few techniques have been suggested to perform on-chip frequency-domain testing of mixed-signal circuits. These approaches normally focus on one or two simple parameter tests such as cutoff frequency of a filter and cannot perform rigorous and complete analog tests such as frequency response, linearity, noise, and modulation tests. The goal of prior art techniques was to overcome the complexity of integrating a traditional ac characterization approach [2]. Well-defined techniques for reducing the size of the test set while maintaining high fault coverage have been reported [3], [4]. Some ac BIST techniques inject optimized digital inputs into a linear device under test and extract a dc signature [5], [6]. These approaches are simple, but their precision is limited. On the other hand, Roberts [7] has proposed several methods to make frequency-domain tests using on-chip generated sine waves and analyzing the results with an on-chip digital signal processor (DSP). The approach requires 1-bit sigma-delta digital-to-analog converters (DACs) with moderate area overhead. The precision of the generated frequency is not fine enough to support some analog tests such as various analog modulation and linearity tests using precise two-tones. Several techniques have been published to generate on-chip linear ramps [8]–[11], but the results either depend largely on the accuracy of the additional components in the test circuitry, or have not been proven experimentally. An on-chip ramp generator can perform monotonicity and histogram tests of analog-to-digital converters (ADCs), yet the linearity of the on-chip ramp generator itself needs to be very high. An FFT approximation algorithm was developed for on-chip sinusoidal signals generation and analysis in [12]. The area and power penalties associated with the FFT calculations is large as indicated by the fact that the BIST approach was implemented in the largest Xilinx Virtex-II series FPGA [12].

Analog BIST can be categorized into two types: the analog functional test and the structural fault test. Test waveforms used in structural testing are derived from the circuit implementation

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rather than from the circuit specification. Given that the transistor count of analog circuits is not typically large, structural testing can benefit from inductive fault analysis techniques. In this way, the test waveform is targeted to a set of realistic faults. Additionally, it is possible to derive figures of merit, such as defect and fault coverage, to measure the test pattern effectiveness.

Structural testing focuses on the development of dc and transient testing of analog circuits. In transient testing, the circuit under test (CUT) is excited with a transient test stimulus and the circuit response is sampled at specified times to detect the presence of a fault. The transient waveform can be formed from piecewise linear segments that excite the circuit in such a way that the sensitivity of the fault(s) to the specific stimulus is magnified. These waveforms can have a periodic shape, arbitrary shapes, or as recently proposed, a binary shape with distinct duty cycles. It is also possible to structurally test the circuit by testing its dc conditions, e.g., by inspecting quiescent currents.

An analog functional test is a challenging task even in a manual test by an experienced engineer. It tests the functionality of the circuit against the system specifications. The complexity of the functional test depends on test tasks and the operational frequency. For instance, a baseband amplifier test normally includes its linearity, frequency response, in-band ripple, and 3-dB cutoff frequency. For an RF low-noise amplifier (LNA) test, we need to characterize its noise figure (NF), linearity through the third-order intercept point (IP3), frequency response including phase and gain, and return loss related to the input matching.

In this paper, we present a direct digital synthesizer (DDS)-based BIST approach, which can generate a variety of modulated waveforms and frequency tones for analog functional tests. For baseband digital test features such as the test pattern generator (TPG) and output response analyzer (ORA), we initially designed and synthesized the functionality in field-programmable gate-array (FPGA) technology with the intent to eventually fabricate the design in a CMOS ASIC. We have been investigating and analyzing this DDS-based BIST approach for its ability to detect faults and to assist in characterization and calibration during manufacturing and field testing. A potential problem identified with the BIST approach is that the ORA suffers from phase delays which distort the gain measurement in the frequency response test. This is also a concern during the linearity test near the cutoff frequency. However, we will show that a simple measurement made with the existing hardware of the BIST approach can determine the actual phase delay. This allows us to not only measure the phase delay of a circuit, but also to correct the measured gain and linearity. The proposed BIST scheme, using the existing ADC/DAC, will automatically meet the system dynamic range requirement which fully demonstrates the fidelity of the proposed BIST approach for analog linearity and frequency response tests.

In Section II, we present the DDS-based test pattern generator. In Section III, we will discuss the concept of the proposed approach for testing the analog functionalities in a wireless transceiver. In Sections IV and V, we discuss the application of the proposed BIST approach to frequency response and the linearity tests, respectively. In Section VI, the measured data for analog frequency response and linearity tests will be presented. Finally, the conclusions will be given in Section VII.

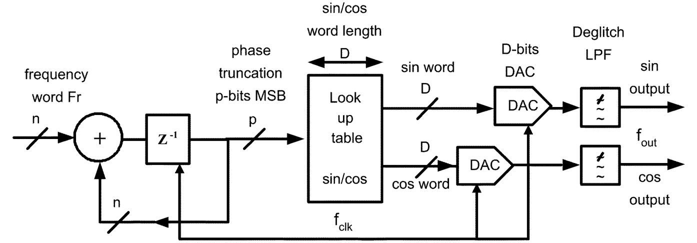

Fig. 1. DDS for test-signal generation.

II. Test Pattern Generator Using DDS

DDS is an important frequency synthesis technique that provides low-cost synthesis with ultra-fine resolution. As shown in Fig. 1, a conventional DDS includes a digital accumulator that generates the phase word based on the input frequency word Fr, where Fr determines the output frequency as $f_{\text{out}} = (Fr/2^n) \cdot f_{\text{clk}}$. The synthesizer step size is defined as $f_{\text{clk}}/2^n$, where n is the number of bits in the accumulator. Fine resolution can thus be achieved using a large accumulator size. The DDS utilizes a lookup table to convert the phase word to a sinusoidal amplitude word, whose length is normally limited by the finite number of input bits of the DAC. Deglitch filters are added after the DAC to remove the spurious components generated in the data conversion process. While a pure sinusoidal waveform is desired at the DDS output, spurious tones can occur mainly due to the following two nonlinear processes. First, in order to reduce the lookup table ROM size, the phase word needs to be truncated before being used as the ROM addresses. This truncation process introduces quantization noise, which can be modeled as a linear additive noise to the phase of the sinusoidal wave. Second, the ROM word length is normally limited by the finite number of bits of the available DAC. In other words, the sinusoidal waveform can be expressed only by words with finite length, which intrinsically contains quantization error additive to the output amplitude. Considering the quantization errors due to phase truncation e_p, and finite amplitude resolution e_A, and assuming the phase quantization error is small relative to the phase, the DDS output can be determined as

$$\begin{aligned} A_{\text{out}} &= A\sin\left(\frac{2\pi Wi}{2^n} + e_p(i)\right) + e_A(i) \\ &\approx A\sin\left(\frac{2\pi Wi}{2^n}\right) + Ae_p(i)\cos\left(\frac{2\pi Wi}{2^n}\right) + Ae_A(i). \end{aligned} \tag{1}$$

Analog functional testing requires fine-frequency resolution and fast-frequency switching time to perform tests such as frequency response and linearity measurements. The resolution and switching speed requirements of an analog BIST system surpass the performance capabilities of conventional analog phase-locked loops (PLLs). The conventional PLL-based frequency synthesizer has difficulty meeting these requirements due to internal loop delay, low resolution, and limited tuning range of the voltage-controlled oscillator (VCO). In contrast, a DDS generates a digitized waveform of a given frequency by accumulating phase changes at a higher clock frequency. DDS is a digital technique for frequency synthesis, waveform

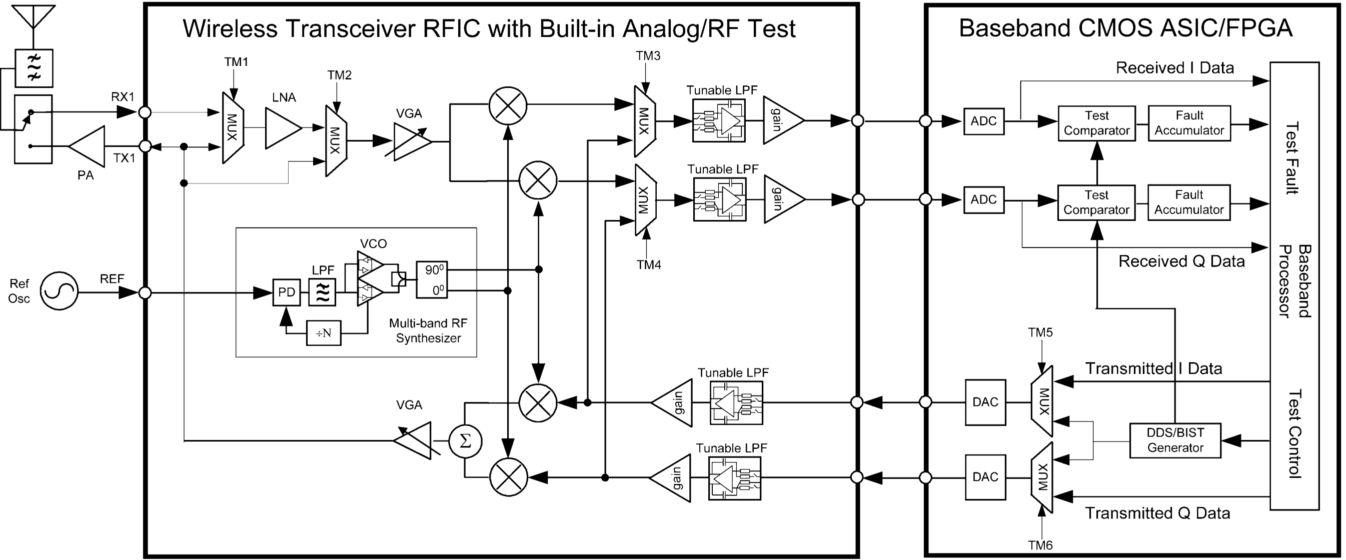

Fig. 2. Wireless transceiver architecture with analog and RF built-in test generator and analyzer.

generation, sensor excitation, and digital modulation/demodulation. Since there is no feedback in a DDS structure, it is capable of extremely fast frequency switching or hopping at the speed of the clock frequency. DDS provides many other advantages including fine frequency-tuning resolution, continuous-phase switching, and various modulations. Thus, it provides a low-cost digital approach to frequency, phase, and amplitude modulations, eliminating costly analog modulators associated with many analog measurements. The modulated waveform generation is a unique feature of the DDS-based BIST approach. None of the prior art analog testing schemes [1]–[12] can perform such complete waveform generation as that of the DDS synthesizer and modulator.

On the other hand, the DDS has two major deficiencies that are related to the inadequacy of the semiconductor technology. The first deficiency is that the output spectrum of the DDS is normally not as clean as the PLL output. The DDS quantization noise floor is limited by the finite number of amplitude bits (DAC input bits) and the finite number of phase bits. A 12-bit DAC provides a theoretical noise floor of -72 dBc, which is less than that of a PLL synthesizer. The DDS also suffers from a high level of spurious output, derived from the discrete phase accumulation and phase truncation processes, as well as the DAC nonlinearity. The second deficiency is that the DDS output frequency is limited by the maximum operation frequency of the DAC and the digital logic. Although DACs with gigahertz sampling frequencies have been reported, they normally consume a large amount of power with poor resolution. Therefore, we propose to use the DDS to generate the fine-tuned frequency and use an RF mixer and PLL to up-convert the DDS output to the RF frequency. With careful design, the best of both DDS and PLL can be achieved in the proposed RF BIST approach [13].

The DDS-based TPG can provide precise frequency tones for many analog tests such as IP3 measurement. The area penalty associated with a conventional DDS approach can be minimized using a delta-sigma noise shaping scheme [14]. While measurement of IP3 is straightforward with a spectrum analyzer, another challenge is the development of an efficient ORA that can make the IP3 measurement on-chip and, with the DDS-based TPG, create a BIST architecture. Such a BIST approach can then be modeled in parameterized hardware description languages such as VHDL or Verilog for easy incorporation in any mixed-signal design. Therefore, the development of the ORA is another important focus of this paper.

III. Transceiver Functionality Tests Using DDS

The approach can also be applied to RF circuit testing as illustrated in Fig. 2 for a wireless transceiver RFIC with automatic analog self-test features. The vast majority of the BIST circuitry resides in the digital portion of the mixed-signal system to minimize area and performance impact on the analog circuitry. The only test circuitry added to the analog domain is the analog multiplexers needed to facilitate a return path for the test signals to the ORA portion of the BIST circuitry. The test scheme utilizes the existing DACs and ADCs associated with conventional transceiver baseband architectures and, thus, provides accurate analog testing without adding much extra hardware.

The DDS-based testing approach can provide precise frequency tones for many analog tests, such as frequency response and IP3 measurements. To test the baseband low-pass filter (LPF) in the transceiver RFIC shown in Fig. 2, the DDS integrated in the baseband ASIC, generates a single frequency tone that loops back from transmitter to receiver through multiplexers control by TM3 and TM4 for the I and Q channels, respectively. The frequency response of the baseband gain stage amplifiers can be tested in the same way as the baseband LPF frequency response. Basically, the DDS generates frequency tones and scans the pass and stop bands of the amplifier. Note that the baseband LPFs and gain stages in the receiver and transmitter paths are normally identical designs in a transceiver RFIC. In order to save area, the baseband LPFs and gain stages are sometimes shared by the receiver and the transmitter for half-duplex operation. The baseband gain stage can also be included in the LPF, as long as the LPF can provide enough gain in the passband. In Fig. 2, we did not show additional switches to test the individual baseband blocks. However, switches can

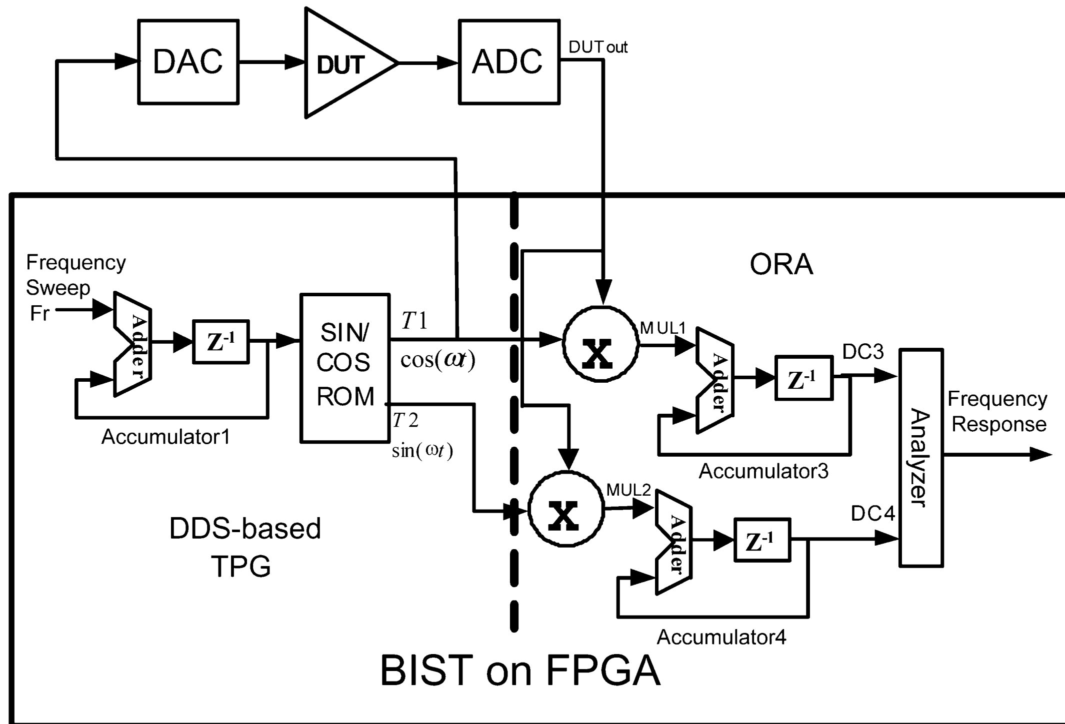

Fig. 3. Frequency-response BIST measurement.

be easily added to test the individual baseband blocks based on the chosen transceiver architectures.

In the ORA, switches TM5 and TM6 are used to select either the transmitted *I/Q* data for normal operation or the test tones generated by the DDS in the BIST mode. The controls to switch the multiplexers in the proposed BIST scheme are generated by the baseband processor based on the operation mode of the transceiver and the type of the tests to be performed.

An RF amplifier such as an low noise amplifier (LNA) or an RF variable-gain amplifier (VGA) can be tested in a similar way as that of a baseband amplifier with the assistance of existing mixers in the RF transceiver. To test the amplifiers at the RF frequency (2–5 GHz), the up-converter and down-converter have to be employed. Again, we use DDS to generate the test tones, namely, scanning tones to test the amplifier frequency response and two-tones to test the amplifier linearity. Those baseband frequency tones can be up-converted to RF frequency by mixing them with the RF-carrier frequency generated by the RF synthesizer. The RF amplifier output is down-converted to baseband by mixing it with the RF carrier frequency generated by the RF synthesizer. The up- and down-converters are image-rejection mixers and, thus, no image tones can be collected. The up-down-converters and RF synthesizers are the building blocks of every RF transceiver and, thus, no extra hardware except a few multiplexers is needed to perform automatic analog testing and calibration of RF amplifiers.

To test the VGA, the RF test tones are looped back to VGA input by selecting the multiplexer controls TM2. To test the LNA, the test signal is fed to the LNA input by selecting the controls TM1. To remove the impact of VGA on LNA test, the VGA should also be tested separately with the same input signals and its output response will be subtracted from the LNA test response.

IV. Frequency Response Test Using DDS

One of the major problems associated with integrated-analog filters is the cutoff frequency variation due to temperature, supply voltage, and process variations. If the cutoff frequency can be monitored on the fly during transmission idle periods (e.g., the preamble period in WLAN applications), its variation can be compensated using built-in tunable circuitry in LPF designs. In addition to production test, the frequency response monitoring can also be used to adjust the gain and bandwidth of the amplifier for multiband and multistandard applications. With wireless standards operating in very different frequency bands, market-leading wireless solutions have to offer multimode interoperability with transparent worldwide usage. Thus, the baseband gain stage needs to be tunable for different wireless standards. The BIST approach can be used to calibrate the frequency response of the baseband-gain stage and LPF in this connection.

The complete TPG and ORA in BIST for the analog frequency response measurement architecture are illustrated in Fig. 3. The DDS-based TPG provides precise frequency tones sweep by controlling the frequency word Fr. It also can generate four quadrant sine waveforms simultaneously by shifting the two MSBs of the phase word. The area penalty associated with the DDS approach is minimized by the delta-sigma noise-shaping scheme [14].

The ORA consists of a D-bit multiplier (where D is the number of bits from the ADC) and a $2D + M$-bit accumulator (where the number of samples to be accumulated is less than 2^M). A 2's complement transformation is performed on negative numbers entering Accumulator3 and Accumulator4, such that subtraction is accomplished by the adders in the accumulators. In addition, the DDS input to the two multipliers

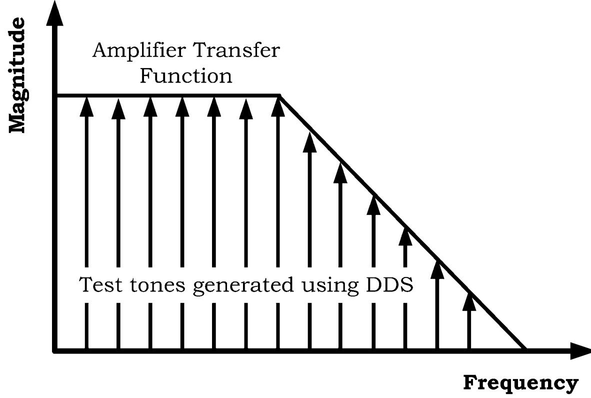

Fig. 4. Frequency response test using DDS.

is converted to a signed magnitude number to remove dc offset from the DDS output. The sign bit is used to control the 2's complement transformation at the accumulator inputs.

Frequency response (both gain and phase response) is the key measure for integrated LPFs and amplifiers. The commonly interested cutoff frequency of the filters and amplifiers can be found by measuring the passband and stopband amplitude response, while the linearity (group delay) can be determined from the phase response. To test the baseband LPF in the transceiver RFIC, the DDS integrated in the baseband ASIC generates a single-frequency tone that loops back from transmitter to receiver through multiplexer controls. The DDS generates frequency tones with fine resolution and can scan the pass and stop bands of the LPF with fine step size to measure the cutoff frequency and passband and stopband ripples of the filter, as illustrated in Fig. 4. However, since there is normally a phase difference between the external path through the DUT (amplifier) and the internal path from the test generator to the test analyzer, phase correction needs to be done prior to the frequency magnitude measurement.

To measure the frequency response, the DDS generates the test tone of $x(t) = A\cos\omega t$ that is applied to the input of an amplifier with transfer function $y(t) = \left[\alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots\right]\exp(j\Delta\phi)$, where coefficients α_j are time invariant. Hence, the amplifier output is given by

$$\begin{aligned} y(t) &= \exp(j\Delta\phi)\Big(\alpha_0 + \alpha_1 A\cos\omega t + \alpha_2 A^2\cos^2\omega t \\ &\qquad + \alpha_3 A^3\cos^3\omega t + \cdots\Big) \\ &= \exp(j\Delta\phi)\left\{\alpha_0 + \frac{\alpha_2 A^2}{2} + (\alpha_1 A + \frac{3\alpha_3 A^3}{4})\cos\omega t\right. \\ &\qquad \left. + \frac{\alpha_2 A^2}{2}\cos 2\omega t + \frac{\alpha_3 A^3}{4}\cos 3\omega t\right\}. \end{aligned} \tag{2}$$

Note that if the input signal A is large, the nth harmonic approximately grows in proportion to A^n. Under small-signal assumption, i.e., the input signal A is small, the system is linear and the harmonics are negligible and the small-signal gain is α_1. For large signal, nonlinearity becomes evident and the large-signal gain is $\alpha_1 + (3/4)\left(\alpha_3 A^3\right)$, which varies when input level

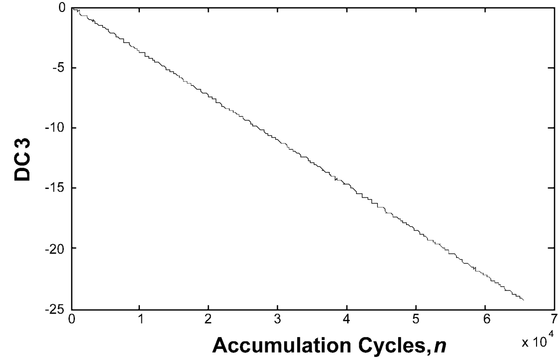

Fig. 5. Accumulated DC_3 component of DUT output mixed with $A\cos(\omega t)$, phase difference $\Delta\phi = 135°$.

changes. If $\alpha_3 < 0$, the output is a "compressive" or "saturating" function of the input signal, namely, the gain is compressed when input magnitude A increases. For small input, the linear transfer function of the DUT is

$$y(t) \approx \exp(j\Delta\phi)(\alpha_0 + \alpha_1 A\cos\omega t). \tag{3}$$

In the ORA, we mix the amplifier output with the test frequency. Since there is normally a phase difference between the external path through the DUT (amplifier) and the internal path from the TPG to the ORA, we assume the test tone to be mixed with DUT output is of the form of $A\cos(\omega t)$. Accumulating the mixer output, we can obtain a dc term given as follows:

$$DC_3 \approx \frac{1}{2}\alpha_1 A^2 \cos\Delta\phi \cdot n \tag{4}$$

where n is the number of accumulation clock cycles and $\Delta\phi$ denotes the phase difference. Next, we mix (multiply) the amplifier output with a test tone of $A\sin(\omega t)$. This mixing process produces another dc term

$$DC_4 \approx \frac{1}{2}\alpha_1 A^2 \sin\Delta\phi \cdot n. \tag{5}$$

Thus, the phase retardation $\Delta\phi$ can be determined by

$$\Delta\phi = tg^{-1}\frac{DC_4}{DC_3}. \tag{6}$$

Once the phase difference is measured, the test tone for the frequency response generated by DDS can be phase adjusted, such that the signals at the mixer inputs can be perfectly in-phase. In this connection, DDS should generate test tones in form of $x(t) = A\cos(\omega t - \Delta\phi)$ for DUT and $A\cos(\omega t)$ for the mixer input in the ORA, respectively. An additional phase can be easily added to the phase word in the DDS architecture as shown in Fig. 1. Since the amplifier may not have a constant group delay, namely, the delay through the DUT is normally frequency dependent, the phase correction should be performed at each frequency step when DDS scan generates the test tones that scan the interested band.

Fig. 5 shows the ORA accumulated DC_3 component of the DUT output mixed with $A\cos(\omega t)$ with phase difference $\Delta\phi = 135°$. Fig. 6 gives the ORA accumulated DC_4 component of the DUT output mixed with $A\sin(\omega t)$ with phase difference $\Delta\phi = 135°$. Notice the slope of DC_3 is negative due to the $\cos\Delta\phi$ term in (4), while the slope of DC_4 is positive due to the

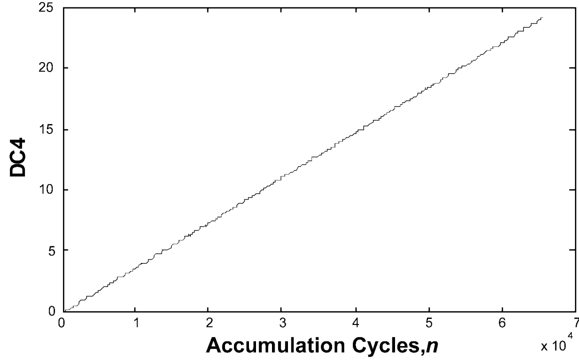

Fig. 6. Accumulated DC_4 component of DUT output mixed with $A\sin(\omega t)$, phase difference $\Delta\phi = 135°$.

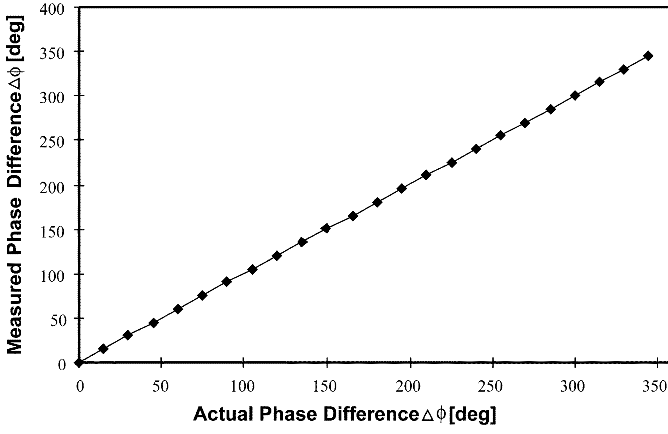

Fig. 7. BIST measured phase difference versus the actual $\Delta\phi$.

$\sin\Delta\phi$ term in (5). Based on the sign of DC_3 and DC_4, we can thus determine the quadrant of the phase difference. Once the phase difference is determined, the actual phase corrected frequency response can be found from either of the DC_3 or DC_4 measurements as

$$DC = \frac{DC_3}{\cos\Delta\phi} = \frac{DC_4}{\sin\Delta\phi}. \tag{7}$$

For better accuracy, it is preferred to use the dc term with the larger slope. For certain phase differences such as the angles close to 0° or 90°, one of the dc terms can approach zero. In those cases, the relative phase difference $\Delta\phi$ can be adjusted by programming the desired phase delay in DDS as shown in [1].

Fig. 7 compares measured phase difference versus the actual $\Delta\phi$ by programming a propagation delay line. As shown, the proposed phase detection scheme truthfully measures the phase difference, which ensures the accuracy of the proposed BIST scheme for linearity and frequency response measurements. Furthermore, this reduces the complexity of the frequency response measurement when compared to [15] where a phase detector was incorporated in conjunction with adjustment of the phase of the tones produced by the DDS.

For on-chip test, we do not have to set up an arctan table to get the exact phase delay from DC_3 and DC_4. As discussed before, the quadrant of $\Delta\phi$ can be determined easily from the sign bits of the accumulated DC_3 and DC_4 digital words. For $(DC_4/DC_3) \ll 1$, $\Delta\phi = \tan^{-1}(DC_4/DC_3) = (DC_4/DC_3) - (1/3)(DC_4/DC_3)^3 + \cdots \approx (DC_4/DC_3)$. For $(DC_4/DC_3) \gg 1$, the phase delay can be approximated by $\Delta\phi \approx (\pi/2) - (DC_4/DC_3)$. For $(DC_4/DC_3) \approx 1$, $\Delta\phi \approx (\pi/4)$. Therefore, one can always find an approximated phase delay $\Delta\phi_0$ regardless where $\Delta\phi_0$ is located in the first quadrant. With the initial phase estimation, the phase in the TPG can be adjusted by sending $x(t) = A\cos(\omega t - \Delta\phi_0)$ as the new test tone. After the initial phase adjustment in TPG, the newly measured phase delay will be a small value such that the ratio of DC_4/DC_3 can represent the $\arctan(DC_4/DC_3)$ fairly accurately.

V. Linearity (IP3) Test Using DDS

Linearity is an important measure of any amplifier performance. Amplifier linearity is normally measured by the third-order inter-modulation product (IP3) using a two-tone test. As will be shown, DDS can be used to generate two frequency tones required in the two-tone test. When the two-tone test signal passes through an amplifier, both fundamental and third-order inter-modulation (IM3) terms will be present at the amplifier output as shown in Fig. 8. The input referred IP3 (IIP3) can thus be found by

$$IIP_3[\text{dBm}] = \left(\frac{\Delta P[\text{dB}]}{2}\right) + P_{\text{in}}[\text{dBm}] \tag{8}$$

where ΔP is the difference between fundamental and IM3 terms, and P_{in} is the signal power at the amplifier input. To measure the IIP3 based on (8), a fast Fourier transform (FFT) would be required to capture the amplifier output spectrum.

IP3 measurement using FFT requires a large amount of hardware and is undesirable for an efficient BIST implementation. As an alternative, we use a multiplier as the down converter to selectively pick the frequency components and down-convert them into a dc signal. The dc level can be further compacted for evaluation by using an accumulator. The following derivation provides a mathematical proof-of-concept for the proposed IP3 testing technique.

Assume two tones $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$ are applied to the input of an amplifier with transfer function expressed as $y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \cdots$, where α_j are, in general, independent of time if the system is time invariant. Inserting the two-tone input into the transfer function, we obtain the amplifier output as

$$\begin{aligned} y(t) =& \frac{1}{2}\alpha_2\left(A_1^2 + A_2^2\right) + \left[\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1\left(A_1^2 + 2A_2^2\right)\right]\cos\omega_1 t \\ &+ \left[\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2\left(2A_1^2 + A_2^2\right)\right]\cos\omega_2 t \\ &+ \frac{1}{2}\alpha_2\left[A_1^2\cos 2\omega_1 t + A_2^2\cos 2\omega_2 t\right] \\ &+ \alpha_2 A_1 A_2\left[\cos(\omega_1+\omega_2)t + \cos(\omega_1-\omega_2)t\right] \\ &+ \frac{1}{4}\alpha_3\left[A_1^3\cos 3\omega_1 t + A_2^3\cos 3\omega_2 t\right] + \frac{3}{4}\alpha_3 \cdot \\ &\times \left\{ A_1^2 A_2\left[\cos(2\omega_1+\omega_2)t + \cos(2\omega_1-\omega_2)t\right] \right. \\ &\left. + A_1 A_2^2\left[\cos(2\omega_2+\omega_1)t + \cos(2\omega_2-\omega_1)t\right] \right\}. \end{aligned} \tag{9}$$

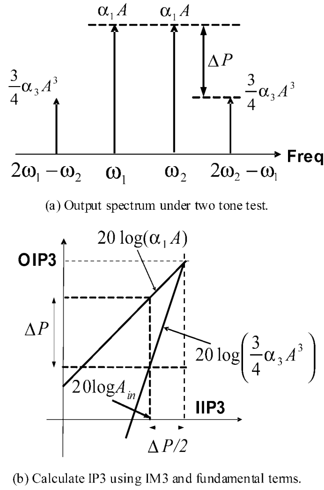

Fig. 8. Linearity (IP3) test using two tones generated by DDS.

According to (9), the input referred IP3 (IIP3) and the output referred IP3 (OIP3) can be found as

$$IIP_3 \approx \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}, \qquad \text{if } \alpha_1 \gg \frac{9}{4}\alpha_3 A^2$$
$$OIP_3 = \alpha_1 IIP_3 \tag{10}$$

where the assumption for IIP3 is normally valid when the test-tone magnitude is relatively small such that the amplifier is not desensitized.

In our BIST approach, we use the following technique for the ORA. As can be seen from Fig. 8, the closest inter-modulation terms to the fundamental are the IM3 terms with frequencies at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. First, mixing (multiplying) the amplifier output (9), with fundamental tone $A_2 \cos \omega_2 t$, produces a dc term

$$DC_1 = \frac{1}{2}A_2^2\left[\alpha_1 + \frac{3}{4}\alpha_3\left(2A_1^2 + A_2^2\right)\right] \approx \frac{1}{2}A_2^2\alpha_1 \tag{11}$$

where the second term in (11) is normally much smaller than the linear gain, α_1, if the input level is small, such that the amplifier is not desensitized. Second, mixing (multiplying) the amplifier output, (9), with the IM3 tone $A_1 \cos(2\omega_2 - \omega_1)t$, produces another dc term

$$DC_2 = \frac{3}{8}A_1^2 A_2^2 \alpha_3. \tag{12}$$

Expressing these two dc terms in dB, we can find the difference ΔP between fundamental, and the IM3 and the IIP3 can thus be measured using (8). Although we can represent dB units using floating-point format, we do not need to find the actual IP3 value using real hardware in an ORA for a BIST implementation. We may precalculate the linear gain requirement to evaluate DC_1 and the IM3 requirement to evaluate DC_2. Then accumulating these values as they exit the multiplier and averaging based on the number of samples, the results can be compared to predetermined ranges of acceptable values for a pass-fail BIST indication. For characterization of the circuit, the accumulated values can be read and averaged off-chip to perform the IP3 calculation. The complete TPG and ORA for the linearity-BIST architecture are illustrated in Fig. 9. It should be noted that the BIST circuitry for frequency response from Fig. 3, is a subset of that required for linearity.

VI. Experimental Results

A. BIST Results of Frequency Response Test

We implemented the BIST approach in hardware to obtain frequency-response measurements of analog circuitry. A first-order low-pass filter was built to be the DUT. An 8-bit DAC with a low-pass filter and an 8-bit ADC, were implemented on a separate printed circuit board with a separate power supply. The digital BIST circuitry was implemented in a Xilinx Spartan XC2S50 FPGA on a Xess XSA50–printed circuit board. Fig. 10 shows the measured DC_3, DC_4 output using BIST at a test input frequency of 48.8 kHz. The measured phase delay by BIST is 79° which matches well with the actual read from oscilloscope. Figs. 11 and 12 show the BIST-measured frequency response of the filter (phase and amplitude, respectively) after running the whole frequency sweep test compared to the actual measurements from the lab using oscilloscope.

B. BIST Results of Linearity Test

Using MATLAB and Verilog, we simulated the BIST scheme for different values of the amplifier third-order coefficient α_3. We used test tones with a small magnitude, such that the amplifier is not desensitized. As an example, the simulated values of the DC_1 accumulator, DC_2 accumulator, and resultant ΔP as a function of the number of clock cycles used to sample the signals, are shown in Figs. 13–15, respectively, for a simulated amplifier with a 20-dB ΔP. As can be seen, the BIST scheme achieves accurate IIP3 measurements without using any FFT algorithm for spectrum analysis. While an FFT scheme tries to calculate the whole spectrum information with a limited number of points, the multiplier-accumulator-based ORA focuses only on the useful spectral information at the two frequencies ω_2 and $2\omega_2 - \omega_1$ under the two-tone test, which is more efficient in terms of area than an FFT implementation.

It is important that the BIST sequence be controlled to run for integer multiple of periods of the lowest-frequency tone $\omega_2 - \omega_1$, since it is the closest tone to dc. The contribution from other tones at a higher frequency is relatively small and can be ignored when a large number of samples is accumulated. The ripples shown in Figs. 13–15, are of the frequency of $\omega_2 - \omega_1$. If we stop the accumulation at an integral multiple of the period of $\omega_2 - \omega_1$, convergent dc values for DC_1, DC_2, and ΔP can be extracted at the ORA output. Due to the symmetry of sinusoidal waves, other frequency tones cancel out after accumulation through integral multiple periods. The error occurs when we stop the accumulation at non-integer multiple of the periods. However, the error is accumulated only for less than one period. Thus, longer accumulation will reduce the impact of residual errors. The need to use a large number of samples for accumulation is apparent in Fig. 15, where the ΔP value becomes more accurate with a larger number of samples. As a result, we can tradeoff accuracy of the measured ΔP value with the BIST area overhead. Thus, the ORA technique provides an efficient means for analog linearity BIST. The BIST scheme can also be used to

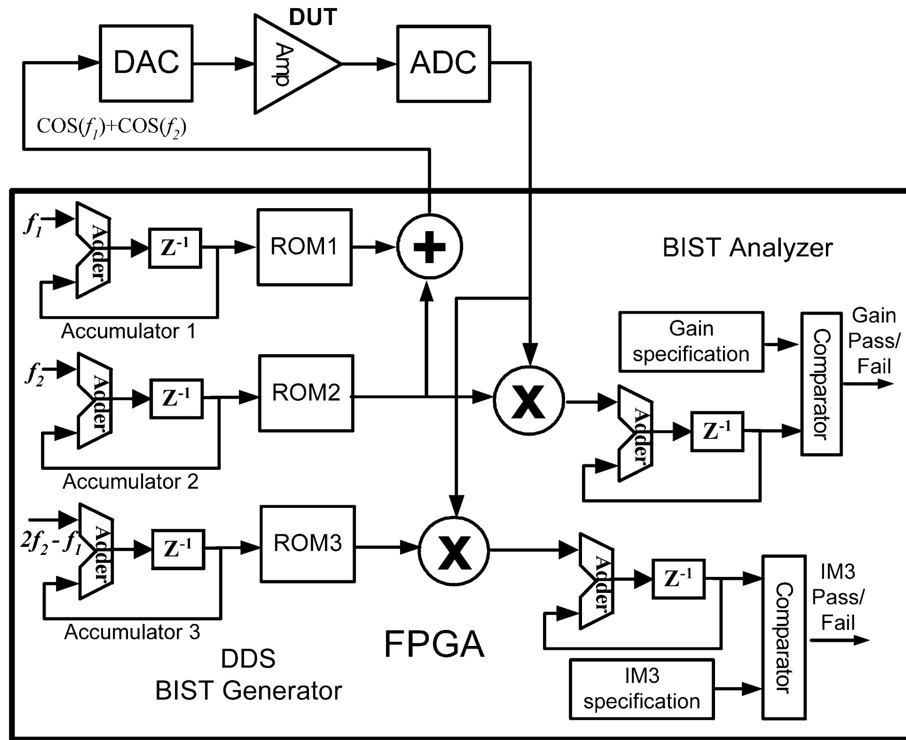

Fig. 9. Linearity-BIST generator and analyzer configuration.

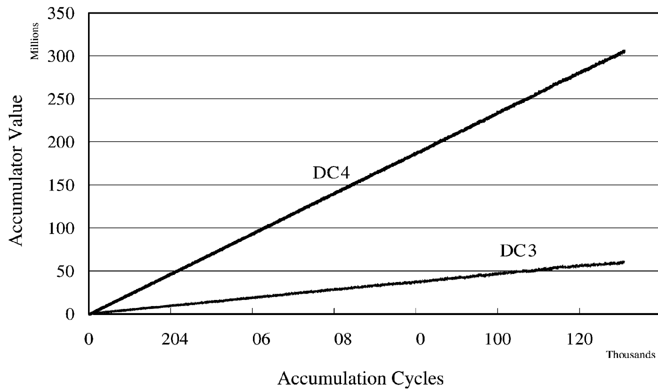

Fig. 10. Actual BIST circuit accumulated DC_3 and DC_4 for a phase delay $\Delta\phi \approx 79°$.

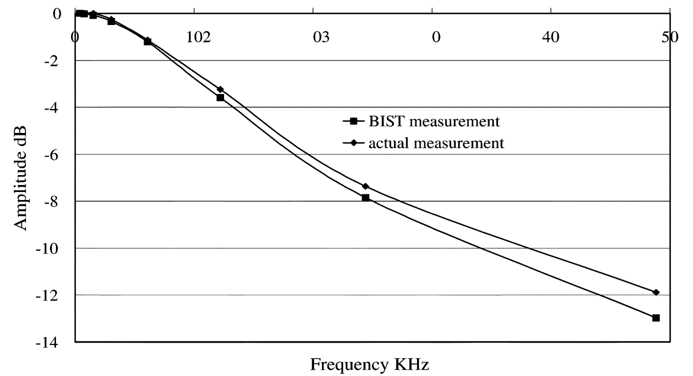

Fig. 12. BIST-measured amplitude response compared to an actual measurement of a first-order low-pass filter.

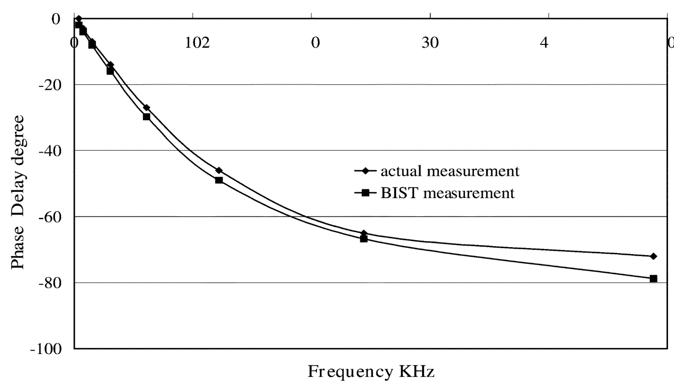

Fig. 11. BIST measured phase response compared to actual measurement of a first-order low-pass filter.

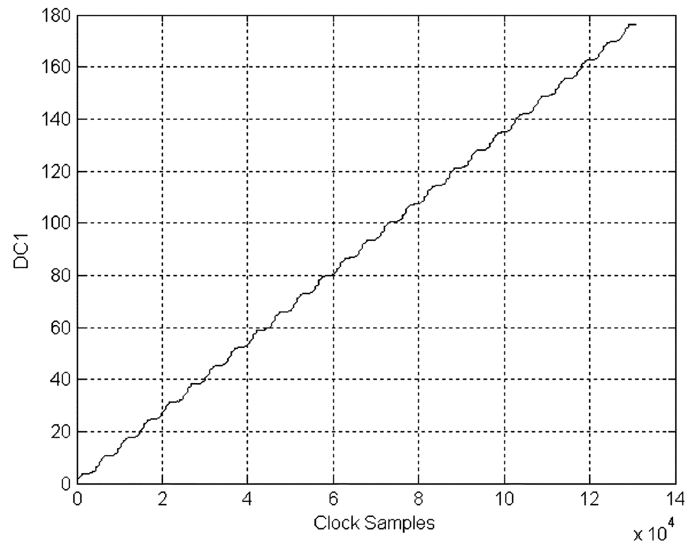

Fig. 13. DC_1 accumulator value versus clock samples.

monitor the linearity variations of analog modules, which is critical for designing automatic linearity compensation circuitry.

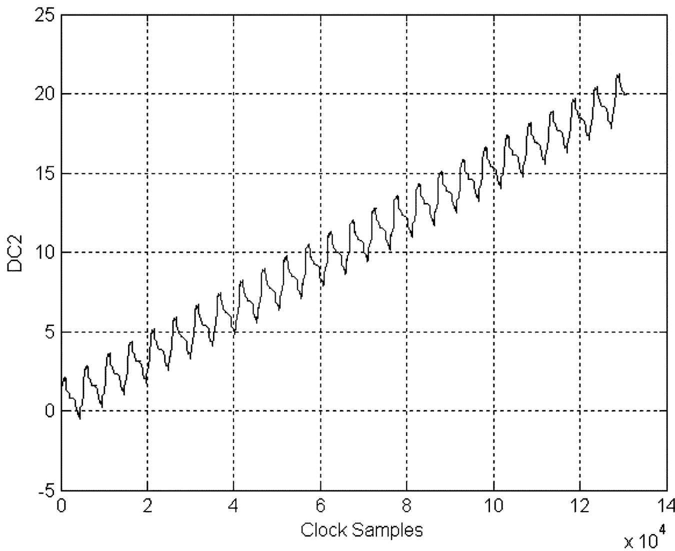

Fig. 14. DC_2 accumulator value versus clock samples.

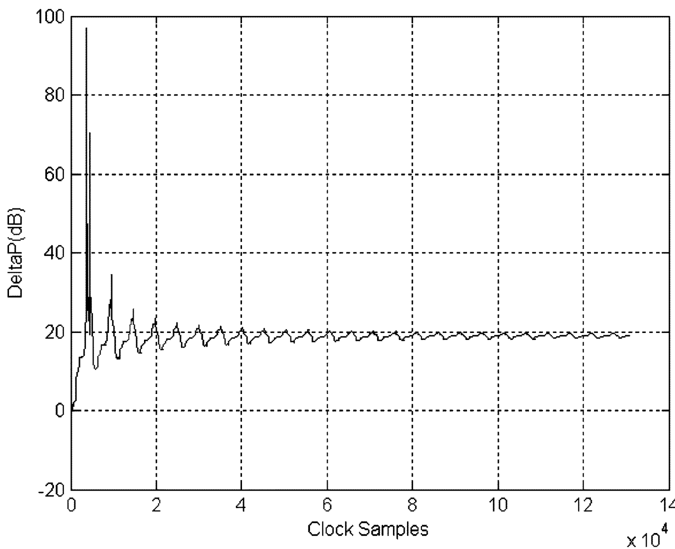

Fig. 15. ΔP value versus clock samples.

We use the DDS-based BIST approach in hardware to obtain measurements for comparison with our simulations. A field-programmable analog array (FPAA) was configured as a linear amplifier and used as the DUT for our IP3 linearity-test configuration. The FPAA amplifier operates around 500 kHz and nonlinearity was introduced into the amplifier by lowering its power supply voltage from 5 V to about 4 V. The remainder of the hardware was the same as that used for the frequency-response measurements described above. The spectrum analyzer measurement of the two-tone test at the output of the amplifier is given in Fig. 16, where ΔP is measured to be 17 dB. The ΔP, measured by our BIST hardware, is given in Fig. 17 as a function of the number of clock cycles used to sample DC_1 and DC_2. As shown, the BIST circuitry measurement also gives a ΔP of 17 dB, which agrees well with the spectrum analyzer measurement. It should be noted that the actual BIST measurement results illustrated in Fig. 17, are more accurate than those originally reported in [16]. This is a result of the redesign of our

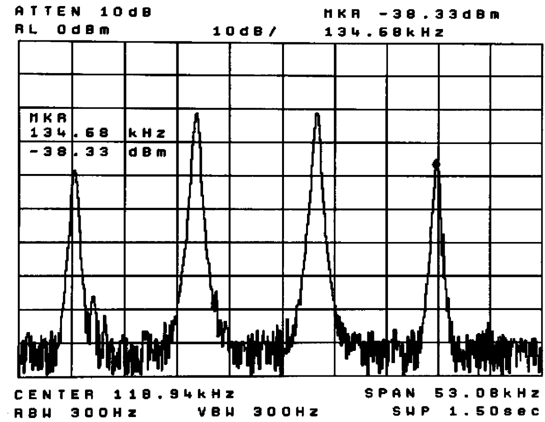

Fig. 16. Spectrum analyzer measurement of two-tone test at the amplifier output.

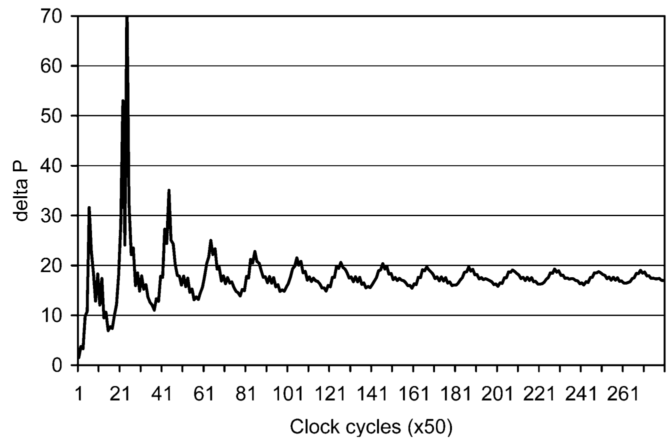

Fig. 17. ΔP value versus clock samples measured by BIST hardware.

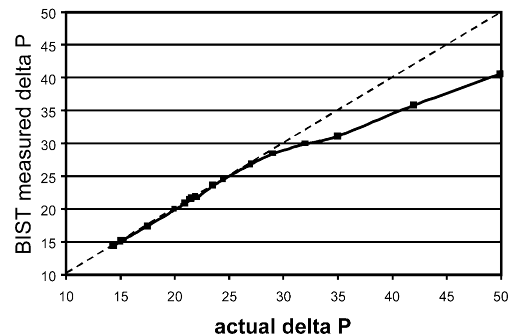

Fig. 18. ΔP measured using the BIST hardware (dots) versus the actual ΔP reading using a spectrum analyzer (straight line).

experimental hardware to reduce noise in the system that can influence the measurements.

Using the spectrum analyzer reading as the reference, we compared the BIST measured ΔP data to the actual ΔP value for various values, as illustrated in Fig. 18. As discussed, we need to stop the accumulator in the BIST analyzer at the integer multiple of period $\omega_2 - \omega_1$ in order to properly extract the dc value. In the measurement, we run the accumulator for 1024×110 clock cycles for every ΔP test. As shown in the plot, linearity measurement, using the proposed BIST, agrees well with the spectrum analyzer reading for ΔP, less than 30 dB. Above 30 dB, the BIST measured ΔP differs from the actual ΔP due to the quantization error of the 8-bit sampling

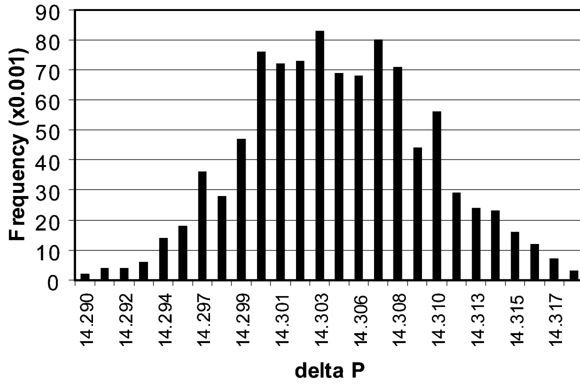

Fig. 19. ΔP distribution measured using the BIST hardware for an actual ΔP of 14.3 dB. Total 1000 tests with mean value of 14.3, standard deviation of 0.0055, and variance of 0.00003.

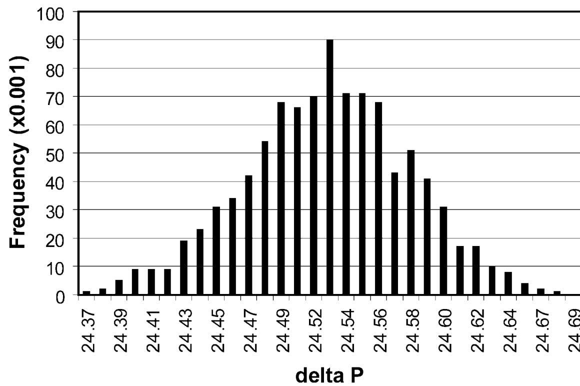

Fig. 20. ΔP distribution measured using the BIST hardware for an actual ΔP of 24.5 dB. Total 1000 tests with mean value of 24.52, standard deviation of 0.0544, and variance of 0.003.

system. We also measured the ΔP distribution by running the BIST 1000 times with a C program to capture the measured ΔP data automatically. The measured ΔP distributions are shown in Fig. 19 for an actual ΔP of 14.3 dB, and in Fig. 20 for an actual ΔP of 24.5 dB, respectively. For the 1000 BIST measurements for an actual ΔP of 14.3 dB, the distribution statistics show a mean value of 14.3, standard deviation of 0.0055, and variance of 0.00003. For the 1000 BIST measurements for an actual ΔP of 24.5 dB, the distribution statistics show a mean value of 24.52, standard deviation of 0.0544, and variance of 0.003. Both deviations are quite small. The ΔP measurement is limited by the dynamic range of the BIST hardware with a limited number of quantized bits. For a communication transceiver, the number of bits for the ADC and DAC are determined by the desired system dynamic range. In other words, if eight bits is chosen for the ADC/DAC, the sample system would require neither better than 30 dB (equivalent 5–6 bits) dynamic range, nor a ΔP larger than 30 dB. Therefore, the proposed BIST scheme using the existing ADC/DAC, will automatically meet the system dynamic range requirement. The loss of accuracy above 30 dB is not a serious problem since one is typically more concerned with lower values where the amplifier is more nonlinear for fault detection, manufacturing or in-system circuit characterization, and on-chip automatic calibration and compensation.

TABLE I
SYNTHESIS RESULTS FOR BIST CIRCUIT

FPGA Attribute	Total in FPGA	2-mult-accum		1-mult-accum	
		Used by BIST	% Usage	Used by BIST	% Usage
# of slices	768	313	40%	212	27%
# of flip-flops	1536	218	14%	158	10%
# 4-input LUTs	1536	572	37%	390	25%
Maximum BIST Clock Frequency = 48.5 MHz					

C. BIST Circuit Synthesis

The DDS-based TPG, test controller, and multiplier-accumulator-based ORA were modeled in Verilog, along with an interface to allow PC control of the BIST circuitry and retrieval of the BIST results. The complete Verilog model is approximately 510 lines of noncommented code. The Verilog code can also be parameterized to facilitate easy adaptation of the BIST circuitry for different size DAC and ADC for synthesis into standard cell based ASICs or into FPGAs. In our implementation, we worked with an 8-bit DAC and ADC and synthesized the BIST circuitry into a Xilinx Spartan XC2S50 FPGA. Table I summarizes the synthesis results to give an idea of the area and performance of the complete BIST circuit. The synthesis results are given for two possible implementations. The first implementation includes two multipliers and two accumulators such that DC_1 and DC_2, or DC_3 and DC_4, are obtained simultaneously during the same BIST sequence as illustrated in Fig. 9. The second implementation includes a single multiplier and accumulator with DC_1 and DC_2, or DC_3 and DC_4, obtained during separate, but identical, BIST sequences. This increases test time since the BIST sequence must be executed twice to obtain each dc value but it reduces the area overhead of the BIST circuitry by almost 50%. It should be noted that the XC2S50 is a small-sized FPGA in the Spartan II series and is the same size as the smallest Virtex FPGA. However, the 8-bit BIST circuitry will also fit in the smallest Spartan II series, the XC2S15. Therefore, the size of the BIST circuitry is reasonably small with the DDS-based TPG accounting for approximately one third of the total circuitry. Moreover, there are additional area penalties for our data capture and monitor purpose, which can be eliminated for actual BIST implementation.

The maximum clock frequency of the BIST circuitry is dominated by delays in the multiplier and accumulator in the ORA and can be increased significantly by simply pipelining the ORA with additional flip-flops at the outputs of the multiplier before entering the accumulator. Since there are many more 4-input LUTs used in the BIST circuitry than flip-flops, pipelining the ORA should cause little, if any, increase in the FPGA utilization because most flip-flops at LUT outputs are unused in the synthesized implementation.

These synthesis results can be compared to the FFT-based BIST approach proposed in [12]. For a 256-point FFT with a 32-point approximate kernel, a Virtex II XC2V8000 was used for implementation of that BIST approach. The XC2V8000 is almost 250 times larger than the XC2S15. Our BIST circuitry requires only about 5% of the logic resources that would be needed to implement an FFT-based approach [12]. For example, a 1024-point radix-2 FFT alone requires 3332 slices in addition

to three 18×18-bit multipliers in a Virtex II or Spartan 3 FPGA [17]. As a result, an FFT circuit alone is more than ten times larger than our complete BIST circuit which also includes the DDS-based TPG, test controller, and PC communications interface. The DAC and ADC are not included in the BIST overhead calculation since the approach is targeted for mixed-signal systems that contain the DAC and ADC as part of the existing design. In addition, the maximum clock frequency of the FFT-based BIST approach was reported to be between 1 and 2 MHz [12], while our approach will operate at 48.5 MHz with no modifications to the architecture to improve performance. Finally, the SNR obtained using the FFT-based BIST are about 24.74 and 21.80 dB for signal generation and signal analysis, respectively, while an SNR of about 30 dB was achieved by our DDS-based BIST scheme with only 8-bit resolution.

D. Test Time

The test time required to make the on-chip linearity and frequency response measurements with the BIST circuitry is a function of several factors including the operating frequency of DDS-based TPG and multiplier/accumulator-based ORA and the number of accumulation cycles in the ORA. While the linearity can be measured in a single test sequence, the frequency response requires measurement at various frequency steps in the spectrum and, as a result, will be a direct function of the number of frequency steps. The overall test time is dominated by the number of accumulation cycles in the ORA, where one can tradeoff accuracy for test time. Recall that we must stop the measurement at an integral multiple of the period of the test tones being multiplied with the output response of the CUT. In general, the test time for a single measurement T_M (as would be the case for IP3), is given by

$$T_M = N_A \times T_P \tag{13}$$

where N_A is the number of accumulation cycles and T_P is the clock period for the BIST circuitry, DAC, and ADC. The total test time for multiple measurements (as in the case of frequency response) is $N_M \times T_M$, where N_M is the number of measurements.

As can be seen in Fig. 17, 10 000 accumulation cycles is more than sufficient to achieve good accuracy in the linearity measurement. As the frequency of the test tones increase, few accumulation cycles are needed, such that the test time is less for higher frequency measurements. For this example, however, we will use $N_A = 10\,000$ taken from Fig. 17. In our experiment hardware implementation, the clock frequency was 25 MHz such that $T_P = 40$ nsec. As a result, linearity can be measured in 0.4 ms and we can obtain the frequency response (both phase and gain) for 100 different frequency steps in 40 ms. In this case, we are sacrificing test time for a smaller, simpler, and cheaper BIST approach to accomodate on-chip and in-system test and measurements.

VII. Conclusion

We have developed a BIST approach for analog circuit functional testing measurement of amplifier linearity and frequency response including both phase and gain. The DDS-based TPG is used to generate two frequency tones required in the two-tone linearity test, as well as single tones for frequency response measurements. The efficient ORA consisting of a multiplier and accumulator, avoids using traditional FFT-based spectrum analysis which consumes much more power and die area. We have implemented the BIST approach in Verilog which was subsequently synthesized into an FPGA and verified on actual hardware with close agreement to traditional measurement techniques and simulations.

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