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Automatic Package and Board Decoupling Capacitor Placement Using Genetic Algorithms and M-FDM

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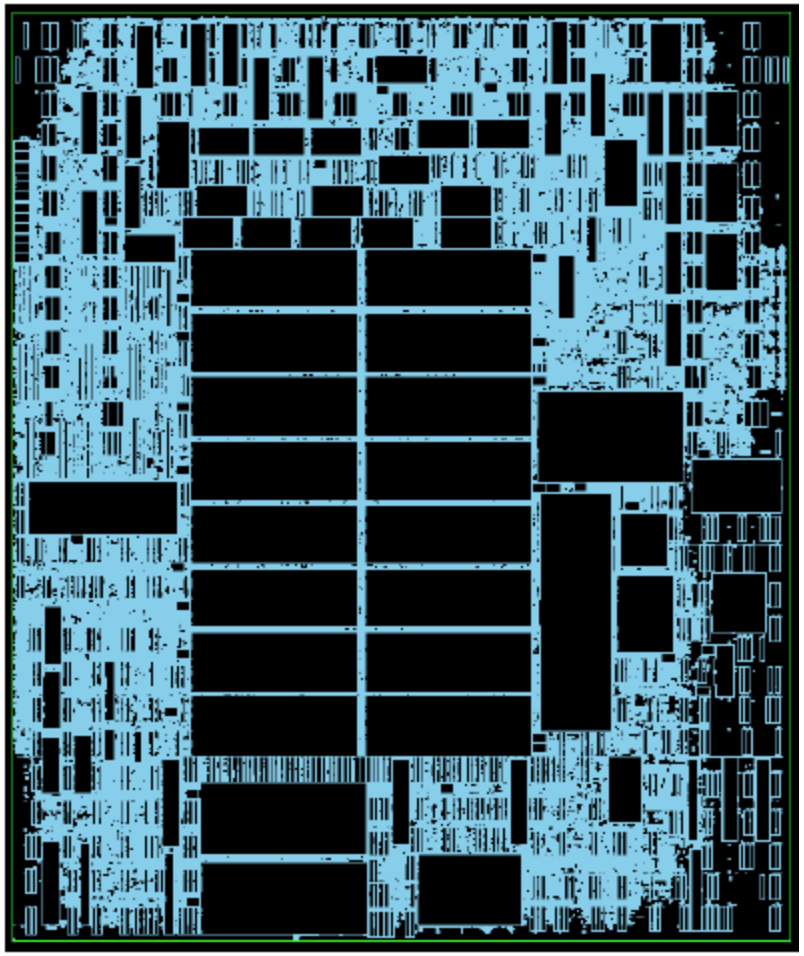
Outline

- Is there Life in ASICs in the era of nanometer designs?
- l The “Power” argument
  - Multiple-supply voltages
  - Multiple-threshold voltages
  - Voltage Islands
    - Fine Grained, Coarse Grained
  - Leakage control
  - Pushing ASIC performance with power neutral techniques

Competition: the problem with configurable fabrics

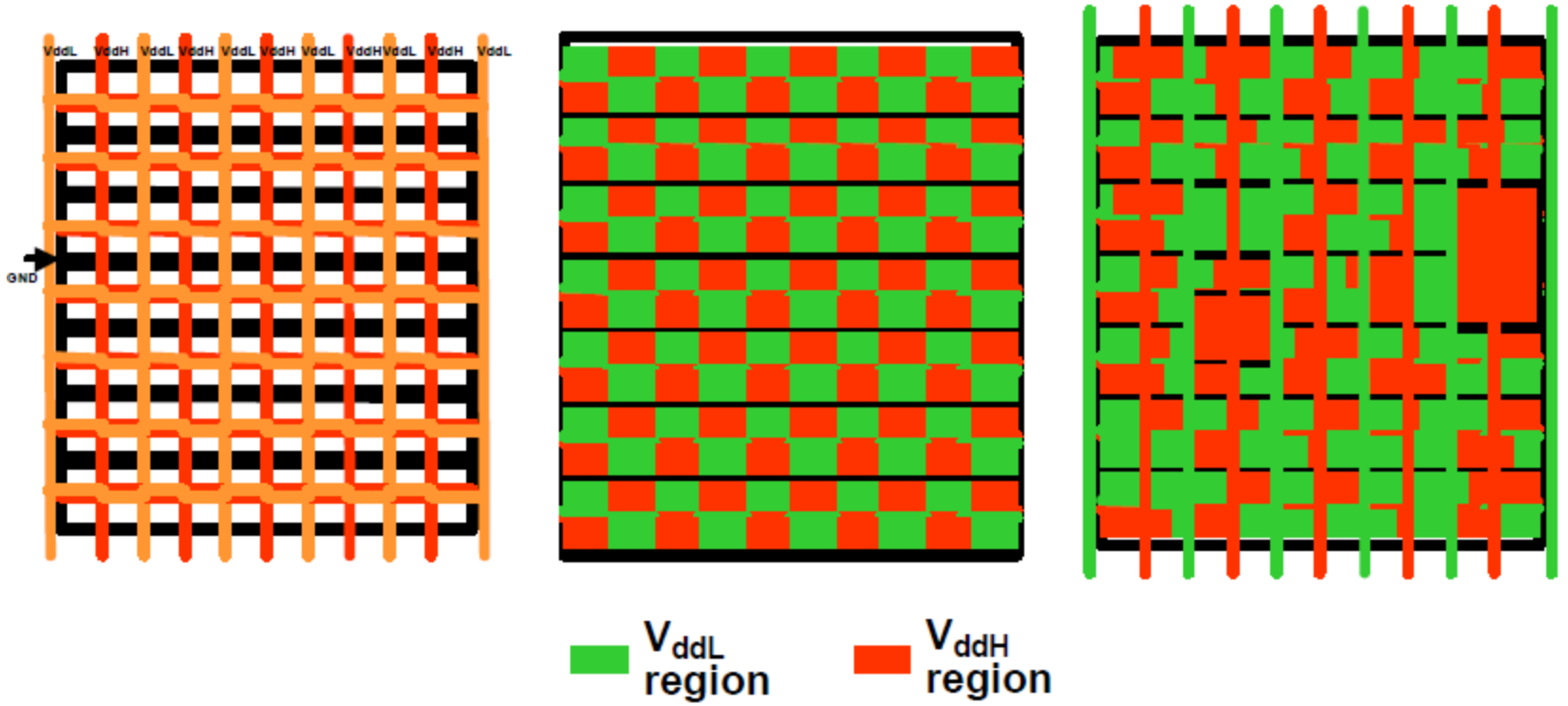
- What do you put on there :
  - IP blocks, Memories, Data-paths, top-level logic
- Compounded by the problem of IP on chip.
- Gets even worse by all the options you want to consider to minimize power:
  - Multiple voltages
  - Multi-thresholds
  - Voltage Islands
  - Coarse Grain, Fine Grain
  - Leakage



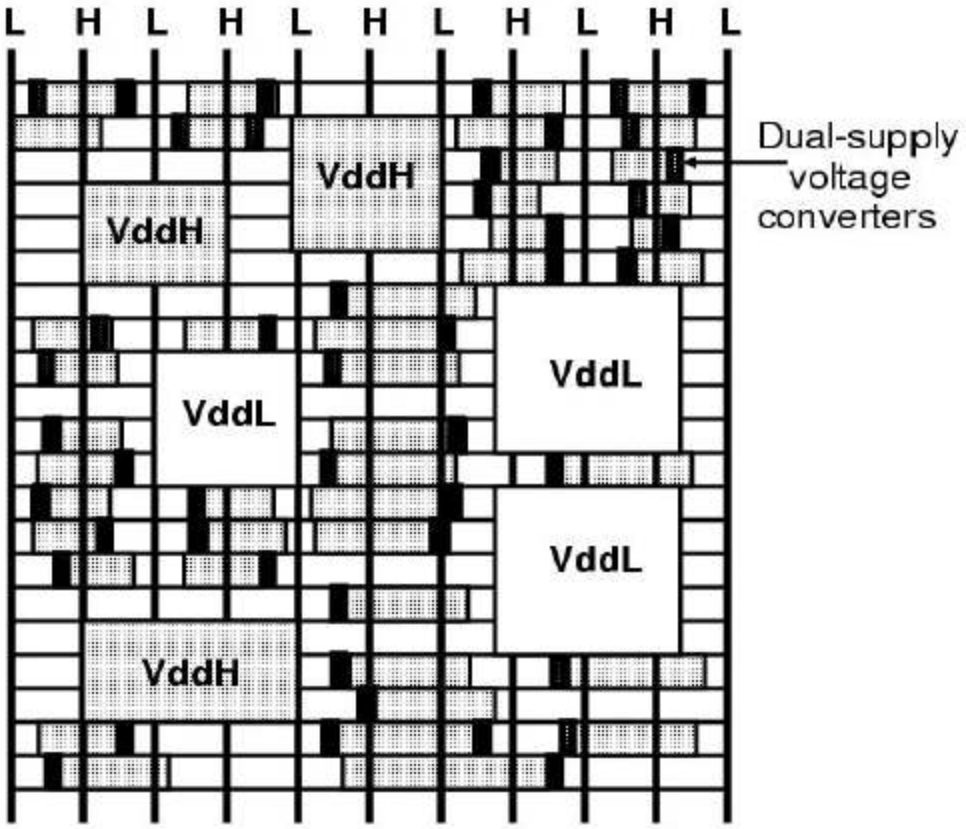
The Power arrgument: exploiting ASICs

- Multi Vdd
- Multi threshold
- Voltage Islands
  - With headers/footers
- Their application is very design specific.
  - How many voltage islands, what size, what header/footer, how many lowVt gates etc..
- Difficult to capture in configurable fabrics.
- Lead to very interesting physical design problems

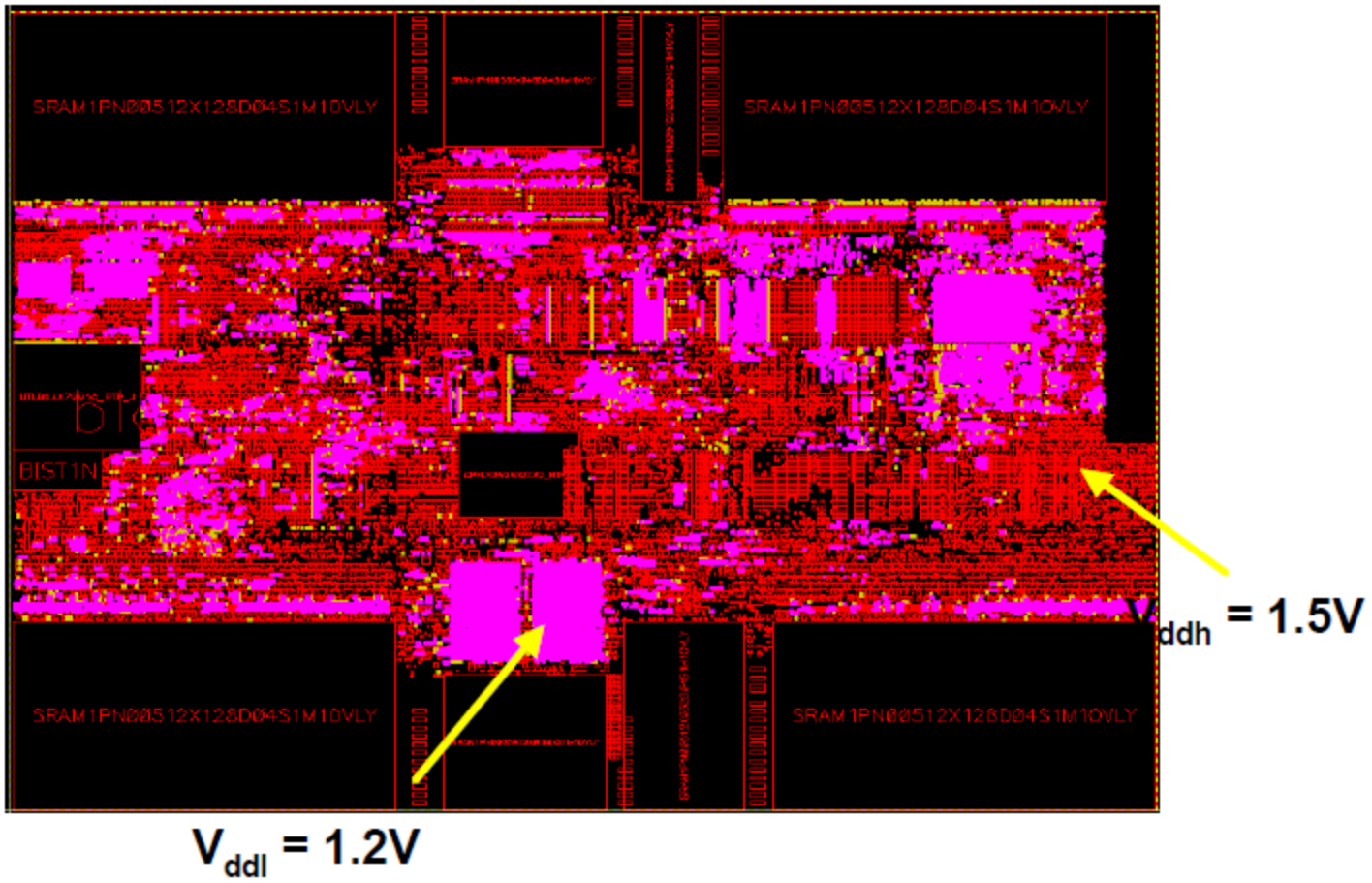
Flexible physical Design approach for dual-supply voltage design



Generic Voltage Island Power Grid

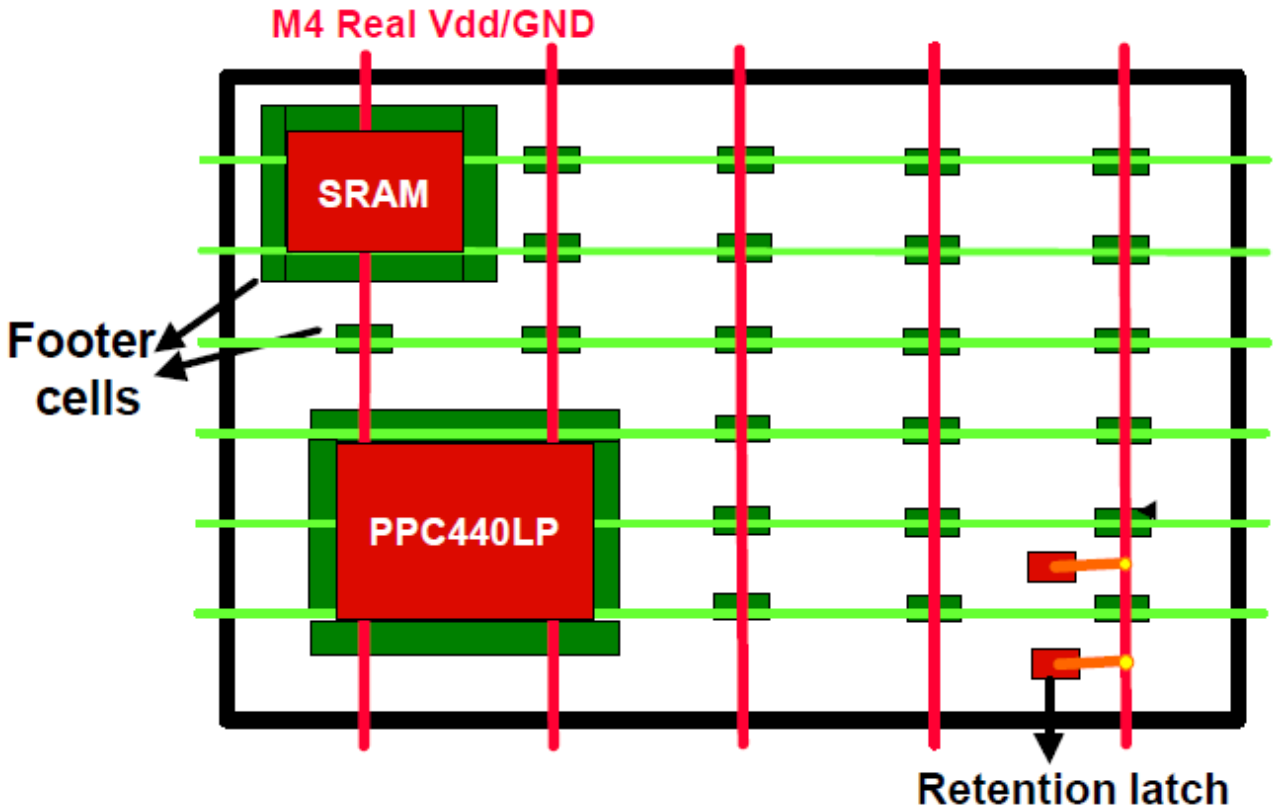


Fine grained voltage islands



Physical Design for Ultra--low leakage

- The same concept can be used to control leakage current with F/H cells in SOC designs



Voltage Island Power Issues

- Power Islands design
  - Pros
    - Reducing switching power dissipation
    - Saving Standby component of power dissipation
  - Cons
    - More complicated with respect to static timing,
    - Power planning and routing
    - Floorplaning

Basic Data Structure

- Each core for individual islands
  - Move two core each other
  - Possibility of merging them each other
  - Lead to lower cost
  - Lower over head for level shifter

Integrated Floorplanning

- Chip level floorplanning
  - Trying arrange the compatible islands in adjacent position by cost function
- Island level floorplanning
  - Applying to each newly merged island
  - The composing cores inside the merged islands
  - Legalizing the newly generated floorplan

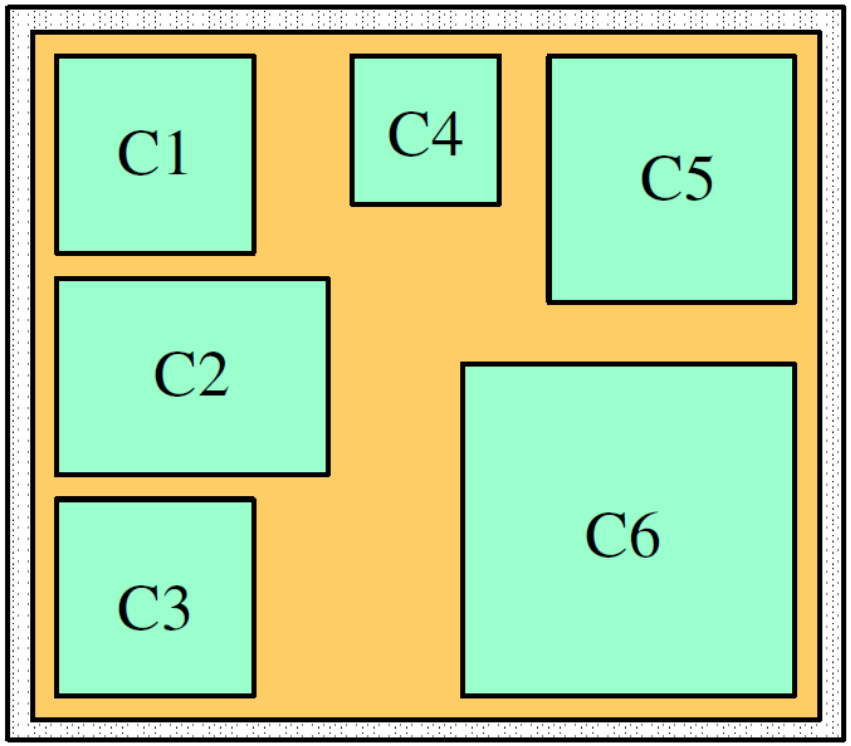
Solution Perturbation

- Island split move
  - Split up into a set of islands
- Island voltage change move
  - Voltage island support two or more legal supply voltage
  - Voltage level switched to one of its legal voltages
- Multi-island voltage change move
  - All the islands which supports li will be assigned to voltage li

Island Merging

- Chip level floorplanning
- The islands that are compatible are likely to be placed in adjacent position
- Two high power consumers and heater dissipater can not be placed each to relief the heat and power issue.

Reliability-Aware SoC Voltage Islands Partition and Floorplan



C1: $v1(r_{11})$, $v2(r_{12})$, $v3(r_{13})$
C2: $v1(r_{21})$, $v2(r_{22})$
C3: $v2(r_{31})$, $v3(r_{32})$, $v4(r_{33})$
C4: $v3(r_{41})$, $v4(r_{42})$
C5: $v4(r_{51})$
C6: $v1(r_{61})$
$v1>v2>v3>v4$

Soft Error Rate (SER) & Component Reliability Level (CRL)

- Characterization of component reliability level for a particular node:

$$Q_{critical} = \int_0^{t_{critical}} I_{drain}(t)dt$$

- Soft error rate:

$$SER_i = exp(\frac{Q_{criticalN} - Q_{criticali}}{Q_s})$$

- Component reliability level:

$$CRL_i = exp(-\alpha \cdot SER_i \cdot t)$$

Soft Error Rate (SER) & Component Reliability Level (CRL) (cont.)

- Component reliability level for a macro cell

$$CRL_i = \prod_{j=1}^{n} R_j$$

- Chip reliability level

$$RL(SOC) = \prod_{i=1}^{m} RL(\Lambda_i)$$

$$RL(\Lambda_i) = \prod_{j=1}^{n} CAR_{ij} * CRL_{ij}$$

$$CAR_i = \frac{i_{th}\ component\ access\ time}{application\ execution\ time}$$

Reliability-aware SoC voltage Island Partition Algorithm

Input : $C_i(V_i, R_i, P_i, CAR_i)$, $RL(SOC)^*$, DT^*
Output : *All possible solutions which meet the criterion*

Algorithm :

1: **For** each SOC component Ci **Do**
2: calculate CRL_i and CP_i
3: **End For**
4: construct a link list (*VILL*) for possible voltage island partitions
5: **For** each partition in *VILL* **Do**
6: update the CAR_i for each component
7: calculate the deadline time *DT* for this partition
8: **If** $DT > DT^*$ **Then**
9: delete this partition from *VILL*
10: **Else**
11: calculate the reliability level $RL(SOC)$
12: **If** $RL(SOC) < RL(SOC)^*$ **Then**
13: delete this partion from *VILL*
14: **Else**
15: calculate the power reduction
16: **End If**
17: **End If**
18: output the head of *VILL*
19: **End For**
20: sort *VILL* by the value of power reduction
21: output all the possible solutions

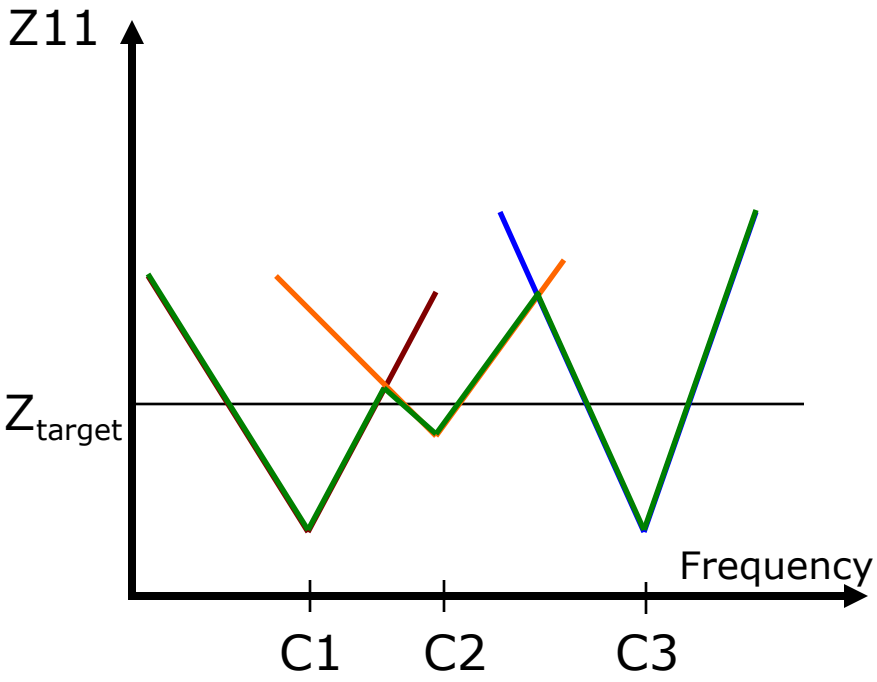
- Penalty function:

$$DT = (1+\delta) \times DT$$

$$RL(SOC) = (1-\epsilon) \times RL(SOC)$$

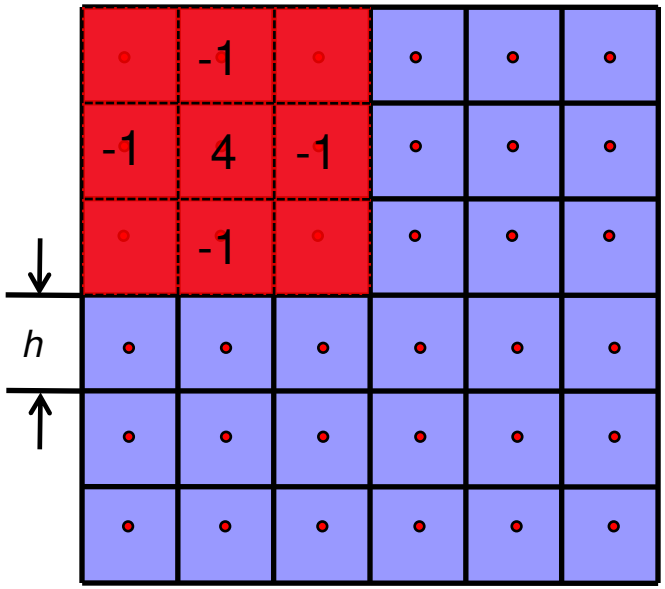
$$P(SOC) = (1+\eta) \times P(SOC)$$

Broadband Decoupling with Multiple Decoupling Capacitors



- Multiple decoupling capacitors with resonance at different frequencies are used for broadband decoupling
- However cross resonances (or anti resonances) occur and are undesirable
- Response is a function of placement
- Of all possible combinations of decaps and corresponding placements, only a small fraction will satisfy specs
- Automatic placement can be accomplished using an optimization engine

Single Plane Pair Case: Finite Difference Scheme

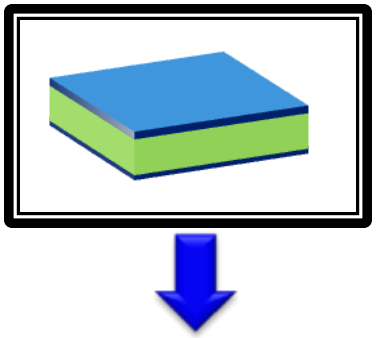


$$\nabla_t^2 = \left(\frac{d^2}{dx^2} + \frac{d^2}{dy^2} \right)$$

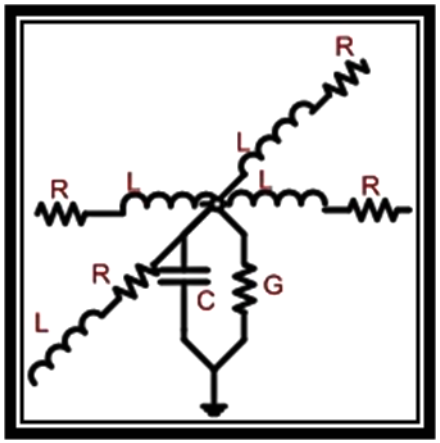
$$k = \omega\sqrt{\mu\varepsilon} \qquad L = \mu d \qquad C = \varepsilon \frac{h^2}{d}$$

- Helmholtz wave equation:
$$\left(\nabla_t^2 + k^2\right) u = -j\omega\mu d J_z$$
- Finite difference mesh using square cells (mesh size *h)*
- At boundary, homogeneous Neumann condition is used (open circuit)
- A five-point approximation is applied to the Laplace operator
- For lossless case, wave equation reduces to
$$\frac{u_{i,j+1} + u_{i+1,j} + u_{i,j-1} + u_{i-1,j} - 4u_{i,j}}{j\omega L} - j\omega C u_{i,j} + I = 0$$
- This gives rise to an equivalent circuit

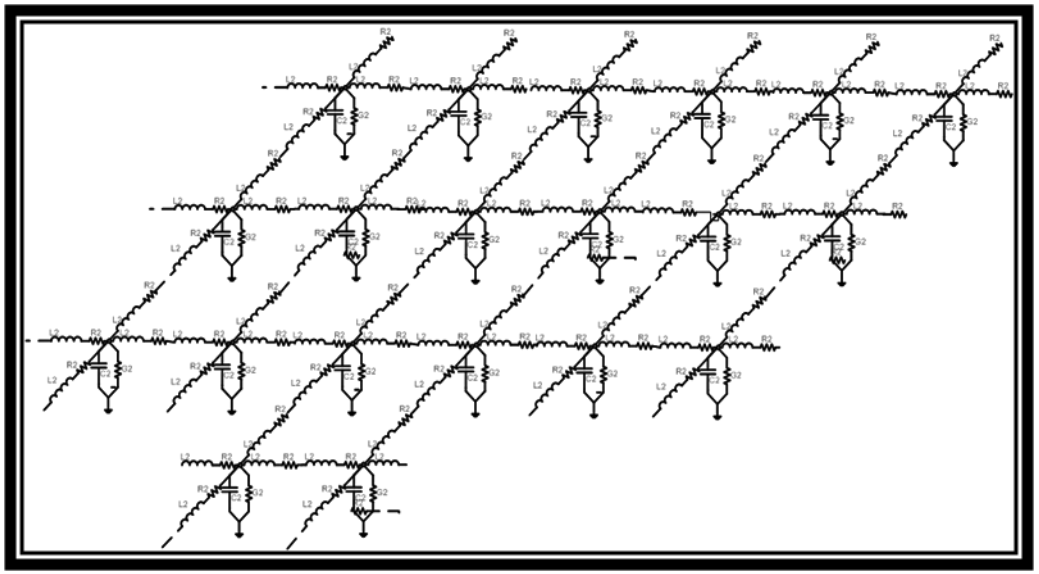
Single Plane Pair Case: Equivalent Circuit



Unit cell model



Representative equivalent circuit

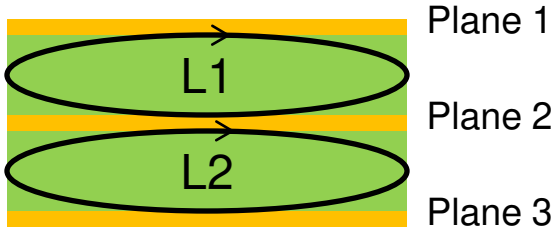


- Number of nodes increases as $O(w^2)$ where w is the linear dimension
- Overall admittance matrix size can be large
- What about solution efficiency?

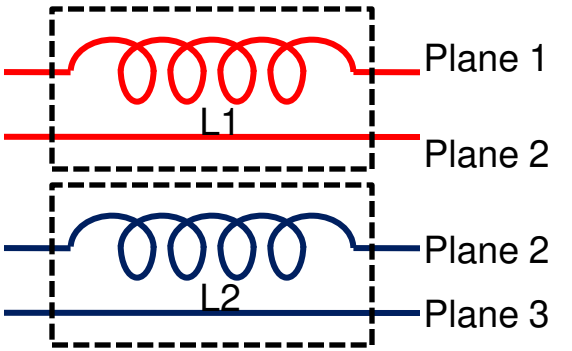
Multilayer Finite Difference Method (M-FDM)

Inductance matrix in multilayer unit cells

- An inductive loop is formed between each pair of planes
- However, each inductive loop is with reference to a local ground representing a return current path
- Shift reference nodes of each plane pair to the common ground

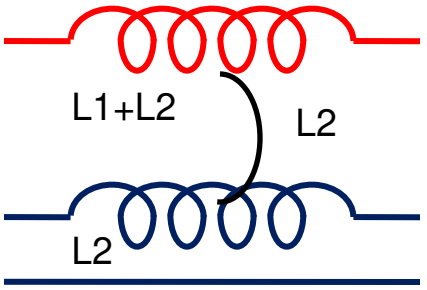


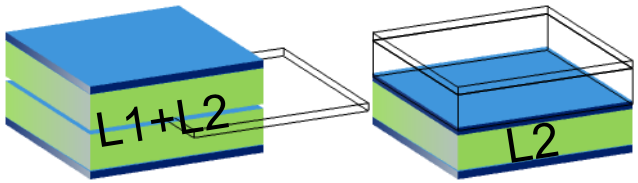
Cross-sectional view of 3-layered package



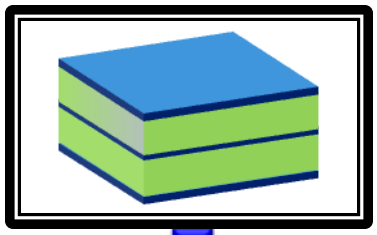
Inductance: Equivalent Circuit and Interpretation

- Combining the grounds results in a pair of coupled inductors
- L1 + L2 represents the total loop inductance between plane 1 and plane 3
- L2 represents the loop inductance between plane 2 and plane 3
- There is complete coupling of the magnetic fields between the two loops
- This is represented by the mutual element L2

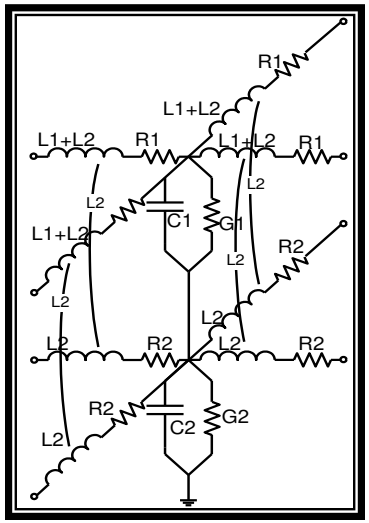




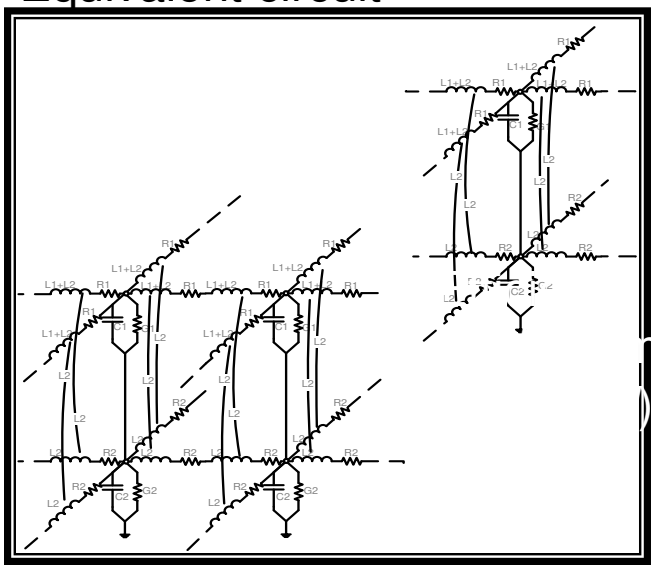
M-FDM: Combined Unit Cell and Equivalent Circuit



Unit cell model



Equivalent circuit



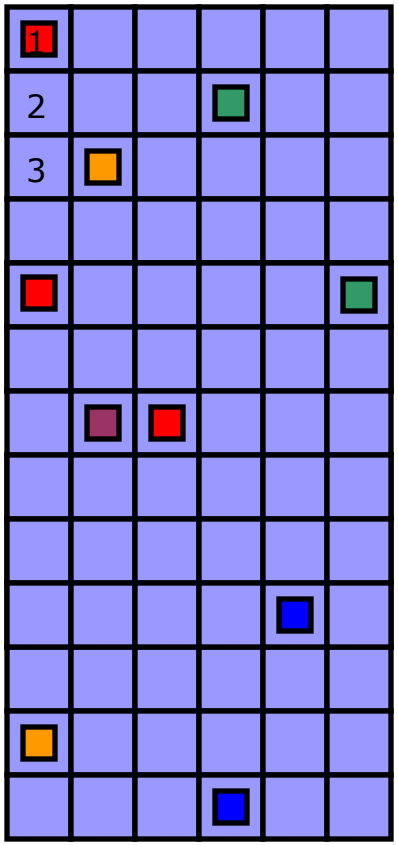
Matrix structure is similar (block tridiagonal)

K. Bharath, A.E. Engin, M. Swaminathan, K. Uriu and T. Yamada, "Computationally Efficient Power Integrity Simulation for System on Package Applications," in *Proc. of 44th DAC*, pp. 612 – 617, June 2007.

Approach

- Inputs:
  - Library of decoupling capacitors
  - Package/Board design with noise source locations
  - Target impedance requirements (impedance, bandwidth)
  - Number of capacitors to place
- Methodology:
  - Each “chromosome” is a string containing decap values and corresponding locations
  - GA works on an initial random population
  - Uses concepts of elitism, mutation and crossover
- Output:
  - Decap values and location that best satisfy target impedance

GA Encoding and Mechanics



No. of capacitors: 5

Chromosome length: 10

Parent	C1	C3	C1	C5	C4	1	9	11	20	29
Parent	C3	C2	C1	C4	C5	5	8	15	24	31

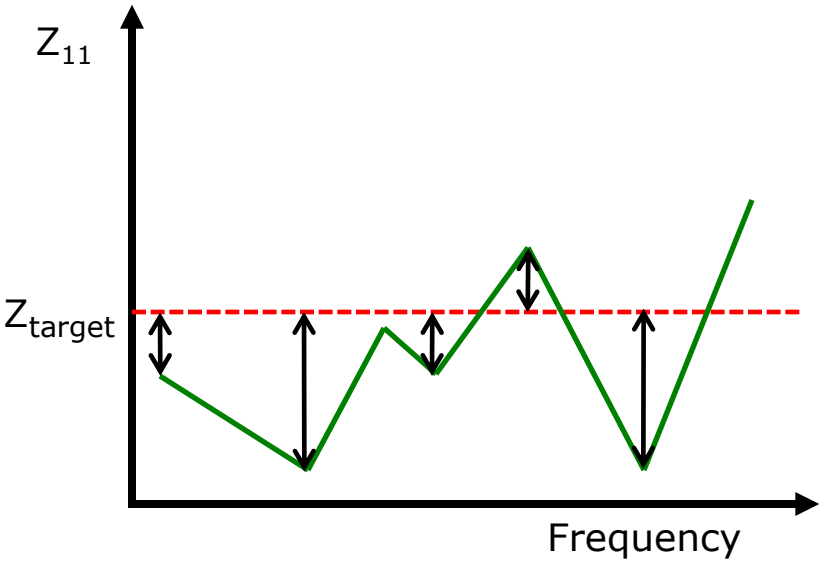
Crossover

	C1	C3	C1	C4	C5	1	9	15	24	31

Mutation

Child	C1	C2	C1	C4	C5	1	9	15	30	31

Fitness Function



- Fitness function:

$$f_i = \sum_{j=1}^{N_{port}} \sum_{k=1}^{N_{freq}} \left(w_1 \left[Z_{tar,j} - Z_{j,j}(k) \right] + w_2 \left[Z_{tar,j} > Z_{j,j}(k) \right] \right)$$

- w_1 and w_2 : empirically determined weights
- $Z_{tar,j}$: Target impedance (specification) at the j^{th} port
- $Z_{j,j}$: Self impedance (simulated) at the j^{th} port

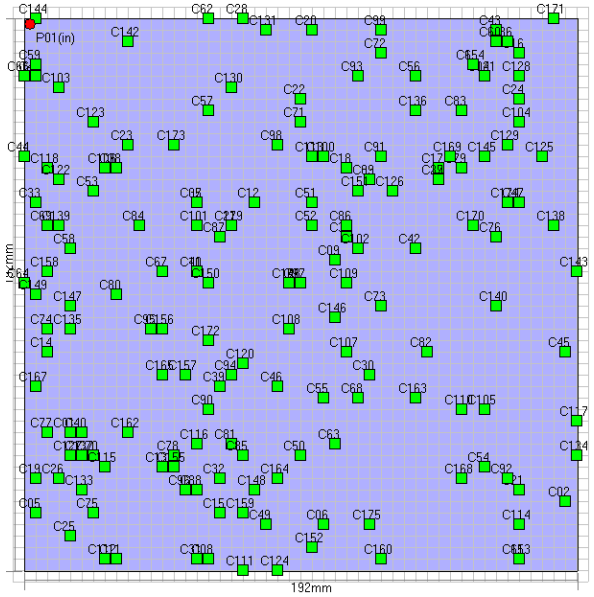
Capacitor Library

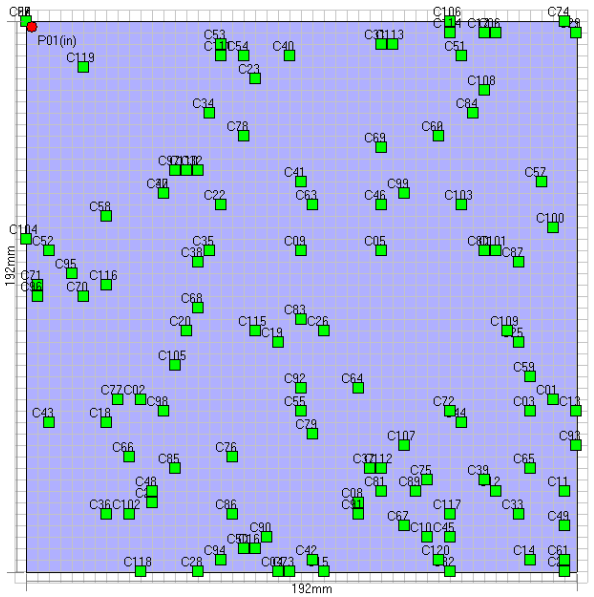
Cap	ESR (mΩ)	ESL (nH)	Res. Freq (GHz)
27 pF	850	0.4	1.5315
33	700	0.4	1.3853
130	373.4	0.458	0.6523
174.4	313.1	0.509	0.5342
207.1	243.1	0.468	0.5112
304.7	148.6	0.413	0.4487
511.4	139.8	0.4	0.3519
598.5	120.0	0.432	0.3137
1.0 nF	75.0	0.370	0.2616
2.2	62.1	0.426	0.1644
2.9	203.8	0.533	0.1280
4.2	141.1	0.523	0.1074

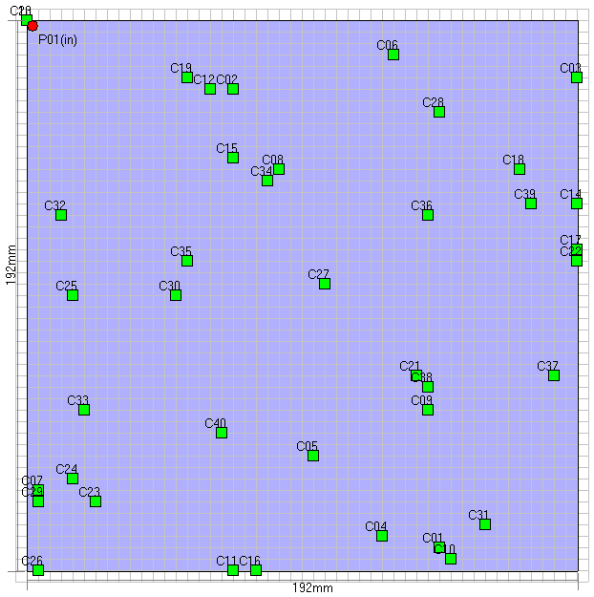
Cap	ESR (mΩ)	ESL (nH)	Res. Freq (GHz)
8.2	88.9	0.519	0.0771
19.8	44.3	0.572	0.0473
41.1	25.7	0.435	0.0376
83	19.9	0.416	0.0271
179	15.9	0.548	0.0161
379	14.1	0.543	0.0111
0.81 uF	9.8	0.485	0.0080
1.93	6.7	0.686	0.0044
3.86	4.8	0.704	0.0031
7.87	5.5	0.876	0.0019
21.2	2.7	1.628	0.0009
81.2	2.5	2.834	0.0003

Madhavan Swaminathan and Ege Engin, Power Integrity Modeling and Design for Semiconductors and Systems, Prentice Hall, 2007

Results: Placement





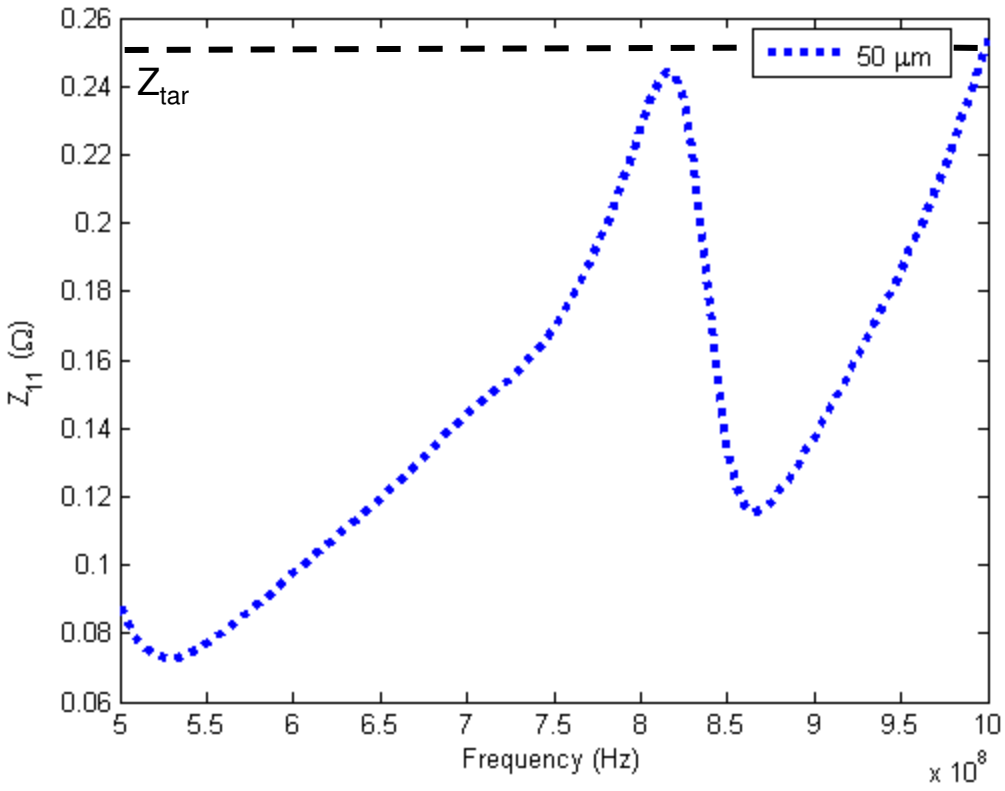


50 µm-
170 Capacitors

25 µm-
120 Capacitors

18 µm-
40 Capacitors

Results: Test Case 1



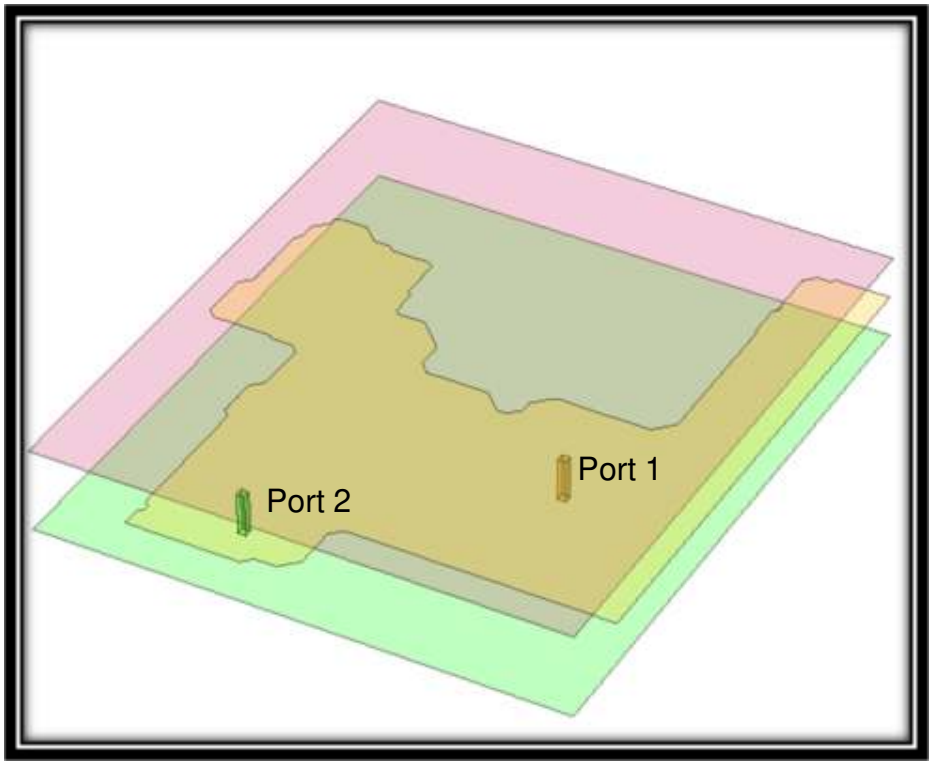
50 µm-
170 Capacitors

25 µm-
120 Capacitors

18 µm-
40 Capacitors

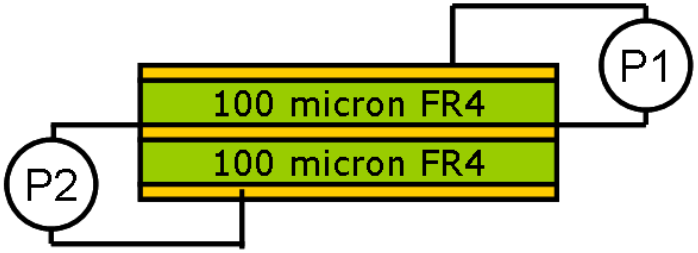
Simulation Specs:
- Time/ GA iteration: 20 s
- Max iterations: 500

Test Case 2: Multilayer Structure



Dimensions 112 mm X 97 mm
Solid top and bottom layers

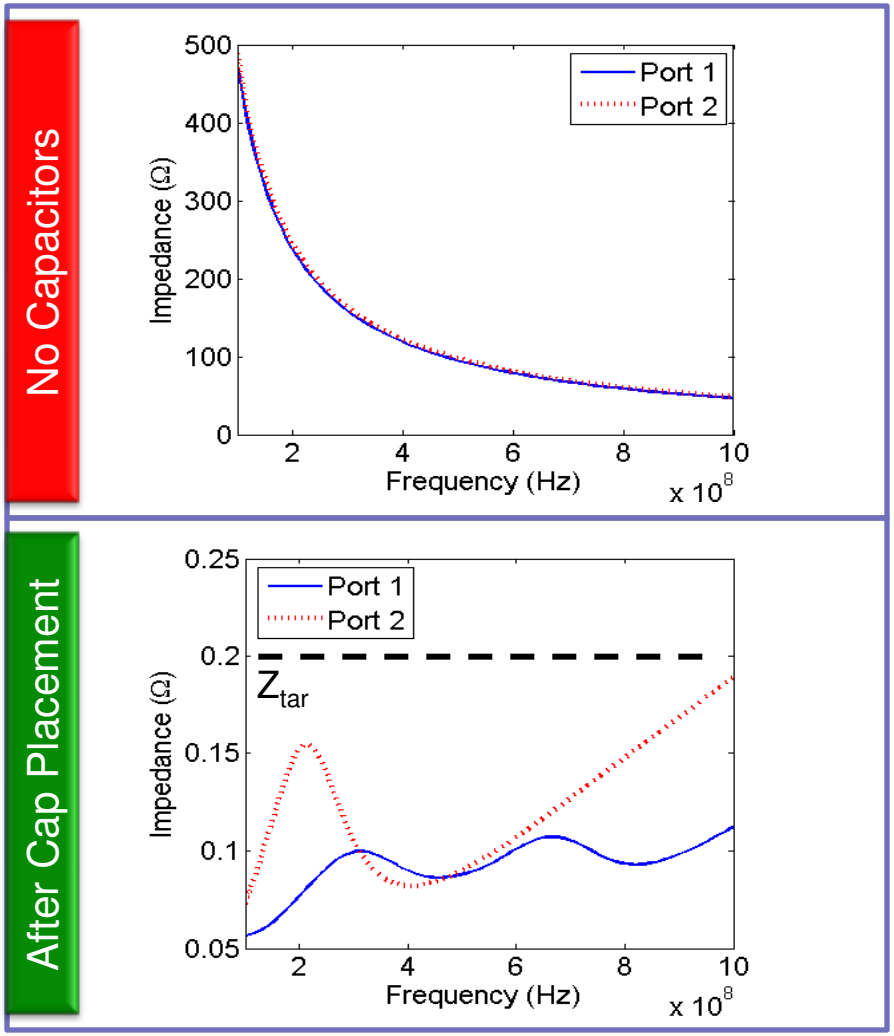
- SSN can couple vertically in multi-layer structures
- Decap placement can be optimized to suppress coupling between vertically separated ports



Number of Decaps : 200

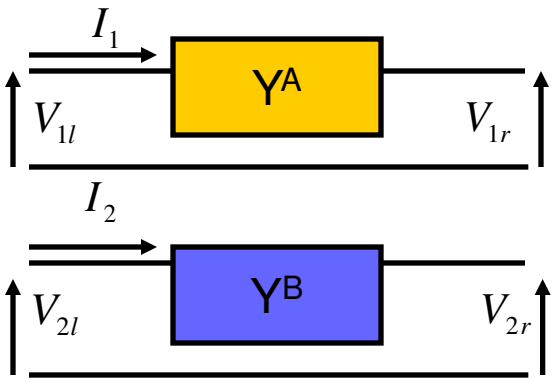
Z_{tar} = 200 mOhm

Results: Test Case 2

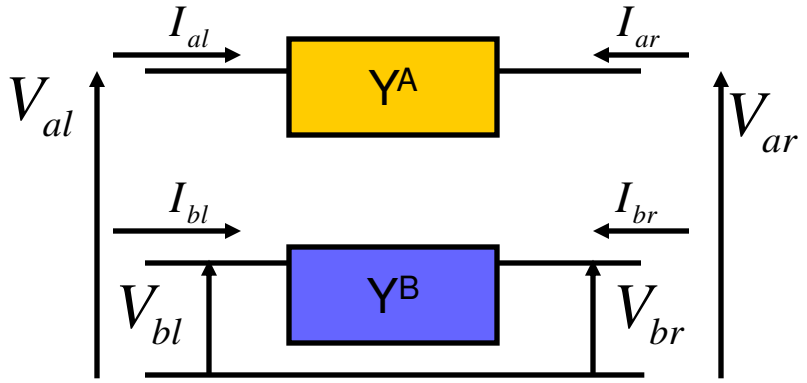


Thank you!

Reference Node Assignment for Two-Port Admittance Matrices



$$Y_{11}^A V_{1l} + Y_{12}^A V_{1r} = I_1$$
$$Y_{11}^B V_{2l} + Y_{12}^B V_{2r} = I_2$$



$$I_{bl} = I_2 - I_1$$
$$where, I_2 = Y_{11}^B V_{bl} + Y_{12}^B V_{br}$$
$$V_{1l} = V_{al} - V_{bl}; V_{1r} = V_{ar} - V_{br}$$
$$V_{2l} = V_{bl}; V_{2r} = V_{br}$$
$$Y_{11}^A (V_{al} - V_{bl}) + Y_{12}^A (V_{ar} - V_{br}) = I_{al} = I_1$$

$$\begin{pmatrix} I_{al} \\ I_{ar} \\ I_{bl} \\ I_{br} \end{pmatrix} = \begin{pmatrix} Y^A & -Y^A \\ -Y^A & Y^A + Y^B \end{pmatrix} \begin{pmatrix} V_{al} \\ V_{ar} \\ V_{bl} \\ V_{br} \end{pmatrix}$$

- KCL equations for isolated systems written
- When shifting ground of Y^A to ground of Y^B , enforce node current I_{bl} to contain return I_1
- Rewrite KCL equations for revised system
- Provides complete system matrix

Reference Assignment for Inductances

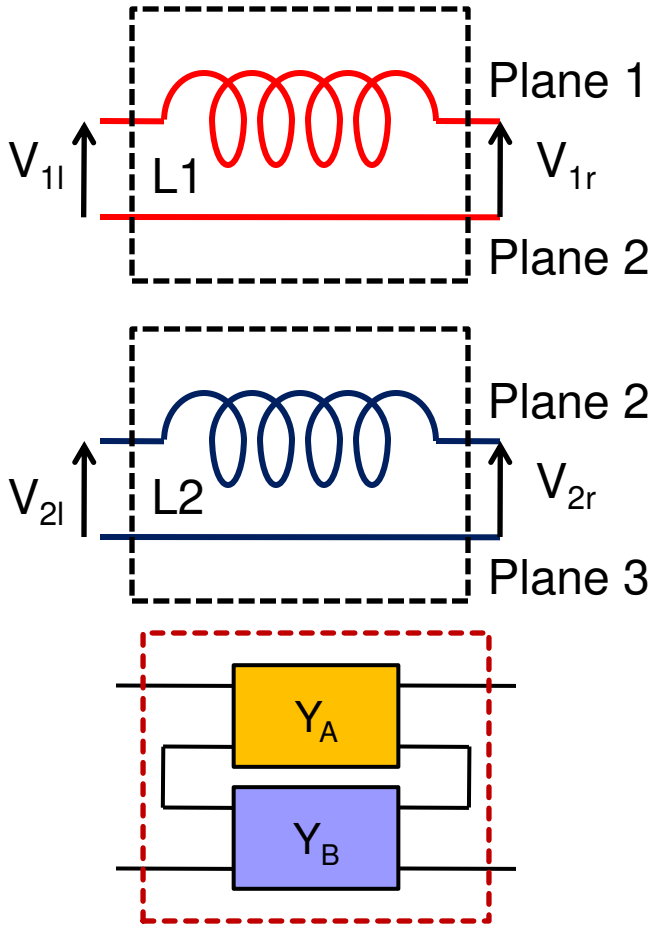
- In this case,

$$Y^A = \begin{pmatrix} \frac{1}{j\omega L_1} & -\frac{1}{j\omega L_1} \\ -\frac{1}{j\omega L_1} & \frac{1}{j\omega L_1} \end{pmatrix} \quad Y^B = \begin{pmatrix} \frac{1}{j\omega L_2} & -\frac{1}{j\omega L_2} \\ -\frac{1}{j\omega L_2} & \frac{1}{j\omega L_2} \end{pmatrix}$$

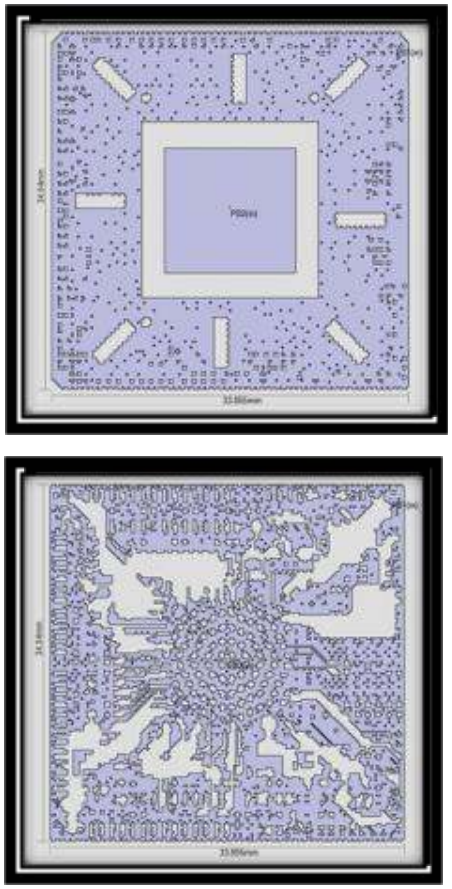
- The combined 4-port system is represented by

$$Y = \begin{pmatrix} \frac{1}{j\omega L_1} & -\frac{1}{j\omega L_1} & -\frac{1}{j\omega L_1} & \frac{1}{j\omega L_1} \\ -\frac{1}{j\omega L_1} & \frac{1}{j\omega L_1} & \frac{1}{j\omega L_1} & -\frac{1}{j\omega L_1} \\ -\frac{1}{j\omega L_1} & \frac{1}{j\omega L_1} & \frac{1}{j\omega L_1}+\frac{1}{j\omega L_2} & -\left(\frac{1}{j\omega L_1}+\frac{1}{j\omega L_2}\right) \\ \frac{1}{j\omega L_1} & -\frac{1}{j\omega L_1} & -\left(\frac{1}{j\omega L_1}+\frac{1}{j\omega L_2}\right) & \frac{1}{j\omega L_1}+\frac{1}{j\omega L_2} \end{pmatrix}$$

- Can this be represented by an equivalent circuit?



M-FDM Results: Scalability and Timing



2 representative layers of a realistic package

Simulation setup:
Dual processor 3.2 GHz workstation with 3 GB RAM

# Layers	# Nodes	Time (s)/freq point
2	38,800	0.93
3	77,600	1.78
4	116,400	3.92
5	155,200	6.8
6	194,000	10.19
7	232,800	16.33
8	271,600	23.56
9	310,400	32.99
10	349,200	42.53

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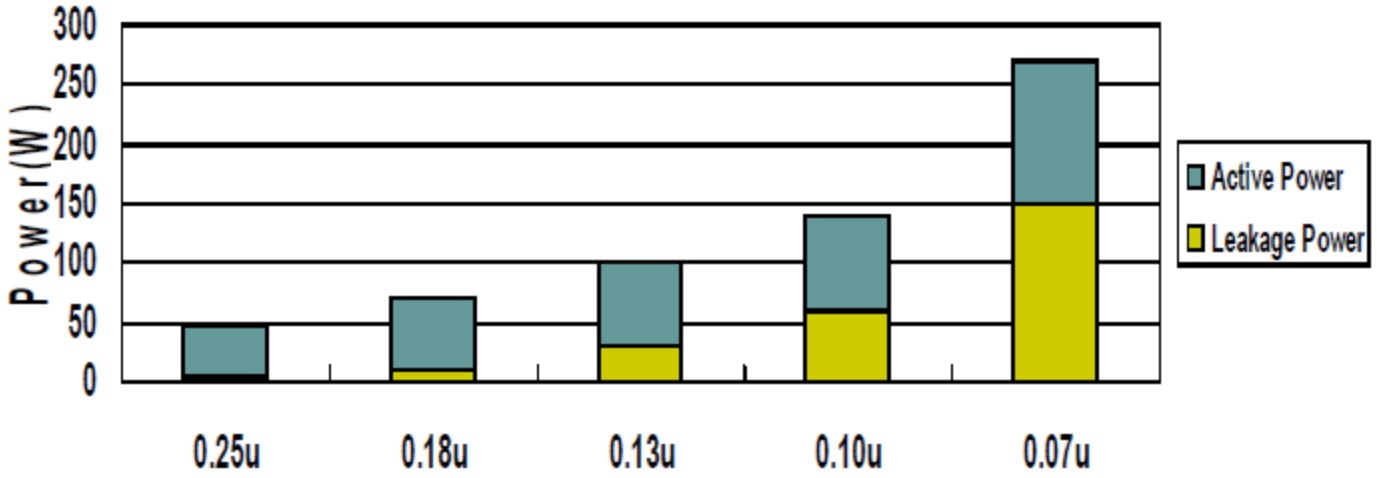
Introduction

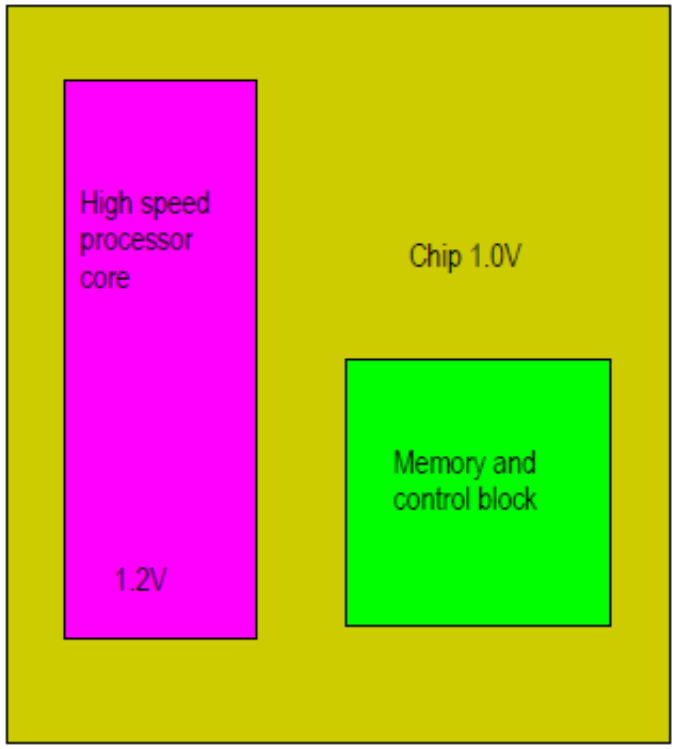
- VLSI design issues
  - Power optimization
  - High performance, low power consumption
  - Multi-function device on single chip
  - Battery operated power saving chip

Introduction (cont.)

- Power consumption
  - Active power and dynamic power



Introduction (cont.)



Example of Timing-critical Voltage Island

- Voltage islands
  - Reduce active power and dynamic power
  - Performance critical logics (procesor)use highest voltage
  - Memory and control logics use lower voltage
  - Place to nearby power pins
  - Level converters needed
  - Area and delay overhead