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Automatic Repositioning Technique for Digital Cell Based Window Comparators and Implementation within Mixed-Signal DfT Schemes

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Abstract

The possibility of using window comparators for the on-chip evaluation of signals in the analogue circuit part has been demonstrated and is shortly summarised. One of the problems is the lot-to-lot variation of the comparator window. An automatic window repositioning technique is detailed that allows to compensate the window shift. The components for the implementation comprising a reference comparator and the evaluation comparators are described along with the implementation of the technique. It is shown, that this technique allows the automatic lot condition adjustment of the evaluation comparators. Furthermore the technique can provide lot specific information to an automated test equipment that can be documented in the test results due to its diagnosis capability.

1. Introduction

Safety systems in electronics are one of the key issues in highly reliable applications, such as railway, automotive, aeronautics and other industries. Besides the process quality cost-effective testing is one of the parameters to achieve this high quality. The most cost-effective way of testing in terms of test time optimization and also time-to-market is Design-for-Testability (DfT). Today a wide range of DfT techniques exists for digital integrated circuits (IC), but only a few proposals are known for analog and mixed-signal ICs. Since test costs can always be traded off against die area, DfT also becomes interesting for cost sensitive products like consumer or automotive mixed-signal ICs. For those products an interesting test solution consists in checking certain DC-operating points or signal levels on critical circuit nodes. This check can be performed at different (test) time instances, supply voltage conditions and temperatures. Furthermore, the continuous observation of critical nodes can also be used during the application to achieve on-line self-checking capabilities (similar like for digital ICs) [1] e.g. to flag failures to a control unit in safety-critical applications.

In order to check the correctness of analogue voltages at selected nodes comparators are required. Different proposals have been made addressing this type of DfT. In [2] the design of checkers aimed at the concurrent test of analog and mixed-signal circuits is considered. In this paper the inherent redundancy of the circuit to be tested was exploited which results in the use of a code for the analog signals. In [3] a strobed comparator with a variable threshold is proposed, that can be used as a waveform digitizer. This solution, however, demands high requirements in terms of bandwidth and clock skew/jitter. Another scheme describes a very specific application of on-chip analogue differential comparator [4] targeted at measuring the dynamic performance of the differential SRAM sense amplifier. The result is compared with an externally applied differential signal. A bias-programmable, clocked, two-mode comparator with hysteresis for mixed-signal ICs is introduced in [5-6]. In this approach the analogue comparator is implemented by a functional conversion of system OTAs or operational amplifiers (OpAmp) during test mode [6], in which different thresholds can be programmed via the biasing from the digital part.

Recently a simple comparator scheme has been presented in detail based on digital gates and referred to as digital window comparator [7-9]. As it has been described this type of comparator is sensitive to the lot-to-lot variation of the threshold voltages of the NMOS and PMOS [9].

This paper deals with the different possibilities to stabilize the width and position of this window automatically against changes due to technological parameter spread. This technique allows to some extend to monitor the actual process condition. The possible insertion of those comparators in an already existing scan path is also investigated, in order to make the test solution easy and flexible.

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2. Principle of a Digital Window Comparator

As described in detail in [7] and depicted in fig. 1 a simple digital window comparator can be implemented with an i-input NAND, a j-input NOR and additionally with an EXOR gate. The target of this DfT approach is to implement a simple on-chip evaluation circuit which only requires digital logic gates without the need of additional analogue I/Os.

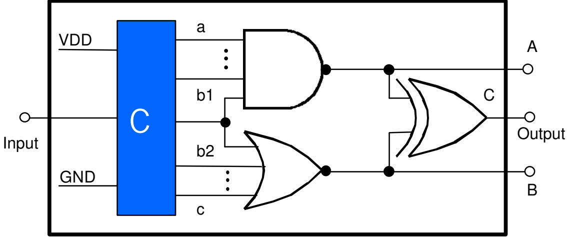

Fig. 1 General Digital Window Comparator

The principle is based on the fact that the logical threshold V_{LT} of NANDs and NORs can be shifted in opposite directions depending on the number of gate inputs connected together (input) and connected to V_{DD} and ground, respectively. At least one input of the NAND and NOR gate (b_1, b_2) must be connected together to form the comparator input. The required width and position of the window dictates the number of inputs for the NAND (i) and NOR (j) and also how many of those gate inputs must be connected to V_{DD}, ground or to the common comparator input. In fig. 1 this connection configuration is represented by the block C. Those inputs of the gates that are not connected with the comparator input are either connected to the supply V_{DD} (NAND) or the ground GND (NOR). The outputs of the NAND and the NOR can be connected to an EXOR gate to compress the comparator into a single bit output.

For digital inputs the comparator output (EXOR) is always at logically zero. If, however, an anlogue input signal is applied, the output of the EXOR depends on the actual level of the input signal. If the logical thresholds of the NAND and NOR are different, then there exists a range (V_{LT_NAND}–V_{LT_NOR}) where the comparator output (C) switches to logically one. This range is referred to as comparator window. The NAND and the NOR basically operate as inverters with a shifted logical threshold V_{LT} depending on the W/L ratios and the number of inputs of the NAND and the NOR connected to V_{DD} (NAND) or GND (NOR). For such an inverter configuration the logical thresholds can be derived from equation 1[9,10]:

$$V_{LT} = \frac{VDD + V_{thp} + \sqrt{\beta} * V_{thn}}{1 + \sqrt{\beta}} \qquad \text{(Eq. 1)}$$

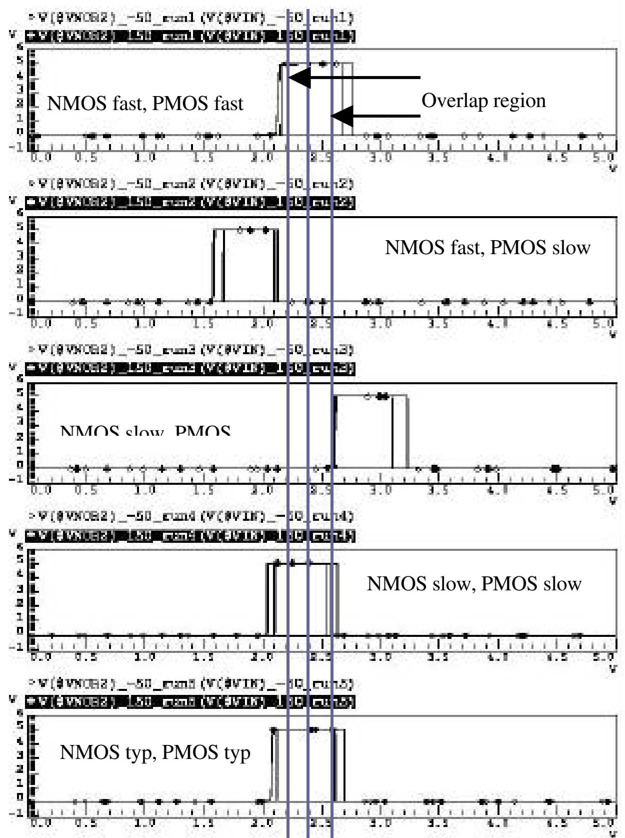

Fig. 2 Characterization of a 2-input NAND/NOR window comparator for -40°C and +150°C

with V_{thp} and V_{thn} being the threshold voltages for the p and n-transistor, respectively, V_{DD} the supply and β is defined as:

$$\beta = \frac{Kn * (Wn / Ln)}{Kp * (Wp / Lp)} \qquad \text{(Eq. 2)}$$

Note, that if $V_{thp} = - V_{thn}$ and β=1 the logical threshold voltage becomes $V_{DD}/2$. As can be seen in equation 1 depending on β the logic threshold V_{LT} can be moved up and down. Thus, it can be adjusted within some range between ground and the supply V_{DD}. The details on how to build the respective comparators is given in [9].

3. Window shift due to Lot-to-lot Variation

The applicability of the comparator concept depends on the variation of the two properties of the comparator window: a) the window width and b) the window position. Both depend on the ambient temperature and the lot-to-lot variation of the technology. During the circuit design those impacts are addressed within the process of the so-called circuit characterisation. This can either performed by Monte-Carlo simulations or by worst case simulations assuming corner lots. The impact of the ambient temperature is covered by temperature sweep simulations, e.g between -

40°C and +130°C. As shown in the previous investigations [7, 8] the impact of the actual ambient temperature can be neglected whereas the lot-to-lot variation of the threshold voltages of the NMOS and PMOS showed significant impact. In fig. 2 the result of the characterisation for an example comparator is depicted. Four corners and the typical case have been simulated characterised by the speed of the transistors:

1 NMOS fast PMOS fast
2 NMOS fast PMOS slow
3 NMOS slow PMOS fast
4 NMOS slow PMOS slow
5 NMOS typical PMOS typical

As can be seen from fig.2 the combinations 2 and 3 are the critical ones, as in those cases the windows move out of the common overlap region marked by the left and right straight lines. The centre line indicates the DC level of the assumed node under test. Note, that this simulation also shows the temperature impact (-50°C and +150°C). As can be seen the position of the window is not affected, but the width. The amount of the window shift depends on the lot-to-lot variation and is a technology depend parameter. Therefore only the characterisation data can identify whether or not this is a problem for the application of the window comparator. The target of this paper is to investigate the possibilities to stabilise the window position if the window can move outside the overlap region. Two problems have to be solved. First, to detect that the position of the window has moved for an actual lot and secondly to compensate this window shift. Both problems are addressed under the condition to keep the increase in the complexity of the implementation as low as possible.

The main contributor for the lot-to-lot variation is the threshold voltage of the PMOS and NMOS (cf. eq. 1). The variation of the oxide thickness across the die and across different lots can be neglected in comparison with the threshold variation. In general the matching of the aspect ratios is also quite accurate and can also be considered as less important (eq. 2). The impact of the mobilities $\mu_{n.p}$ can be considered as a second order effect, which only impacts the βs if the μ's are deviating in opposite directions.

With respect to the lot-to-lot variation of the threshold voltages two cases have been investigated. The threshold voltages of the PMOS and NMOS move:

a) both by the same percentage but opposite directions, i.e. V_{thp} becomes smaller and V_{thn} larger by the same amount

b) by the same percentage in the same direction, i.e. V_{thp} and V_{thn} become larger by the same amount.

Those conditions can be considered as worst case conditions. From equation 1 it can easily be seen, that for β close to 1 the impact in case a) is almost cancelled out since always $V_{thp} = - V_{thn}$ is valid. However, if the deviations occur as described in case b) this is not true anymore. If in equation1 β is increased, V_{LT} tends towards V_{thn}, while for small values of β the logical threshold tends towards $V_{DD}- |V_{thp}|$. Thus, any deviation in the threshold voltages directly impacts the logical threshold of the comparator in either case a) and b). Case b), however, constitutes the worst case of the two, since already for $\beta=1$ the V_{LT} shifts by the difference of the threshold voltages $|V_{thp}| - V_{thn}$ if they do not match. Simulations showed that within the considered range of βs and for the maximum mismatch of $\pm$ 30% between the threshold voltages, the maximum relative error for the NAND mounts to ±19.4% whereas for the NOR it amounts to 13,2%.

4. Window Repositioning

As shown in the previous characterization of the comparator in fig. 2 the position of the comparator window can shift even outside the overlap region. However, in order to keep the comparator operation reliable this shift due to the lot-lot variation has to be compensated. This can be achieved by modifying the comparator configuration accordingly. This technique will be described in this paragraph.

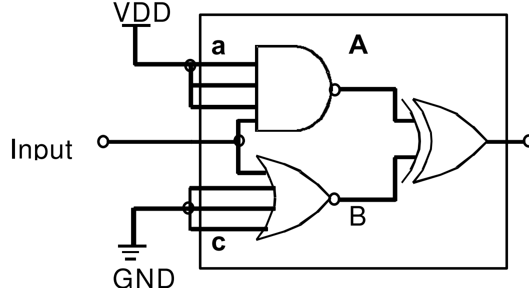

Fig. 3 Comparator configuration for typical technology

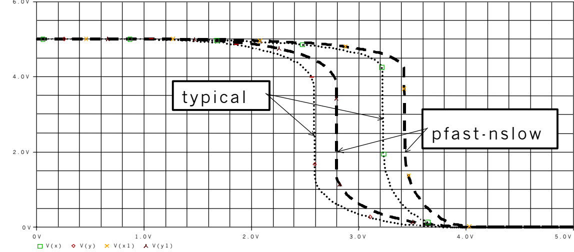

Fig. 4 Observation window shift due to PMOS fast-(pfast) NMOS slow (nslow)variation.

In fig. 3 a digital window comparator is shown. The configuration is assumed to be the one that matches the window of 600mV exactly around the DC signal of 2,9V in case of a typical technology with typical values of the V_{thp} and V_{thn}. The respective window is shown in fig. 4 (typical). If for the same comparator configuration a corner lot with

PMOS_fast-NMOS_slow occurs (pfast-nslow) the window is shifted by 200mV in this case. Note, that in this case there is still an overlap region, which confirms that a characterization is required to verify the amount of window shift.

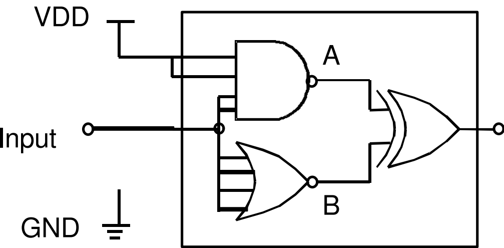

Fig. 5 The comparator of fig. 3 in a different configuration chosen to reposition the window in case of “pfast-nslow”.

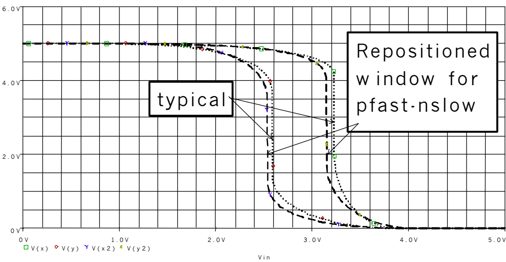

Fig.6 The effect of the configuration shown in fig.3: the window is now positioned in the overlapping region of the window for typical parameters

To reposition the window, the actual comparator configuration can be changed such, that in case of this corner lot the window is again centered around the DC signal of 2,9V. In fig. 5 the respective configuration is depicted. Note, that the configuration of the inputs have been changed for both, the NAND and the NOR. After the change of the configuration now the window has been repositioned and is again centered around 2,9V. Thus, if the lot is typical the configuration in fig. 3 has to be used. If, however, the particular lot is a corner lot of “pfast-nslow” the configuration must be changed to the one depicted in fig. 5. As has been described in [7,8] there are different configurations possible to achieve the same result and it is up to the designer which configuration to choose. The same technique can be employed to reposition the window for the corner lot condition “pslow-nfast”. One effect that has to be considered is the impact of the window width which can be affected depending on the chosen configuration. Beside the possibility to change the comparator configuration the logic gates themselves can be modified by changing the aspect ratio of the NMOS and/or PMOS.

Whether or not the window has to be repositioned depends on the actual lot and the amount by which the window is shifted. As long as the shift is tolerable no repositioning is required. The decision can be made based upon the characterization result. In general the first attempt is to find a different comparator configuration. Only if no satisfying configuration is found a modification of the aspect ratios of the NMOS and PMOS transistors of the logic gates should be considered, since the target is to used gates from a standard library. Another reason to modify the aspect ratio instead of using another comparator configuration can arise from the impact of the configuration on the window width.

5. Implementation of the Repositioning concept into a DfT scheme

In the previous paragraph the problem of the lot dependent repositioning of the window has been solved. However, the problem to identify the actual lot condition was not yet addressed. This paragraph will describe the implementation concept.

For the implementation three problems have to be solved:

1 identifying the actual lot condition
2 applying the respective comparator configuration
3 automatic on-chip selection of the right configuration

Since the actual lot condition can not be known up-front, it is not possible to implement the right comparator configuration. Thus, in the first step the actual lot condition must be detected. Before the different component of will described, the concept will be outlined. The basic idea is to implement a special comparator that detects the lot condition by an automatic on-chip measurement. This reference comparator then generates three control signals for the conditions “nfast-pslow”, “typical” and “nslow-pfast”. Those control signals are used to automatically select the right comparator configuration of the actual signal evaluation comparators. In general the configuration for the evaluation comparators could be selected by a multiplexer network (block C in fig. 1). This however, would involve switches in the signal path that could interfere with the signal under observation. Therefore this paper proposes another solution where three comparators are implemented. Each comparator configuration is chosen such that its window is centred around the signal under evaluation under one of the three lot conditions. Once the lot condition is detected, the respective evaluation comparator configuration is chosen and connected to an EXOR-tree or scan-path. The implementation of the different components is described in the following in detail.

6. Automatic lot condition detection

One solution to perform an on-chip lot condition detection is the implementation of special comparator which is connected to a on-chip reference or via an available or

multiplexed pin to an external reference supplied by the automatic test equipment (ATE).

As long as the actual pin count of the package is not exhausted this solution should be preferred. The on-chip reference should not be linked to the same technology step from which the threshold voltages of the logic gates are depending. For example a band-gap voltage or a simple resistive divider could be used.

The reference comparator comprises basically of three window comparators The principle is depicted in fig. 7. It basically operates like the window comparator in fig.1 and can be easily understood if the NANDs and NOR are replaced by simple inverters with different logical thresholds, whereas the NOR at the bottom (nfast-pslow) exhibits the lowest logical threshold and the NAND at the top exhibits the highest logical threshold (nslow-pfast). To identify whether the lot is a corner lot the typical signal level is applied (externally or internally). If the lot is typical then the NAND and the NOR of the bottom comparator are zero and the output C1 is also zero. The EXOR output of the "typical" comparator (B1) is one since the applied reference level falls into the window of this comparator, i.e. the level is between

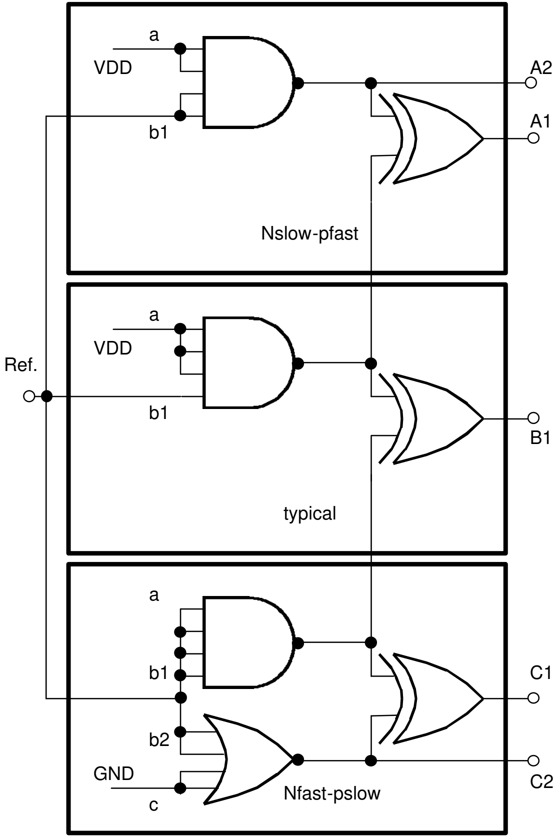

Fig. 7 Reference comparator for automatic lot condition detection

the logical threshold of the bottom NAND and the NAND of the typical comparator. Since the reference level in case of a typical lot is below the "nslow-pfast" comparator this output (A1) is zero. If however the lot is either "nslow-pfast" or "nfast-pslow" this is indicated by A1=1 or C1=1. The outputs A2 and C2 are optional to indicate whether the lot is even outside the worst case corners and could be included in a scan-path to flag this condition to the ATE. The control signals A1 – B1 – C1 can now be used to select the right comparator configurations of the other window comparators of the IC. Note, that only one reference comparator is needed.

7. Evaluation comparators

The evaluation comparators (fig. 8) consist of actually three comparators with different configurations. Each configuration is chosen such, that the window of one comparator is centred around the signal under evaluation, i.e. depending from the lot condition "nfast-pslow, typ, nslow-pfast". Each single comparator resembles a copy of the comparator as shown in fig.1.

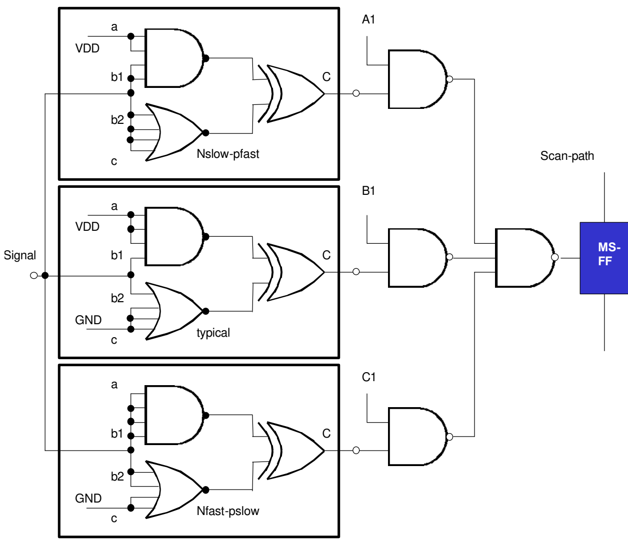

Fig. 8 Evaluation comparator with selection logic for different corner lot conditions without diagnosis function

Via the control signals A1-C1 one of the comparator configurations is connected via the selection logic to a master-slave flip-flop which can be part of a scan path chain. Note, that the selection of the right comparator configuration is done automatically via the reference comparator as shown in fig. 7. The schematic shown in fig. 8 depicts an evaluation comparator without diagnosis function, i.e. it only indicates whether the evaluated signal is within or outside the window. With a modification however, an additional diagnosis is possible. The modified evaluation comparator is shown in fig. 9.

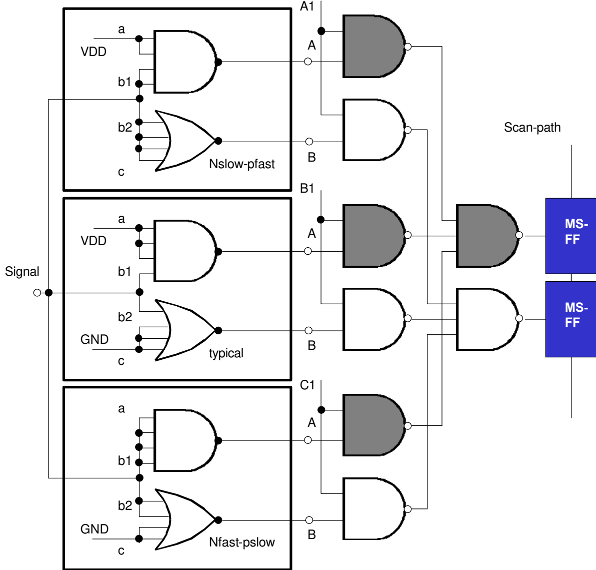

Fig. 9 Evaluation comparator with selection logic for different corner lot conditions with diagnosis function

In this implementation version the EXORs can be omitted as the outputs of the NANDs and NORs are directly evaluated. As has been described in [6, 7] in this configuration both outputs A and B are available and depending on the values the signal level can be diagnosed to be either inside the comparator window, or beyond or below. In this implementation the selection logic and the master-slave flip-flop (MS-FF) are duplicated which is compensated by the saving of the three EXORs.

8. Test Procedure

If the reference comparator is accessible via an available or multiplexed pin the reference comparator can be tested for stuck-at failures. This is performed during the pre-test phase. During this phase a test signal is to be assign to the comparator input. In fig. 10-11 an example is shown. In this particular case a piece wise constant signal is applied at the reference input and then the different test response can be observed if the reference comparator is included in the scan-path or when connected to an EXOR-tree. The test responses depend on the technological condition. In fig. 10 the test response for a typical lot is shown, in fig. 11 for a corner lot "pslow-nfast" and in fig. 12 for a corner lot "pfast-nslow". Three phases can be distinguished. First signal part corresponds to a "nfast-pslow" lot condition, the second phase the input signal is zero and all comparator outputs are zero as well. Finally the third phase corresponds to a "nslow-pfast" condition. Sampling the output signals at a suitable frequency different patterns will be detect which in turn will enable the detection of the lot condition as well as the comparator configuration to be selected for the particular technological situation. Table 1 summarises what can be seen already from the fig. 10-12. It shows in fact the resulting pattern at the output of the comparator when the sampling signal centres each of the levels imposed at the input by the test signal chosen. In this table, the sequence "000" at the EXOR outputs of the single evaluation comparator cell detects the respective technology condition. Thus, if at one comparator output the pattern "000" appears in turn also the actual technology condition is known through this kind of test. Note, that this is a synergy effect that provides additional information about the particular lot.

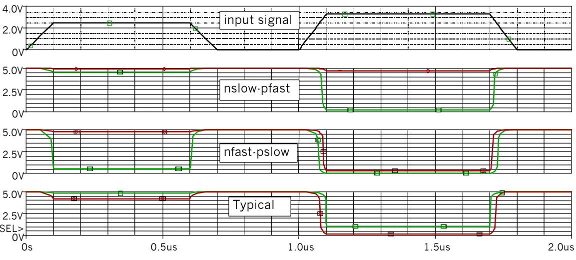

Fig. 10 Test response for typical lot condition

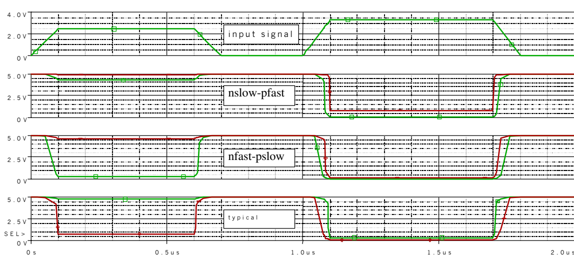

Fig. 11 Test response for pslow-nfast lot condition

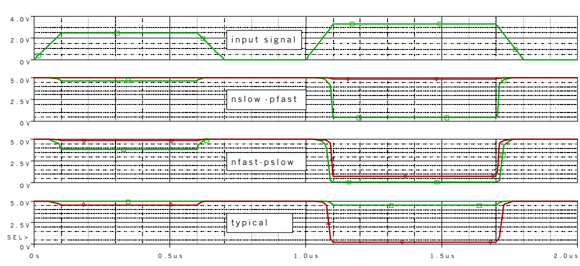

Fig. 12 Test response for pfast-nslow lot condition

Tab. 1 logical responses of evaluation comparators to test input

EXOR OUTPUT	Typical lot			pslow-nfast lot			nslow-pfast lot		
typ	0	0	0	1	0	0	0	0	1
nfast-pslow	1	0	0	1	0	0	0	0	0
nslow-pfast	0	0	1	0	0	0	0	0	1

In order to bring the test result both from the reference comparator as well as from the evaluation comparators at least one output pin must be available. This pin can be a

multiplexed digital pin. If an input pin is available the test as described above can be performed. This pin however, must be an analogue input pin, which could also be multiplexed. The read-out of the test responses can either be done via an EXOR-tree or via a scan-path. For each evaluation comparator one master-slave flip-flop is required if no signal level diagnosis is required. If the diagnosis is requested two MS-FFs are necessary. In the latter case the EXORs for each of the comparators can be omitted.

Currently the whole implementation concept is under refinement to further same gates and make the implementation more robust and more efficient.

9. Conclusion

A simple DfT-scheme for mixed-signal ICs is described that uses digital window comparators to observe the DC levels on analogue circuit nodes. Two comparators have been described: a reference comparator to detect the lot condition and to automatically select on-chip the correct configuration of evaluation comparators and secondly an adaptive evaluation comparator scheme. The latter one comprises of three different configurations of digital window comparators. Each is designed to fit the signal under evaluation for an actual corner lot condition. Via three internally and automatically generated control signals the actual evaluation comparator can be selected. The evaluation comparators can either be used with or without diagnosis capability to detect the range of the signal under evaluation. To bring the test result off-chip one digital pin is required that can also be multiplexed if no digital pin is available. The comparator outputs can be connected to an EXOR-tree or included in a scan-path. In case of required diagnosis two master-slave flip-flops are required per evaluation comparator. Is no diagnosis required one master-slave flip-flop is sufficient. If the output of the reference comparator is also included in the EXOR-tree or scan-path the lot condition can be brought off-chip and thus, can be stored in the result file of the automated test equipment for later tractability. For the implementation of the comparator and the selection logic only few digital standard or dedicated logic gates are required. It was shown that the limitations from the lot-to-lot variation of the threshold voltages of the P- and NMOS can be overcome. The described technique allows to reposition the comparator window to match the signal under investigation also in the presence of window shifts due to lot-to-lot variation. The solutions are based on the possibility to shift the observation window of the comparator by changing the inputs connections or by modifying the aspect ratios of the NMOS and/or PMOS transistors. In particular the ability to compensate the threshold variations of the NMOS and PMOS in case of deviations in opposite directions i.e. the condition pfast-nslow, nslow-pfast has been investigated. It was shown that during the pre-test phase the actual lot condition can be identified.

Currently the implementation concept is under refinement to achieve increased robustness and lower gate count for the implementation.

10. References

[1] C. Metra, M. Favalli, P. Olivo, B. Riccò " On-line Detection of Bridging and Delay Faults in Functional Blocks of CMOS Self-Checking Circuits}, IEEE Trans. on Computer Aided Design, vol. 16, p.770, 1997.

[2] V. Kolarik, S. Mir, M. Lubaszewski and B. Courtois. Analogue checkers with absolute and relative tolerances. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 14(5):607-612, May 1995.

[3] K. Loftstrom, "Early Capture for Boundary Scan Timing Measurements", proc. ITC, pp. 417-422, 1996 and Systems, 14(5):607-612, May 1995.

[4] R. D. Adams, E. S. Cooley, P. R. Hansen, "A Self-Test Circuit for Evaluating Memory Sense-Amplifier Signals", proc. ITC, pp.217-225,

[5] D. De Venuto, M. J. Ohletz, "Bias-Programmable Hardware Reconfiguration for On-Chip Test Response Evaluation", IEEE proc. IMSTW 2000, June 21-23, Montpellier, France pp. 58-63, 2000.

[6] D. De Venuto, M.J. Ohletz: On-chip test for Mixed-signal ASICs using two-mode comparators with bias-programmable reference voltages, on Journal of Electronic Testing (JETTA) vol. 17 n. 3/4, June/August 2001, pp. 243-253, Kluwer Academic Publisher USA..

[7] D. De Venuto, M. J. Ohletz, B. Riccò, " On-Chip Signal Level Evaluation for Mixed-Signal ICs using Digital Window Comparators", Proc. IEEE ETW01, 29 May - 1 June 2001, Stockholm, Sweden, pp. 175-179, 2001.

[8] D. De Venuto, M. Ohletz, B. Riccò: Digital window comparator for mixed-signal IC's design for testability, on Journal of Electronic Testing (JETTA) January vol. 18 n.2, April 2002 , pp.121-128, Kluwer Academic Publisher USA.

[9] D. De Venuto, M. J. Ohletz, B. Riccò, " Testing of Analogue Circuits via (Standard) Digital Gates", Proc. of IEEE 3rd International Symposium on Quality Electronic Design (ISQED 2002), pp.112-119, March 18 – 20, 2002 San Jose, CA, USA

[10] N. H. E. Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Addison-Wesley Publishing Company, ISBN 0-201-53376-6, pp. 61-69, 1994.