SCISPACE
formerly Typeset

Open access • Journal Article • DOI:10.1109/LPEL.2004.839638

Avalanche behavior of low-voltage power MOSFETs — Source link

Cyril Buttay, T.B. Salah, Dominique Bergogne, Bruno Allard ...+2 more authors

Published on: 22 Nov 2004 - IEEE Power Electronics Letters (IEEE)

Topics: Avalanche breakdown, Avalanche diode, Single-photon avalanche diode, Zener diode and Avalanche photodiode

Related papers:

- Temperature Sensing for Power MOSFETs in Short-Duration Avalanche Mode
- Paralleling of low-voltage MOSFETs operating in avalanche conditions
- Safety drain voltage avoiding avalanche breakdown in MOSFET
- The Impact of Repetitive Unclamped Inductive Switching on the Electrical Parameters of Low-Voltage Trench Power nMOSFETs
- High current repetitive avalanche of low voltage trench power MOSFETs

Share this paper:

View more about this paper here: https://typeset.io/papers/avalanche-behavior-of-low-voltage-power-mosfets-3kucjwaozi

Avalanche Behavior of Low-Voltage Power MOSFETs

Cyril Buttay, Tarek Ben Salah, Dominique Bergogne, Bruno Allard, Hervé Morel, Jean-Pierre Chante

▶ **To cite this version:**

Cyril Buttay, Tarek Ben Salah, Dominique Bergogne, Bruno Allard, Hervé Morel, et al.. Avalanche Behavior of Low-Voltage Power MOSFETs. IEEE Power Electronics Letters, Institute of Electrical and Electronics Engineers, 2004, 2 (3), pp.104-107. 10.1109/LPEL.2004.839638 . hal-00138863

HAL Id: hal-00138863

https://hal.archives-ouvertes.fr/hal-00138863

Submitted on 28 Mar 2007

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Avalanche Behavior of Low-Voltage Power MOSFETs

Cyril Buttay, *Student Member, IEEE*, Tarek Ben Salah, Dominique Bergogne, Bruno Allard, *Senior Member, IEEE*, Hervé Morel, *Member, IEEE*, and Jean-Pierre Chante

***Abstract*—This letter addresses the behavior of low voltage power MOSFETs under avalanche, with a paralleling point of view. It is shown that during avalanche, up-to-date technology MOSFET transistors exhibit a resistance far in excess of their on-state resistance ($R_{\mathrm{DS_{on}}}$). A novel test setup is proposed to measure "avalanche" resistance. A simple model of breakdown voltage is then proposed. It becomes possible to perform fast simulations using this model to study current balance between paralleled transistors under avalanche operation. It is shown that considering avalanche resistance reduces the influence of breakdown voltage mismatches and allows for better current sharing.**

***Index Terms*—Avalanche, avalanche resistance, electrothermal model, low-voltage MOSFET, temperature estimation.**

I. Introduction

LOW-VOLTAGE MOSFET transistors have become devices of choice in automotive applications. Their low on-resistance ($R_{\mathrm{DS_{on}}}$) allows high current operation while keeping efficiency at a high level. Dramatic improvements of $R_{\mathrm{DS_{on}}}$ for low voltage transistors (<50 V) have been permitted by increasing cell density up to several million per square inch [1]. This was made possible by modifying the classical vertically doubly diffused (VD)MOS cell layout.

In some applications, such as integrated starter alternator (ISA), MOSFETs have to be paralleled to supply higher current (up to several hundred amperes). In order to keep $R_{\mathrm{DS_{on}}}$ low, transistors are selected with the lowest breakdown voltage rating available (typically 20-V devices for 14-V applications) as V_{BR} and $R_{\mathrm{DS_{on}}}$ are closely related [2]. This choice leads to avalanche operation of the body diode at each commutation.

In ISA applications (constituted by a reversible alternator connected to an inverter feeding a battery), the inverter has to protect the electrical network of the vehicle from voltage surges during spurious battery disconnection, while the alternator is delivering high current [3] (Load-dump condition). Due to intrinsic instability of low-voltage power MOSFETs in a saturated region [4], the only way to clamp alternator output voltage is to use low breakdown voltage transistors. Body diodes of the transistors will therefore have to sustain avalanche during several hundreds of milliseconds, until demagnetization of the alternator [5]. The avalanche operation of the body diode remains nondestructive, given adequate thermal conditions.

Manuscript received July 24, 2004, revised October 22, 2004. Recommended by Associate Editor P. L. Chapman..

The authors are with the CEGELY INSA de Lyon, 69621 Villeurbanne, France (e-mail: cyril.buttay@insa-lyon.fr).

Digital Object Identifier 10.1109/LPEL.2004.839638

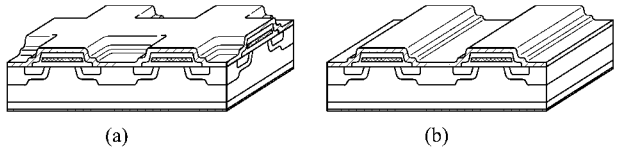

Fig. 1. (a) Cellular layout. (b) Strip layout.

Unfortunately, manufacturers cannot ensure tight tolerances on breakdown voltage, due to process dispersions. One can notice V_{BR} dispersions of several Volts between two 20 V rated devices of the same reference. Avalanche breakdown voltage is a well known temperature sensitive parameter that increases when the transistor heats. It is, therefore, usually considered that paralleled MOSFETs—even with unmatched V_{BR}—will reach an equilibrium where the transistor with the lowest avalanche voltage conducts first, then self-heats, increasing its V_{BR} up to the V_{BR} of the remaining MOSFETs [6]. Current balance between paralleled MOSFET transistors is therefore, supposed to be satisfied, with differences in V_{BR} resulting only in a different transistor temperature equilibrium.

However, as thermal transients are relatively slow (some tens to hundreds of microseconds to heat the active area of a transistor, depending on avalanche power level), it can be suspected that only one single transistor will carry all the current during this period. Furthermore, when equilibrium is reached (after up to several hundreds of microseconds from beginning of avalanche), high V_{BR} unmatching between transistors could result in high differences (several tens of Celsius degrees) in transistor temperatures. The MOSFET with the lowest V_{BR} is therefore, suspected to be more stressed during *and* after transient.

In the first part of this letter, specifics of low-voltage power MOSFETs are recalled. An experimental setup is proposed to show that the avalanche breakdown voltage is both temperature- and current-dependent. A very simple electrothermal model is then proposed for circuit simulation and for paralleling optimization purpose.

II. Low Voltage MOSFET Structures

The main direction for reducing $R_{\mathrm{DS_{on}}}$ of low-voltage MOSFETs is the improvement of the channel density [2]. Although cellular design [Fig. 1(a)] (whatever is the cell shape) allows for better channel density than strip layout [Fig. 1(b)], the shrinking is limited by process tolerances. At very small cell dimensions (some micrometers), it becomes impossible to ensure opening of windows in the polysilicon area [7]. Strip design is more robust

1540-7985/04$20.00 © 2004 IEEE

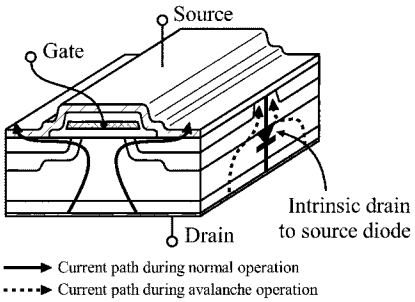

Fig. 2. STMicroelectronics StripFET MOS structure [8].

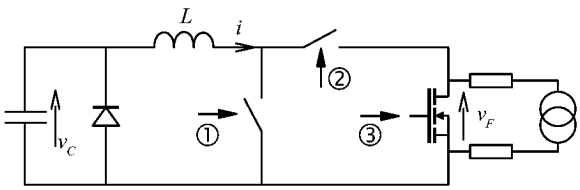

Fig. 3. Test setup allowing temperature profile measurement.

and overcomes previous limitations. Smaller geometries therefore become possible, resulting in a higher channel density. The experimental results presented thereafter are related to MOSFETs of the latter technology.

This letter addresses experimental issues involving the MOSFET transistor structure depicted in Fig. 2.

III. Experiment

The aim of the proposed testbench is to measure chip temperature of a power MOSFET during avalanche. Once the temperature transient is recorded, it is compared to drain-to-source voltage (equal to $V_{\rm BR}$) and drain current waveforms. To measure chip temperature with acceptable time accuracy, a thermal sensitive parameter of the transistor is used: the body-diode forward voltage [9]. As monitoring of this parameter requires disconnection of drain and source terminals of the MOSFET, the complete temperature curve is obtained by successive acquisitions, with increasing pulse length.

A. Measurement Setup

A specific measurement setup, enabling temperature measurement by means of body-diode forward-voltage monitoring has been developped and is pictured in Fig. 3.

Typical waveforms are shown in Fig. 4. At the beginning of a measurement cycle (phase 1), the voltage across the capacitance is v_c, and current in the inductor is zero. During the second phase, the inductor L is charged by turning on switch 1, forcing v_c to decrease to zero. At this point (phase 3), the current in L is maximum and switch 1 is opened (switches 1 and 2 were closed the instant before). Therefore, the current flows through switch 3, which is the device under test (DUT). Some microseconds later (short enough for self-heating to be negligible) the DUT is turned-off, triggering the avalanche operation. As switch 1 has a higher $V_{\rm BR}$ rating, avalanche occurs in the DUT (phase 4). After an arbitrary delay, switch 1 is closed again to change the inductor current, then switch 2 is opened to isolate the DUT

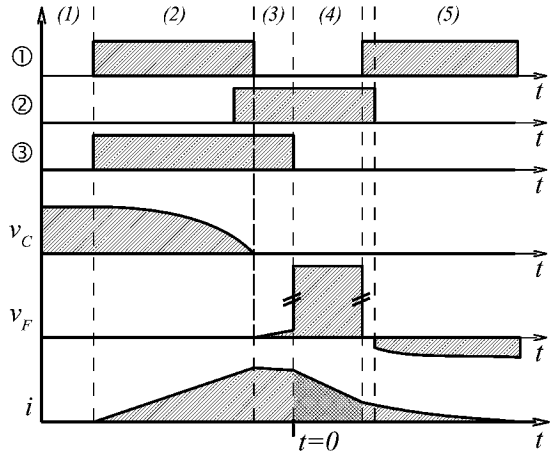

Fig. 4. Waveforms in the test setup.

(phase 5). Temperature is obtained by forward biasing the intrinsic body diode of the MOSFET under a low-value current and measuring the voltage drop V_F. The complete temperature curve is obtained by varying successively the duration of phase 4.

B. Results

The drain current and the drain-to-source voltage during avalanche for a 20 V, 120 A-rated *STMicroelectronics* MOSFET are plotted in Figs. 5(a), and (b). Their "sliced look" is due to the superposition of successive acquisitions where avalanche phase duration is increased (phase 4 in Fig. 4). At the end of each acquisition, the body-diode forward-voltage is recorded, and plotted in Fig. 5(c).

Prior to avalanche measurement, the body-diode forward-voltage has been calibrated with respect to temperature ($V_F[V] = -0.729 + 0.0019 \cdot T[^\circ\mathrm{C}]$). It is therefore, simple to work out temperature from V_F measurements in Fig. 5(c). Extrapolations have been performed to determine the V_F value at the exact end point of avalanche pulse (there is a 20 microseconds dead-time between end-of-avalanche and the beginning of the V_F measurement). The temperature transient is plotted in Fig. 6.

One interesting fact is that the peak temperature and the drain-to-source peak voltage are not reached concurrently [repectively, at $t = 400\ \mu$s for peak temperature in Fig. 6 and at $t = 150\ \mu$s for peak drain-to-source voltage in Fig. 5(b)]. This shows that $V_{\rm DS}$ is not related only to the die temperature. Furthermore, $V_{\rm DS}$ is higher at the beginning of the current pulse (where the chip temperature is as low as 30°C, and the drain current is more than 100 Amps) than at the end of the current pulse (the temperature is then almost 100°C, but the current is near zero). This demonstrates a resistive behavior during avalanche.

IV. Simple Behavioral Model

A simple approximation of $V_{\rm BR}$ with temperature is the following linear relation:

$$V_{\rm BR}(T) = V_{\rm BR_0} + \beta T \tag{1}$$

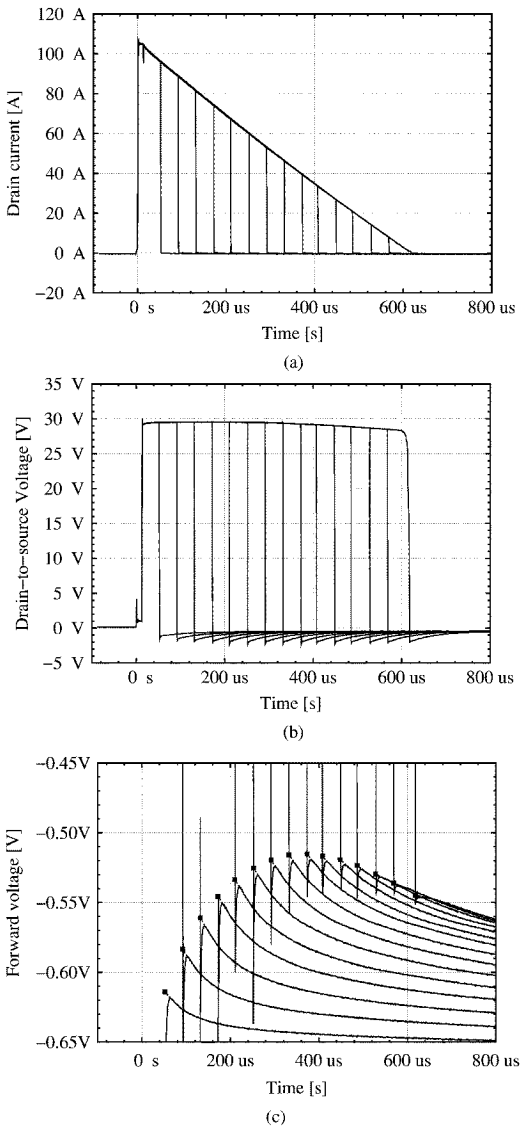

Fig. 5. (a) Experimental drain current and (b) drain-to-source voltage during avalanche for various widths of avalanche pulse. (c) Experimental drain-to-source voltage when the body diode is forward-biased after the avalanche pulse, for various pulse widths; dots are extrapolated values at the end of the corresponding pulse. The time origin is the same as in Fig. 4.

where T is the transistor temperature (in Celsius degrees), V_{BR_0} is the 0°C breakdown voltage, and β reflects temperature dependence of $V_{\mathrm{BR}}(\mathrm{V}{\cdot}^{\circ}\mathrm{C}^{-1})$. A simple electro-thermal model for avalanche behavior may be extrapolated

$$V_{\mathrm{BR}}(T, I_D) = V_{\mathrm{BR}_0} + \beta T + R_{\mathrm{BR}} I_D. \tag{2}$$

R_{BR} being a so-called avalanche resistance (Ω). It can be seen on Fig. 2 that current paths differ between normal and avalanche operation. Therefore, R_{BR} is not expected to have the same value as $R_{\mathrm{DS_{on}}}$.

Identification of the model parameters is carried out with the breakdown voltage waveform shown in Fig. 5(b). The breakdown voltage transient is computed using (2) and the recorded values of I_D (Fig. 5(a)) and T (Fig. 6). R_{BR_0}, β and R_{BR} are chosen so as to minimize the difference between recorded and calculated V_{DS}. The comparison is plotted in Fig. 7.

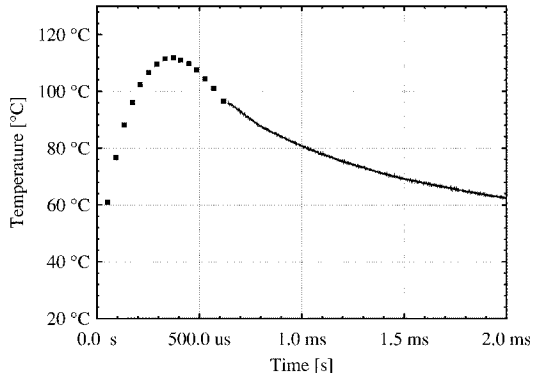

Fig. 6. Temperature profile of the transistor during (dots) and after (plain) avalanche.

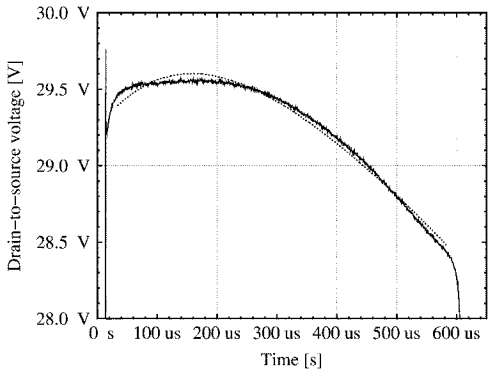

Fig. 7. Comparison of measured (plain) and simulated (dots) drain-to-source voltage during avalanche.

TABLE I
MODEL PARAMETERS FOR STRIP FET STB210NF ($R_{\mathrm{DS_{on}}} = 2,6\ \mathrm{m}\Omega$)

Parameter	Value
V_{BR_0}	27.3 V
V_{BR_1}	14 $mV.K^{-1}$
R_{BR}	12 $m\Omega$

Parameter values are given in Table I. The R_{BR} value (12 mΩ) has to be compared to $R_{\mathrm{DS_{on}}}$ of the MOSFET (2.6 mΩ) and the dynamic resistance of the body diode (1.5 mΩ). During avalanche, the transistor exhibits a resistive behavior that is far in excess with respect to these latter resistances. The higher resistance is probably due to the small contact area of the body diode metallization (see Fig. 2), but this assumption has to be validated. A similar resistive behavior has also be noticed on trench MOSFETs.

V. CONCLUSION

One result detailed in this paper is that low-voltage MOSFETs exhibit a resistive behavior during avalanche that is far in excess of the quoted $R_{\mathrm{DS_{on}}}$. This has been verified experimentally. This so-called avalanche resistance has no detrimental effect *a priori*, since the transistor power losses during avalanche are limited by the external circuit (stray inductances energy or alternator magnetic energy).

Another result concerns the paralleling of MOSFET transistors. A better current balance between the paralleled devices is also reached through this avalanche resistive behavior. An estimation of current sharing inside a parallel assembly when neglecting the avalanche resistance would predict the largest current for the MOSFET transistor with the lowest breakdown voltage. Then temperature would alone moderate the current unbalance in favor of the MOSFET transistors with larger breakdown voltages. When considering the avalanche resistance, the estimation of current sharing inside a parallel assembly would predict a less pessimistic current unbalance, due to the resistive voltage drop effect.

An electrothermal model (2) has been presented that shows good agreement with measurements. The model is intended to be implemented in a classical MOSFET transistor model instead of using the existing breakdown voltage expression. Then it becomes possible to simulate the maximum junction temperature and the current sharing of paralleled transistors during avalanche by performing worst case simulations to account for devices V_{BR} dispersions. Such a model has been successfully implemented into Pspice and gives good agreement with experimental data.

REFERENCES

[1] R. Ferret, P. Aloïsi, D. Chatroux, D. Lafore, J.-M. Li, M.-L. Locatelli, D. Planson, B. Rivet, and J.-L. Schanen, *Interrupteurs électroniques de puissance*. Paris, France: Lavoisier, 2003.

[2] B. J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS-Kent, 1996.

[3] T. Efland, M. Manternach, A. Marshall, and J. Mings, "The load dump," in *Conf. Rec. IEEE Workshop Electronics Applications Transportation*, 1990, pp. 73–78.

[4] A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor, and A. Magrì, "Thermal instability of low voltage power-mosfet's," *IEEE Trans. Power Electron.*, vol. 15, pp. 575–581, May 2000.

[5] C. S. Namuduri, B. V. Murty, and M. G. Reynolds, "Load dump transient control of a 42 v automotive generator," in *Conf. Rec. IEEE Power Electronics Specialists*, Aachen, Germany, June 2004, pp. 389–394.

[6] J. Chen, S. Downer, A. Murray, and D. Divins, "Analysis of avalanche behavior for paralleled mosfets," in *Conf. Rec. SAE*, Detroit, MI, Mar. 8–11, 2004.

[7] G. Belverde, C. Guastella, M. Melito, S. Musumeci, R. Pagano, and A. Raciti, "Advanced characterization of low-voltage power mosfets in synchronous-rectifier buck-converter applications," in *Conf. Rec. 38th IEEE IAS Annu. Meeting*, vol. 3, Denver, CO, Oct. 12–16, 2003, pp. 1802–1809.

[8] S. Musumeci, R. Pagano, A. Raciti, G. Belverde, C. Guastella, and M. Melito, "Low-voltage mosfets with improved performances in advanced dc-dc converter applications," in *Conf. Rec. Eur. Power Electronics*, Toulouse, France, Sept. 2003.

[9] D. L. Blackburn and D. W. Berning, "Power mosfet temperature measurements," in *Conf. Rec. IEEE Power Electronics Specialists*, June 1982, pp. 400–407.