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AUTHOR(S):

Negoro, Y; Miyamoto, N; Kimoto, T; Matsunami, H

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Avalanche Phenomena in 4H–SiC p–n Diodes Fabricated by Aluminum or Boron Implantation

Yuuki Negoro, Nao Miyamoto, Tsunenobu Kimoto, and Hiroyuki Matsunami, *Senior Member, IEEE*

***Abstract*—Characteristics of p–n junction fabricated by aluminum-ion (Al^+) or boron-ion (B^+) implantation and high-dose Al^+-implantation into 4H–SiC (0001) have been investigated. By the combination of high-dose (4×10^{15} cm^{-2}) Al^+ implantation at 500 °C and subsequent annealing at 1700 °C, a minimum sheet resistance of 3.6 kΩ/□ (p-type) has been obtained. Three types of diodes with planar structure were fabricated by employing Al^+ or B^+ implantation. B^+-implanted diodes have shown higher breakdown voltages than Al^+-implanted diodes. A SiC p–n diode fabricated by deep B^+ implantation has exhibited a high breakdown voltage of 2900 V with a low on-resistance of 8.0 mΩcm^2 at room temperature. The diodes fabricated in this study showed positive temperature coefficients of breakdown voltage, meaning avalanche breakdown. The avalanche breakdown is discussed with observation of luminescence.**

***Index Terms*—Avalanche breakdown, ion implantation, p–n diode, SiC, silicon carbide.**

I. Introduction

Silicon carbide (SiC) is an attractive material for high-power, high-temperature, and high-frequency devices because of its superior properties such as wide bandgap, high breakdown field, high thermal conductivity, and high saturation electron drift velocity [1]. These properties have roots in a strong chemical bonding between silicon and carbon. However, it brings difficulties to device processing: for example a relatively high temperature is generally required. Device process technologies in SiC are one of crucial issues to realize high-performance SiC electronic devices. Successful selective doping can be easily made by ion implantation, because the low diffusion coefficients of impurities in SiC [2] make the diffusion process using a SiO_2 mask very difficult. To form selective p-type regions in SiC, aluminum-ion (Al^+) or boron-ion (B^+) implantation is commonly employed. Aluminum is particularly attractive for implantation to form heavily doped p^+-regions with low sheet resistances, because Al acceptors have a smaller ionization energy (190 meV [3] and 240 meV [4]) than B acceptors (285 meV [5] and 300 meV [6]) in 4H– and 6H–SiC, respectively. Whereas the use of boron is much effective for implantation to form deep p–n junctions because of its lighter mass and resulting larger projected ranges.

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The authors are with the Department of Electronic Science and Engineering, Kyoto University, Kyoto 606-8501 Japan.

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In many device applications, low contact resistances between metal electrodes and p-SiC, and localized p-type regions with low resistivities such as the anode of p–n diodes are fundamental requirements. The high-dose implantation of Al^+, however, induces a high density of defects in the implanted regions [7]. To reduce implantation-induced damages, ion implantation at an elevated temperature (hot implantation) [8] and postimplantation annealing at a high temperature, [5], [9] have been used recently. In this point, Al^+ implantation has been a major obstacle in the SiC processing technology, because of its high sheet resistance of 10 kΩ/□ [10]. In addition, it is important to understand the characteristics of p–n junction which controls the performance of various power devices such as p–n diodes and double-implanted MOSFETs (DIMOSFETs) [11], [12]. A positive temperature coefficient of breakdown voltage is one of the most essential requirements for reliable power devices. To our knowledge, only a few reports on this characteristics for SiC high-voltage p–n diodes by implantation have been published [13]. It has not been fully understood how the implants and/or their profiles affect the blocking characteristics.

In this paper, the authors realized a low sheet resistance below 4 kΩ/□ by hot implantation of Al^+. The characteristics of p–n junction diodes were investigated. Clear positive temperature coefficients of breakdown voltage, meaning avalanche breakdown, are demonstrated. Luminescence of the diodes at breakdown is shown and discussed.

II. High-Dose Al^+ Implantation

For the investigation of high-dose Al^+ implantation, nitrogen-doped n-type 4H–SiC epilayers were grown on off-axis 4H–SiC (0001) by chemical vapor deposition [1] in the authors' group. 4H–SiC has been regarded as the most promising SiC polytype, owing to its higher bulk mobility and smaller anisotropy. The net donor concentration of epilayers was 4×10^{15} cm^{-3}. Multiple Al^+ implantation was carried out at either RT or 500 °C to form a 0.25 μm-deep box profile of Al. The implant energies and dose ratios were 180, 120, 80, 30, 10 keV and 0.518, 0.207, 0.150, 0.088, 0.037, respectively. The total implant dose was either 4×10^{15} cm^{-2} or 1×10^{16} cm^{-2}. Post-implantation annealing was performed in a CVD reactor at either 1600 or 1700 °C for 30 min in a pure Ar ambience. The electrical properties of Al^+-implanted regions were characterized by Hall effect measurements using the van der Pauw configuration at room temperature. For ohmic contacts, Al/Ti was evaporated on the surface through a metal mask followed by annealing at 900 °C for 10 min in Ar. To

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avoid leakage current along the sample edges, mesa structures were fabricated by reactive ion etching.

In the case of room-temperature (RT) implantation of Al^+, the sheet resistance takes a minimum value as high as 95 kΩ/□ after annealing at 1700 °C. The minimum sheet resistances of Al^+-implanted layers ever reported were 22 kΩ/□ for RT implantation and 1500 °C-annealing [9], and 10 kΩ/□ for hot implantation and 1650 °C-annealing[10]. In this study, hot implantation at 500 °C has resulted in much lower sheet resistances compared to RT implantation, in good agreement with previous reports. The sheet resistances and electrical activation for Al^+-implanted regions were significantly improved by increasing the annealing temperature up to 1700 °C. A low sheet resistance of 3.6 kΩ/□ has been obtained by implantation at 500 °C followed by 1700 °C-annealing, when the total implant dose was 4×10^{15} cm^{-2}. In the case of 1600 °C annealing, a higher sheet resistance of 10 kΩ/□ has been obtained. Although this sheet resistance of 3.6 kΩ/□ (p-type) is one of the lowest values ever reported, further investigation is required to reduce the sheet resistances.

III. p–n JUNCTION CHARACTERISTICS

Three types of diodes were fabricated by employing Al^+ or B^+ implantation at room temperature. The first group of diodes (“Al^+-implanted diodes”) were fabricated by Al^+ implantation to form a 0.45 μm-deep box profile with an acceptor concentration of 1×10^{18} cm^{-3}. The second group (“B^+-implanted diodes”) has a 0.45 μm-deep B profile with an acceptor concentration of 2×10^{18} cm^{-3}. The last group (“deep B^+-implanted diodes”) was formed by high-energy B^+ implantation, leading to a 0.7 μm-deep B profile with the same acceptor concentration as the second group. All the implantations were carried out into N-doped n-type 4H–SiC epilayers grown on off-axis 4H–SiC (0001) substrates. The donor concentrations of epilayers and substrates were 3.5×10^{15} cm^{-3} and 3.0×10^{18} cm^{-3}, and the thicknesses were 20 μm and 330 μm, respectively. Since RT implantation has an advantage of higher productivity than hot implantation, p–n junctions were formed by Al^+ or B^+ implantation at RT in this study. However, hot implantation is essential to form a heavily doped p^+-region with a low sheet resistance in SiC as mentioned before. Therefore, only the surface p^+-regions for contacts were formed by hot implantation at 400 °C using an Al metal mask for all types of the diodes.

In the diode fabrication, the post-implantation annealing was performed at 1700 °C for 30 min in a pure Ar ambience using a CVD reactor. The surface of the diodes was passivated with 40-nm-thick thermal oxides grown by wet oxidation at 1150 °C for 2 h. Al/Ti and Ni annealed at 800 °C for 10 min were employed for ohmic contacts on the implanted regions and n^+-substrates, respectively. The diameters of diodes were 100–800 μm. The schematic cross section of the diode with a planar structure is shown in Fig. 1 No junction termination extension (JTE) structure was employed in all the diodes.

Fig. 2 demonstrates the current density versus voltage characteristics of Al^+-, B^+-, and deep B^+-implanted diodes. The three types of diodes with a diameter of 100 μm were measured at RT. The forward voltage drops at a current density of 100 A/cm^2 were 3.8–4.7 V. The specific on-resistances determined at 100 A/cm^2 level were 6.3–9.1 mΩcm^2, and typically 8.0 mΩcm^2 for the deep B^+-implanted diodes. These on-resistances include the substrate resistance of 4.1 mΩcm^2, so that, the contact resistances onto the shallow Al^+-implanted p^+-region was roughly estimated to be less than 2.2 (6.3–4.1) mΩcm^2. These results indicate that reasonable ohmic contacts were formed on the p^+-region implanted with Al^+ at an elevated temperature of 400 °C. In addition, the conductivity modulation of n^--epilayers by minority-carrier injection decreases the on-resistances. There was no significant difference in the forward characteristics for all types of diodes. In terms of switching, a typical turn-off time was about 10 ns, showing a fast recovery. Both point and structural defects still remain in the implanted regions, although postimplantation annealing at 1700 °C was employed to remove defects. Hence, the implantation-induced defects remaining in n^--epilayer near the junction act as a lifetime killer for minority carriers, resulting in very fast switching time [13].

One clear difference among the three diodes is a higher breakdown voltage for the deep B^+-implanted diodes. The Al^+-, B^+-,

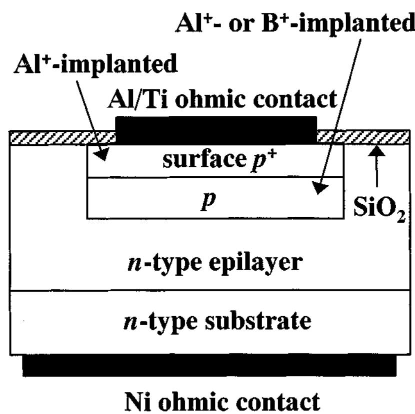

Fig. 1. Schematic cross section of 4H–SiC p–n junction diode fabricated by Al^+- or B^+-implantation into an n–type epilayer. Shallow Al^+-implantation was done to reduce a contact resistance. There is no junction termination extension (JTE) structure in the diode.

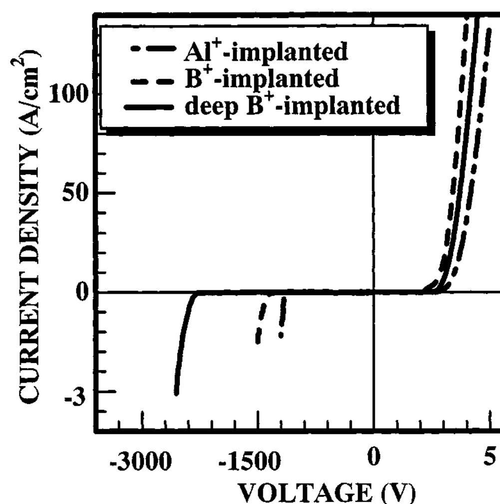

Fig. 2. Current density versus voltage characteristics of Al^+-, B^+-, and deep B^+-implanted diodes at room temperature.

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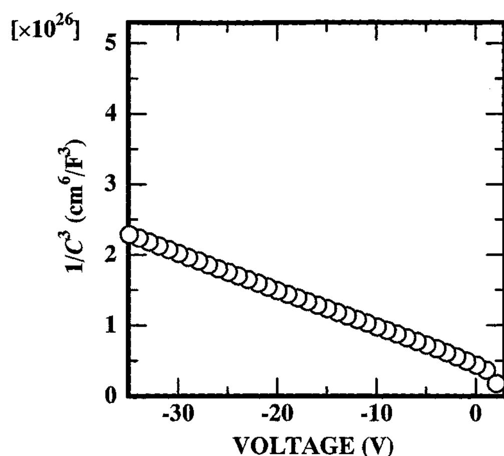

Fig. 3. Capacitance versus voltage characteristics of deep B^+-implanted diodes at room temperature.

and deep B^+-implanted diodes could block 1300, 1500, and 2600 V, respectively. These breakdown voltages are approximately 40, 50, and 80% of the ideal (parallel plane) breakdown voltage (about 3200 V) in this device structure, respectively. All types of diodes exhibited nondestructive breakdown. In particular, the deep B^+-implanted diode did not extend to destructive failure even at a high reverse current density of 3.0 A/cm^2 and a reverse voltage of -2600 V, mainly owing to effective alleviation of electric field crowding at the edge of p-anode.

The alleviation of electric field crowding may be attributed to the following causes. A larger straggle of deeply-implanted B atoms enlarged the curvature at the edge of p–n junction. The diffusion of B atoms in the lateral direction during high-temperature annealing [14] may create a p^--region, which further reduce the electric field crowding. Besides, the thermal oxides grown by wet oxidation generate a high density of negative fixed charges at the oxide/n-SiC interface [15]. The negative charges enhance the extension of a space charge region in the SiC side, leading to "self-junction termination."

Furthermore, the in-diffusion of B atoms during high-temperature annealing [16], [17] broadened the distribution tail of implanted B atoms, forming an intrinsic layer (i-layer) at the junction. Fig. 3 shows the $1/C^3$–V plot of the deep B^+-implanted diode. The thickness of i-layer was estimated to be 1.0–1.5 μm from the capacitance–voltage (C–V) analysis of the diode. Assuming that the capacitance is a series connection of the capacitances of the i-layer and linearly graded junction, the measured C–V data were analyzed with fitting parameters of the i-layer thickness and an impurity gradient. This analysis revealed that a thickness of i-layer of 1.0–1.5 μm well reproduces the measured total capacitance in a wide bias-voltage range. Under the high reverse-bias condition, a voltage of about 200 V may be dropped in the 1.0 μm-thick i-layer.

As described, the deep B^+ implantation and post-implantation annealing create the thicker i-layer near the junction as well as the p^--region due to the lateral diffusion of B atoms, and alleviate electric field crowding at the edge of p–n junction, resulting in the higher and stable breakdown in the case of deep B^+-implanted diodes. In particular, the alleviation of electric field at the edge of p–n junction critically affects the blocking characteristics, as confirmed later.

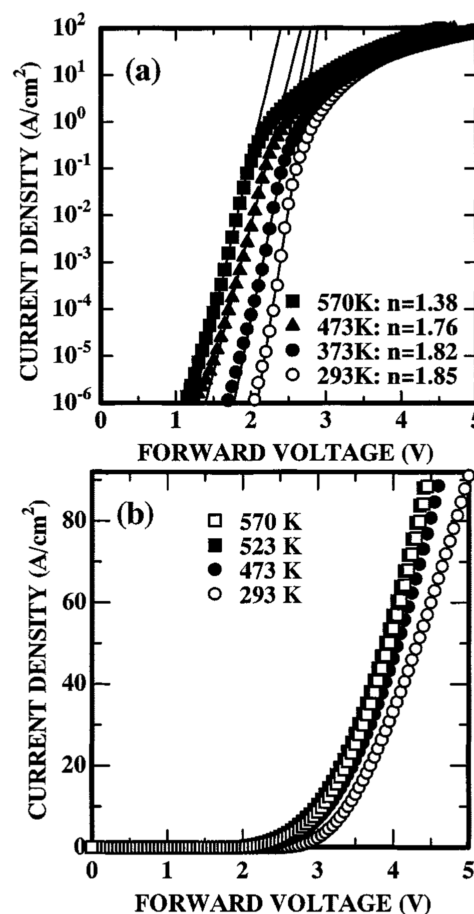

Fig. 4. Forward current density versus voltage characteristics of deep B^+-implanted diode: (a) semi-logarithmic scale and (b) linear scale.

The blocking characteristics had differences between the diodes with larger diameters and smaller diameters. The diodes with larger diameters tended to show lower breakdown voltages, because the larger diodes contain more defects.

Fig. 4(a) denotes the semi-logarithmic forward current density versus voltage characteristics of deep B^+-implanted diodes at different temperatures. The ideality factor (n) is represented at each temperature. The n factor decreases with increasing the temperature, suggesting that the current transport mechanism is dominated by the diffusion of minority carriers as the temperature increases. The diffusion current increases with increasing temperature more than the recombination current. It is because the diffusion current and recombination current are roughly estimated in proportion to n_{i}^2 and n_{i}, respectively, where n_{i} is the intrinsic carrier concentration that increases exponentially with increasing temperature.

The linear forward current density versus voltage characteristics of deep B^+-implanted diodes at different temperatures are demonstrated in Fig. 4(b). A turn-on voltage slightly decreases with increasing temperature. Because the built-in potential, the difference of the conduction band between p- and n-region, becomes lower at the higher temperatures due to the decrease of band gap, and slight shifts of both Fermi levels of p- and n- layers toward the intrinsic level. The on-resistance at 523 K was 35% smaller than that at RT. This result may be attributed to increasing minority-carrier lifetime and longer diffu-

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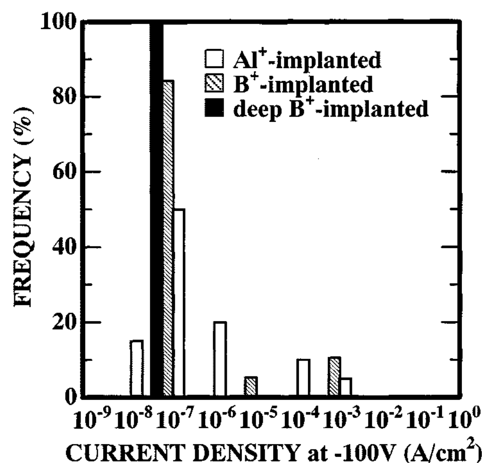

Fig. 5. Histograms of reverse leakage current density at -100 V for Al^+-, B^+-, and deep B^+-implanted diodes.

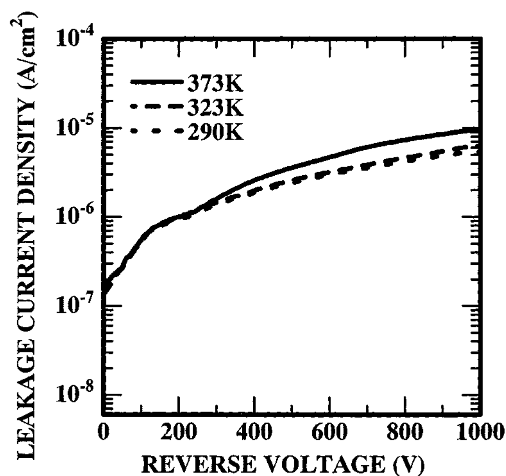

Fig. 6. Reverse leakage current density versus voltage characteristics of deep B^+-implanted diode.

sion length at the high temperatures, which brings more effective conductivity modulation. At 570 K, however, the on-resistance becomes slightly higher than that at 523 K, probably due to the increase of substrate resistance because the electron mobility decreases and the electron concentration is almost constant in this temperature range for n-SiC. These results are very consistent with a previous report [18]. The Al^+-implanted and the B^+-implanted diodes show characteristics similar to the deep B^+-implanted diode in the matter of temperature dependence.

Fig. 5 shows the histograms of reverse leakage current density at a bias voltage of -100 V for Al^+-, B^+-, and deep B^+-implanted diodes at RT. Approximately 20 diodes with a diameter of 100 or 300 μm were measured for each of the three types. In all the types of diodes, the typical reverse leakage current density is in the range of 10^{-7} A/cm^2. In particular, all the deep B^+-implanted diodes measured show a leakage current density of 10^{-7} A/cm^2. In the present measurement system, the lowest limit of measurable current density was 10^{-7}–10^{-8} A/cm^2. The larger straggle and in-diffusion of B atoms cause a lower density of implantation-induced damages for the deep B^+-implanted diodes, resulting in the lower leakage current density.

Fig. 6 shows the reverse leakage current density versus voltage characteristics of the deep B^+-implanted diode at

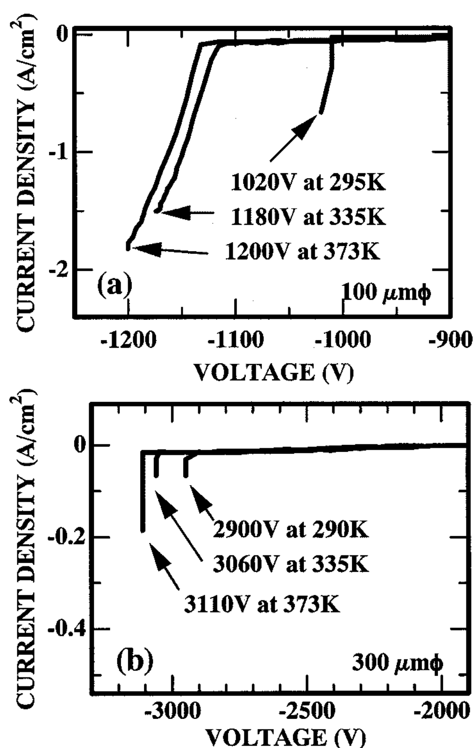

Fig. 7. Reverse blocking characteristics of (a) Al^+- and (b) deep B^+-implanted diodes.

different temperatures. At RT, a low leakage current density of 5×10^{-7} A/cm^2 at -100 V and 7×10^{-6} A/cm^2 at -1000 V has been obtained. With the increase of temperature, the leakage current density increases slightly. At 373 K, however, the leakage current density was still low, 5×10^{-7} A/cm^2 at -100 V and 9×10^{-6} A/cm^2 at -1000 V. This little temperature dependence shows that the leakage current may be caused by surface recombination, not by bulk recombination via deep defect centers. The bulk recombination generally increases exponentially with increasing temperature. This is very attractive for low-loss, high-power application at a high operating temperature.

Fig. 7 shows the reverse blocking characteristics of (a) Al^+- and (b) deep B^+-implanted diodes measured at RT, 335 K, and 373 K. At RT, the Al^+- and deep B^+-implanted diodes could block 1020 and 2900 V, respectively, which were approximately 32% and 90% of the ideal breakdown voltage. The breakdown voltage of each diode increased with increasing temperature. All types of the diodes, including B^+-implanted diodes, showed positive temperature coefficients of reverse breakdown voltage, meaning avalanche breakdown, not other mechanism such as defect-assisted tunneling. This result is one of the most crucial characteristics required for reliable power devices, while such characteristics have not been clearly demonstrated in high-voltage SiC devices so far except for only a limited report [13].

To investigate the avalanche behavior, the luminescence was observed in the all types of diodes as shown in Fig. 8 At breakdown, the luminescence at the whole edge of circular p–n junction was observed in the Al^+-implanted diode [Fig. 8(a)]. When a high reverse current was induced by the avalanche breakdown at 610 V, the luminescence was observed at the whole edge of p–n junction. Although the calculated electric

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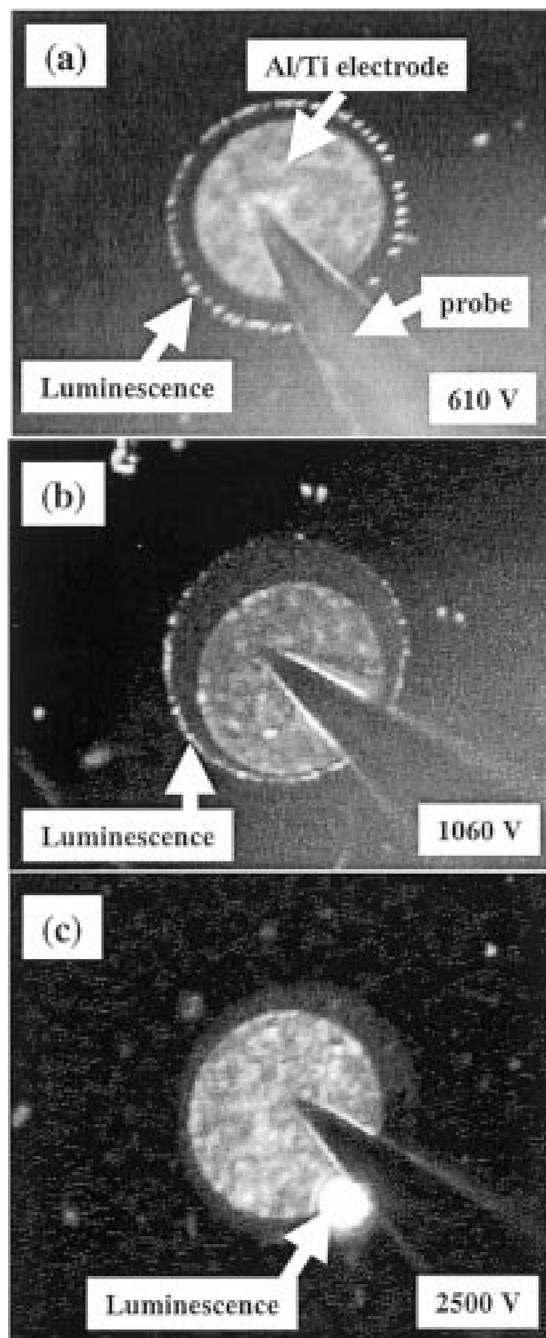

Fig. 8. Luminescence at breakdown for (a) Al^+-, (b) B^+-, and (c) deep B^+-implanted diodes.

field at 610 V is 0.9 MV/cm (parallel plane), the electric field crowding at the edge of p–n junction reaches a critical value ∼2.2 MV/cm. The electric field crowding at the edge of p–n junction causes avalanche multiplication. As opposed to a tunneling process, the avalanche multiplication generates a high density of electron–hole pairs, a part of which yields luminescence through radiative recombination. The intensity of the luminescence tends to increase with increasing the avalanche multiplication-induced current. Similar luminescence was observed in the B^+-implanted diode at 1060 V as shown in Fig. 8(b). In this diode, the electric field crowding causes avalanche multiplication when the calculated electric field is 1.2 MV/cm, which is higher than that of the Al^+-implanted diode.

On the other hand, there is no visible luminescence at the edge of p–n junction, in the case of deep B^+-implanted diodes [Fig. 8(c)]. No visible luminescence at the edge was attributed to the less avalanche multiplication, which means less electric field crowding even at 2500 V, when the calculated electric field is close to the breakdown filed (2.23 MV/cm). These results indicate that the alleviation of electric field crowding at the edge of p–n junction makes the breakdown voltage higher for deep B^+-implanted diodes. However, spotty luminescence was observed inside the p–n junction. The luminescence is speculated to be observed at structural defects such as dislocations. When the reverse voltage is sufficiently high, the luminescence may be firstly observed at the weakest spots in SiC, such as dislocations.

The Al^+- and B^+-implanted diodes blocked a relatively low electric field (0.9–1.2 MV/cm) so that the electric field strength at defects does not reach a critical value, at which defect luminescence is initiated. Instead, the severe electric field crowding causes the luminescence at the anode edge. These difference of the alleviation of electric field crowding are ascribed to the curvature of the edge of p–n junction. Deep implantation naturally forms p–n junction with a larger curvature, resulting in a higher breakdown voltage.

IV. Conclusion

Al^+ implantation into 4H–SiC at either room temperature or elevated temperatures has been investigated. Al^+ implantation at 500 °C followed by 1700 °C-annealing has brought a low sheet resistance of 3.6 kΩ/□, although further improvement is required. The junction characteristics of 4H–SiC p–n diodes fabricated by Al^+ or B^+ implantation into n-type SiC epilayers have also been investigated. P–n junction diodes with a planar structure formed by Al^+, B^+, or deep B^+ implantation exhibited low on-resistances of 6.3–9.1 mΩcm^2, indicating that good ohmic contacts were formed on the hot-implanted p^+-region. The deep B^+-implanted diodes exhibited a higher breakdown voltage of 2900 V and lower leakage current on average. The higher breakdown voltage with stable breakdown of deep B^+-implanted diodes is ascribed to the voltage drop in a thicker i-layer and the alleviation of electric field crowding at the edge. This alleviation is also revealed by the luminescence at breakdown. A positive temperature coefficient of breakdown voltage was obtained in all types of the diodes, which means avalanche breakdown.

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Yuuki Negoro was born in Osaka, Japan, on November 10, 1977. He received the B.E. degree in electrical and electronic engineering from Kyoto University, Kyoto, Japan, in 2001, where he has worked on SiC material characterization and p-n diodes. He is currently pursuing the M.E. degree at Kyoto University.

His current activities include characterization of ion implanted SiC, and high-power and high-temperature SiC devices.

Nao Miyamoto was born in Chiba, Japan, on October 14, 1974. He received the B.E. and M.E. degrees in electrical and electronic engineering from Kyoto University, Kyoto, Japan, in 1988 and 2000, respectively.

He is currently with Hitachi Co., Ltd., Tokyo, Japan.

Tsunenobu Kimoto received the B.S.E.E., M.S.E.E., and Ph.D. degrees from Kyoto University, Kyoto, Japan, in 1986, 1988, and 1996, respectively. His Ph.D. work involved SiC epitaxial growth, material characterization, and device fabrication such as high-voltage diodes.

In April 1988, he joined Sumitomo Electric Industries, Ltd., Hyogo, Japan, where he conducted research on amorphous Si solar cell applications and semiconducting diamond materials for high-temperature devices. In 1990, he started SiC research work as a Research Associate with Kyoto University. From September 1996 to August 1997, he was a Visiting Scientist at Linköping University, Sweden, where he was involved in fast epitaxy of SiC and high-voltage Schottky diodes. He is currently an Associate Professor in the Department of Electronic Science and Engineering, Kyoto University. His main research activity includes SiC epitaxial growth, optical and electrical characterization, ion implantation, MOS physics, and high-voltage diodes. He has published over 120 papers in scientific journals and international conference proceedings. He also holds several patents in the semiconductor field.

Hiroyuki Matsunami (M'84–SM'00) received the B.E., M.E., and Ph.D. degrees, all from Kyoto University, Kyoto, Japan, in 1962, 1964, and 1970.

He has been a Research Associate, Associate Professor and since 1983, Professor at Kyoto University. He was a Visiting Associate Professor at North Carolina State University, Raleigh, from 1976 to 1977. His professional work is on semiconductor science and engineering. He has also been working on semiconductor material synthesis, characterization, and device demonstration. He began his work on semiconductor SiC in 1968. He has worked in SiC blue light–emitting diodes, heteroepitaxial growth of SiC on Si, and step-controlled epitaxial growth of SiC on SiC substrates. He has contributed greatly to the progress in SiC devices by bringing high-quality epitaxial layers grown by the concept of step-controlled epitaxy, such as high-performance Schottky diodes and high-channel electron mobility in SiC MOSFETs. He has published more than 200 papers in scientific journals and more than 100 papers in international conference proceedings. He is one of the three editors of *Silicon Carbide I, II* (Berlin, Germany: Akademie Verlag, 1977). He is on the editorial board of *Solar Energy Materials and Solar Cells*, and an Associate Editor of *Diamond and Related Materials*.

Dr. Matsunami is a Fellow of The Institute of Electronics, Information, and Communication Engineers, and a member of The Institute of Electrical Engineers of Japan, The Japan Society of Applied Physics, and the Japanese Association of Crystal Growth.