

**$\beta$ -Gallium oxide power electronics**

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*APL Mater.* 10, 029201 (2022)

<https://doi.org/10.1063/5.0060327>



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Cite as: APL Mater. 10, 029201 (2022); doi: 10.1063/5.0060327  
Submitted: 17 June 2021 • Accepted: 14 December 2021 •  
Published Online: 7 February 2022



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## ABSTRACT

Gallium Oxide has undergone rapid technological maturation over the last decade, pushing it to the forefront of ultra-wide band gap semiconductor technologies. Maximizing the potential for a new semiconductor system requires a concerted effort by the community to address technical barriers which limit performance. Due to the favorable intrinsic material properties of gallium oxide, namely, critical field strength, widely tunable conductivity, mobility, and melt-based bulk growth, the major targeted application space is power electronics where high performance is expected at low cost. This Roadmap presents the current state-of-the-art and future challenges in 15 different topics identified by a large number of people active within the gallium oxide research community. Addressing these challenges will enhance the state-of-the-art device performance and allow us to design efficient, high-power, commercially scalable microelectronic systems using the newest semiconductor platform.

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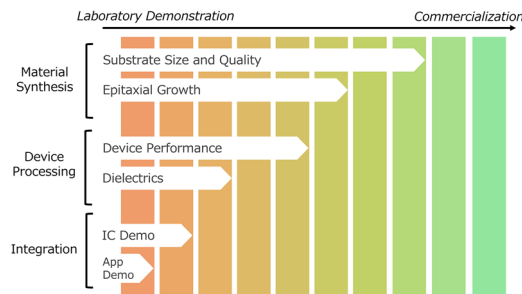
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## I. INTRODUCTION

**Andrew J. Green, James Speck, Grace Xing**

With extreme rarity, a materials result has the power to rally the research community around a new semiconductor technology. There are many reasons for this, but first and foremost, potential leap-ahead performance must be present from multiple rare intrinsic material properties. Second, a materials supply chain must often be created and sustained by multiple long-term government investments (semiconductor research tends to be cost prohibitive). Finally, the research community must break through technical barriers that inhibit performance and commercialization. For the first time in decades, a research community has risen in support of a new technology.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has the technical and programmatic momentum not seen in decades since the rise of SiC and GaN research in the 1990s.

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is unique. The material has a collection of properties that, until recently, has not been observed in one system.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has an ultra-wide bandgap of nearly 5 eV. The material can not only conduct electrons but also maintain extremely high fields. Most importantly, it has a large, scalable low-cost substrate. These properties existing together have enabled one of the most exciting fields to explode. The availability of substrates is greater now than it ever has been, and with new companies developing substrates for commercialization in the near future, the pace of progress is expected to grow. Figure 1 shows commercialization progress for various sectors in the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> semiconductor development chain. As expected, materials synthesis has made the most progress toward large scale production as high-quality materials are almost a prerequisite for advanced device development. While



**FIG. 1.** A top-level view of the technology progress for various sectors toward commercialization of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> applications as of October 2021.

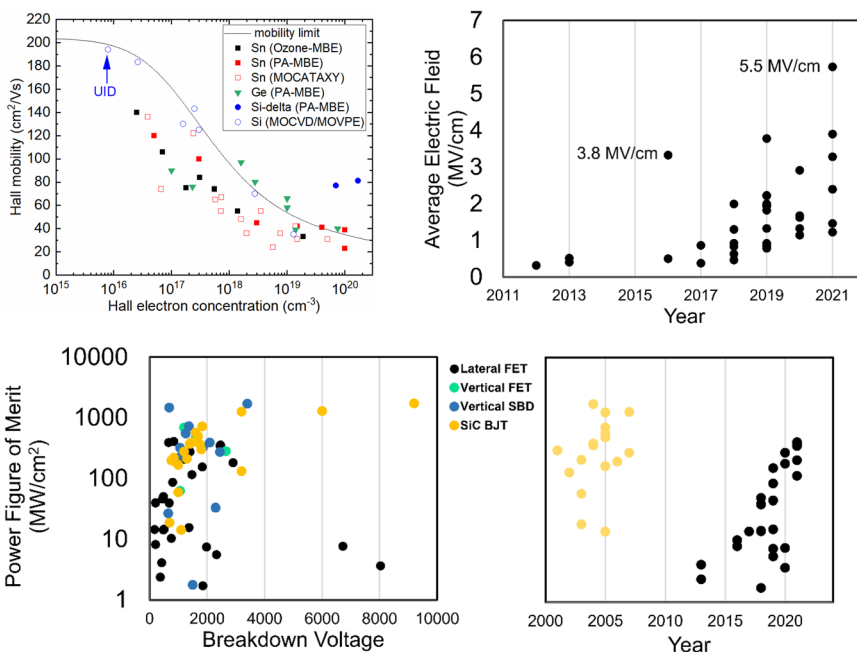
many device demonstrations have taken place, many design optimizations still need to be explored. The relatively new opportunity to purchase 2-in. diameter substrates will enable large-scale experiments. The large bandgap and field strength have created a new set of problems for materials and device researchers. To this date, avalanche breakdown has not been measured in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Every device breakdown to date has resulted from catastrophic dielectric failure. Until avalanche breakdown is observed, the true potential of this technology will not be known. Finally, integration and application demonstrations have still yet to be realized. The availability of large-scale substrates should be a significant enabling factor for the circuit and application demonstrations. One major step forward requires the community needs to reach up to application engineers to probe for requirements that  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> can address. Overall, the maturation of this material has progressed with incredible pace.

Per Baliga's Figure of Merit, mobility and field strength are the main predictors of conduction losses and therefore performance for a power device. As seen in Fig. 2 (left), multiple groups have been able to demonstrate bulk doping for a variety of

concentrations. This enabled the device community to make quick strides in fabricating high performance devices. Figure 2 (right) shows a collection of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral device results. Until 2016, no device in any material had measured a greater average critical field strength than SiC. (2.5 MV/cm). Since then,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has repeatedly pushed the boundaries for high field devices.

The large breadth of the device that results over the past decade is a testament to the materials quality and availability. Figure 3 shows the Power Figure of Merit (PFOM) as a function of device breakdown voltage (BV) for multiple device topologies. There are major gaps which have yet to be demonstrated. Surprisingly, voltages >3 kV have been rare in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. This is expected to change over in the next five years as field management issues are addressed. On the right-hand side of Fig. 3, historical progress of lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device PFOMs is compared to SiC bipolar junction transistors (BJTs). Incredibly, the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> PFOM has improved exponentially over the past decade approaching that of the BJT from the middle to late 2000s. For continued improvement, parasitic removal and field management will need to be achieved.

There has been incredible progress over the past decade, but there is still work to be done. This document serves to identify the main challenges that currently limit  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> from reaching the full performance potential. For each chapter in this Roadmap, the state of the art is described briefly followed by an analysis of the most important technical barriers in each respective section. This serves as a call to action, for if the community can address these barriers, it will enable  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> to be the next commercialized semiconductor.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is at a critical point in the development cycle. The materials supply chain is healthy. Device results are swift and encouraging. The technology readiness level is improving, but the community must establish application pull to attract serious investment further motivating development. This guide will help inform future research directions and help propel  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> to the world's next great commercial semiconductor technology.



**FIG. 2.** (Left) Hall mobility is plotted as a function of electron concentration. A wide range of bulk doping is available for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> from the contact regime to the high blocking voltage regime. (Right) Average field ( $V_{BK}/L_{GD}$ ) is plotted as a function of time for lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FETs.

**FIG. 3.** (Left) The Power Figure of Merit (PFOM) is shown for multiple  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> topologies (black: lateral FET, teal: vertical FET, and blue: vertical SBD) as well as the SiC BJT (yellow). (Right) PFOM is plotted as a function of time for SiC BJTs and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral FETs. Initial exponential growth is observed in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> due to the rapidity of materials and device optimization.



## II. AN OUTLOOK TO THE COMMERCIAL MARKET OPPORTUNITIES OF $\beta$ -Ga<sub>2</sub>O<sub>3</sub> BASED POWER DEVICES

Peter Moens, Fredrik Allerstam, Krister Gumaelius, Thomas Neyer

### A. Status of the area

For many decades, Si-based devices dominated the field of power electronic devices. Substantial progress and device improvement was achieved by the commercialization of the HEXFET<sup>®</sup> transistor in the 1980s, the insulated gate bipolar transistor (IGBT) in the 1990s, and the superjunction transistor in the 2000s. Each major improvement was due to clever junction engineering using Si as the base substrate. However, since 2010, devices based on other material systems entered the market and the focus shifted from junction engineering to materials engineering. SiC diodes were introduced around 2010 and junction field-effect transistors (JFETs) and MOSFETs followed soon after. Steady and continuous improvement in SiC material quality, increase in wafer size (up to 200 mm today), and better process control have resulted in lower cost substrates. In 2019, SiC devices took up ~3% of the total power device market (including modules) growing to exceed 12% in 2025.<sup>1</sup> Recently, GaN-based vertical power devices are available from several suppliers (JFETs and MOSFETs). These devices are built on native GaN bulk substrates, similar to SiC. The wafer size is limited to 100 mm. Another emerging class of devices are based on AlGaIn/GaN high-electron-mobility transistors (HEMTs), which can be built on low-cost 200 mm Si wafers on which a thin (~few  $\mu$ m) GaN-based layer is grown by metal organic chemical vapor deposition (MOCVD).<sup>2</sup> Although their market share is small, it is expected to grow substantially over the next few years, serving applications below 900 V. This is a similar technology to what is used for RF devices for mm wave applications. First successful attempts to grow GaN-on-Si on 300 mm have been published.<sup>3</sup>

Looking toward the future, a number of other wide-bandgap materials are currently being explored in research. The most studied is **diamond** that is considered to be the “ultimate material.” However, technological obstacles (lack of efficient n-type doping, conductive surface channels, lack of substrates, and difficulties to make ohmic contacts) have for a long time blocked the demonstration of performant devices. Unless spectacular progress is made on these issues, no real-world implementations are expected in the foreseeable future.<sup>4</sup> **AlN** is probably the most interesting wide bandgap material because it combines high thermal conductivity with a very large bandgap of 6.2 eV. The bandgap is even higher than that of diamond (5.5 eV). Currently, a few AlN bulk substrate suppliers exist and the substrates are 2 in. in diameter or below.

**Gallium oxide** is the only wide bandgap material that can be grown from a melt and as such is potentially a low-cost material. It can be n-type doped by several elements with good control over a wide range. Doping from a melt results in resistivity down to 10 m $\Omega$  cm. Halide vapor phase epitaxy (HVPE) grown epi can be controlled corresponding to doping concentrations ~10<sup>19</sup> and mid 10<sup>15</sup> cm<sup>-3</sup>, respectively. By Si implantation, resistivity can be as low as 1 m $\Omega$  cm. Ohmic and Schottky contacts can be made by

using standard metals (Ti, Al, and Ni) and relatively low annealing temperatures.<sup>5</sup> Wafering and lapping can be done using standard production tools. Different dielectrics [e.g., atomic layer deposition (ALD) deposited Al<sub>2</sub>O<sub>3</sub>] can be used as a gate dielectric. Recently, a number of publications reported on promising device characteristics and performance.<sup>6–9</sup>

### B. Current and future challenges

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is a material system with a high critical electric field and a relatively low mobility, which allows devices with improved performance compared to SiC and even GaN. Equally important, the material can be grown from a melt and can thus be produced with a very high crystalline quality at low cost when compared to (bulk) GaN, SiC, AlN, and diamond. The crystal growth techniques used today allow scaling from 100 to 150 mm.

Figure 4 depicts the estimated critical electric field  $E_c$  vs the bandgap energy  $E_g$  for different material systems which are attractive to power semiconductor applications. Only homo-epitaxial material systems are included, which are the ones of interest for making vertical devices.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is well positioned in terms of  $E_c$  and has an estimated substantial lower material cost than any other ultra wide bandgap material. Figure 5 shows the predicted device performance (on-state resistance  $R_{on}$  vs blocking voltage capability  $V_{bd}$ ), with the assumptions on substrate thickness and resistivity, bulk and inversion layer mobility, device pitch, etc., as calculated from basic device physics. Figure 5 clearly shows the potential to reach lower  $R_{on}$  for a given breakdown voltage  $V_{bd}$  (e.g., for a 1.2 kV device, a typical breakdown is around 1.5 kV).

Besides on-resistance ( $R_{ON}$ ) and breakdown voltage ( $V_{BK}$ ), also switching capacitance, output capacitance, charge, and energy are important. Based on the physics equations that relate the output

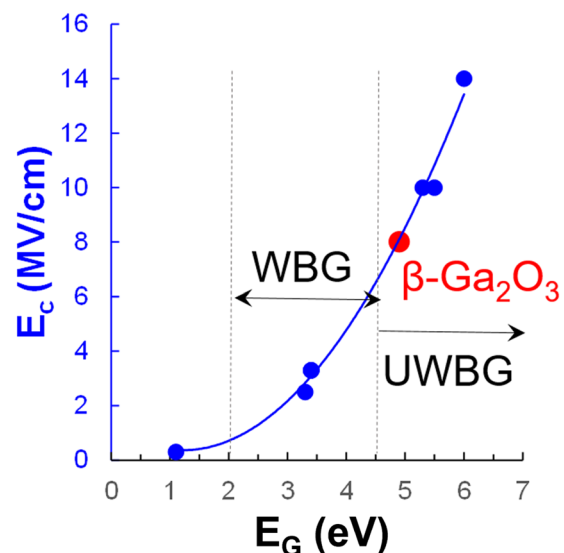
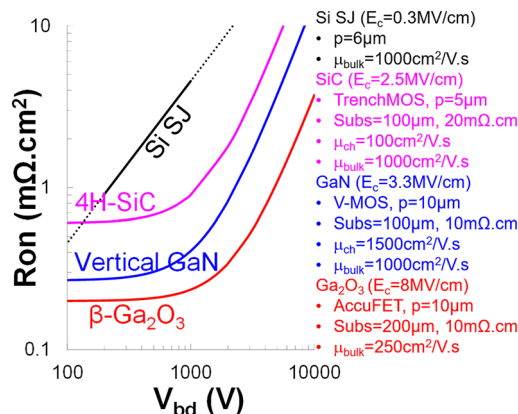


FIG. 4. Estimated critical electric field  $E_c$  vs the bandgap energy  $E_g$  for the different material systems that are attractive to power semiconductor applications. Bulk materials only, no no hetero-epitaxy (e.g., for HEMTs).



**FIG. 5.** Calculated theoretical performance ( $R_{\text{ON}}$  vs  $V_{\text{BK}}$ ) for vertical power devices. Assumptions used in the calculation are listed on the right. The model takes into account the contact, channel, drift, and substrate resistances;  $p$  denotes the cell-pitch.

capacitance ( $C_{\text{OSS}}$ ), charge ( $Q_{\text{OSS}}$ ), and energy ( $E_{\text{OSS}}$ ) to the expansion on the depletion width,  $R_{\text{ON}} \cdot Q_{\text{OSS}}$  and  $R_{\text{ON}} \cdot E_{\text{OSS}}$  can be calculated using the same assumptions as shown in Fig. 5. Table I shows the calculated values for a 1.2 kV rated device (with an assumed  $V_{\text{bd}} = 1.5$  kV). The prime transistor figures of merit  $R_{\text{ON}} \cdot Q_{\text{OSS}}$  and  $R_{\text{ON}} \cdot E_{\text{OSS}}$  are  $\sim 3\times$  better than for 4H-SiC and  $\sim 20\%$  better than for bulk GaN. Figure 5 and Table I show the great promise of  $\beta\text{-Ga}_2\text{O}_3$  as a material for power switching devices.

There are, however, some important obstacles and areas of research which need to be overcome to make  $\beta\text{-Ga}_2\text{O}_3$  based power devices economically viable and a reality in real-life power switching applications.

### 1. Low thermal conductivity

With a value of  $\sim 0.2$  W/cm K,  $\beta\text{-Ga}_2\text{O}_3$  has a thermal conductivity which is  $8\times$  lower than bulk GaN and  $\sim 30\times$  lower than SiC. Efficient heat transfer is a must for power devices. This is especially true for transistors with a small overall die area. As can be deduced from Table I, for a device with the same voltage and current (or on-resistance) rating, a  $\beta\text{-Ga}_2\text{O}_3$  die will be  $10\times$  smaller than a

corresponding SiC die. Therefore, die thinning ( $<50\mu\text{m}$ ) is a must, and technologies to transfer thin die directly to the lead frame need to be explored. The possibility to easily cleave the  $\beta\text{-Ga}_2\text{O}_3$  may pose a way forward to produce very thin die. In addition, heat removal from the top surface needs to be studied through innovative assembly technologies. Demonstrations of heat removal techniques<sup>10,11</sup> are expected to be a major research area as devices begin to be distributed throughout the community in the next five years. This will have major ramifications with respect to application space (i.e., power rating and duty cycle).

### 2. Lack of a p-type

To date, there is no p-type doping in  $\beta\text{-Ga}_2\text{O}_3$  since acceptor states are deep in the bandgap,  $>1$  eV from the valence band. The valence band is also theorized to be flat resulting in negligible hole transport. This means that no avalanche p-n junction can be made. The lack of an avalanche junction is a concern for applications that are used in regions with noisy power grids or need to take over large inductive loads rapidly, like UPS systems.

### 3. The lack of p-type may also be a problem for junction termination design

Management of the electric fields at the die edge is an important device design focus point, as it impacts the voltage rating of the transistor or diode as well as its reliability. For termination structures, the lack of p-type can perhaps be mitigated by the integration of p-type oxides, such as sputtered NiO. Also beveled terminations are under investigation.

### 4. Wafer size limitation

Today, the maximum wafer size that is commercially available is 100 mm. From a practical commercial point-of-view, the minimum wafer size should be 150 mm, with a roadmap to 200 mm. Larger wafer size does not only reduce the product cost but also allows the device processing in more advanced fabrication lines, which result in better process control, lower defect densities, etc.

### 5. Several poly-types

$\text{Ga}_2\text{O}_3$  has many poly-types, among which the  $\alpha$ -phase and  $\beta$ -phase are the most investigated.  $\alpha\text{-Ga}_2\text{O}_3$  is rhombohedral, has a high  $E_c \sim 10$  MV/cm, but is only thermally stable up to  $\sim 600$  to  $700^\circ\text{C}$ . Since  $\text{Al}_2\text{O}_3$  and epitaxial  $\text{In}_2\text{O}_3$  have the same  $\alpha$ -structure,

**TABLE I.** Calculated prime transistor parameters for a 1.2 kV rated vertical power transistor. Assumptions for the calculation are listed in Fig. 5. The prime transistor figures of merit  $R_{\text{ON}} \cdot Q_{\text{OSS}}$  and  $R_{\text{ON}} \cdot E_{\text{OSS}}$  are  $\sim 3\times$  better than for 4H-SiC and  $\sim 20\%$  better than for bulk GaN.

$V_{\text{RATING}} = 1200$ V						
Parameter	Unit	Si	Si SJ	4H-SiC	Bulk GaN	$\beta\text{-Ga}_2\text{O}_3$
$R_{\text{ON}}$	( $\text{m}\Omega\text{ cm}^2$ )	227	6.84	1.8	0.589	0.189
$Q_{\text{OSS}}$	(nC/cm <sup>2</sup> )	313	6260	2150	2710	7080
$E_{\text{OSS}}$	( $\mu\text{J}/\text{cm}^2$ )	125	250.4	857	1082	2829
$R_{\text{ON}} \cdot Q_{\text{OSS}}$	(m $\Omega$ nC)	71 051	42 818	3870	1596	1338
$R_{\text{ON}} \cdot E_{\text{OSS}}$	(m $\Omega$ $\mu\text{J}$ )	28 375	1713	1543	637	535

it paves the way to hetero-structures in a similar way as is done for the AlN/GaN/InN material system. P-type would be possible through combination with  $\alpha$ -Ir<sub>2</sub>O<sub>3</sub> and  $\alpha$ -Rh<sub>2</sub>O<sub>3</sub>, which are p-type oxides. These hetero-structures are, however, lateral device types.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is monoclinic, can be grown from a melt, and is thermomechanically stable until 1700 °C. From a research perspective, the multitude of different phases is interesting, but from a commercialization point of view, it would be preferred if the development effort could be focused on the  $\beta$  phase due to the maturity of the sample supply chain.

### 6. E-mode device design

The lack of p-type also puts restrictions on how to make e-mode transistors. First results using fin field-effect transistors (FINFET) type of accumulation FETs are promising but require tight process control and advanced processing equipment. It remains to be seen if this is a viable option. Another option is to use a depletion mode transistor cascoded with a Si (or other) low voltage MOSFET. Market adoption for cascaded SiC JFETs or AlGaN/GaN HEMTs is limited due to the fact that the internal node cannot be controlled during switching.

### 7. Lack of reliability data

Reliability on any type of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device (diode or transistor) is still in its infancy.

### C. Concluding remarks

From a power device manufacturer's perspective,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is the preferred ultra wide bandgap material because it can be grown from a melt and has a high crystalline quality and a relatively low cost. There is a roadmap to 150 mm. The lack of p-type is a serious drawback for transistors. On the plus side, most of the fundamental process modules for making  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky diodes are available: standard Ohmic and Schottky metallization's, good control of the n-type doping of the epi, and low resistivity substrates. Termination structures for the diodes will have to be optimized and further developed. A good market entry point for these diodes could be the 600 V and 1.2 kV voltage classes, where they will compete with SiC diodes, e.g., for high-end power supplies used in server farms or in boost stages of energy efficient power converters. These devices could potentially offer better than SiC performance at reduced cost. According to Ref. 1, this market alone will amount to 100 M\$ by 2025 and is driven by efficiency standards mandated by governments.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes will potentially enable a further improvement step from "80 plus" titanium (currently the highest certification level for power supply efficiency) with efficiencies exceeding >95% at full load. If by that time  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> diodes can prove reliability at good cost and they can be sourced easily on the power electronic market, they could take significant share of the TAM in 2025.

At higher voltage classes (e.g., 1.7 kV and beyond), doping control has to be proven to be reproducible and stable for production. In addition, the larger surface fields will create additional challenges with the passivation layers on top of the termination. Below 600 V, there will be competition also with lateral devices that are not limited to bulk properties.

## III. DEFENSE BASED POWER CONVERTER APPLICATIONS

### Andrea Arias-Purdue, Vivek Mehrotra

Much of the traditional military system's power conversion needs have been fulfilled by sub-assemblies that have continuously leveraged improvements in commercial semiconductors and integrated circuits, such as state-of-the-art MOSFETs, drivers, and controllers. For applications ranging from low-voltage to kV power converters, switched-mode power supplies have become the dominant approach due to their efficiency benefits. For example, switching regulators (such as buck converters) offer typical efficiencies of 70%–95%, up to switching frequencies in tens of megahertz for commercial parts<sup>12,13</sup> and up to hundreds of megahertz in research.<sup>14–16</sup> This remarkable progress is also complemented by research efforts such as DARPA's Microscale Power Conversion (MPC) program,<sup>17,18</sup> where DARPA requested a ~1 GHz switching GaN-based power converter to enable very high bandwidth and efficiency supply modulators for power amplifiers. Significant challenges surfaced during the MPC effort. The switches and gate drivers developed needed to have at least an order of magnitude less total gate charge and power dissipated, respectively, for efficient 1 GHz switching converters (28 mΩ nC<sup>19</sup> is the lowest  $R_{ON} \times Q_G$  demonstrated under MPC). It also became apparent that the co-design of the power amplifier and the switch modulator would result in the most efficient system design.

As new wider bandgap semiconductor materials have matured and have become widely available (i.e., SiC and GaN devices), state-of-the-art modules with progressively improved performance have followed—improvements in size, weight, efficiency, operational temperature range, and cost. In addition, several DoD systems require ruggedness at high ambient temperature: for this reason, ultra wide bandgap (UWBG) materials, such as  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, are excellent candidates for maximizing performance even under these extreme environmental conditions. While several circuit techniques can be employed to effectively switch a power circuit at a frequency higher than its individual branches, we note that the maximum performance benefit is often achieved when the power commutation path is monolithically (or perhaps 3D) integrated using the least number of components, thus operating at the maximum feasible switching frequency as allowed by the device's dynamic losses and as permitted by the intrinsic losses of the wiring closing the critical power commutation path.

### A. Current and future challenges

Switching power converters operating at >1 GHz remain a challenge due to the stringent  $R_{ON} \times Q_G$  requirements imposed on the main switch, a necessary condition to achieve high efficiency. Owing to its ultra-high Baliga figure of merit,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs with over 3.8 and 5.3 MV/cm of mean peak breakdown field strengths<sup>20</sup> have been demonstrated, constituting the highest field of any lateral FET measured to date. The key requirements for next-generation  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices and ICs are low loss power devices for high frequency operation: low conduction ( $R_{ON}$ ) and switching losses ( $Q_G$ ) and low turn-on and turn-off energy. We estimate that a sheet

charge density  $N_{SH}$  of  $9.6 \times 10^{12} \text{ cm}^{-2}$  and a state-of-the-art mobility of  $200 \text{ cm}^2/\text{Vs}$  along with a contact resistance of  $0.1 \text{ } \Omega \text{ mm}$  and sub-micrometer access regions will enable  $\beta\text{-Ga}_2\text{O}_3$  devices with a total gate charge  $Q_G \sim 0.8 \text{ pC/mm}$  for a  $>100 \text{ V}$  breakdown voltage lateral device, a  $>5\times$  improvement with respect to state-of-the-art GaN switches.

One of the key advantages of UWBG materials is their ability to withstand high ambient temperature, as demonstrated in Ref. 21, where  $\beta\text{-Ga}_2\text{O}_3$  MOSFETs showing stable operation up to  $300^\circ\text{C}$  were reported. In addition, packaging to enable high reliability in harsh environments will be required, taking into account coefficient of thermal expansion (CTE) matching and incorporating heat spreading, given the low coefficient of thermal conductivity for  $\beta\text{-Ga}_2\text{O}_3$ . It is likely that the development of new encapsulation compounds will be needed, simultaneously requiring low signal-loss and considering the device thermal budget. These challenges will need to be addressed at the multi-chip package level. Monolithic integration of power devices, gate drivers, and passives for lower parasitic beyond a certain critical frequency ( $\sim 1 \text{ GHz}$ ) becomes necessary, since stray inductance and capacitance can completely negate the benefits of high frequency switching. Currently, magnetics are available which address switching frequencies at  $1 \text{ GHz}$ . Advanced 3D integration that can enable approximately tens of micrometers pitch between different chips is also a viable option.

High switching frequency ( $>1 \text{ GHz}$ ) enables size reduction of magnetics and capacitors as well as high bandwidth control for special applications, such as transient loads and envelope tracking (ET). For example, for ET, the output of the converter may be a pulse-width modulated signal with a control bandwidth that needs to be  $10\times$  faster than the signal bandwidth. Reduced volume magnetics are especially relevant for size-constrained platforms, such as Unmanned Aerial Vehicle (UAV) power systems and phased array power distribution, which necessitate both high efficiency due to limited heatsinking and small components due to the constrained area available in arrays operating at mm-wave frequencies. The magnetics required to support  $1 \text{ GHz}$  converters will have negligible hysteresis and Eddy current losses, with enough magnetic permeability and saturation flux density up to  $\sim 10 \text{ GHz}$ . We note that to materialize high speed converters, these passive components will have to be developed alongside emerging  $\beta\text{-Ga}_2\text{O}_3$  devices. Novel materials such as FeSi-based magnetic compounds are possible candidates.<sup>22</sup>

### 1. Gate driver requirements

Gate drivers are key to the implementation of the converter: they are essentially pulse amplifiers. The input pulse train from a control circuit defines the interval during which the main power switch should be on and off. The function of the gate driver circuit is to supply and remove charge from the gate of the main switch rapidly so that its state reflects the desired condition. The rate at which this charge is delivered and taken away is a major factor in determining how fast the main device switches. To maintain a square gate pulse, power delivery to each switch gate containing up to several harmonics of  $1 \text{ GHz}$  carrier fundamental is required to preserve high efficiency. In addition, realizing high efficiency, the gate driver output stage capacitances must be considerably less than those of the power device. To minimize switching losses, the gate driver must be able to turn the switch on and off at least additional  $10\times$  faster

(10% of the period), leading to an extremely challenging  $20 \text{ ps}$  rise and fall time requirement of the converter's pulse width modulated (PWM) output waveform, for a  $1 \text{ GHz}$  carrier converter. We note that the current state-of-the-art commercial gate drivers exhibit  $\sim 350 \text{ ps}$  of rise and fall times,<sup>23</sup> while research gate drivers have been demonstrated to switch at  $1 \text{ GHz}$  carrier while exhibiting  $106 \text{ ps}/122 \text{ ps}$  transitions and consuming  $3 \text{ W}$  of power,<sup>24</sup> not yet adequate for  $1 \text{ GHz}$  converters—since  $\sim 5\times$  faster transitions are required. Therefore, to enable  $1 \text{ GHz}$   $\beta\text{-Ga}_2\text{O}_3$  converters, a new class of ultra-short transition and low power consumption gate drivers must be developed, and critically, they must be integrated alongside the main switch power commutation loop so that stray inductance does not significantly lower the system efficiency. While highly scaled GaN could potentially be used if a suitable complementary technology was developed, it is possible that the most efficient gate driver solution would come from specifically tailored highly scaled  $\beta\text{-Ga}_2\text{O}_3$  MOSFETs.

### 2. Topology and controls considerations

For Pulse Width Modulated (PWM) converters, the switch rise and fall times must be negligible as compared to both carrier frequency and minimum duty cycle—this is important to maintain low switching losses. Both the power switch and the control elements' bandwidth must be at least  $20\times$  greater than the fundamental switching frequency for negligible dynamic losses. In addition to switching frequency, control rise/fall time can be optimized to better leverage the  $\beta\text{-Ga}_2\text{O}_3$  device's low gate charge by generating very high device slew rates, thus minimizing dynamic losses. An application where this feature can offer a critical advantage is direct AC to AC conversion.

For many applications, a synchronous converter topology can be chosen to maximize efficiency: this is expected to also apply to  $\sim 1 \text{ GHz}$  switching converters.

We note that for power distribution systems, an intermediate bus structure and Point of Load (PoL) regulators provide flexibility and maximize efficiency, and coupled with their high frequency and smaller footprint,  $\beta\text{-Ga}_2\text{O}_3$  converters will provide the necessary degrees of freedom for high performance power system design.

### 3. Projected $\beta\text{-Ga}_2\text{O}_3$ switch performance and comparison to GaN devices

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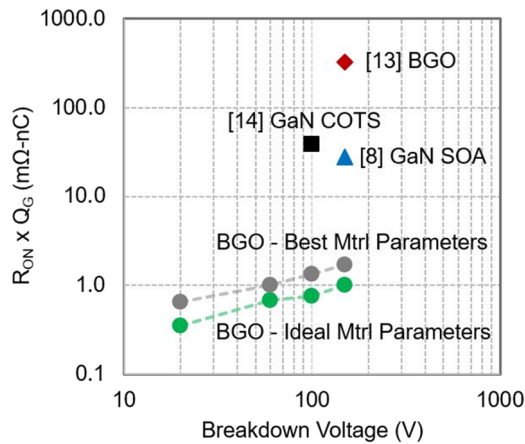


FIG. 6. Comparison of GaN,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, and projected  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> performance.<sup>19,25</sup>

and smaller footprint,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> converters will provide the necessary degrees of freedom for high performance power system design.

#### 4. Projected $\beta$ -Ga<sub>2</sub>O<sub>3</sub> switch performance and comparison to GaN devices

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> and GaN switch performance is compared in Fig. 6. The projected  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> curves correspond to aggressively scaled devices (50 nm of gate length with sub-micrometer drain to source spacing assuming 383 and 500 V/ $\mu$ m of breakdown voltage for the best material parameters and ideal material parameters curves, respectively). The assumed material and calculated device parameters are included in Table II. We note that even based on the best  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> material parameters reported to date, our projected  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device has a considerably lower  $R_{ON} \times Q_G$  product as compared to both COTS and SOA GaN HEMTs of similar voltage rating.

#### 5. Next generation power systems

Future DoD needs include next generation phased array power distribution: high efficiency will require point of load (PoL) power conversion at the element/tile array level while also leveraging high bandwidth adaptive supplies to maximize the transmitter efficiency. It will be important to leverage high control bandwidths and ultra-low size and weight in mm-wave arrays (very compact platforms due to the  $\lambda/2$  spacing requirement) to fulfill the need for high efficiency. UAV applications, typically also requiring lower voltage, will

consist of similar needs—ultra-size, optimized PoL converters. We envision a modular library of PoL  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices that can fulfill these needs for a host of power conversion ratios—both boost and down converters—and power levels.

#### B. Concluding remarks

Reduced size, high efficiency converters for emerging applications, such as mm-wave digitally steered arrays and next generation UAVs, will necessitate fundamentally advanced power switches.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is poised to enable next generation power systems due to its superior material properties that enable its potential for significantly lower dynamic power losses as compared to Si and GaN, as well as its ability to withstand harsher environmental conditions, in part, due to its wider bandgap.

While it might not be advantageous to increase the converter switching frequency for high power applications (>100 W), the control bandwidth can be increased, thereby resulting in significant system efficiency improvements. To better understand these practical limitations, the intrinsic material-driven losses (wiring stray capacitance and inductance) must be considered within the converter design space to establish a fundamental switching frequency vs power loss trend for the wiring environments (including filter components) available to the power electronics designer.

### IV. ECONOMIC MODEL

Akito Kuramata, Kohei Sasaki, Shinya Watanabe, Kimiyoshi Koshi

#### A. Status of the area

The most important index affecting the economic model of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> for power-device applications is the device price per unit current. The index is determined by the wafer price and the current density of devices. It is expected that  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> wafers will be able to be manufactured at low cost because  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is suitable for melt growth, has medium hardness, and can be easily processed.<sup>26</sup> This expectation is in contrast to the situation of other new power device materials, such as SiC or GaN, which suffer from high wafer manufacturing costs due to difficulties in bulk growth and wafer processing. Furthermore, since Baliga's figure of merit for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is larger than that of SiC or GaN, it is expected that the on-resistance of diodes or transistors can be reduced, and as a result, the current

TABLE II. State-of-the-art and ideal material parameters for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices.

Device	$N_{SH}$ (cm <sup>-2</sup> )	Mobility	$R_{SH}$ ( $\Omega$ /sq)	BV (V/ $\mu$ m)	$R_C$ ( $\Omega$ mm)	$v_{e-}$ (cm/s)	WG (cm)	$I_D$ (A)	$Q_G$ (C)	$R_{ON}$ ( $\Omega$ ) BV = 20 V	$R_{ON}$ ( $\Omega$ ) BV = 60 V	$R_{ON}$ ( $\Omega$ ) BV = 100 V	$R_{ON}$ ( $\Omega$ ) BV = 150 V
Best mtrl. param.	$9.60 \times 10^{12}$	150	4340	383	0.20	$1.00 \times 10^6$	0.10	0.154	$7.68 \times 10^{-13}$	0.853	1.307	1.760	2.213
Ideal mtrl. param.	$9.60 \times 10^{12}$	200	3255	500	0.10	$2.00 \times 10^6$	0.10	0.307	$7.68 \times 10^{-13}$	0.460	0.880	0.981	1.307

density can be made large.<sup>27</sup> Low-cost production will be enabled by filling the technological gaps in terms of the two factors mentioned above. In this chapter, we describe the challenges to reducing the wafer price of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. See the discussion in Chaps. II, III, XI, XII, and XIII for challenges involved with improving device performance.

The present commercialization status of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates and epitaxial wafers are as follows: Currently, substrates made by the edge-defined film-fed growth (EFG) method in wafer sizes up to 4 in. are commercially available. In addition, 6-in. EFG substrates have been fabricated<sup>5</sup> and 2-in. substrates made by the Czochralski (CZ) method are expected to be commercially available in 2021.<sup>28</sup> Growth of 2-in. bulk crystals by using the vertical Bridgman (VB) method has been reported.<sup>29</sup> As for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial wafers, 4-in. wafers grown by halide vapor phase epitaxy (HVPE)<sup>30</sup> and 1-in. wafers grown by molecular beam epitaxy (MBE) are commercially available.<sup>31</sup> Metal organic chemical vapor deposition (MOCVD) epitaxial growth with excellent electrical properties has been reported.<sup>32</sup>  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial wafers are still more expensive than SiC epitaxial wafers of the same size because  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices have not been commercialized yet and few wafers have been produced.

## B. Current and future challenges in this area

The challenges of low-priced wafer production are described below.

### 1. Substrates

The biggest challenge to lowering the manufacturing cost of bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal is that some of the expensive precious metal crucibles are lost during crystal growth or by recasting. In the EFG method and CZ method, Ir, which has a high melting point and can be used only in a low-concentration oxygen atmosphere, is used as a crucible material. Galazka *et al.* pointed out that a small amount of Ga exists in an equilibrium state of the gallium oxide melt above the melting point, and when it reacts with Ir, part of the crucible is lost.<sup>33</sup> This problem becomes more serious as the size of the substrate increases. In the case of the EFG method, the lifespan of the crucible is about 6 months in the production of 2-in. bulk crystals, whereas during trial production of 6-in. bulk crystals, some holes opened at the bottom corner of the crucible after a considerably shorter period. In the case of 6-in. bulk crystals, the amount of Ga increases as the amount of Ga<sub>2</sub>O<sub>3</sub> melt increases, and the temperature difference inside the crucible increases, resulting in increased reaction in the high-temperature part of the crucible. These phenomena are presumed to shorten the lifespan of the crucible. As far as the EFG method and CZ method go, it is possible to solve this problem by reducing the size of the crucible. In the VB method, the temperature distribution in the furnace can be narrowed and the maximum temperature can be lowered, which expands the choice of metal materials. On the other hand, the method requires an atmosphere with a high oxygen concentration. Under such conditions, Pt–Rh alloy is a suitable crucible material.<sup>29</sup> The VB method can reduce the amount of precious metal lost in one growth, but it is necessary to recast the crucible after each growth. Therefore, the amount of precious metal wear cannot be reduced by more than an order of magnitude. The floating zone (FZ) method enables crystal growth without using precious metals, but the diameter of the reported

crystals is as small, about 1 cm, and there are no reports of large crystals having been successfully grown.

The challenge regarding the wafer fabrication process is to increase the number of substrates taken from one bulk. To meet it, the thickness of the substrate should be reduced.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has the property of being easily cleaved on the (100) and (001) planes. In order to suppress cracking of the wafer due to cleavage, bevel processing has to be performed with high accuracy. Since gallium oxide has a crystal structure of a monoclinic system with low symmetry, the ease of scraping and cracking of the crystals differs depending on the position of the outer peripheral portion of the wafer. As such, a fine processing technique is required, such as by changing the processing conditions according to the position of the outer periphery of the wafer. The crystallographic planes of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates commercially available at present are the (100), (010), and (001) because epitaxial layers with good crystalline quality can be grown on these planes. Other intrinsic material properties of interest are transport (which is thought to be isotropic), thermal conductivity, and field strength (which is thought to be anisotropic). Manufacturers have chosen to prioritize yield and growth quality when producing wafers, although other orientations may be of interest. Process optimization should be done in different ways appropriate for each plane. It is also necessary to take measures to reduce the amount of scraping in the polishing process. The related steps are the slicing step, grinding step, polishing step, and Chemical Mechanical Polishing (CMP) step, but in each step, it is necessary to remove a region thicker than the damaged layer generated in the previous step. To reduce the total amount of scraping as much as possible, a processing method that causes less damage has to be developed. To date, a detailed methodology above has not been published. Optimization of this process may have significant impact on the future of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> manufacturing cost.

### 2. Epitaxial wafers

HVPE or MOCVD is a candidate of the epitaxial growth method for vertical power devices that require a thick film, while MOCVD or MBE is a candidate for lateral power devices that require a film with a flat surface. Regardless of which epitaxial growth method is chosen, the cost challenge is the same, which is to increase the number of wafers to be manufactured per unit equipment per unit time.

One solution is to use multi-wafer equipment. However, at present, there is no multi-wafer equipment capable of mass production in HVPE or MOCVD. It is expected that with increased investment into the technology, multi-wafer equipment will be offered by tool manufacturers. The current HVPE apparatus has a hot-wall-type configuration with a reactor made of quartz, since GaCl is used as a raw material. The reactor made of quartz makes it difficult to build large, reproducible manufacturing equipment. In particular, the gas flow changes because of the low dimensional accuracy of the quartz parts. If the HVPE method is to be used in the future, a mass production furnace with high dimensional accuracy has to be developed. HVPE systems have not been commercially available but have been originally designed. We are planning to develop an advanced HVPE system to increase the production volume. The system will be developed by 2023 which will produce  $7 \times 150 \text{ mm}^2$  epitaxial wafers per run. On the other hand, the barrier to realizing multiple-wafer growth in MOCVD is low because it usually uses a stainless-steel



reactor. However, the MOCVD has another problem: the Ga metal organic raw material it uses is expensive.

Another solution is to increase the rate of epitaxial growth. The current growth rate is about 10  $\mu\text{m/h}$  in the HVPE method and about 1  $\mu\text{m/h}$  in the MOCVD method (while maintaining high mobility). The HVPE method is desired to be several times faster, whereas MOCVD is desired to be one order of magnitude faster. In addition, countermeasures to shorten the interval between growths, such as by using a maintenance-free furnace or high-temperature transportation system, would affect a cost reduction.

Figure 7 shows the expected  $\beta\text{-Ga}_2\text{O}_3$  wafer price against production volume. The values were calculated by considering the progress level of  $\beta\text{-Ga}_2\text{O}_3$  crystal growth and epi-film formation technology which will be available in 2027 for 150 mm wafer size. The  $\beta\text{-Ga}_2\text{O}_3$  wafer price is anticipated to decrease drastically with increasing production volume due to several factors as explained earlier in this section. These low-priced wafers will offer substantial cost-competitive merits in the discrete market sector.

### C. Concluding remarks

In this chapter, we described the technical challenges to reducing the wafer price of  $\beta\text{-Ga}_2\text{O}_3$ . If the challenges described here can be resolved and the number of wafers manufactured increased to mass production scale through commercialization of  $\beta\text{-Ga}_2\text{O}_3$  power devices, the price of  $\beta\text{-Ga}_2\text{O}_3$  epitaxial wafers may be reduced to less than one-third those of SiC epitaxial wafers. If devices with low electrical resistance and low thermal resistance per unit area are developed owing to advances in device design and fabrication technology, the device price per unit current is presumed to fall even further. If they are achieved, it is expected that the manufacturing of  $\beta\text{-Ga}_2\text{O}_3$  power devices will proceed and capture a large market, especially in the high voltage and high current applications. Performance at a cost reduction is quite possibly the most attractive trait of  $\beta\text{-Ga}_2\text{O}_3$  due to the rampant competition in the semiconductor sector. Although continuous improvement of SiC material quality and scaling in wafer size up to 150 mm have resulted in low-cost substrates, the  $\beta\text{-Ga}_2\text{O}_3$  substrate quality has also been improving in line with expanding in diameter at a rate more than twice of SiC since 2004. With time, 150 and 200 mm  $\beta\text{-Ga}_2\text{O}_3$  wafers are expected to be commonplace which will offer significant

cost competitive advantages for vertical FETs and Schottky barrier diodes (SBDs).

## V. BULK GROWTH

### John Blevins

In this section, we examine the techniques used for growth of bulk  $\beta\text{-Ga}_2\text{O}_3$  single crystals. Gallium oxide is known to form five crystalline polymorphs. The  $\beta$  phase is the only stable polymorph at growth temperatures above 1800  $^\circ\text{C}$  and 1 atm pressure. The application of melt-based growth techniques provides significant manufacturing, cost, and scalability advantages compared to vapor transport processes used for other wide bandgap single crystals, such as SiC, GaN, and AlN.  $\beta\text{-Ga}_2\text{O}_3$  is the only wide bandgap semiconductor capable of crystallization from a melt utilizing industrial scale manufacturing techniques, such as Vertical Bridgman (VB),<sup>34</sup> Czochralski (CZ),<sup>35</sup> Edge-Defined Film-fed Growth (EFG),<sup>36</sup> and Float Zone (FZ).<sup>37</sup> The majority of  $\beta\text{-Ga}_2\text{O}_3$  bulk growth research and development to date has focused on the CZ and EFG techniques. Presently, Novel Crystal Technology (NCT, Japan) is the only commercial provider of bulk  $\beta\text{-Ga}_2\text{O}_3$  substrates utilizing the EFG technique. High quality  $\beta\text{-Ga}_2\text{O}_3$  substrates of differing orientations and doping are commercially available in sizes ranging from  $25 \times 25 \text{ mm}^2$  for (010) and 100-mm for (201).<sup>26</sup> Kuramata *et al.* showed the growth of (201) oriented crystals up to 150-mm by the EFG method.<sup>38</sup> The Leibniz Institute for Crystal Growth (IKZ Germany) is a leading research institute for CZ  $\beta\text{-Ga}_2\text{O}_3$ , having made numerous contributions to understanding the scalability of  $\beta\text{-Ga}_2\text{O}_3$  single crystals.<sup>33</sup> Their research clearly demonstrated the necessity of increasing the  $\text{O}_2$  concentration in the growth atmosphere with increased crystal diameter. IKZ has grown 50-mm diameter single crystals exceeding 50-mm in length weighing up to 1 kg and are the largest grown by any method. In the U.S., Northrop-Grumman SYNOPTICS has been developing both 25 and 50 mm semi-insulating (010) CZ  $\beta\text{-Ga}_2\text{O}_3$  substrates (Fig. 8) that have recently become commercially available. Typical x-ray rocking curves are  $<75$  arc sec with surface roughness  $<1 \text{ nm}$ . The prospect for growing large diameter, low cost  $\beta\text{-Ga}_2\text{O}_3$  bulk crystals provides an added incentive for development of this promising next generation semiconductor material.

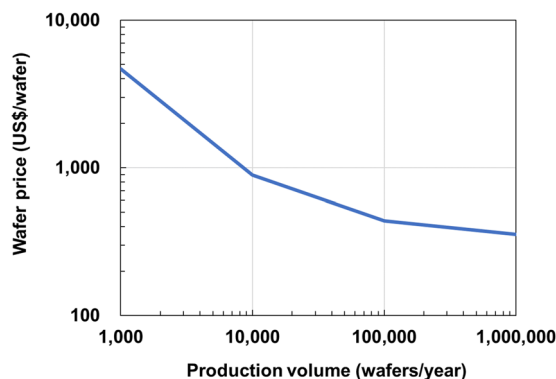


FIG. 7. Expected  $\beta\text{-Ga}_2\text{O}_3$  wafer price in 2027 as a function of production volume.

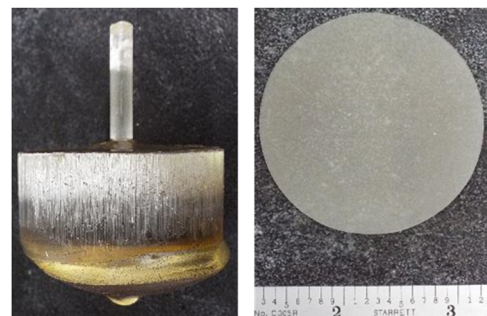


FIG. 8. SYNOPTICS 50 mm (010) Fe-doped  $\beta\text{-Ga}_2\text{O}_3$  as-grown boule and 50 mm substrate.

## A. Key challenges

Impressive device results and early demonstration of large diameter single crystals has stimulated interest in this promising next generation semiconductor. The maturation of any semiconductor device technology can be accelerated by the availability and/or promise of large diameter, high quality, and low-cost native substrates. Wide bandgap semiconductors, namely, SiC, faced significant commercialization challenges due to monumental sublimation growth technology barriers. It took Cree (Wolfspeed) 20 years from the company founding to the commercial release of 100 mm substrates. Approximately 16 years transpired between the commercial availability of 25 and 100 mm SiC substrates.<sup>43</sup> Today, 100 and 150 mm SiC substrates are manufactured at a cost, quantity, and quality never thought possible. The wide bandgap semiconductor manufacturing infrastructure has evolved such that a minimum of 100 mm diameter substrates will be required to access large scale, compound semiconductor manufacturing facilities. A 2019 National Renewable Energy Laboratory (NREL) study estimated a 3× cost advantage of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> compared to SiC substrates leading to 2× lower cost power electronic devices.<sup>44</sup> This study alluded to the relative ease of scaling and potential for low-cost manufacturing of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates, providing a solid foundation for rapid commercialization. Despite rapid progress with CZ and EFG growth process development, it should be recognized that specific “bulk” material requirements remain largely undefined beyond a preference for N-type or semi-insulating. Significant work remains with epitaxial and device process development before bulk crystalline requirements, such as dopant, defect density, and resistivity, are clearly understood. Semiconductor manufactures tend to be growth technology agnostic rather focusing on a combination of technical, manufacturing, and cost factors for selecting a substrate.

Fabrication and polishing of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> merits discussion. Processing of boules and ribbons present differing challenges. The presence of two strong cleavage planes parallel to the (100) and (001) planes complicate boule fabrication and polishing. These crystal planes are highly susceptible to mechanical stress and can easily form cleaves and/or crack during fabrication (coring, grinding, and wire sawing) and polishing. EFG ribbons are typically not subjected to these mechanical processes. As such, fabricating substrates from ribbons are less susceptible to damage. However, ribbons are not the preferred method of manufacturing semiconductor substrates.

Regardless of the crystal growth technique utilized, standards for substrate parameters, such as flats, orientation, thickness, flatness, surface roughness, total thickness variation, and associated tolerances, will be required. Additionally, electrical (resistivity, doping levels) and crystalline (dislocation density and x-ray rocking curves) requirements will evolve as the device fabrication process matures. Substrates that are round and flat (bow/warp <20  $\mu$ m) with FWHM <50 arc sec and “epi-ready” surfaces should be the immediate focus of the industry. Near term availability of 50 mm substrates will broaden research and development interest, but production will likely demand 100 mm or larger substrates. Both CZ and EFG appear to be well positioned to address near term substrate requirements. Regardless of the advantages melt-based crystal growth processes provide, bulk growth of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is not without significant technical hurdles which are further highlighted below.

## 1. Czochralski (CZ)

Czochralski (CZ) is the *de facto* standard method for manufacturing a variety of large diameter single crystal boules, such as silicon, sapphire, germanium, and gallium arsenide. CZ’s primary attributes are its scalability, manufacturability, and low cost. Due to the high growth temperature (>1800 °C) of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, crucible options are presently limited to iridium due to the high growth temperature and oxidizing environment. The use of iridium introduces significant cost and manufacturing challenges due to susceptibility to oxidation in atmospheres of only a few percent oxygen and decomposition of the melt forming metallic gallium further reacting with the iridium crucible forming eutectic or intermetallic phases.<sup>40</sup> Increasing the oxygen partial pressure can suppress the decomposition of the melt but will subject the iridium crucible to further oxidation. Galazka *et al.* showed that **undoped layers have been shown to be insulating** scale-up of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal size is strongly affected by the formation of metallic gallium in the melt and that scale-up to 100 mm diameter crystals may require oxygen containing atmosphere up to 100%.<sup>33</sup> SYNOPTICS has shown that an atmosphere of 91% CO<sub>2</sub> and 9% O<sub>2</sub> is sufficient for growth of (010) Fe-doped single crystals up to 60 mm in diameter, but crucible lifetime remains an ongoing concern.<sup>28</sup>

### a. Current/future challenges.

- Management of growth atmosphere and melt decomposition.
- Iridium crucible cost and maintainability.
- Diameter scalability to 100 mm and larger.
- Defect identification and mitigation.
- Uniform dimensional, crystalline and electrical parameters.
- Boule and substrate yield.

## 2. Edge defined film fed growth (EFG)

Edge Defined Film Fed Growth (EFG) was originally developed by LaBelle and Mylavski for growth of sapphire ribbons. EFG remains the technology of choice for growth of large sapphire windows and complex geometries. It is not the preferred approach for large scale manufacturing of semiconductor substrates. EFG’s primary attributes are its high growth rates exceeding 10 mm/h, scalability, and manufacturability of large single or multiple ribbons. Iridium crucibles are still required but are less susceptible to oxidation and melt volatilization due to the reduced area of the exposed melt surface. NCT has successfully commercialized EFG for a variety of sizes, orientations, and dopants and demonstrated scalability of (201) substrates up to 150 mm.<sup>38</sup>

### a. Current/future challenges.

- Scalability of (010) oriented substrates beyond 25 mm.
- Manufacturing throughput and cost.
- Defect mitigation.
- Uniform dimensional, crystalline, and electrical parameters.

## 3. Float zone

a. *Optical floating zone (OFZ).* The float zone method is a melt-based technique most commonly used to manufacture high resistivity silicon single crystals up to 200 mm diameter. The OFZ

method is a variation of the float zone method used to grow  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Single crystals of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> are grown without a crucible, enabling the use of high oxygen atmosphere. A uniform polycrystalline rod is required and is readily available for silicon but not for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. High purity  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> powders must be combined with preferred dopant and compacted and sintered to form a suitable rod. The use of an RF heat source is not an option due to the low conductivity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Rather halogen lamps provide the heat source. Villora *et al.* was the first to demonstrate growth of 25 mm in diameter crystals with three differing crystallographic orientations: (100), (010), and (001).<sup>37</sup>  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> single crystals were grown in the [010] direction at a growth rate of 6 mm/h. The OFZ method is not easily scalable beyond 25 mm and as such is not competitive with other melt-based techniques.

#### b. Current/future challenges.

- Diameter scaling severely limited by halogen lamp heat source.
- Doping techniques.
- Industrial research and development commitment.
- Defect identification and mitigation.
- Uniform dimensional, crystalline and electrical parameters.

### 4. Vertical Bridgman

Vertical Bridgman and/or its variants (vertical gradient freeze) are common techniques used in manufacturing III–V single crystals up to 150 mm in diameter. This technique involves the directional solidification of the melt from the hot zone to the cold zone by controlling the movement of the crucible or hot zone. Single crystals can be grown with or without seed utilizing a Pt–Rh alloy crucible, enabling the use of high oxygen atmosphere without risk of crucible oxidation. Diameter control is unnecessary because the diameter is determined by the inner diameter of the crucible. The first application of the vertical Bridgman (VB) method to  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> was demonstrated by Hoshikawa *et al.*, and they reported growth of 25 mm diameter (100) single crystals without a seed in ambient air, with no adhesion of the crystals to the crucible wall.<sup>34</sup> Recent efforts demonstrated 50 mm diameter Sn-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystals with growth orientation perpendicular to the (001) plane utilizing a resistance heating furnace with platinum–rhodium alloy crucibles in ambient air.<sup>29</sup>

#### a. Current/future challenges.

- Scalability of the growth process.
- Industrial research and development commitment.
- Use of a Pt–Rh alloy crucible.
- Defect identification and mitigation.
- Uniform dimensional, crystalline and electrical parameters.

### B. Conclusion

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is a novel ultra-wide bandgap semiconductor that combines high theoretical figure of merits with growth of single crystals with proven manufacturing techniques such as CZ and EFG. While a variety of growth techniques have been utilized to grow  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> single crystals, it is too early in the development cycle to suggest that one technique is superior to competing approaches.

Until such a time that a volume application emerges, it is conceivable for multiple techniques to co-exist. Generally speaking, near term (1–3 years) availability of 50 mm  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates with desired surface orientation, N<sup>+</sup> or semi-insulating ( $>10^8 \Omega \text{ cm}$ ), good crystallinity (FWHM  $<50 \text{ arc sec}$ ), and low defect density ( $<10^4 \text{ cm}^{-2}$ ) should be a goal for the industry going forward. The availability of such substrates should sustain development for several years to follow. Ultimately, a minimum of 100 mm will be required for access and subsequent transition to commercial compound semiconductor foundries. Presently, both CZ and EFG techniques appear to be best positioned to address near term substrate requirements. The extent of research and development of these techniques exceeds other approaches. EFG substrates produced by NCT have been commercially available for several years. CZ substrates from SYNOPTICS have become commercially available in 2021. EFG is not the preferred approach for semiconductor substrate manufacturing, but it could address  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> requirements for non-(010) oriented substrates. CZ has a long history of scalability and low-cost manufacturing; there will always be a preference for CZ. However, CZ faces unique challenges not faced with other techniques. Galazka *et al.* showed that CZ scalability will be dictated by the ability to control the growth environment such that melt decomposition and crucible oxidation are mitigated, enabling a cost-effective manufacturing process. The recent market spike in iridium prices could impact development and manufacturing. Vertical Bridgman remains an attractive approach notwithstanding the lack of a stronger industrial developmental commitment as well as addressing the added cost Pt–Rh alloy crucibles. The commercial availability of native larger diameter  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates are critical to the long-term development of this novel ultra-wide bandgap semiconductor technology.

## VI. MOLECULAR BEAM EPITAXY

### Oliver Bierwagen

#### A. Status

Close to a decade ago, the research field of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>-based power electronics got started by the seminal work of Higashiwaki *et al.*,<sup>27</sup> describing the theoretical potential of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> coupled with the demonstration of a MESFET device with high breakdown voltage. This demonstrator device was based on a homoepitaxial, Sn-doped layer grown by molecular beam epitaxy (MBE) on a (010)-oriented, semi-insulating, Fe-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate. It has to be stressed that the availability of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate from bulk growth enables the homoepitaxial growth of functional layers by MBE and other film growth techniques with highest structural quality. Living up to its pioneering role by realizing high quality layers with simpler growth chemistry than metal organic vapor phase epitaxy (MOVPE)/MOCVD, the MBE growth of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has evolved rapidly in the past years: homoepitaxy has been demonstrated with growth rates up to few nm/min on the available orientations [(100), (010), (001), and ( $\bar{2}01$ )].<sup>45,46</sup> Undoped layers have been shown to be insulating,<sup>47</sup> and the n-type conductivity has been controlled by donor doping with Sn,<sup>31,48</sup> Ge,<sup>49</sup> and Si<sup>50</sup> up

to electron concentrations of  $10^{20} \text{ cm}^{-3}$ . Widening the bandgap<sup>51</sup> by alloying with  $\text{Al}_2\text{O}_3$ <sup>52</sup> enabled the MBE-growth of modulation-doped  $(\text{Al,Ga})_2\text{O}_3/\text{Ga}_2\text{O}_3$  single<sup>53</sup> and double<sup>54</sup> heterostructures that confine a two-dimensional electron gas (2DEG). With average breakdown fields of  $\sim 3 \text{ MV/cm}$ , these high-electron-mobility transistor (HEMT) structures are promising candidates for high frequency and high-power device applications.

Despite these advances, a number of challenges need to be addressed for MBE-grown layers to be used in competitive power electronics devices. Some of these challenges are specific to MBE, whereas others are universally observed.

## B. Current and future challenges

General challenges for the epitaxy of  $\beta\text{-Ga}_2\text{O}_3$  relate to *extended structural defects* in the film, the *film morphology* that deviates from a flat surface, as well as *limits for the alloy composition* of  $(\text{Al,Ga})_2\text{O}_3$  and  $(\text{In,Ga})_2\text{O}_3$  with consequences on band-offsets and electron confinement. The low symmetry of the monoclinic crystal structure and related anisotropy plays an important role for most of these general challenges posing the question of “the ideal” surface orientation for devices and epitaxial film growth. As mentioned earlier, this has ramifications with respect to bulk orientation preference as well. Challenges more specific to MBE concern *the growth rate*, as well as *doping* by intentional and unintentional impurities as well as possibly point defects.

### 1. MBE: Growth rate

In comparison to other epitaxial techniques, MBE is usually limited to comparably low growth rates, which are sufficient for horizontal devices but too small for vertical devices requiring thick (e.g.,  $>5 \mu\text{m}$ ) layers. Conventionally, the MBE growth of  $\beta\text{-Ga}_2\text{O}_3$  is realized by the reaction of Ga vapor with reactive oxygen (ozone or plasma) on the heated substrate surface in a high-vacuum environment. Unlike in the MBE of GaAs or GaN, the MBE growth rate and temperature of  $\text{Ga}_2\text{O}_3$  are strongly limited by temperature-driven desorption of the volatile suboxide  $\text{Ga}_2\text{O}$  (instead of Ga) that is formed as an intermediate reaction product on the substrate before further oxidation to  $\text{Ga}_2\text{O}_3$ .<sup>55</sup> The strong anisotropy of the surface free energy<sup>56</sup> and related bonding strength to adatoms (e.g., Ga) or ad-molecules (e.g.,  $\text{Ga}_2\text{O}$ ) results in a strong dependence of the growth-rate limiting suboxide desorption on surface orientation with the resulting largest growth rate ( $3 \text{ nm/min}$ ) and surface free energy for the (010) surface and smallest ones ( $0.17 \text{ nm/min}$ ) for (100) as well as a typical limit of  $750^\circ\text{C}$  for the growth temperature.<sup>31,57</sup> Recently, an exceptionally high growth rate of  $7 \text{ nm/min}$  has been reported for the (010) surface at a growth temperature of  $700^\circ\text{C}$ .<sup>58</sup> A catalytic growth mechanism that is based on the easy oxidation of a co-supplied catalyst vapor (i.e., In<sup>59</sup> or Sn<sup>60</sup>), and subsequent thermodynamically driven exchange of the catalyst metal ion by Ga, has been identified in heteroepitaxy and has been termed metal-exchange catalysis<sup>59</sup> (MEXCAT) or metal-oxide catalyzed epitaxy (MOCATAXY).<sup>61</sup> In its In-mediated variety, this mechanism has been demonstrated to enable significantly higher growth rates and temperatures than conventional MBE for the (010), (001),  $(\bar{2}01)$ , and (100) orientations,<sup>45,48,62</sup> e.g.,  $1.5 \text{ nm/min}$  (100)<sup>62</sup> or  $5 \text{ nm/min}$  (010)<sup>48</sup> at temperatures up to  $950^\circ\text{C}$ . Significantly higher growth rates of  $25 \text{ nm/min}$  have recently

been reported for the homoepitaxy on (010) oriented substrates by suboxide-MBE (S-MBE), i.e., providing  $\text{Ga}_2\text{O}$  instead of Ga from the source, at growth temperatures as low as  $550^\circ\text{C}$ .<sup>63</sup> Despite the low growth temperature, the layers had a high structural quality, which may be related to the simpler one-step growth kinetics involving just the oxidation of the supplied suboxide on the substrate. The high suboxide fluxes, required for this growth rate, are realized by a mixed Ga +  $\text{Ga}_2\text{O}_3$  charge in the effusion cell and exceed the Ga flux from a pure Ga or  $\text{Ga}_2\text{O}_3$  charge significantly at given cell temperature.<sup>64</sup>

n-type doping has been successfully demonstrated for conventional MBE<sup>31,57</sup> and MOCATAXY.<sup>48</sup> To prove suitable for the growth of thick layers used in vertical devices, higher growth rates in MEXCAT-MBE/MOCATAXY, e.g., by scaling up the fluxes, or successful donor doping with high electron mobilities in S-MBE needs to be demonstrated.

### 2. MBE: Electrical quality doping, purity, and point defects

When it comes to power electronics devices, well-defined donor concentrations are required that should be uncompensated to achieve high electron mobilities. Drift regions of vertical devices are most demanding in this respect as they require particularly low donor concentrations. These requirements translate into the need of a good control on intentional doping with simultaneous absence of unintentional doping.

Intentional donor doping of MBE-grown  $\beta\text{-Ga}_2\text{O}_3$  has been demonstrated with Sn, Ge, and Si but comes with related challenges, summarized in Table III. Figure 9 summarizes published data on the Hall electron mobility as a function of Hall electron concentration categorized by dopant and flavor of MBE in comparison to the highest published mobilities from Si-doped MOCVD/MOVPE-grown films as well as the empirical mobility limit based on the highest measured Hall electron mobilities in  $\beta\text{-Ga}_2\text{O}_3$ .

Sn doping can be quite well controlled using the Sn or  $\text{SnO}_2$  source material and covers the widest range of electron concentrations, but the mobilities are consistently below the empirical mobility limit, likely related to the large donor activation energy.<sup>46</sup> Dopant segregation, in agreement with the metal-exchange catalyzing effect of Sn,<sup>60</sup> compromises the controllability under standard MBE conditions but can be avoided using Sn-doping during In-catalyzed MOCATAXY at elevated growth temperature, which results in similar electron mobilities to that of standard MBE.<sup>46</sup> In comparison, Ge doping seems to produce higher electron mobilities, but the incorporation of the dopant was found to be strongly depending on the MBE growth conditions, compromising the controllability.<sup>49</sup> The highest reported electron mobilities were realized by Si-doped, MOCVD/MOVPE-grown films, suggesting Si to be the electronically best suited donor cation. The control of Si-doping in oxide MBE, however, is challenged by source oxidation resulting in drift of the Si flux, which is why only delta-doped layers have been reported historically.<sup>50</sup> Their electron mobilities exceed those of homogeneously doped films since the electron wavefunction spreads out into donor-free film regions, resulting in significantly decreased ionized impurity scattering. More recently, AFRL has demonstrated Si-doped homoepitaxy.<sup>69</sup> To complicate doping with Si, it has been found to be mediated by the formation and evaporation of the suboxide  $\text{SiO}$  instead of elemental Si from the source, resulting in



TABLE III. Comparison of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> bulk growth techniques.

Technique	Boule diameter	Surface orientation	Crucible material	Doping	Manufacturability	Commercial availability	References
CZ	25/50 mm	(010)(010)/(100)/(001)	Ir	Fe	Good	SYNOPTICS research	33 and 39–41
	100 mm	(001)	Ir	Mg/Sn/Si	N/A		
	50 mm	(001)	Ir	Sn	Good	NCT	
EFG	50 mm	(201)	Ir	Sn/UID/Fe	Good	NCT	26 and 38
	25 × 25 mm <sup>2</sup>	(010)	Ir	Fe	Good		
	10 × 15 mm <sup>2</sup>	(001)/(010)/( $\bar{2}$ 01)	Ir	Sn/UID/Fe	Good		
FZ	50 mm	(100)	None	Sn	N/A	Research	37 and 42
	<25 mm	(100)	None	Fe	N/A	Research	
VB	25 mm	(100)	Pt–Rh	Sn	N/A	Research	29 and 34
	50 mm	(001)	Pt–Rh		N/A	Research	

a dopant flux that depends on the background oxygen pressure rather than the cell temperature.<sup>70</sup> Table IV can be referenced for a qualitative summary of the pros and cons of dopant type.

Unintentional doping by variety of sources has been reported for MBE-grown films. In particular, unintentional Si-doping has been identified to severely limit the lowest achievable donor concentration in MBE-growth films, possibly explaining why electron concentrations in MBE-grown layers significantly exceed the lowest one reported for an unintentionally doped MOCVD grown layer<sup>66</sup> [indicated as “unintentionally doped (UID)” in Fig. 9]. SiO bypassing the cell shutter of the Si source<sup>71</sup> and Si species from the quartz cavity of the oxygen plasma source<sup>71,72</sup> were identified as primary sources of unintentional Si. Si accumulation at the substrate/film interface may also arise from the typically performed oxygen plasma-treatment before growth or from contaminations on the substrate surface

but can be mitigated by Ga-polishing prior to growth<sup>53</sup> or intentional doping by the deep acceptor Fe.<sup>73</sup> Moreover, unintentional incorporation of N as a compensating acceptor has been associated with the use of a plasma-source<sup>72</sup> but also enabled the formation of a normally off MOSFET. Another source of unintentional acceptors are the Fe-doped, semi-insulating substrates that lead to Fe segregation during MBE growth by riding the growth front.<sup>74</sup> Thick UID buffer layers were found to be essential in improving the performance of FETs by reducing the Fe-concentration near the channel,<sup>75</sup> and low growth temperatures allow reducing the surface-riding Fe by increasing its incorporation into the layer.<sup>74</sup> Consequently, the generally larger thickness of layers grown by MOCVD/MOVPE may also explain their often higher electron mobilities.

Future work to improve the control of Si-doping may involve the intentional use of SiO sources realized by mixtures of Si and SiO<sub>2</sub><sup>64</sup> or the direct use of the SiO source material.<sup>76</sup> Unintentional N and Si-doping may be further mitigated by the use of O<sub>3</sub> instead of O-plasma sources. The purity of the used source material—especially when oxide sources are used—should always be a concern. Successful doping in S-MBE growth is still to be realized. Intentional doping by deep acceptors may be helpful in the purposeful implementation of normally off devices or semi-insulating layers. Point defects, such as donor-like Ga-interstitials or O-vacancies as well as acceptor-like Ga-vacancies, need to be investigated and may be controlled by purposefully using Ga-rich or O-rich growth conditions. Finally, anion site doping is largely unexplored but may help increase electron mobility by placing the ionized donor on the atom that does not contribute to the conduction band minimum.

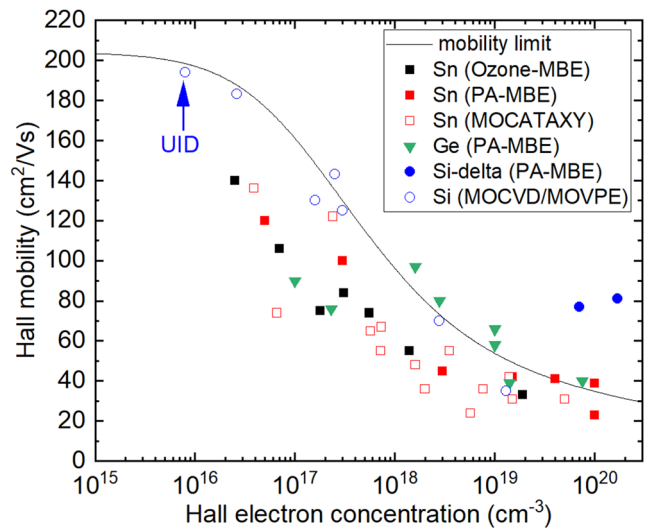


FIG. 9. Overview of Hall electron mobility as a function of Hall electron concentration for MBE-grown films compared to the empirical mobility limit. The growth method is given in parentheses. Data sources: “Sn (ozone-MBE),”<sup>31</sup> “Sn (PA-MBE),”<sup>46,49</sup> “Sn (MOCATAXY),”<sup>48</sup> “Ge (PA-MBE),”<sup>49</sup> “Si-delta (PA-MBE),”<sup>50</sup> and “Si (MOCVD/MOVPE),”<sup>32,65</sup> “UID,”<sup>66,67</sup> “mobility limit.”<sup>68</sup>

TABLE IV. Pros (“+”) and Cons (“–”) of the different donor dopants used in the MBE of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. “o” denotes in between pros and cons, and “?” denotes insufficient data to draw conclusions.

Dopant	Electron mobility	Source control	Incorporation stability
Si	+	–	+
Ge	+	?	–
Sn	–	+	o

### 3. Epitaxy: Crystallinity and extended defects

Despite the use of homoepitaxy, on some surface orientations, the low symmetry of the monoclinic structure can result in twin formation irrespective of the epitaxial method due to possible double positioning of Ga atoms and island coalescence. Such twins have been reported for the MBE growth on (100)<sup>77</sup> and  $\bar{(201)}$ <sup>45,78</sup> oriented substrates. The incoherent twin boundaries forming upon island coalescence are detrimental to the electrical properties of the layers as they can trap electrons, leading to a drastically decreased electron mobility and doping efficiency.<sup>79</sup> The growth on (010) and (001) oriented substrates is not affected by this problem and results in layers with high structural quality.<sup>45</sup>

As already demonstrated for the growth by MOVPE,<sup>56</sup> the use of (100)-oriented substrates off-cut into the  $-c$ -direction prevents the double positioning and twin formation through consistent nucleation at the (201)-type step also in In-mediated MEXCAT-MBE.<sup>62</sup>

On  $\bar{(201)}$ -oriented substrates, a reduction of the density of twin boundaries by increasing the MBE growth temperature has been reported,<sup>78</sup> yet the application of a proper offcut for complete removal of such twins remains to be determined. Heteroepitaxial  $\text{Ga}_2\text{O}_3/\bar{(201)}$  films free of rotational domains and with high electrical quality have been successfully grown by low-pressure chemical vapor deposition by virtue of  $\text{Al}_2\text{O}_3(001)$  substrates offcut into the  $\langle 110 \rangle$  direction,<sup>80</sup> providing a blueprint for the homoepitaxy of untwinned  $\beta\text{-Ga}_2\text{O}_3/\bar{(201)}$  films.

### 4. Epitaxy: Surface and interface morphology

Horizontal devices benefit from smooth growth surfaces that enable sharp heterointerfaces as well as delta-doping profiles through higher mobilities of the confined electrons due to reduced interface roughness scattering. Irrespective of the epitaxial technique, rough morphologies of the growth surface can arise from island coalescence and facet formation. The former one has been prevented by step-flow growth, demonstrated on (100)-oriented substrates with suitable offcut into the  $+c/-c$  direction by MBE,<sup>81</sup> MEXCAT-MBE,<sup>62</sup> or MOVPE.<sup>82</sup> Similarly, a slight offcut into the  $+c/-c$  has been reported to prevent roughness from island coalescence on (010)-oriented substrates by MBE and MEXCAT-MBE.<sup>83</sup> Notwithstanding, surface faceting, typically visible as morphological features (other than monolayer steps) elongated into a particular crystalline in-plane direction, can be generally observed for epitaxial films grown on all but (100)-oriented substrates. In the case of (010) films,<sup>84</sup> these facets were identified to be (110) and  $\bar{(110)}$  oriented, suggesting these orientations to have lower surface free energy than the (010) one. Initial growth experiments on (110)-oriented substrates<sup>85</sup> revealed surface roughness that could be related to island coalescence or faceting, thus calling for more in-depth growth studies on this orientation.

Future work to optimize surface and interface morphology is needed to enable step flow growth and prevent faceting on all surface orientations other than the (100) one, particularly the (001) and (010).

### 5. Epitaxy: Alloys and heterostructures

Low loss power devices for high frequency operation are horizontal devices with high electron mobility and high sheet electron

density. Such devices are best realized by modulation-doped field-effect transistors (MODFETs) hosting a two-dimensional electron gas (2DEG) in a quantum well structure, such as that formed at a single heterointerface. The on-resistance of MODFETs depends critically on the maximum sheet electron density in the 2DEG (that can be achieved without parallel conducting channel), which is proportional to the conduction band offset (CBO) between the channel and barrier material. MODFETs have so far been realized by  $\beta\text{-Ga}_2\text{O}_3$  channels and pseudomorphically strained  $(\text{Al}_x\text{Ga}_{1-x})_2\text{O}_3$  barriers with the highest reported 2DEG density of  $4.7 \times 10^{12} \text{ cm}^{-2}$  at an effective mobility of  $150 \text{ cm}^2/\text{Vs}$  for a barrier with Al content of  $x = 17\%$  grown on (010) oriented  $\beta\text{-Ga}_2\text{O}_3$  wafers.<sup>73</sup> Increasing the Al content  $x$  has been experimentally<sup>86</sup> and theoretically<sup>87</sup> shown to increase the CBO between  $\beta\text{-Ga}_2\text{O}_3$  and  $\beta\text{-(Al}_x\text{Ga}_{1-x})_2\text{O}_3$  but  $x$  has so far been practically limited by phase separation or strain relaxation to values below 20% on (010) oriented substrates.<sup>52</sup>

Harnessing the anisotropy of the  $\beta\text{-Ga}_2\text{O}_3$  crystal structure and related properties provides a huge potential for increasing the CBO: For example, (100) oriented  $\beta\text{-(Al}_x\text{Ga}_{1-x})_2\text{O}_3/\text{Ga}_2\text{O}_3$  structures have been predicted by theory to have a higher CBO<sup>88</sup> and sustain a higher critical thickness for layer cracking<sup>89</sup> than differently oriented ones at the same  $x$ . In addition, reports on MBE grown  $(\text{Al}_{0.61}\text{Ga}_{0.39})_2\text{O}_3(100)$  layers<sup>90</sup> and MOCVD grown  $(\text{Al}_{0.48}\text{Ga}_{0.52})_2\text{O}_3/\bar{(201)}$  layer<sup>86</sup> suggest that appropriate growth conditions can stabilize high Al-contents. A further increase in the CBO can be achieved by using an  $(\text{In}_x\text{Ga}_{1-x})_2\text{O}_3$  channel layer whose conduction band minimum is theoretically predicted to be below that of  $\text{Ga}_2\text{O}_3$  but whose lower bandgap<sup>91</sup> likely comes with a decreased breakdown field. Finally, the use of double heterostructures with the channel layer sandwiched between two barrier layers allows us to increase the 2DEG density above that achievable by single heterostructures.<sup>54</sup> *In situ* growth of dielectric layers for MOSFET applications has not yet been explored.

### C. Concluding remarks

MBE has undoubtedly pioneered  $\beta\text{-Ga}_2\text{O}_3$ -related power devices and may keep doing so by using its versatility. For example, the simple chemistry, involving only cations and oxygen, enables the uncomplicated exploration of new dopants, and the general ability to grow crystalline and amorphous layers enables the exploration of dielectrics for all-MBE-grown device stacks. To date, however, MOCVD/MOVPE has caught up overcoming MBE in terms of growth rate and purity, leaving the domain of lateral devices based on heterostructures requiring high precision on the layer thickness for MBE. To gain relevance for vertical devices and the related thick  $\beta\text{-Ga}_2\text{O}_3$  layers, effective doping in suboxide MBE and further increased growth rates in MEXCAT-MBE/MOCATAXY would have to be demonstrated. The doping control, particularly that of Si, and the removal of unintentional dopants need to be improved. Based on the still limited number of growth studies, the optimum wafer orientation for epitaxy depends on the target application; (010) yielding the highest growth rates is preferable for (thick) vertical devices, but (001), available as large area substrates, can achieve similarly high growth rates in MEXCAT-MBE, and (100) offcut toward [001] is theoretically superior for lateral heterostructure devices calling for further exploration.



## VII. METALORGANIC VAPOR PHASE EPITAXY

Sriram Krishnamoorthy

### A. Status

Rapid advances have been made over the last few years in metal organic vapor phase epitaxy (MOVPE) homoepitaxial growth of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub>, clearly establishing the promise of the MOVPE growth technique for high performance lateral and vertical power device applications. Growth rates [(010) orientation unless otherwise specified] up to 10  $\mu\text{m/h}$ ,<sup>92</sup> unintentional doping as low as  $7.4 \times 10^{15} \text{ cm}^{-3}$  with a room temperature mobility of 176  $\text{cm}^2/\text{Vs}$ ,<sup>66</sup> low temperature (46 K) electron mobility exceeding  $10^4 \text{ cm}^2/\text{Vs}$ ,<sup>93</sup> low  $10^{14} \text{ cm}^{-3}$  free carrier concentration using N<sub>2</sub>O as the oxygen precursor,<sup>94</sup> low temperature epitaxy with an unintentional electron concentration of  $2 \times 10^{16} \text{ cm}^{-3}$  and a room temperature mobility of 186  $\text{cm}^2/\text{Vs}$ ,<sup>95</sup> record high electron mobility of 194  $\text{cm}^2/\text{Vs}$  at an electron concentration of  $8 \times 10^{15} \text{ cm}^{-3}$ ,<sup>67</sup> and low point defect concentrations in MOVPE-grown  $\beta$ -Ga<sub>2</sub>O<sub>3</sub><sup>96</sup> have already been demonstrated. Finally, a high Hall mobility of 153  $\text{cm}^2/\text{Vs}$  has been measured for the (100) orientation at a carrier concentration of  $1.4 \times 10^{17} \text{ cm}^{-3}$ , achieved via control of twins and stacking faults.<sup>65</sup> Controlled n-type doping with a wide range of electron concentration ( $10^{16}$ – $10^{20} \text{ cm}^{-3}$ ), with high mobility values compared to other epitaxial techniques, has been reported in homoepitaxial (010)-oriented  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> by several groups. Despite the significant early progress in MOVPE homoepitaxy, the understanding of the growth science toward achieving the ultimate limits of material quality relevant for medium voltage and high voltage vertical devices is still a very open question. In this article, we focus on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> homoepitaxial growth to leverage the availability of bulk substrates. Some of the pertinent research challenges are discussed below.

### B. Current and future challenges

#### 1. Substrate orientation and growth window

The choice of the substrate and epilayer orientation could be very important, as the impact ionization parameters could have a dependence on the crystal orientation. Growth along the (100) orientation is particularly challenging due to the observation of independent nucleation of two-dimensional islands causing double positioning on the (100) plane leading to twin lamellae and stacking faults.<sup>82</sup> In order to prevent the twinning promoted by transformation of (001)-B facets into ( $\bar{2}$ 01) facets,<sup>56</sup> homoepitaxial growth on the (100) substrate has been shown to favor a 6° miscut toward [00 $\bar{1}$ ]<sup>82</sup> but has also been demonstrated with as low as 2°.<sup>97</sup> The offcut angle has been reduced to 2° to conserve material during boule slicing by altering growth conditions to increase the diffusion length on the 100 surface.<sup>97</sup> Such defect generation has also been observed in homoepitaxial ( $\bar{2}$ 01)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, resulting in severe charge compensation.<sup>98</sup> It should be noted that (001) and ( $\bar{2}$ 01) orientations offer the largest area substrate (up to 6 in. slabs) available currently,<sup>38</sup> but the growth along these orientations are less explored. Vicinal substrates with a specific offcut direction could play an important

role in eliminating twin boundaries and achieving superior material quality, including the considerations of the anisotropic diffusion lengths and faceting. A comprehensive understanding of the growth phase diagram and the growth window is still lacking, although preliminary studies indicate a much larger growth window<sup>95</sup> for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. The growth window could potentially be further expanded using approaches, such as MOCATAXY, which is currently unexplored in MOVPE growth. Epitaxy for vertical power device drift layers necessitates understanding of the growth processes and the evolution of surface morphology at high growth rates while simultaneously maintaining high material quality. Understanding of the high growth rate regime ( $>5 \mu\text{m/h}$  growth rate) relevant for vertical devices needs to be explored to understand and control step bunching, step meandering, and other morphological instabilities that could exacerbate growth front roughening. Growth uniformity over a large substrate area needs to be studied. An understanding of the growth processes<sup>99</sup> is required at the fundamental level via detailed studies of adatom adsorption, desorption, anisotropic diffusion lengths, nucleation processes, and growth velocities on various growth orientations as a function of growth conditions via *in situ* and *ex situ* characterization and quantitative kinetic growth modeling approaches.

#### 2. Material purity

A vertical power device with high voltage blocking capability requires low-doped drift regions. Vertical devices with high blocking voltage necessitate a high electron mobility drift layer with controlled ultra-low n-type doping with negligible acceptor compensation, minimized intrinsic defects, and external impurities. The low compensating acceptor concentration ( $<10^{14} \text{ cm}^{-2}$ ) in homoepitaxial (010)-oriented  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>,<sup>100</sup> even at this early stage of materials development, offers the tantalizing possibility of achieving ultra-low doped ( $10^{13}$ – $10^{15} \text{ cm}^{-3}$ ) drift layers suitable for medium voltage applications. At such low doping regimes, it is critical to understand and control intentional and unintentional impurity incorporation. Currently, the unintentional doping appears to be limited by unintentional silicon incorporation.<sup>67</sup> However, detailed understanding of impurities and impurity incorporation is not available. The role of carbon that could incorporate from the metal-organic source is yet to be understood experimentally. The origin and the limits of unintentional donors and compensating acceptors needs to be thoroughly understood. The ultimate low-doping concentration that can be achieved will be eventually limited by the lowest possible concentration of compensating acceptors. Material purity is expected to be a strong function of the growth regime and the choice of gallium and oxygen precursors. The very low concentration regime relevant to the evaluation of material purity necessitates innovative characterization techniques.

#### 3. Dopants and defects

Silicon has showed promising performance as a donor, and the other donor candidates, such as Ge, Sn, Zr, and Hf, are less explored in the context of MOVPE growth. The effect of growth conditions and precursors (metal-organic precursors vs gas sources) on dopant incorporation, segregation, and dopant substitution in crystallographically distinct sites remain to be studied in detail. While

achieving appreciable hole concentration and hole conduction is an open challenge, the detailed study of Mg-doped,<sup>101</sup> Fe-doped, and N-doped Ga<sub>2</sub>O<sub>3</sub> epitaxial layers can enable controlled energy barriers in device structures for electric field management and current blocking capabilities. The interplay between doping and point defects remain to be explored in a comprehensive manner. It is furthermore critically important to study the doped drift layer material under high electric fields and high temperatures to understand defect formation, annihilation, and defect transport under extreme conditions.

#### 4. Alloys and heterostructures

The ability to form heterostructures in the (Al,Ga,In)<sub>2</sub>O<sub>3</sub> material system sets it apart from other (U)WBG materials, such as SiC and diamond.  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> with Al content  $x$  upto ~26%–27% has also been demonstrated in the (010) orientation.<sup>102</sup> A high aluminum concentration up to 52% has been reported in the case of the growth of (100)-oriented AGO,<sup>86</sup> with a band offset as high as 1.2 eV at the AGO/GO interface.<sup>86</sup> Degenerate doping of (Al<sub>0.26</sub>Ga<sub>0.74</sub>)<sub>2</sub>O<sub>3</sub> with a resistivity as low as 2.6 m $\Omega$  cm<sup>103</sup> is comparable or better than the lowest resistivity achieved in ultrawide bandgap semiconductors with similar bandgap (Al<sub>0.7</sub>Ga<sub>0.3</sub>N).<sup>104</sup> Furthermore, delta doping with electron concentration in the range of  $2\text{--}8 \times 10^{12}$  cm<sup>-2</sup> with a sharp apparent charge profile enabled by low temperature epitaxy and AGO/GO heterostructure channels with a room temperature sheet resistance as low as 5.3 k $\Omega$ /□ including contribution from a parallel channel in AGO has been reported.<sup>105</sup> To realize the predicted high electron mobility 2DEG channels,<sup>106</sup> it is important to achieve high quality AGO/GO heterojunctions with highest band offsets that can enable confinement of  $>5 \times 10^{12}$  cm<sup>-3</sup> 2DEGs, which requires maximized aluminum content in the barrier. Transport properties, phase purity, and defects in films with aluminum content more than 26% have not been studied yet. Uniform doping and delta doping control in AGO, segregation of dopants, activation energy of dopants and modulation efficiency in AGO/GO heterostructures needs to be explored thoroughly to investigate the potential and limitations of GO 2DEG channels. In addition to crystalline heterojunctions, *in situ* MOCVD-grown dielectrics<sup>107</sup> can potentially offer the superior dielectric/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface with a low density of interface trap states.

#### C. Concluding remarks

The advances in the MOVPE homoepitaxial growth of high-quality thin films and heterostructures are very impressive, considering that the efforts are fairly recent. The highest electron mobility achieved in epitaxial films, the outstanding low temperature mobility, and the low concentration of extracted compensating acceptors make MOVPE a very attractive epitaxial technique for future high-performance devices. Although early strides are being made, a comprehensive understanding of the growth phase diagram is yet to be undertaken. With the extensive exploration of the growth science and understanding of the limits of material purity and doping control, MOVPE can enable a scalable pathway toward high performance lateral and vertical diodes and transistors.

### VIII. OTHER GROWTH METHODS: HALIDE VAPOR PHASE EPITAXY, LOW PRESSURE CHEMICAL VAPOR DEPOSITION, MIST CHEMICAL VAPOR DEPOSITION, AND PULSED LASER DEPOSITION

Kevin Leedy

#### A. Status

The epitaxial growth methods of MBE and MOCVD have attracted significant interest in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> research as discussed previously. Both techniques have yielded films with a wide range of doping control and the added benefit of being commonplace equipment sets in commercial device foundries. They are not without their limitations, however, including high deposition temperatures, slow deposition rates, and high capital equipment expense. Additional growth techniques, such as halide vapor phase epitaxy (HVPE), low pressure chemical vapor deposition (LPCVD), mist chemical vapor deposition (Mist-CVD), and pulsed laser deposition (PLD), have generated comparable epitaxial film results with compelling benefits including low deposition temperatures, large carrier concentration ranges, wide range of alloying, high deposition rates, and relatively inexpensive equipment. Although significant progress has been made in demonstrating initial epitaxial films from these deposition techniques, overall epitaxial film development remains at an early stage.

An increased understanding of epitaxial growth parameters and control of film properties is required to yield the high-quality films necessary to realize the full potential of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> in commercial semiconductor devices. In addition, sustained implementation of consistent and high-quality material in devices is lacking. An overarching goal is to achieve control of active carrier density with maximized electron mobility. Additional key obstacles to overcome in epitaxial growth include growth rate and alloy and phase control. Driven by  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> native substrate availability with increasing substrate diameters, homoepitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> film growth has attracted the most interest associated with lowest defect densities. Indeed, homoepitaxial growth is crucial to capitalize on the superior crystal quality only achieved through growth on native substrates. Concomitant development of native substrates, including comprehensive analyses of growth surfaces, subsurface damage, cleave planes, and impurities, is essential to enable further improvements in film quality. Although a major emphasis is placed on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> homoepitaxial film growth, heteroepitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> films and other Ga<sub>2</sub>O<sub>3</sub> phases have high value and must also be thoroughly investigated to fully exploit the benefits of Ga<sub>2</sub>O<sub>3</sub>.

#### B. Current and future challenges

##### 1. Halide vapor phase epitaxy

For vertical device power applications requiring thick and unintentionally doped (UID)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> drift layers, HVPE produces some of the highest quality epitaxial films.<sup>108</sup> Low H and C impurity incorporation translates to excellent UID films. HVPE is particularly notable for fast growth rates  $>20$   $\mu$ m/h enabling thick films.<sup>5,109</sup> Commercially available HVPE films on 100 mm diameter substrates are available. Schottky barrier diodes were produced

with 12  $\mu\text{m}$   $\beta\text{-Ga}_2\text{O}_3$  capitalizing on the high material purity.<sup>30</sup> As shown in Fig. 10, films with  $10^{15}\text{ cm}^{-3}$  carriers have been fabricated and more recent efforts have also achieved a doping range up to  $10^{19}\text{ cm}^{-3}$ .<sup>5,109,110</sup> Heteroepitaxy and growth of multiple  $\text{Ga}_2\text{O}_3$  phases have also been demonstrated.<sup>109</sup>

Challenges to be addressed in HVPE include high film surface roughness requiring post-deposition chemical-mechanical processing and high deposition temperatures which could allow unintentional diffusion of species between the film and substrate. HVPE also has significant issues with doping and thickness uniformity. As HVPE  $\beta\text{-Ga}_2\text{O}_3$  is a Cl-based growth process, the potential incorporation of Cl in films must be considered. Prior to successful deposition, substrates require a suitably controlled miscut and have minimal subsurface damage.<sup>109</sup> Improvements in substrate chemical-mechanical polishing are likely required to achieve consistent epi-ready surfaces. In addition, HVPE is performed in custom equipment and hence requires further development to establish a multi-wafer and repeatable commercial deposition process. Low thickness uniformity across the substrate diameter is a known issue that could be addressed with improved injector nozzle designs. Finally, more widespread studies of film growth, and device integration, are vital to fully demonstrate the potential of HVPE.

## 2. Low pressure chemical vapor deposition

LPCVD has intriguing potential to substantially impact the  $\beta\text{-Ga}_2\text{O}_3$  power device community by capitalizing on several key features. First, LPCVD utilizes a simple and relatively inexpensive equipment configuration that is well understood and adopted in commercial batch reactor semiconductor device fabrication facilities. Second, LPCVD exhibits fast and tunable growth rates up to 35  $\mu\text{m}/\text{h}$  although at the expense of higher rms surface roughness (3–5 nm) achieved with other epitaxial growth techniques.<sup>5,115</sup> The higher growth rates are conducive to fabrication of thicker films necessary for drift layers in vertical devices; Schottky barrier diodes have

been demonstrated.<sup>5</sup> Finally, homoepitaxial films and heteroepitaxial films on sapphire have been fabricated with Si doping to achieve carrier concentrations up to  $10^{19}\text{ cm}^{-3}$ , as shown in Fig. 10.<sup>5,80,112</sup> For unintentional doped films, a homoepitaxial film with a high Hall mobility of  $156\text{ cm}^2/\text{Vs}$  and  $3 \times 10^{16}\text{ cm}^{-3}$  concentration compares quite favorably with the results from HVPE and trails only MOCVD data for the highest recorded mobility to date.<sup>112</sup>

Challenges for LPCVD are focused on films with high film surface roughness, which may necessitate chemical-mechanical polishing prior to device fabrication, and high deposition temperatures up to  $1050^\circ\text{C}$ , which may exacerbate elemental diffusion, both similar to HVPE limitations. However, the high surface roughness in  $\sim 10\text{ }\mu\text{m}$  thick films fabricated by LPCVD and HVPE may also be expected from any deposition technique capable of producing these thicknesses. Since the overwhelming majority of  $\beta\text{-Ga}_2\text{O}_3$  LPCVD results to date comes from one institution, additional studies on epitaxial film growth and properties, as well as device insertion, by others in the research community are vital to validate reproducibility and, thus, more fully realize the benefits of  $\beta\text{-Ga}_2\text{O}_3$ .

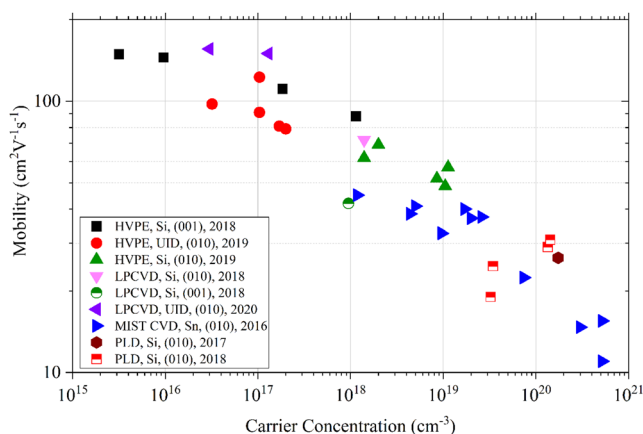
## 3. Mist chemical vapor deposition

A variant of CVD referred to as mist-CVD has been used to deposit thin films of multiple  $\text{Ga}_2\text{O}_3$  phases and associated alloys. While the  $\beta\text{-Ga}_2\text{O}_3$  phase is the focus for power devices in this Roadmap, most of the published  $\text{Ga}_2\text{O}_3$  work using mist-CVD centers on heteroepitaxial growth of the metastable  $\alpha\text{-Ga}_2\text{O}_3$  phase and numerous heterostructures with Al and In on sapphire. Heteroepitaxy studies of  $\alpha\text{-Ga}_2\text{O}_3$  emphasize the larger bandgap, higher breakdown strength, and utility of inexpensive, similar-lattice sapphire substrates.<sup>5</sup> The  $\alpha\text{-Ga}_2\text{O}_3$  films are implemented in commercially available Schottky barrier diodes with a specific on-resistance of  $0.1\text{ m}\Omega\text{ cm}^2$ .<sup>116</sup> Transport results from  $\beta\text{-Ga}_2\text{O}_3$  homoepitaxial films with an electron concentration range of  $10^{18}\text{--}10^{20}\text{ cm}^{-3}$  shown in Fig. 10 demonstrate dopant control in mist-CVD on native substrates.<sup>117</sup> The atmospheric pressure, solution-based deposition process is scalable, simple, and of low cost compared to vacuum based epitaxial growth methods.

However, mist-CVD utilizes custom equipment typically associated with a newer deposition process and is far from adaptation as a commercial multi-wafer and substrate-scalable deposition capability, such as MOCVD. Heteroepitaxial growth inherently possesses higher defect densities than homoepitaxial films, the impact of which has not been thoroughly characterized by the community. High impurity concentrations and high growth temperatures are commonly associated with solution-based growth methods, such as mist-CVD.<sup>118</sup> Implementation of C-free precursors has addressed contamination issues.<sup>5</sup> More widespread implementation of mist-CVD is vital to achieve a more thorough understanding of the growth capabilities and film properties and to gain acceptance of the device fabrication industry.

## 4. Pulsed laser deposition

One of the strengths of PLD is the ability to fabricate films under a wide spectrum of deposition conditions, including temperature, pressure, and gas species. Studies have demonstrated  $n^+\text{ Si}$  doping,<sup>113,114</sup> as shown in Fig. 10, and Al alloying<sup>119</sup> of homoepitaxial  $\beta\text{-Ga}_2\text{O}_3$  films at low deposition temperatures  $<600^\circ\text{C}$ . Degenerate Si-doped films have been implemented as an ohmic contact



**FIG. 10.** Hall effect mobility vs carrier concentration for homoepitaxial  $\beta\text{-Ga}_2\text{O}_3$  films deposited by HVPE, LPCVD, mist CVD, and PLD.  $\beta\text{-Ga}_2\text{O}_3$  substrate orientation and dopants are noted in the legend. Data sources: "HVPE, Si, (001), 2018;"<sup>110</sup> "HVPE, UID, (010), 2019;"<sup>109</sup> "HVPE, Si, (010), 2019;"<sup>109</sup> "LPCVD, Si, (010), 2018;"<sup>111</sup> "LPCVD, Si, (001), 2018;"<sup>111</sup> "LPCVD, UID, (001), 2020;"<sup>112</sup> "MIST CVD, Sn, (010), 2016;"<sup>112</sup> "PLD, Si, (010), 2017;"<sup>113</sup> and "PLD, Si, (010), 2018."<sup>114</sup>

TABLE V. Growth conditions and general limitations of HVPE, LPCVD, mist CVD, and PLD for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> films.

	HVPE	LPCVD	Mist CVD	PLD
Growth temperature (°C)	1000	850	700	590
Growth rate (nm/min)	Up to 333	22	8	3
Potential impurities	Cl	C, H		
Substrate crystal orientations	(001), (010)	(001), (010)	(010)	(001), (010)
Limitations	No commercial multi-wafer deposition, substrate miscut required, high deposition temperatures	High deposition temperatures	No commercial multi-wafer deposition, scaling	No commercial multi-wafer deposition, scaling

regrowth layer in a  $\beta$ -(Al<sub>0.14</sub>Ga<sub>0.86</sub>)<sub>2</sub>O<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub> modulation-doped FET achieving an extracted ohmic contact resistance of 1  $\Omega$  mm<sup>5</sup> Heterostructures of  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> with x = 0–0.37 were also achieved.<sup>119</sup>

A primary detractor to commercial utilization of the PLD method is limited scaling capabilities due to the laser energy source. As a result, PLD is typically relegated to demonstrating technology capabilities, with other deposition techniques identified that are more suitable for production. Current PLD deficiencies are also predicated on a dearth of experimental studies on doping control, alloying, and low deposition rates. Yet to be demonstrated are low to mid-range impurity doping control in PLD homoepitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> films with appreciable mobilities as already reported from MOCVD and MBE studies. Low deposition rates of 0.2  $\mu$ m/h are also common with PLD, although the addition of oxygen radicals to an 800 °C deposition process prevented sublimation and the associated low deposition rate, usually observed at such temperatures.<sup>5,119</sup> In the future, a more extensive adaptation and exploitation of PLD capabilities to address homoepitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> film nuances is critical to enable the development of device-quality film solutions. Table V summarizes key  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> growth conditions and general limitations of the deposition methods in this section.

C. Concluding remarks

The numerous  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial film studies in recent years have yielded continued improvements in film structural and electrical properties across all epitaxial deposition processes. A thorough fundamental understanding of consistent doping control, specifically translated to reproducible device operation, remains elusive. HVPE, LPCVD, mist-CVD, and PLD collectively are strategically significant epitaxial growth technologies impacting the expanding  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> field as they offer unique attributes, including high growth rates, excellent wide range doping capability, and associated high mobilities. However, substantial work remains to better understand the role of defects, incorporation and activation of carriers, substrate crystal orientation, mobility improvement, alloying, and unintentional species diffusion among others in order to optimize films required for fabrication of reliable high-performance devices for any given growth method or substrate orientation. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> phase has garnered the most interest in epitaxial growth primarily due to the availability of native substrates. Continued investment and technological progress in the development of commercial-scaled

deposition equipment and native substrates certainly are principal drivers in this rapidly developing field. Heteroepitaxial film development also merits continued investigations to capitalize on widely available and inexpensive non-native substrates.

IX. CHARACTERIZATION

Aaron R. Arehart, Adam T. Neal, Shin Mou, Steven A. Ringel

A. Status

Compared with most contemporary semiconductors, defect characterization of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, specifically the characterization of electrically active defects that contribute deep levels throughout the bandgap, is at an early stage. Quantitative characterization of traps throughout the bandgap of ultrawide bandgap semiconductors (UWBGs) is a challenge, but combinations of techniques, including thermally and optically based deep level transient and optical spectroscopies (DLTS/DLOS) and admittance spectroscopy (AS), enable complete coverage of their large bandgaps. These techniques enable extraordinary trap sensitivity (~5 orders of magnitude lower than the background doping); quantitative trap energy and concentration analysis for individual defect states; trap characterization of material test structures and devices, including application-optimized diodes and transistors using derivative techniques like constant drain current DLTS/DLOS (CI<sub>D</sub>-DLTS/DLOS);<sup>120</sup> and determination of how these traps impact materials and device characteristics. Additionally, because these methods provide electronic information about each defect type, this information can be used in device simulations to show the impact of specific trap states on leakage current, dynamic on-resistance, threshold voltage instability, linearity, etc. This leads to the development of experimentally informed predictive models to guide device optimization in terms of performance, stability, and reliability.

In terms of current status, a wide range of early  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> materials, including bulk crystal substrates and epitaxial layers, have been explored<sup>98,121–123</sup>—mostly trying to optimize material quality, assessing baseline trap spectra, identifying the physical sources of traps, and modifying techniques to handle the unique properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Figure 11 shows the trap distributions obtained



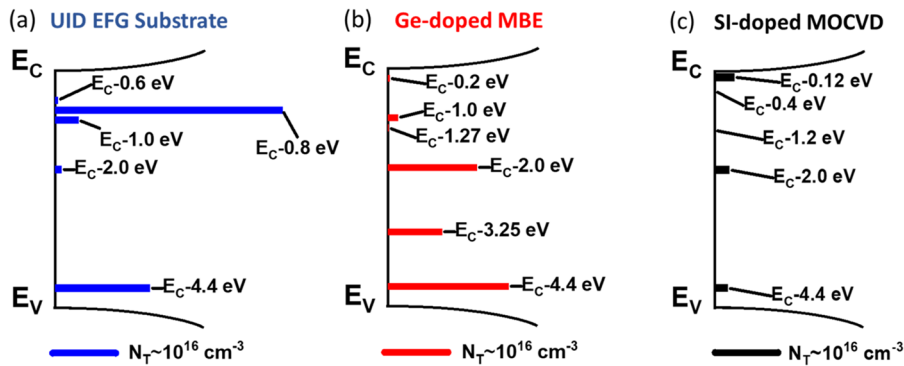


FIG. 11. Trap spectra of (a) unintentionally doped (UID) edge-defined film-fed grown (EFG)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates, (b) Ge-doped molecular beam epitaxy (MBE)-grown  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layers, and (c) Si-doped metal-organic chemical vapor deposition (MOCVD)-grown  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layers all on the (010) plane where the length of the bars indicates the trap concentration given in the legend at the bottom of the figures.<sup>96,121,124</sup>

from a selection of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> materials. It is clear that traps throughout the entire bandgap exist, and several have already been linked with carrier compensation,<sup>124</sup> deep donors,<sup>96</sup> and transistor threshold voltage instability,<sup>125</sup> for example. It is also clear that the total trap concentrations vary by more than 20 $\times$  between different growth methods and the trap distribution (i.e., dominant traps) vary as well. Getting these levels understood, identified, and mitigated are all critical to successful insertion of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices.

## B. Current and future challenges

Defect control and mitigation are critical for the future of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>-based power devices for several reasons. First, multi-kilovolt devices require extremely low doping (low- $10^{15} \text{ cm}^{-3}$  range maximum), with low concentrations of compensating defects, unintentional background dopants, and any other charged defects since any uncontrolled changes in these concentrations will result in an inability to adequately control the doping. Second, even relatively low concentrations of traps in transistors can cause dynamic on-resistance, threshold voltage instability, etc. This is because voltage switching in normal operation forces the quasi-Fermi levels to move through the bandgap within the device. This leads to modulation of trap occupancy; i.e., the Fermi level can swing from below a trap level to above the level, or vice versa, which, in turn, leads to trap emission or capture of charge carriers, and this changes the local charge densities that affect the transistor terminal characteristics in a time-dependent fashion. The standard response by device developers is to derate the transistor, design circuits with much wider margins, and otherwise keep the technology further away from the theoretical limits, thereby reducing the gains from the switch to UWBGs. The third reason that defect control and mitigation are critical is that defect states can lead to leakage currents or reduced mobility if concentrations reach moderate levels or if operating temperatures are sufficient to be in an ionized impurity limited regime. Hence, there is a significant drive to characterize trap by determining their energy levels in the bandgap, their individual concentrations, their physical sources, their physical locations within the device, their connection with materials growth, processing, and device design variables and to develop strategies that eliminate or mitigate each problematic trap.

With the importance of traps established, the current and future challenges become clearer. First, identification of the physical source of each trap is paramount to inform growth optimization. Second, identification of the specific traps responsible for transistor non-idealities (e.g., dynamic on-resistance, threshold voltage shift) is needed to determine the most critical traps upon which to focus. Third is the development of strategies to eliminate or mitigate critical traps created during growth and processing.

Defect studies in MBE, MOCVD, EFG, CZ, and other growth methods are already under investigation<sup>96,121,123,124,126</sup> but have revealed several current challenges. The  $E_C - 2.0$  eV trap has been shown to be a strong carrier compensation center and potentially ascribed to a  $2V_{Ga} - Ga_i$  defect complex.<sup>127</sup> If, indeed, this is a native defect complex, and to date it is typically present even in very high quality (e.g., electron mobility  $>175 \text{ cm}^2/\text{V s}$ )  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial layers having doping in the  $10^{15}$ – $10^{16} \text{ cm}^{-3}$  range,<sup>96</sup> this already suggests that further defect concentration reduction or mitigation strategies will be needed for controllable background doping at the required low concentrations. Figure 12 shows that the  $E_C - 0.8$  eV

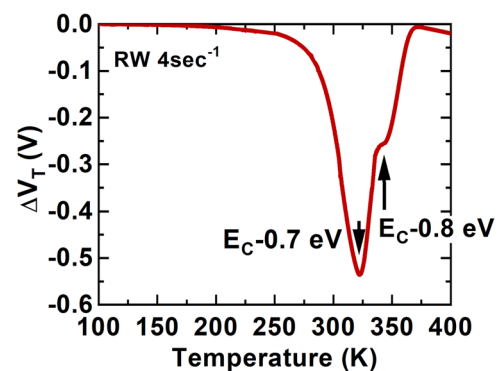


FIG. 12. Gate-controlled CLD-DLTS of a Si  $\delta$ -doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFET showing two traps at  $E_C - 0.7$  and  $E_C - 0.8$  eV, which are responsible for a 0.7 V threshold voltage instability. The  $E_C - 0.8$  eV trap is due to Fe, while the  $E_C - 0.7$  eV is a native point defect potentially related to  $V_{Ga}$  or  $Ga_O$  based on theory and radiation studies.<sup>123,125</sup>

Fe-related trap was limiting in early transistors, causing  $\sim 0.3$  V threshold voltage ( $V_T$ ) instability for Si delta-doped MESFETs.<sup>125</sup> This is problematic for devices grown on Fe-doped substrates if the substrate is too close to the channel or if the surface segregation of Fe during epitaxial growth is not mitigated. Recently, the surface riding issue of Fe is being successfully addressed in ongoing studies by growing an intermediate layer at low temperature to bury the Fe.<sup>75</sup> However, the nearby trap at  $E_c - 0.7$  eV (Fig. 12), for which radiation experiments imply is due to a native point defect,<sup>123,125</sup> caused significantly more  $V_T$  instability than the  $E_c - 0.8$  eV Fe trap and might be more insidious with respect to its mitigation or removal compared with Fe.<sup>122</sup> The  $\sim 0.1$  eV difference in energy levels for these states with totally different sources within a bandgap of  $\sim 4.8$  eV highlights the need for very careful defect state characterization.<sup>125</sup> The  $E_c - 4.4$  eV trap, also found to be a strong compensation center, had been tentatively connected to self-trapped holes in very early studies<sup>128</sup> but has since been observed to be sensitive to the growth technique, and initial proton radiation studies suggest that this trap may be related to native point defects. Typically, the  $E_c - 4.4$  eV trap concentration is among the highest of all deep states in any sample and is always observed. Confirmation of its source remains a high priority challenge. Many other traps have also been observed and characterized.<sup>5</sup> A prominent example of a trap that appears to influence carrier transport is the  $E_c - 0.1$  eV trap<sup>98, 131, 129</sup>. This state is observed in Hall Effect measurements and admittance spectroscopy as a deep donor, and in some cases, it has the highest trap concentration in MOCVD-grown epitaxial layers. This defect not only causes unintentional doping in setting the lower limit of the background doping density but also degrades the device performance with its incomplete ionization at around room temperature.<sup>129</sup> Efforts are under way to identify the sources of all these levels leading toward growth optimization, but we are only touching on the challenges that remain for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> electronics to be successful.

The current state-of-the-art has the best reported mobility values at nearing 200 cm<sup>2</sup>/V s at room temperature<sup>67</sup> and around 11 000 cm<sup>2</sup>/V s at cryogenic temperature.<sup>93</sup> While it was estimated by theory that the electron-phonon scattering limited mobility is expected to be 200 cm<sup>2</sup>/V s at room temperature, the uncertainty of the polar optical phonon (POP) energy convoluted with the ionized impurity scattering caused by defects/dopants makes it non-trivial to decide the upper limit of the mobility value at room temperature experimentally.<sup>130</sup> It remains to be seen how much mobility improvement we can obtain by eliminating the unwanted defects.

There are numerous long-term challenges for defect characterization that will evolve with the advancement of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device technology, and its importance will continue to increase. These include continued guiding of growth optimization; characterization of traps in  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> having much wider bandgaps than  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>; understanding and mitigating defect states in UWBG dielectric/AlGaO interfaces; identifying direct linkages between specific traps, device parameters, and reliability; and developing new testing protocols.

From the materials perspective, current challenges will continue that are related to defect identification in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> due to lack of (but improving) consistency from various material sources to suppliers and growth methods. More systematic and correlative

defect-growth studies that consider independent variables, including growth temperature, growth regime, choice of precursors, growth rate, and choice of dopant species, while starting to appear, are needed.

(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> is almost completely unexplored in terms of defects but yet is enabling for transistors with high 2DEG concentrations and high mobility and other devices. Interface states, surface states, and bulk traps all need to be explored with techniques that may lack the range to fully characterize traps throughout the exceedingly large bandgaps. MOSFETs and other  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors already show great promise, but little has been done to understand how defects in each layer or interface impact device stability (e.g., dynamic  $R_{ON}$ ,  $V_T$  instability, and  $g_m$  changes) and performance (e.g., noise,  $f_T$ ,  $f_{max}$ , and linearity) to this point. As seen in Ref. 131, traps can impact system level metrics in GaN. So as commercial products ready, this will need to be explored as well.

Another key challenge in the future is the development of qualification methodologies and testing protocols for both materials and devices. Having standard specifications for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates and epilayers that include the full set of properties identified as having high impact on device reliability, stability, and performance, which are beyond the current standards based on methods such as x-ray diffraction (XRD) and secondary ion mass spectroscopy (SIMS), will be needed. For example, device-critical defects, such as atomic vacancies, cannot easily be characterized, especially at their low but non-negligible concentrations. Additionally, extrinsic defects are present at concentrations often below SIMS detection and yet have already been shown to play key roles in device degradation. Fast, simple, and preferably non-contact methods to evaluate native and extrinsic defect concentrations will need to be devised for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power electronics that have doping in the low 10<sup>15</sup> cm<sup>-3</sup> range or less. Beyond materials qualifications, device qualification based on random part testing must consider bias, time, and environmental conditions and here would be the last chance to catch any defect or other material or fabrication issues. New protocols, which might include some variant of quantitative defect spectroscopy that are sensitive to defects with the appropriate degree of sensitivity, should significantly improve device uniformity, stability, performance, and yield for the end user.

## C. Concluding remarks

In this chapter, the roles of defects, characterization methods, and future challenges were discussed. Overall, defect characterization, identification, and mitigation strategies are well under way where significant gains on all these fronts are occurring. However, significant challenges remain, especially in terms of physical source identification for specific traps, defects in the (Al,Ga)<sub>2</sub>O<sub>3</sub> alloy system, impacts of traps on transistors, device and circuit parameters, transistor designs that minimize trapping effects, technical improvements to accommodate the even wider bandgaps of (Al,Ga)<sub>2</sub>O<sub>3</sub>, and development of suitable test methodologies and protocols to monitor traps throughout the material and device supply chain. With the success of this,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices will greatly exceed the incumbent technology limitations at very high voltages and, with cost and other improvements, can become the next-generation high-voltage, high-power handling solution.



## X. FUNDAMENTAL MATERIALS AND TRANSPORT PROPERTIES

Avinash Kumar, Ankit Sharma, Krishnendu Ghosh, Uttam Singiseti

### A. Status of the area

It is vital to fully understand the fundamental band and electron transport properties in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> to accurately simulate and predict the device performance in power, RF, and RF switching applications. The low symmetry of the monoclinic  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal structure, along with ten-atom unit cell that results in multiple polar phonon modes, provides considerable challenges to the transport calculations using the traditional approaches used for the Si, III-Vs, and III-Ns. However, exploiting the recent advances in the *ab initio* computation methods, several researchers correctly identified the strong polar optical phonon scattering as the limit to the room temperature low field electron mobility in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.<sup>132–135</sup> Although the presence of 12 IR active polar modes makes the use of simple relaxation time approximation (RTA) for transport calculations imprecise, a good fit to experimental mobility is observed using a LO phonon energy in the range of 40–50 meV (Fig. 13). These transport calculations also provided an estimate of the non-polar deformation potential parameters,<sup>136</sup> which are very difficult to measure or estimate in early stages of materials development. The low field transport calculations have been validated by direct experimental measurements of the scattering times using pump–probe experiments.<sup>137</sup>

The experimental room temperature mobilities ( $\sim 200$  cm<sup>2</sup>/V s) have approached the theoretically calculated values. Moreover, the electronic band parameters of  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> (AlGaO) alloys and  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub> heterostructures were computed theoretically<sup>87,88</sup> and validated by experiments. The success in predicting the fundamental band and transport properties makes the *ab initio* based approach an indispensable tool. Additionally, high field transport in bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has also been explored, providing the saturation velocity which is an important parameter for RF devices. Despite the tremendous progress described here, there are still several challenges that we discuss below.

### B. Status of the area

#### 1. 2DEG transport properties

Even though the POP limited electron mobility is high enough in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, both RF and power devices will benefit from increased mobility. In SiC power devices, reduced field effect channel mobility plays a major role in the device design and considerable research is dedicated to increase this mobility. Similarly, increased channel mobility will help in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power device performance.

For RF devices, the low field mobility will determine the effective channel velocity and hence the high frequency performance. Using heterostructures to form two-dimensional electron gas (2DEG) is an attractive way to enhance the mobility. Recent work suggests (Fig. 14) the role of plasmon–phonon coupling and dynamic screening to enhance the mobility.<sup>106</sup> Both roughness scattering and remote impurity scattering were observed to impact the mobility. Using a relatively lower Al composition AlGaO barrier layer, the authors predict that the mobility could be increased to more than twice that of bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> at a 2DEG density of  $5 \times 10^{12}$  cm<sup>-2</sup>. However, the primary challenge is to achieve such high 2DEG densities with no parallel channel formation and thick enough spacer layers. The whole design space for AlGaO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> heterostructures has not been fully explored. It will be interesting to see how the mobility changes with even higher 2DEG densities where inter-sub-band scattering can be expected play a significant role. The accuracy of these calculations can be improved using mode-resolved non-polar scattering rates. The damping of the plasmon–phonon modes can also impact the mobility, which needs to be incorporated in the calculations. All the calculations to date have assumed an equilibrium phonon distribution. Coupled electron and phonon calculations can provide more insights into the ultimate limits to mobility. The high field velocity–field profile in AlGaO/Ga<sub>2</sub>O<sub>3</sub> is not explored. It would be very informative to see if the plasmon–phonon coupling and dynamic screening have any role in the high field transport behavior.

#### 2. AlGaO properties

As described previously, achieving high 2DEG density could potentially enhance the mobility in AlGaO/Ga<sub>2</sub>O<sub>3</sub> heterostructures. Growth of high composition AlGaO layers will greatly help in achieving high 2DEG densities as the larger conduction band offsets will confine the 2DEG. Hence, understanding and control of AlGaO electronic properties is an important area. Peelaers and

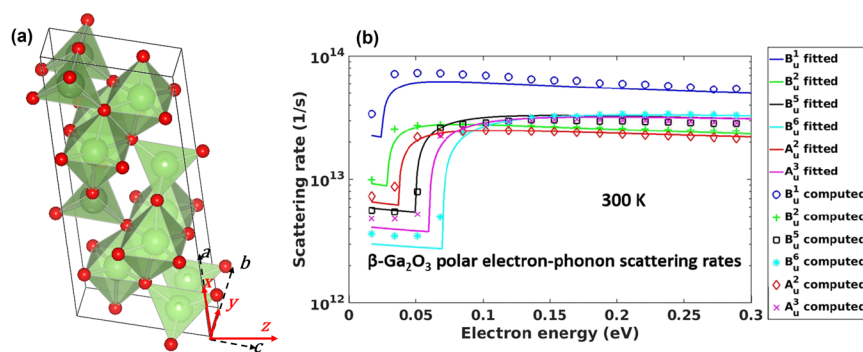
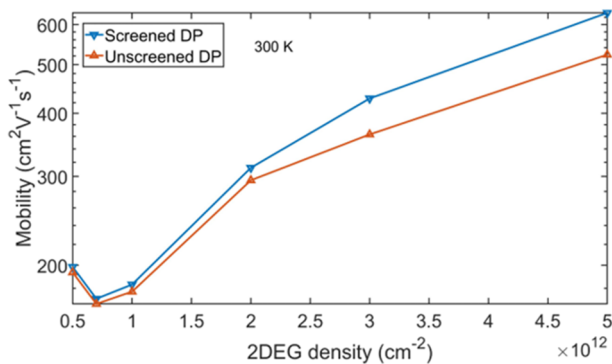


FIG. 13. (a) Conventional unit cell of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, (b) Spherically averaged POP scattering rates for 6 of the 12 IR modes with highest rates, showing the role of multiple phonon modes in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.<sup>135</sup>



**FIG. 14.** Calculated 2DEG mobility with increasing 2DEG density. For both screened and unscreened non-polar scattering cases, mobility is enhanced at  $5 \times 10^{12} \text{ cm}^{-2}$ .<sup>106</sup>

Mu *et al.* investigated the electronic band properties of AlGaO alloy layers from first-principles calculations.<sup>87,88</sup> These calculations show that the band alignment between AlGaO and Ga<sub>2</sub>O<sub>3</sub> has a staggered line up (Type II alignment), which helps in the increasing the confinement of 2DEG in heterostructures. They also predict that at 50% Al composition, the AlGaO should be an ordered alloy; an ordered alloy will not have any alloy fluctuation scattering that could enhance 2DEG's mobility. The conduction band offset in AlGaO/Ga<sub>2</sub>O<sub>3</sub> heterostructures was found to be dependent on the orientation with highest offset in the (100) direction. The calculated band line up was validated recently by experiments.<sup>86,138</sup> It is predicted that the monoclinic phase is energetically favorable over the corundum phase up to 70% Al composition. This should not be an obstacle for high 2DEG density designs as at 70% AlGaO, the conduction band offset is sufficiently high. A rather more difficult challenge is the ability to dope the AlGaO layers that are the source of electrons in the 2DEG. *Ab initio* based calculation of the energetics of potential shallow dopants in AlGaO will provide valuable knowledge to both growers and device engineers. The random nature of alloy and the need to use large size supercells in these calculations provide considerable computational challenges. Additionally, the energetics of defects, defect-dopant complexes in AlGaO, and doping compensation needs to be explored.

### 3. Impact ionization parameters

Several groups have demonstrated the high critical field strength of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> experimentally and the community has generally accepted the empirically extrapolated 8 MV/cm as the critical

field strength in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. However, the critical field strength has not been quantitatively determined either by theoretical calculations or measured experimentally using current multiplication in p–n diodes due to the absence of p-doping. The theoretical calculations suffer from the computational complexity arising from the multiple closely spaced valence bands in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Assuming a single representative flat valence band, Ghosh *et al.* used *ab initio* based scattering rates coupled with Monte Carlo simulations to obtain the ionization coefficients of electrons.<sup>139</sup> An interesting observation in this study is the predicted large anisotropy in the ionization coefficient of electrons (Fig. 15).

The calculated anisotropy is more than the calculated anisotropy in either mobility or saturation velocity. The calculated ionization coefficients provide first quantitative parameters for evaluating the theoretical limits of the field strength. However, the hole ionization coefficients are not calculated. The problem is further complicated by the self-trapping nature of holes, which suggest a completely new mechanism for breakdown. However, recently the hole mobility was estimated from *ab initio* calculations ignoring the self-trapping effect.<sup>133</sup> **It will be informative to estimate the hole ionization coefficient even** if the likelihood of finding a shallow acceptor is low.

### C. Concluding remarks

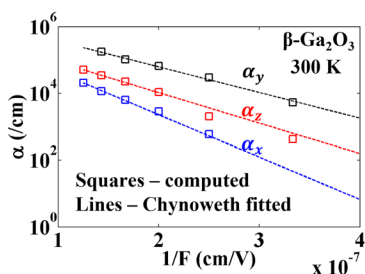
In summary, *ab initio* based calculations have provided deep insights into the fundamental band and transport properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and related alloys. Experimental validation of the calculated parameters further emphasizes the importance of these studies. However, there are still significant knowledge gaps both in the transport and band properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and AlGaO alloys. Sustained research along with experiments will provide significant boost to the transition of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> from academic laboratories to real world applications.

## XI. SCHOTTKY BARRIER DIODES

Wenshen Li

### A. Status of the area

Owing to the inherently fast switching speed and low on-state voltage drop ( $V_{ON}$ ), Schottky barrier diodes (SBDs) are indispensable for high efficiency power conversions. Since the device structure is relatively simple, vertical  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBD is likely among the first



	$a$ (/cm)	$b$ (V/cm)	$\int_0^L \alpha dx$
$x$	$0.79 \times 10^6$	$2.92 \times 10^7$	0.38
$y$	$2.16 \times 10^6$	$1.77 \times 10^7$	6.16
$z$	$0.706 \times 10^6$	$2.10 \times 10^7$	1.19

**FIG. 15.** Calculated electron ionization coefficients in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> for different crystal directions. Chynoweth fitting parameters for electrons.<sup>139</sup>

device types to enter commercialization, similar to SiC. The past few years have witnessed fast-paced development of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs. High breakdown voltage up to  $\sim 3000$  V,<sup>140,141</sup> a Baliga's figure-of-merit (FOM) of close to 1 GW/cm<sup>2</sup> while simultaneously maintaining a low leakage current,<sup>141</sup> a high current carrying capability of over 100 A,<sup>142</sup> high temperature operation at 500 °C,<sup>143</sup> fast switching,<sup>144</sup> as well as near ideal  $I$ - $V$  characteristics under both forward and reverse bias have all been demonstrated.<sup>145</sup>

These achievements certainly benefit from the excellent quality of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial layers and substrates, which exhibit not only low dislocation density  $<10^4$  cm<sup>-2</sup> but also no clear correlations between dislocations and leakage current.<sup>146</sup> In addition, early studies of barrier height<sup>147</sup> as well as ohmic contact process provide important underpinning. However, realization of on-state voltage drop and soft breakdown voltage that are comparable to or exceed those of commercial SiC power SBDs have not been demonstrated yet.

Structurally, both the trench-MOS SBD<sup>141</sup> and junction-barrier Schottky (JBS)<sup>148</sup> structures have been realized for the reduction of the reverse leakage current via the reduced surface field (RESURF) effect. In particular, realization of the JBS structure made use of the  $p$ -NiO/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> p-n heterojunction, which maybe one of the more promising options for the realization of p-n junctions needed for electric-field management.

To address the field crowding at the anode edge, various types of edge termination methods have been explored, including field plating,<sup>149</sup> implanted terminations,<sup>144</sup> junction termination extension (JTE)-like,<sup>150</sup> deeply etched mesa,<sup>145</sup> and floating metal guard rings.<sup>151</sup> However, reliable soft breakdown and ideal reverse leakage have not yet been consistently achieved.

## B. Current and future challenge

### 1. On-resistance limit

Before discussing the challenges of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs, we first evaluate the limit of their conduction loss. For an optimum conduction loss under a given voltage rating or breakdown voltage (BV), one should minimize  $V_{on}$  under a given on-current density ( $J_{ON}$ ). This is equivalent to minimizing the specific SBD on-resistance ( $R_{on,SBD} = V_{on}/J_{on}$ ) under a given on-current density ( $J_{ON}$ ), as given approximately by<sup>152</sup>

$$R_{on,SBD} \approx \frac{\Phi_B}{J_{on}} + \frac{4BV^2}{\epsilon_s \mu \mathcal{R}^3 E_{surf}^3}. \quad (1)$$

Here,  $E_{surf}$  is the surface electric field at BV,  $\Phi_B$  is the barrier height in volts,  $\mu$  is the electron mobility,  $\epsilon_s$  is the dielectric constant of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, and  $\mathcal{R}$  is the RESURF factor, which equals to unity for regular SBDs.<sup>152</sup> Note that  $R_{on,SBD}$  includes the effect of the junction voltage drop ( $\sim \Phi_B/J_{ON}$ ) and, thus, is different from the differential on-resistance typically used for benchmarking according to the Baliga's FOM. Distinct from p-n diodes, the maximum  $E_{surf}$  in SBDs is typically limited by the reverse leakage current due to barrier tunneling and, thus, is lower than the critical electric field. By using the standard breakdown criteria of a maximum reverse leakage current ( $J_{R,max}$ ) of 1 or 100 mA/cm<sup>2</sup>, we have previously established quantitative relationships between the maximum  $E_{surf}$  and the barrier

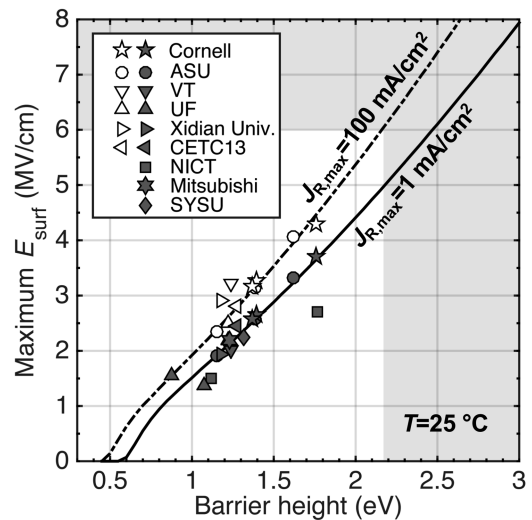
height in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs,<sup>145</sup> as shown in Fig. 16. With the maximum  $E_{surf}$  as a function of  $\Phi_B$ ,  $R_{on,SBD}$  in Eq. (1) can be minimized by solving for the optimum  $\Phi_B$  under a given BV and  $J_{ON}$ .

Figure 17(a) shows the calculated  $R_{on,SBD}$  limit as a function of BV in regular  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs under  $J_{ON} = 100$  A/cm<sup>2</sup>. The physical parameters used in the calculation are listed in Fig. 17(b). It can be clearly seen that the effect of the junction voltage drop ( $\sim \Phi_B$ ) renders the  $R_{on,SBD}$  limit much higher than the unipolar limit, which only includes the resistive voltage drop across the drift layer, especially when BV is low.

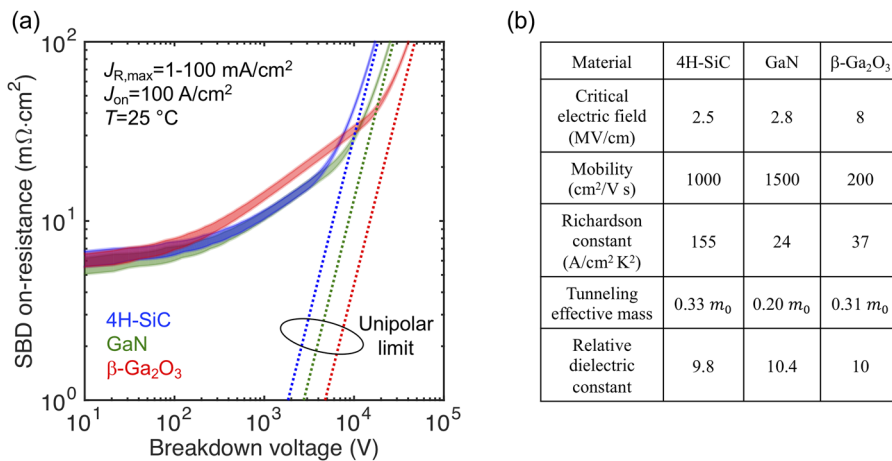
Also shown as comparisons are the  $R_{on,SBD}$  limits of regular SiC and GaN SBDs. It can be seen that under the low voltage range ( $<100$  V), there are negligible differences between these three materials. Between 100 and 2000 V, where wide-bandgap SBD market primarily resides, regular  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs have slightly higher  $R_{on,SBD}$  than SiC and GaN counterparts due to the lower mobility, but the difference is very small. It is worth noting that within this voltage range, the maximum  $E_{surf}$  in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs under the optimum  $\Phi_B$  is lower than 3 MV/cm, rendering the advantage of its high unipolar limit (Baliga's FOM) not present in regular SBDs. In fact, this emphasizes that the major motivation for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> based SBDs is the significant cost reduction due to scalable bulk substrates decreasing manufacturing cost as discussed in the first chapter.

### 2. Strategies for $R_{on,SBD}$ optimization

Based on these results, two main strategies for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs arise. To offset the slight disadvantage in mobility,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs can be operated under a smaller  $J_{ON}$ , rendering a  $V_{ON} = J_{ON} R_{on,SBD}$  smaller than that of GaN and SiC SBDs. This is equivalent to enlarging the device area/chip size. Of course, the switching loss would increase due to the increase of the overall capacitance. Future studies are required to quantify the exact trade-off relationship between



**FIG. 16.** Calculated maximum surface electric fields in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs defined at a  $J_{R,max}$  of 1 or 100 mA/cm<sup>2</sup> at 25 °C. Experimental data from the literature are also shown [hollow for  $J_{R,max} = 100$  mA/cm<sup>2</sup> and solid for  $J_{R,max} = 1$  mA/cm<sup>2</sup>, adapted from Li *et al.*, Appl. Phys. Lett. **116**, 192101 (2020) with the permission of AIP Publishing].



**FIG. 17.** (a) Calculated  $R_{on,SBD}$  limits in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, GaN, and 4H-SiC regular SBDs ( $\mathcal{R} = 1$ ) under  $J_{ON} = 100$  A/cm<sup>2</sup> and  $J_{R,max} = 1$ –100 mA/cm<sup>2</sup> at 25 °C. (b) Physical parameters used for the calculation of the  $R_{on,SBD}$  limits.

switching loss and conduction loss for the optimum design space. Other than being simple and straight-forward, this method also alleviates the burden on thermal engineering while taking advantage of the projected low-cost device platform.

Alternatively, one can utilize the aforementioned RESURF effect in advanced devices structures to lower  $R_{on,SBD}$ . With RESURF,  $E_{surf}$  can be smaller than the maximum electric field ( $E_{max}$ ) in the drift layer.<sup>152</sup> Consequently, the RESURF factor  $\mathcal{R}$  in Eq. (1) becomes larger than 1, thereby lowering  $R_{on,SBD}$ . Experimentally,  $\mathcal{R} \sim 6$  and  $E_{max} = 4.3$  MV/cm have been realized in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> trench-MOS SBDs.<sup>141</sup> However, the reliability of the dielectric layer under such a high  $E_{max}$  is a serious issue, which needs to be addressed via the development of stronger dielectric materials or p-type shields. It is also possible to replace the MOS structures with metal or oxidized metal contacts if the barrier height is sufficiently high to support a high electric field without excessive leakage current (see Fig. 16). As for JBS structures,<sup>148</sup> it is important to ensure that the p–n heterojunction interface is of high quality such that no interface leakage current and interface charge trapping are present. In addition, the breakdown mechanism of the heterojunctions should be identified. Ideally, repeatable soft breakdown via impact ionization should be realized. This is essentially equivalent to addressing the grand challenge of p-type doping in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.

Other than these two main strategies, it is also of great importance to employ optimized epitaxial specifications (doping concentration, thickness, and drift mobility) such that a non-punch-through design is obtained to minimize the drift layer resistance.<sup>149</sup> In addition, reduction of the substrate resistance via substrate thinning or replacement is also desirable. These methods have been generally lacking in current state-of-the-art SBDs.

### 3. Edge termination

No matter what the diode structure is, a robust and effective edge termination is necessary. It is well-known that the electric field at the anode edges could be several times higher than the parallel-plane or one-dimensional electric field in the device bulk if proper edge termination is not implemented. For JBS-like structures, the edge termination may need to support a parallel-plane of  $\sim 4$  MV/cm or higher.<sup>152</sup> For regular  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs, the requirement is lessened,

as the parallel-plane  $E_{max}$  is only about 2 MV/cm at a voltage rating of 1000 V.

In commercial SiC power SBDs, the edge termination is typically realized by JTE and guard rings. With effective native p-type doping still elusive in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, however, realization of such termination methods would require p–n heterojunctions. Again, it comes down to the challenge of achieving a high quality junction interface. In addition, it would be desirable to have controllability over the doping level of the heteroepitaxial p-type region. Alternative structures such as N, Mg, F implanted termination, deeply etched mesa, field plates, and metal guard rings may also be effective. However, their effective and robustness await further validation.

### 4. Barrier height control

As discussed previously, there exist optimum barrier heights in both regular SBDs and JBS-like diode structures, depending on the rated breakdown voltage. It can be shown that the optimum  $\Phi_B$  lies roughly in the range of 0.7–1.4 V for regular SBDs and 0.7–1.1 V for JBS-like structures under a rated BV of  $<2$  kV. While barrier height values above 1 V have been frequently reported and utilized,<sup>147</sup> values below 1 V have not. It should be highlighted that these low barrier heights may be necessary under certain scenarios, and much research attention is required. Thermal, electrical, and chemical stability of the barrier also need to be further established, along with scientific understanding of the pinning/de-pinning mechanisms and the associated crystallographic orientation dependence.

While a wide range of characterization is still required, realization of ultra-high barrier heights for voltage-blocking/electric-field management has made important progress, with up to 2.2–2.4 V demonstrated with oxidized metal contacts.<sup>153</sup> It remains to be seen, however, whether a barrier height value beyond half of the bandgap can be obtained, as required to support the critical electric field.<sup>145</sup>

### 5. Thermal management

Finally, we briefly discuss the requirements on thermal management pertaining to  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs. Under normal operating condition, at least top-side thermal managements are necessary to alleviate the more severe self-heating effect than SiC SBDs.<sup>154</sup> For



surge current ruggedness, more elaborate thermal solutions may be needed, such as double-side cooling via thinned or bonded substrates. As SBDs circulate the research community, it is expected that more rigorous thermal management requirements will be defined.

### C. Concluding remarks

Due to the additional junction voltage drop, as well as the constraint on the maximum surface electric field due to reverse leakage current, optimization of the conduction loss in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs is not simply via increasing  $E_{\max}$  to reach a high Baliga's FOM but rather requires multifaceted efforts involving barrier height optimization, structural innovation, and trade-off with switching loss. In this chapter, we summarized two main strategies for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs to obtain lower power loss than SiC and GaN counterparts: by enlarging the chip size or by employing JBS-like structures. In addition, challenges and requirements on edge termination, barrier height control, and thermal managements are identified. For a successful market penetration,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs will not only need to be competitive against SiC and GaN SBDs on performance and reliability, but they will need to see significant cost reduction as well. The interplay between these factors must be considered in the future development of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs.

## XII. VERTICAL DEVICES

Grace Xing

### A. Status of the area

All devices can take a lateral or a vertical form or a hybrid topology. Among the two-terminal devices, Schottky barrier diodes (SBDs) and photodetectors (PDs) are two popular ones due to their simplicity and commercialization potentials. While SBDs are thoroughly discussed in Sec. XI, it is worthwhile to note some primary differences between SBDs and PDs in order to appreciate the impact of device topology.

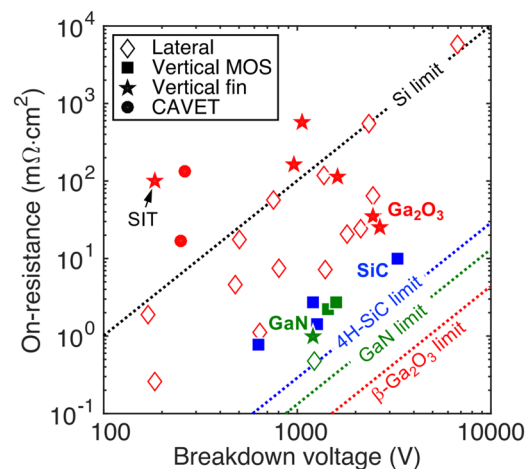
A PD needs to absorb photons first, and then generated mobile carriers can be swept under an electric field toward the electrodes. This electric field can arise from an externally applied voltage or a built-in potential in a junction. For example, employing two different SB junctions in an M-S-M photodetector can lead to non-zero photocurrent at zero external bias, i.e., power- or battery-free operation, similar to a solar-cell. The absorption coefficient of photons with an energy higher than the bandgap of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is about  $10^5 \text{ cm}^{-1}$  or higher. This implies that a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layer as thick as a few hundred nanometers is sufficient to absorb >90% of the above-bandgap photons. As a result, the MSM photodetector often adopts a lateral topology with an active layer of hundreds of nanometers thick to maximize photon absorption as well as take advantage of facile fabrication by printing both electrodes on the wafer surface.

On the other hand, a power device with a target voltage rating of >3 kV necessitates a drift layer with a thickness higher than about  $5 \mu\text{m}$  using the single side abrupt junction approximation and a non-punch through device. Considering a vertical SBD with a  $5\text{-}\mu\text{m}$  thick drift layer and a lateral SBD with a  $1\text{-}\mu\text{m}$ -thick and  $5\text{-}\mu\text{m}$ -long drift region, one can readily see that for the same device size on the wafer,

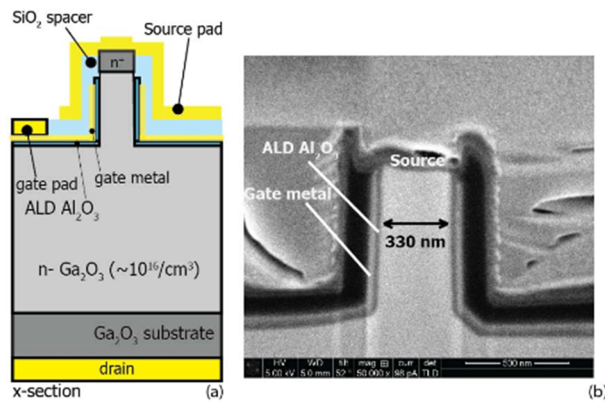
the lateral SBDs will deliver an output current only  $\sim 1/5$  of the vertical SBDs. In this example, the current density along the current flowing direction is assumed to be the same for thermal and reliability considerations. Similar arguments can be applied to vertical vs lateral transistors; moreover, it is equally important to remember that a fin-shaped channel with sidewall gates is essential to provide efficient gating of a *thick* FET channel. However, the validity of these arguments starts to diminish and even reverse in high-frequency transistors since the source-drain distance in a lateral finFET optimized for high-frequency operation can become smaller than the *thickness* of the channel. Based on the above considerations, we limit discussions in this section on power devices employing a vertical topology with an operation frequency <1 GHz, while the RF or high-frequency power devices, often adopting a lateral topology, will be discussed in Sec. XIII.

Other than SBDs, vertical  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices demonstrated to date are of three types: (1) fin-shaped channel metal-insulator-semiconductor (MIS) field effect transistors (FinFETs),<sup>7,9</sup> also called vertical trench MOSFETs;<sup>155</sup> (2) static induction transistors (SITs)—essentially a short-gate vertical FET—the FinFETs reported in Ref. 156 were discovered to have a gate length of  $\sim 50 \text{ nm}$  under transmission electron microscopy, therefore appropriate to rename them as SITs; and (3) current-aperture vertical FETs (CAVETs).<sup>152,157</sup> This landscape is primarily limited by the fact that in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, n-type conduction and semi-insulating properties are readily achieved, while p-type conduction in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> faces fundamental challenges. The community is still searching for p-n heterojunctions that possess a built-in potential higher than 3 eV and enable avalanche in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.

As of today, the experimentally demonstrated BFOM in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> finFETs is  $0.31 \text{ GW/cm}^2$  under pulsed conditions and  $0.28 \text{ GW/cm}^2$  under DC (Figs. 18 and 19).<sup>9</sup> These values are comparable with the BFOM achieved in state-of-the-art  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> SBDs so far; however, they still lag behind those of vertical transistors demonstrated in GaN and SiC.



**FIG. 18.** Benchmark plot of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power transistors. This will be updated to include the CAVET, SIT data, SiC JFET, and MOSFET data and remove all other data points far worse than the Si limit.



**FIG. 19.** Cross-sectional diagram (a) and FIB (b) of a vertical transistor showing the channel region, gate, and source electrodes.<sup>7</sup>

## B. Current and future challenges in this area

In any FET, it is essential to employ the most favorable gate structure(s) in that material system. Generally, p–n junction based, metal–semiconductor (M–S), or metal–insulator–semiconductor (MIS) based gates are the three major choices.

### 1. Design similarities between a trench SBD and a FinFET

A trench SBD and a vertical finFET both feature sidewall MIS-gated fin channels as the core building block. While the electrical performance goals are similar, geometrically they differ due to enhancement mode requirements, gate and channel lengths, and an extra ohmic top contact. Whereas trench SBDs have a Schottky contact, thus having some inherent voltage blocking capability, finFETs have an ohmic contact on top of the fin channel, thus solely relying on the potential barrier induced by the gate for voltage-blocking. As a result, vertical finFETs require a higher aspect ratio ( $>2$ ) for the fin channel, i.e., a smaller fin width under the same fin height, such that drain induced barrier lowering (DIBL) is not excessive. In practice, finFETs typically have a fin width of  $<0.5\ \mu\text{m}$ . This alleviates the electric field crowding at the fin bottom corner, which could be an issue in trench SBDs.<sup>152</sup> However, the requirement on edge termination is no different from the case of trench SBDs, as already discussed in the SBD section.

### 2. Threshold voltage control and stability

Other than the consideration on DIBL, the design of fin channel geometry also need to weigh in the requirement on the threshold voltage ( $V_{th}$ ). This is true for all other vertical transistors as well.

For fail-safe operations, normally off operation or  $V_{th} > 0$  is desired. In the generally employed n-type doping channels, normally off operation basically relies on the full depletion of the channel charge due to the built-in potential of the gate stack. For MIS or M–S gates, this built-in potential is governed by the gate-metal work-function. As a result, it is difficult to obtain a  $V_{th} > 1.5\ \text{V}$ , especially when considering the additional voltage drop with the gate dielectric and the channel. For a higher  $V_{th}$ , special work-function engineering is required. Recent observation of the high effective work function in oxidized metal may offer some benefits.

Otherwise, p–n junction-based gates will be needed for a higher built-in potential. This again requires a high-quality epitaxial heterojunction interface.

Other than the control of the  $V_{th}$  value, its stability is equally important. For MIS gates, this is only possible with a high-quality dielectric–semiconductor interface. It is far from trivial, as slow trapping/detrapping and the related threshold voltage shifts are frequently observed in  $\beta\text{-Ga}_2\text{O}_3$  MOSFETs. For any potentially promising dielectric material, a mapping of the interface states as well as its optimization is required, together with standard stability tests, such as Positive Bias Temperature Instability (PBTI).

### 3. Reliability of MIS structures for reaching high fields in $\beta\text{-Ga}_2\text{O}_3$

As have already been alluded to in the SBD section, the reliability of the dielectric layer in MIS structures under very high electric field is a serious concern. It is well-known that amorphous dielectric materials exhibit time-dependent dielectric breakdown (TDDB) behaviors, which limits the maximum electric field to be well-below the ultimate dielectric breakdown strength for a sufficient device lifetime. Considering the high field operation required for the high power figure-of-merit in  $\beta\text{-Ga}_2\text{O}_3$ , the dielectric reliability could be a major limiting factor for the efficiency of  $\beta\text{-Ga}_2\text{O}_3$  power devices. In vertical  $\beta\text{-Ga}_2\text{O}_3$  devices employing MIS structures, this issue could be combated with proper design of p-type shielding, which again requires the development of proper p–n junctions. Without p-type shielding, one would need to develop stronger dielectric materials with high TDDB lifetime under a high electric field—a general grand challenge for all wide-bandgap power devices.

### 4. Current aperture employing semi-insulating $\beta\text{-Ga}_2\text{O}_3$

CAVET<sup>158</sup> offers an alternative solution to vertical  $\text{Ga}_2\text{O}_3$  FETs. It has the advantage of the all-ion implantation based fabrication process and a fully planar surface and, thus, can be manufactured with low cost. Currently demonstrated  $\beta\text{-Ga}_2\text{O}_3$  CAVETs show decent on-state performance, but a high breakdown voltage beyond 600 V is yet to be reached.<sup>157</sup> The challenge mainly resides in the voltage-blocking capability of the semi-insulating current blocking layer since it lacks mobile holes and external electrical contacts as in a vertical double-diffused MOSFET (VD-MOSFET) where the current aperture is defined by p-type regions with well-controlled fermi levels. It remains to be seen whether such a layer could provide sufficient voltage-blocking under both steady-state and dynamic operation conditions, without inducing threshold voltage instability and degradation to the on-state performance.

### 5. P–n heterojunctions

In a semiconductor material system with both mature n-type and p-type doping technologies, the following vertical devices are often also explored: (heterojunction) bipolar junction transistors (BJTs and HBTs), vertical junction FETs (JFETs), vertical double-diffused MOSFETs (VD-MOSFETs), trench MOSFETs, insulated gate bipolar transistors (IGBTs), thyristors, avalanche diodes, etc. By strategically placing the high-quality p–n junction capable of avalanche within the device structure (vertical and/or lateral junctions), it is possible to minimize electric-field crowding and implement RESURF schemes, thus approaching the unipolar limit of the



semiconductors. Furthermore, the avalanche capability afforded in high-quality p–n junctions lend these devices the ability to survive surge events. For applications that can live with bipolar carrier-limited switching frequencies, the unipolar limit of a semiconductor is exceeded by employing superjunctions. In Si, CoolMOS is one of the most prominent examples taking advantage of superjunctions, while in SiC and GaN, superjunctions have been actively pursued. High-quality p–n homo- or heterojunctions that enable avalanche in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> will for sure open up a plethora of opportunities for device design, thus application spaces.

### C. Concluding remarks

Assuming an interface with zero interfacial charges due to defect states and polarization discontinuity, etc., the displacement current near the interface is the same in the two joint materials:  $\epsilon_1 E_1 = \epsilon_2 E_2$ . We can readily examine how this relationship fares for Si/SiO<sub>2</sub>. The critical breakdown field in Si at the low doping limit is 0.3 MV/cm, while that for SiO<sub>2</sub> can be 10 MV/cm or slightly higher depending on the deposition method and thickness of SiO<sub>2</sub>. However, a practical field of about 2 MV/cm in SiO<sub>2</sub> is chosen to ensure a higher than 10-year lifetime without serious dielectric degradation. A field of 2 MV/cm in SiO<sub>2</sub> translates to 0.6 MV/cm in Si, which indicates that Si can undergo avalanche before forcing SiO<sub>2</sub> to undertake a dangerously high field, thus an accelerated TDDb. On the other hand, for any semiconductor with a critical field higher than 2 MV/cm, the performance of a MIS structure over time is most likely determined by the insulator. Crucial effort is necessary to develop high-quality MIS structures for all wide bandgap semiconductors. Section XV on ultra-high k dielectrics is an excellent example on this topic. The ultimate choice to unleash the full potential of a wide bandgap semiconductor is its p–n junctions with avalanche capability. After all, the breakdown behavior of a p–n junction is supported collectively by the p-region and the n-region of the wide bandgap semiconductor. In fact, the critical electric field increases with the doping concentration; for instance, in SiC and GaN, the field increases from  $\sim 2.6$  MV/cm at a doping concentration of  $10^{15}$  cm<sup>−3</sup> to  $\sim 4$  MV/cm at a doping concentration of  $10^{18}$  cm<sup>−3</sup>. In summary, the combination of the judicious device design and sufficiently high-quality MIS junctions and/or p–n junctions is key to enable practical and commercializable products based on (ultra)wide bandgap semiconductors, including  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.

## XIII. LATERAL DEVICES

### Kelson Chabak, Kyle Liddy

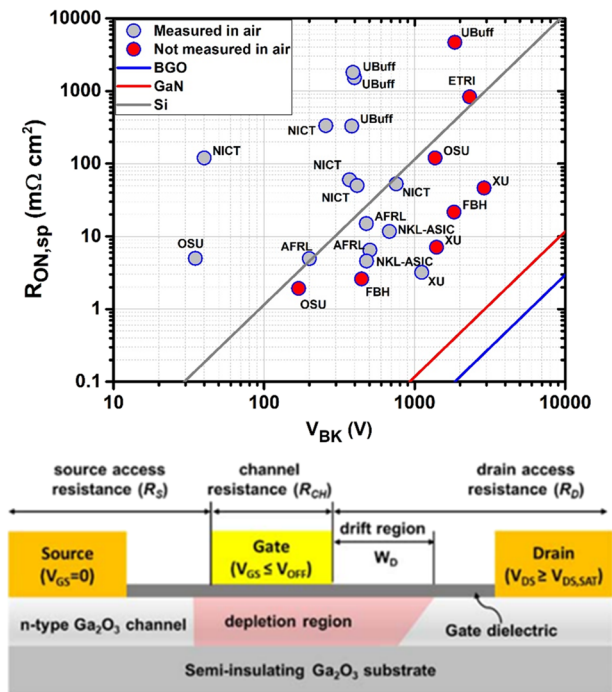
Lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices come in multiple topologies with their associated benefits. The simple Schottky junction MESFET<sup>27</sup> is a simple structure that can be used to decrease capacitance and increase gain. Inserting an oxide between the gate and channel (MOSFET)<sup>21</sup> significantly reduces gate leakage. More advanced designs, such as  $\beta$ -(Al<sub>x</sub>Ga<sub>1−x</sub>)<sub>2</sub>O<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub> heterojunctions (MODFET),<sup>53</sup> localize sheet charge for increased transport properties and device gain. It should be noted that all device types are majority carrier devices as shallow acceptors are not currently known and hole transport is negligible due to self-trapping. Lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>

transistors are ideal for applications that involve switching—power switching, RF switching, and switch-mode power amplifiers designed to operate efficiently between on and off states.<sup>25</sup> In contrast to a vertical topology, lateral transistors uniquely offer a small capacitive (gate charge,  $Q_G$ ) footprint with low on-resistance ( $R_{on}$ ) to meet aggressive  $R_{on}$   $Q_G$  targets. The ultimate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral transistor will resemble Si LDMOS with a self-aligned design to the gate and drift region made with ion implantation. Gate length ( $L_G$ ) scaling can be explored by borrowing III–V epitaxial designs, such as delta-doping to support vertical scaling in pursuit of short-gate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices. So far, AFRL has reported the only self-aligned gate-to-source (SAG)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistor,<sup>159</sup> while Ohio State University has shown that delta-doping is a viable approach for scaling homoepitaxial lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors.<sup>160</sup> These devices are poised for fast-switching power converters with pervasive reach across commercial and military applications to shrink and integrate power conversion at point-of-load. The fast-switching lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistor application space is niche and will likely require technology development of a pervasive commercial application, such as low-cost (dollars/Amp), high-performance SBDs offering SiC-like performance at a fraction of the SiC cost. In many ways, this resembles the same cycle as GaN RF technology that leaned heavily on the success of commercial GaN LEDs. Otherwise, technology maturation of lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors will depend largely on investments by DoD and DoE akin to the DARPA Wide Band Gap Semiconductors (WBGs)-RF program for the GaN-on-SiC RF platform.

### A. Current and future challenges in this area

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> has relatively low mobility ( $\mu$ ) in exchange for a phenomenal  $\sim 8$  MV/cm estimated critical field strength ( $E_{max}$ ). It is imperative to operate  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> in a high Ecrit regime to realize its high performance predicted by the various power semiconductor figures of merit. The total switching losses in a power switch trade off conduction losses ( $\sim E_{max}^3$ ) in the limit of slow switching and dynamic switching losses ( $\sim E_{max}^2$ ) for high frequency switching.<sup>25</sup> For high Ecrit operation, it is critical to design the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral transistor without source access resistance ( $R_s$ ) and only enough drift region to match the estimated depletion width calculated from a one-side abrupt junction approximation.

Green *et al.* first demonstrated high  $E_{max}$  operation in 2016 using a simple lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFET that achieved an average  $E_{max} > 3.8$  MV/cm and peak  $E_{max} > 5.1$  MV/cm.<sup>20</sup> Multiple high  $E_{max}$  lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistor results followed in short order achieving 3.9<sup>161</sup> and 4 MV/cm.<sup>162</sup> These results are key as they surpassed the theoretical  $E_{max}$  for bulk GaN and SiC while also demonstrating  $\sim 4\times$  Ecrit than modern GaN HEMTs achieve with field plates ( $\sim 1$  MV/cm). Figure 20 shows representative lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistor performance from a conduction loss perspective (specific on-resistance,  $R_{on,SP}$ , vs breakdown voltage,  $V_{BK}$ ), which consistently surpasses the silicon theoretical limit. Huang's Unipolar Material FOM (HMFOM), a switch loss FOM from a  $Q_G$  perspective, is given by  $E_{max} \cdot \mu^{0.5}$ . Using the latest  $\mu$  and  $E_{max}$  values reported in the literature, lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors have even edged GaN HEMT technology using the HMFOM benchmark (GaN:  $\mu = 2000$  cm<sup>2</sup>/V s,  $E_{max} = 1$  MV/cm;  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>:  $\mu = 150$  cm<sup>2</sup>/V s, and  $E_{max} = 4$  MV/cm). Additional gains will require (1) careful optimization of  $R_{on}$  (higher



**FIG. 20.** (Upper) Specific on-resistance vs breakdown voltage for lateral epitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors. For larger gate-drain distances, the breakdown field seems to be limited to slightly above 2 MV/cm. (Lower) Lateral device (MOSFET) schematic showing resistances associated with their respective geometries.<sup>163</sup>

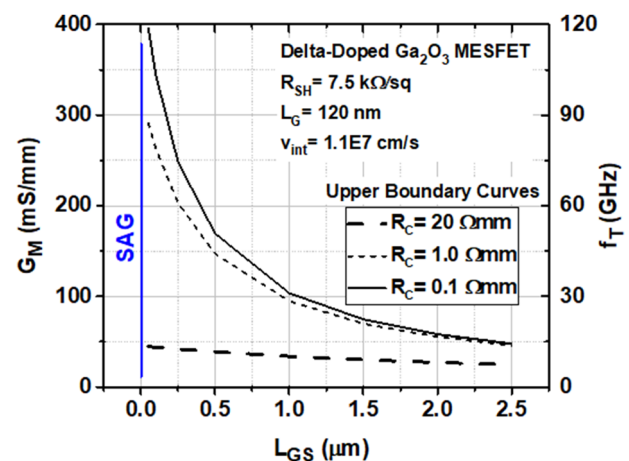
measured  $E_{\max}$ ) and (2) epitaxial innovations to increase  $\mu$  beyond current bulk values. It is important to note that  $E_{\text{crit}}$  matters more than  $\mu$  for power switching applications.

All high  $E_{\max}$   $\beta$ -Ga<sub>2</sub>O<sub>3</sub> transistors listed above achieved this with short gate-to-drain distances compared to GaN and SiC. This feature of high  $E_{\max}$   $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is especially unique at lower voltages where the depletion width may be <500 nm. For example, a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> buck converter with 28 V input to power low-voltage logic may require a lateral transistor with  $V_{\text{BK}} = 90$  V breakdown voltage. At  $V_{\text{BK}} = 90$  V and  $E_{\max} = 8$  MV/cm, the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> drift region would be just 220 nm and require electron beam lithography to precisely define. Assuming  $L_G$  would be equal or less than the drift region, an optimal high-speed lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power switch would require a source-drain distance ( $L_{\text{SD}}$ ) < 500 nm. For GaN HEMTs, one can achieve a similar  $L_{\text{SD}}$  using regrowth and EBL alignment for a T-gate. For GaN, the gate placement can afford to be offset from the source because the channel sheet resistance ( $R_{\text{SH}}$ ) is <300  $\Omega/\square$  in many cases. The opposite is true for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> as  $R_{\text{SH}}$  has been typically reported in the realm of 5–10 k $\Omega/\square$  because of lower mobility. Even a small slice of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> creates enough access resistance ( $R_S$ ) to deteriorate the extrinsic transconductance ( $G_M$ ) for reduced power and RF performance. The highest  $G_M$  values reported in the literature remain <50 mS/mm and are mostly limited by  $R_S$  from either high contact resistance ( $R_C$ ) or non-negligible  $R_{\text{SH}}$  in the gate-source region. For this reason, a SAG design with implant doping and subtractive refractory metal process appears mandatory for high-speed switching. Achieving  $n^+$  implanted contacts with  $R_{\text{SH}} < 100 \Omega/\square$  is

a critical aspect of this. So far, low  $R_{\text{SH}}$  implant doping is viable and has been reported as low as 96  $\Omega/\square$ .<sup>164</sup>

First-order analytical equations illustrate the significance of  $R_S$  challenges for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Assume a rectangular gate structure with capacitive structure defined by  $\epsilon/\tau$ , with  $\tau$  defined as the gate oxide thickness and partially depleted channel in series. The intrinsic velocity ( $v_{\text{int}}$ ) of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is conservatively estimated as  $\sim 1.1 \times 10^7$  cm/s, assuming mid-high impurity doping (though it has been reported as high as  $\sim 2 \times 10^7$  cm/s for un-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>).<sup>159</sup> Therefore, an intrinsic transconductance ( $g_m$ ) can be estimated from  $v_{\text{int}} \cdot C_G/L_G$  and an upper bound for  $G_M$  can be inferred from an  $R_S$  analysis using  $G_M = g_m \cdot (1 + R_S \cdot g_m) - 1$  by varying  $R_C$  and  $R_{\text{SH}}$  vs gate-source gap ( $L_{\text{GS}}$ ) for a Ga<sub>2</sub>O<sub>3</sub> lateral transistor. The analysis is reasonably close to the optimized device design from Xia *et al.* that predicts a  $G_M/C_G$  ratio with a current gain cutoff frequency ( $f_T$ ) up to 24 GHz (measured 27 GHz); however, moving the T-gate from  $L_{\text{GS}} = 1.35 \mu\text{m}$  to  $L_{\text{GS}} = 0.5 \mu\text{m}$  would raise the  $f_T$  potential to  $\sim 50$  GHz.<sup>166</sup> Likewise, lower  $f_T$  samples reported by AFRL were limited by high  $R_C$  and  $L_{\text{GS}}$  offset. This analysis predicts  $f_T < 15$  GHz and  $G_M < 35$  mS/mm, which resembles most of the measured data without implanted contacts. Figure 21 illustrates the effect of  $R_C$  and  $L_{\text{GS}}$  on  $G_M$  (upper bound) for a representative lateral  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> delta-doped MESFET with  $R_{\text{SH}} = 7.5$  k $\Omega/\square$  and delta sheet inserted 20 nm below the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> surface. For high  $R_C = 20 \Omega/\text{mm}$ ,  $G_M$  will not surpass 50 mS/mm, regardless of a scaled  $L_{\text{GS}}$  design. However, when  $R_C = 1 \Omega/\text{mm}$ , a  $G_M$  in excess of 100 mS/mm is possible with careful attention to  $L_{\text{GS}}$ . Additional gains are possible from  $L_G$  reduction that corresponds with proper vertical  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> epitaxial designs. Device performance becomes very sensitive to  $L_{\text{GS}}$  with an optimized  $R_C$ , and a SAG transistor design is likely required.

For lateral Ga<sub>2</sub>O<sub>3</sub> power switching,  $\mu$  matters less than  $E_{\max}$ , although any improvements will propel the technology forward and be more appealing to RF applications. Obtaining a high sheet charge density confined in a two-dimensional electron gas (2DEG) with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> will resemble the development of GaAs technology. Homoepitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layers with a delta-doped sheet charge



**FIG. 21.** Extrinsic  $G_M$  and  $f_T$  vs gate-source distance and  $R_C$  for the specified delta-doped Ga<sub>2</sub>O<sub>3</sub> MESFET.

inserted below the surface have shown high performance just like GaAs MESFETs did early in its development cycle. Xia *et al.* demonstrated this with a quasi-2DEG  $\mu = 95 \text{ cm}^2/\text{V s}$ .<sup>159</sup> Mobility improvements are expected with a MODFET design using the AlGaO/GaO structure designed like an AlGaAs/GaAs MODFET. Zhang *et al.* reported a  $(\text{Al}_x\text{Ga}_{1-x})_2\text{Ga}_2\text{O}_3$  with  $x = 0.18$  MODFET with record high 2DEG electron mobility exceeding  $180 \text{ cm}^2/\text{V s}$ .<sup>167</sup> The main challenge presented for MODFETs will be obtaining a large enough conduction band offset to confine a high sheet charge density. Some recent studies have shown progress with  $x = 0.4$  with MOCVD<sup>102</sup> and In-catalyzed MBE growth (MOCATAXY) up to  $x = 0.2$ ,<sup>61</sup> although delta doping these layers will require further development. Theoretically, Ghosh *et al.* predicted that room temperature 2DEG mobility in  $\beta\text{-Ga}_2\text{O}_3$  could be as high as  $500 \text{ cm}^2/\text{V s}$ , which has sparked many groups to explore this topic area.<sup>136</sup>

The outlook for  $\beta\text{-Ga}_2\text{O}_3$  transistors is promising when it comes to efficient switching and RF applications. The pace will be dictated by the development and commercialization of high-performance  $\beta\text{-Ga}_2\text{O}_3$  SBDs. Like prior successful semiconductor technologies (GaAs, GaN), niche applications beyond pervasive ones, such as fast-switch point-of-load power conversion, will leverage commercial interest and require substantial DoD investments. In the meantime, device groups should continue exploring improvements in power and RF figures of merit, with the goal being to apply the most innovative device designs to breakthroughs in materials discoveries. Removing parasitic resistance, applying designs such as SAG combined with implant-doping  $<100 \text{ }\Omega/\square$ , and patterning these device features with electron beam lithography will produce high-impact device results. Transferring device breakthroughs to vertically scaled epitaxial structures on 3 in. or greater native substrates produced by melt growth will take  $\beta\text{-Ga}_2\text{O}_3$  lateral transistors to the next level.

#### XIV. DIELECTRIC ENGINEERING

##### Ahmad Islam

Integration of dielectric on any semiconductor in a MOSFET configuration has always been a challenge. MOSFET waited its commercial introduction in the late 1960s, which was almost five decades after its original inception, as integration of native silicon dioxide ( $\text{SiO}_2$ ) on silicon required the discovery in terms of hydrogen passivation of the  $\text{SiO}_2/\text{Si}$  interface. It is, therefore, not surprising that the newest compound semiconductor  $\beta\text{-Ga}_2\text{O}_3$  still does not have an electronic-grade dielectric. MOSCAPs and MOSFETs fabricated using different dielectrics on  $\beta\text{-Ga}_2\text{O}_3$  show different degrees of hysteresis in the measured capacitance–voltage (C–V) and current–voltage (I–V) characteristics. The extracted defect densities from such hysteresis suggest a defect density of  $10^{11}\text{--}10^{13} \text{ cm}^{-2}$ .<sup>5</sup> These defects mostly lie at the dielectric/semiconductor interface. The energy level of these defects are spread within the bandgap of  $\beta\text{-Ga}_2\text{O}_3$  and these energy levels can be probed using the conductance method, Terman method, UV-assisted C–V, deep level transient spectroscopy, deep level optical spectroscopy, etc.

The ultra-wide bandgap of  $\beta\text{-Ga}_2\text{O}_3$  limits the choice of dielectrics, which are mainly deposited on  $\beta\text{-Ga}_2\text{O}_3$  substrates using

atomic layer deposition (ALD) and sputtering.<sup>5</sup> Although  $\text{Al}_2\text{O}_3$  is the most popular among the dielectrics, dielectrics like  $\text{SiO}_2$  have also been used to take advantage of its higher conduction band offset. Table 25.1 in Ref. 5 lists all the dielectrics that have so far been integrated on  $\beta\text{-Ga}_2\text{O}_3$ . (Recently, ultrahigh- $\kappa$  dielectrics have been used to reduce the peak electric field in the gate–drain region. Section XIV discusses this field management idea in more detail.)

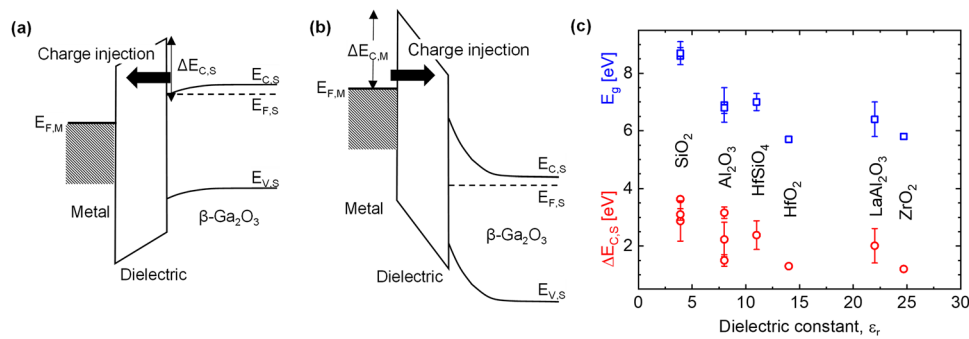
A successful dielectric integration requires low defect density. Defects are present at the interface and bulk of a dielectric and their density depends on the surface preparation steps followed before dielectric deposition, deposition temperature, and processing conditions applied after dielectric deposition. To date, negligible defect density has only been reported by depositing dielectrics, such as  $\text{Al}_2\text{O}_3$ ,  $\text{AlSiO}$ , and  $\text{SiO}_2 + \text{Al}_2\text{O}_3$ , on  $\beta\text{-Ga}_2\text{O}_3$  substrates that has been cleaned with piranha or ozone before dielectric deposition.<sup>163,168,169</sup> Some recent studies where dielectrics were deposited on (010) or (001)  $\beta\text{-Ga}_2\text{O}_3$  substrates<sup>168,169</sup> discussed the need for an additional HF treatment for obtaining a small defect density. The universality of these approaches in reducing hysteresis for different dielectrics deposited on different  $\beta\text{-Ga}_2\text{O}_3$  substrates and the role of post-dielectric deposition processes in modifying the property of these dielectrics are yet to be explored.

#### A. Challenges

There are generally three requirements for having an electronic-grade integration of dielectric on an ultra-wide bandgap semiconductor like  $\beta\text{-Ga}_2\text{O}_3$ :

- (1) The dielectric should have negligible bulk defects.
- (2) The dielectric/semiconductor interface and the gate/dielectric interface should have negligible interface defects.
- (3) Both the above interfaces should have large conduction band offsets.

Any dielectric needs to have negligible bulk defects to work as an insulator in a MOS configuration. Defects within the dielectric can cause trap-assisted tunneling and can act as weak spots for inducing dielectric breakdown at voltages lower than the dielectric strength of the material. The main challenge for dielectric integration, however, comes from the requirement of having a *good dielectric/semiconductor interface* with a defect density of  $10^{10}\text{--}10^{11} \text{ cm}^{-2}$ . Such low defect density will ensure low hysteresis in the C–V and I–V characteristics and enable the device to have sufficient accumulation of electrons underneath the gate. Accumulation of electrons will also require a *high conduction band offset at the dielectric/semiconductor interface* ( $\Delta E_{C,S}$ ) to reduce carrier injection into the dielectric [Fig. 22(a)]. This carrier injection from the semiconductor into the dielectric and the movement of these carriers via the conduction band edge states can result in Frenkel–Poole conduction through the dielectric.<sup>170–172</sup> In addition, for interfaces with small  $\Delta E_{C,S}$  and for cases when the electric field near the interface reaches  $1 \text{ V/nm}$ , carrier injection can occur via Fowler–Nordheim tunneling.<sup>170</sup> These conduction mechanisms through the dielectric can weaken the dielectric and eventually cause its breakdown at an electric field, which can be lower than the expected breakdown



**FIG. 22.** Schematic representation of energy-band diagrams across the metal–dielectric–semiconductor interface of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> based MOSFET in (a) on-state and (b) off-state for the device. In these diagrams, the Fermi-levels in the metal and semiconductor sides are represented using  $E_{F,M}$  and  $E_{F,S}$  and conduction-band offsets in the two sides are represented using  $\Delta E_{C,M}$  and  $\Delta E_{C,S}$ , respectively. Among other symbols,  $E_{C,S}$  and  $E_{V,S}$  represent the conduction and valence band profile in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, respectively. (c) Plot of bandgap ( $E_g$ ) and  $\Delta E_{C,S}$  for different dielectrics deposited on n-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates. Here, relative dielectric constants ( $\epsilon_r$ ) are either estimated from capacitance–voltage measurements (for HfSiO<sub>4</sub>, HfO<sub>2</sub>, LaAlO<sub>3</sub>, and ZrO<sub>2</sub>) or assumed to be equal to the standard known values (for SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>). Data for this plot are taken from Table 25.1 of Ref. 5.

strength of the dielectric. The use of high  $\kappa$  dielectric having a negative valence band offset<sup>5,172,173</sup> can also result in higher gate leakage under deep-UV illumination.

In addition to the above-mentioned instabilities, defects present at the dielectric/semiconductor interface will reduce the mobility of electrons due to Coulomb scattering. When this interface is rough, which is typically the case for epitaxially grown films on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates,<sup>83,85,174</sup> there will be added concerns from surface roughness scattering affecting carrier mobility. Fermi level pinning is another concern for interfaces having high density of interface defects. Although Fermi-level pinning is routinely studied for the metal/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface,<sup>175</sup> its consequence is not well studied for the gate/dielectric and the dielectric/semiconductor interfaces in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> literature.

Along with the on-state device operation requirements discussed above, the off-state device operation (at a negative gate voltage and at a large positive drain voltage) requires the *gate/dielectric interface to have a high conduction band offset* ( $\Delta E_{C,M}$ ) to ensure negligible electron injection from the gate toward the dielectric [Fig. 22(b)]. As with the on-state carrier injection discussed above, a smaller band-offset at the gate/dielectric interface can cause breakdown of the dielectric at a lower applied electric field.

Figure 22(c) plots the bandgap ( $E_g$ ) and  $\Delta E_{C,S}$  for different dielectrics deposited on n-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates. As expected for any dielectric/semiconductor interfaces,  $\Delta E_{C,S}$  reduces with the increase in the relative dielectric constant ( $\epsilon_r$ ). In addition, dielectrics with higher  $\kappa$  often have a negative valence band offset,<sup>5,172,173</sup> resulting in higher gate leakage under deep-UV illumination. However, these high- $\kappa$  dielectrics are important for device scaling. Several recent efforts, therefore, have explored the integration of higher  $\kappa$  dielectrics using bilayer dielectrics with SiO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> as the first layer interfacing with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>.<sup>176,177</sup> More research on this aspect will benefit proper integration of these bilayer dielectrics. The data in Fig. 22(c) also show a large spread in  $E_g$  and  $\Delta E_C$  for different dielectrics. This variation is due to the use of different techniques (e.g., REELS, XPS, and some are theoretically calculated; cf. references in Table 25.1 of Ref. 5) used for collecting data on different dielectrics deposited using different methods (ALD and

sputter) by different research groups. A recent study<sup>178</sup> has observed variation in measured  $\Delta E_C$  for the Al<sub>2</sub>O<sub>3</sub> dielectric deposited using different methods. This suggests the need for systematic measurements using a single technique for similarly formed dielectrics to comprehend the dielectric dependence of  $E_g$  and  $\Delta E_C$  and to understand their variations, if any, with variations in deposition methods, substrate orientation, annealing/processing conditions, etc.

In addition to the materials requirements discussed above, we will also need to consider the following device processing issues. Electronic-grade integration of single-layer and/or bi-layer dielectrics on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> will require tight control of the quality of dielectric deposition by choosing appropriate dielectric deposition methods and by choosing appropriate process sequences. For example, for ALD, we can control the quality of dielectrics (thus reduce bulk defects within the dielectric) by controlling the dielectric deposition and post-deposition conditions. However, the challenge arises during surface preparation for dielectric deposition (which is required for reducing interface defects at the dielectric/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface) and for gate metallization (which is required for reducing interface defects at the gate/dielectric interface). Dielectric deposition with negligible interface defects requires pristine, smooth  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrates prepared with appropriate surface treatment. However, pristine substrates are also beneficial for forming good contacts with a low contact resistance that needs to go through different processes to reduce contact resistance. This leads to the following two compromising situations between interface quality and contact resistance in a device:

- (1) We can first deposit a dielectric on a pristine  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate and then form contacts by removing the dielectric from the contact areas using a wet or dry process. The contact formation will also involve ion implantation and activation annealing. Such a *dielectric-first* process will deposit the dielectric on a good surface with low interface defects but may have a higher contact resistance, as contacts are not formed on a pristine surface. In addition, the standard processes needed for reducing contact resistance<sup>179,180</sup> can adversely affect the dielectric and



dielectric/semiconductor interface due to crystallization and inter-diffusion of atoms,<sup>181</sup> thereby compromising dielectric integration. One can circumvent this challenge by modifying this dielectric-first process into a *gate-last process*,<sup>182</sup> where one initially protects the dielectric/semiconductor interface with a dummy gate/dielectric stack and later partially or entirely removes the dummy gate/dielectric stack and replaces that with a final stack. The success of a gate-last process might have significant implication toward successful integration of a dielectric on a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate.

- (2) Alternately, we can form contacts on a pristine  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate with appropriate ion implantation, metallization, and activation annealing and then deposit dielectrics and gate metal to complete the device. Such a *dielectric-later* process has never been used in the semiconductor industry, as it heavily compromises the dielectric/semiconductor interface due to the incorporation of contamination on the semiconductor surface during contact formation. For this case, the presence of contacts on the substrate excludes the possibility of a thorough cleaning of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> surface using, for example, piranha, which adversely affects the metal contacts and increases the contact resistance. Therefore, resultant devices have dielectrics deposited on a moderately cleaned  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> surface and have high interface defects.

## B. Concluding remarks

An electronic-grade integration of dielectric on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate will allow us to attain high breakdown voltage for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices, thereby enhancing the potential of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> in power electronics applications. A good integration will also enable the high frequency operation of devices made with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> as a better dielectric will enable devices to operate with a higher drive current and lower knee voltage. Moreover, the integration of the high- $\kappa$  gate dielectric with sufficient conduction band offset will enable an increase in gate capacitance and hence increase the operating frequency of the device.

## XV. ULTRA-HIGH $\kappa$ DIELECTRICS

### Siddharth Rajan

The high breakdown field of ultra-wide bandgap materials, such as gallium oxide, AlGaIn, and diamond, may require new methods for field management for two-terminal diodes and field effect transistors. In the case of gallium oxide, the optimal design to minimize on-resistance losses requires channel sheet charge density. Depleting high channel charge requires high electric fields normal to the channel as well as along the channel transport direction and is expected to be significantly higher than were necessary for AlGaIn/GaN high electron mobility transistors.

A figure showing the electric field profiles for a generalized field effect transistor is shown in Fig. 23. The fields normal to the channel and along the channel will lead to a peak field at the drain edge of the gate. In a simple device structure such as this, the Schottky barrier breakdown strength limits the maximum voltage achievable in

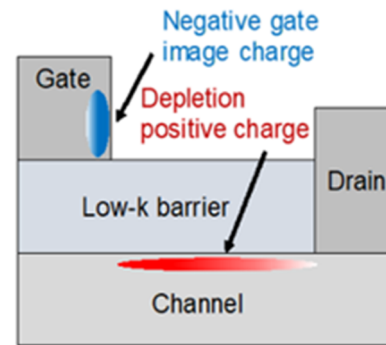


FIG. 23. Schematic of a lateral transistor showing charges induced under off-state conditions.<sup>184</sup>

the device. Assuming an optimally designed device with equal electric fields between directions normal and parallel to the channel<sup>183</sup> and a maximum breakdown field of  $F_{BR} \sim 8$  MV/cm, we find that each of the electric fields would need to be 5.6 MV/cm, and the optimal channel sheet charge density is  $\sim 2.5 \times 10^{13} \text{ q cm}^{-2}$ . Since such high fields cannot be sustained by typical Schottky barriers, a gate dielectric becomes critical to achieve optimal device design.

## A. Challenges

One approach to improve the vertical breakdown strength normal to the channel is to use a high permittivity dielectric as the gate insulator material. Due to electrostatic boundary conditions at the interface, the electric field intensity in the high permittivity dielectric can be significantly lower than in the gallium oxide. This leads to very low electric fields within the dielectric and thereby an increase in the effect barrier width for tunneling from the metal to the semiconductor, as shown in Fig. 24. Experimental work on such interface structures recently showed that parallel plate electric fields of 5.7 MV/cm, with peak fields up to 7 MV/cm, could be sustained by the interface, showing the promise of this approach.<sup>185</sup>

The uniformity of lateral electric fields along the channel is a key issue. At such high sheet charge densities, the electric field along

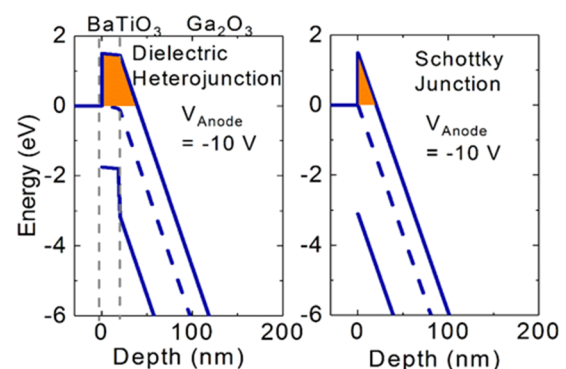
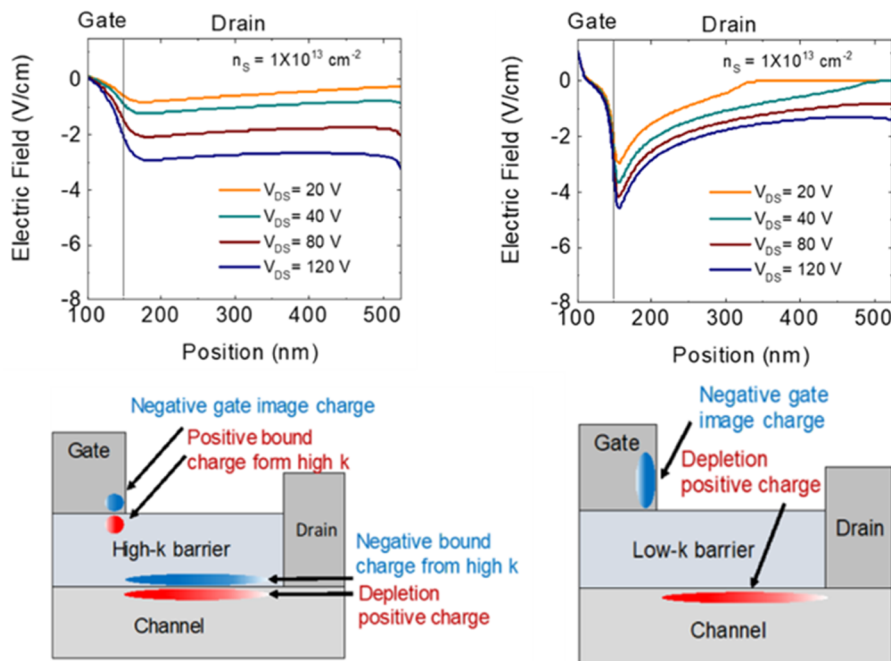


FIG. 24. Energy band diagrams of metal/BaTiO<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub> and metal/Ga<sub>2</sub>O<sub>3</sub> junctions under reverse bias. The shaded regions indicate the barrier to tunneling, which is enhanced in the case with high permittivity BaTiO<sub>3</sub>.



**FIG. 25.** (top) Off-state electric field profile between gate and drain and (bottom) schematics of field effect transistors. The introduction of a high-k region between the gate and drain creates more uniform field profiles and reduces the peaking of the electric field near the drain edge of the gate.

the channel direction becomes highly non-uniform, with peaks at the gate edge that can greatly exceed the average electric field intensity. In conventional Si power devices, advanced techniques using reduced surface field (RESURF) layers consisting of p-type material were used. Under positive drain bias conditions, depletion of acceptors in the RESURF layer compensates the positive depletion charge in the channel and enables fields along the channel to remain uniform. Since it is currently not possible to envisage such a p-type layer with high breakdown field and mobile charge for the case of gallium oxide, other approaches, such as field plates with dielectrics or semiconductors, can be used. An alternative approach is to use high permittivity dielectrics that could enable uniform field profiles to be achieved along the channel under bias.<sup>184</sup> The dielectric polarization in these layers reduces non-uniformity in the gate–drain region and can therefore increase average electric fields. Figure 25 shows electric field distributions along the channel for structures with and without such a high-permittivity layer. Recently, experimental results have enabled high average electric fields in the gate–drain region for gallium oxide as well as AlGaIn, suggesting that this approach could be viable for future device engineering. The theoretical basis for this approach and initial experimental results on gallium oxide have been promising,<sup>162</sup> and lateral electric field strength exceeding 8 MV/cm has been achieved in devices based on AlGaIn.<sup>186</sup> Finally, high permittivity materials may also provide a new approach to realize field termination structures for vertical devices.<sup>187</sup>

Several directions for future research are promising for this direction of research and require a multi-disciplinary effort. The experimental results on integration of high permittivity dielectrics on gallium oxide were achieved using RF sputtering. A detailed investigation of the growth mechanisms, microstructure, and electronic properties, such as breakdown field, and permittivity of these films on gallium oxide by various techniques, would be very

useful for device designers. The electronic defects within the films and leakage mechanisms are not well understood, and a detailed study of these is required. The impact of deposition of these films on the properties of the underlying layer is another key issue that requires further study.

## B. Concluding remarks

Although this technique may apply to many material systems, it looks to be one of the most promising techniques for field management in the absence of a p-type layers in Ga<sub>2</sub>O<sub>3</sub>. Device engineering for high permittivity/semiconductor structures is at an early stage, and several opportunities exist to develop methodologies to analyze and design lateral and vertical diodes and transistors with high performance. Further analyses will help to understand the trade-offs between breakdown voltage, on-resistance, switching losses, and capacitance. Since many of these devices require detailed two-dimensional electrostatics to fully explain the phenomena, there are opportunities for innovations in device simulation coupled with intuitive analytical models. Finally, there are exciting opportunities for advanced device fabrication techniques for realizing high-performance devices for different voltage and power levels with integration of high permittivity dielectrics.

## XVI. THERMAL MANAGEMENT

### Samuel Graham, Sukwon Choi, Zhe Cheng

For all electronic devices, managing heat dissipation to limit the channel temperature and improve the component reliability is critical in their design. Such solutions must account for the thermal

resistance external to the active device (i.e., at the package- and system-levels) while consideration must be also given to the internal thermal resistances within the device itself. When considering ultrawide bandgap materials such as  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, unique challenges arise from the device-level thermal resistance due to the low thermal conductivity of the material. For example, the low and anisotropic thermal conductivity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (27.0, 10.9, and 14.7 W/m K in the [010], [100], and [001] crystallographic directions<sup>178</sup> and as low as 3.1 W/m K for  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> alloys,<sup>189</sup> respectively) has been used in devices. From previous experiments and modeling, the device thermal resistance of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> lateral transistors were shown to be several times larger than GaN-on-SiC high electron mobility transistors (HEMTs) with a similar device layout.<sup>11,154,189-193</sup> The low thermal conductivity alone is not the challenge but also the architecture of the devices since thermal resistance is a function of both thermal properties and geometry. Thus, electro-thermal co-design techniques are essential to push the limits of the thermal management of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> electronics. Ultimately, the design of thermal management solutions must be based on electro-thermal device models that can reproduce the temperature-dependent device electrical output characteristics and the self-heating behavior in response to a specified bias condition. Such device model, in turn, relies upon accurate thermal properties of the base materials that are temperature, size, and compositional (e.g., ternary alloy and superlattice) dependent. Next, cooling strategies that locate heat spreaders and efficient conduction pathways in proximity to the device heat generation region will be key to realize an effective thermal management solution. This strategy of implementation of thermal solutions must also not negatively impact device electrical performance. Therefore, modeling, manufacturing, and experimentation will be key in developing thermal management strategies for future devices.

To date, several reports have been published on the thermal management strategies for lateral and vertical  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices. These include thermal approaches for  $\beta$ -(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub>/Ga<sub>2</sub>O<sub>3</sub> modulation doped field effect transistors,<sup>189</sup>  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs,<sup>11,190,191,193</sup> and  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diodes.<sup>154</sup> In all of these reports, it has been found that strategies involving top-side or flip-chip cooling as well as double-sided cooling may be effective for the thermal management of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> electronics. Challenges that remain for this area of research are outlined below.

### A. Thermal characterization

The knowledge of the thermal resistance between the heat source and heatsink in gallium oxide electronics is a critical need for modeling and designing devices. While several studies have shown that the thermal conductivity of bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is highly anisotropic,<sup>188,194</sup> this property is likely to be impacted by size effects,<sup>195</sup> defects (e.g., vacancies and dopants),<sup>196</sup> and chemical composition (i.e., ternary alloys),<sup>189</sup> which have not been fully characterized. The thermal conductivity of a ~400 nm-thick (100)-oriented  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> exfoliated film was shown to have a thermal conductivity of 8.4 W/m K (~35% lower than that of a bulk crystal), which reveals the strong thickness-dependence of the thermal conductivity.<sup>197</sup> Ternary alloys, such as (Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub>, are used to create heterostructures to be used in advanced device architectures,

such as MODFETs. Such ternary alloys are expected to have much lower thermal conductivities than the binary base crystals (as was shown in Al<sub>x</sub>Ga<sub>1-x</sub>N;<sup>198</sup>). A ternary alloy (Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> with 19% Al composition was shown to have a thermal conductivity as low as 3.6 W/m K in the [010] direction and 3.1 W/m K in the direction perpendicular to the (010)-plane. This reduction in thermal conductivity is already an order of magnitude lower than that for bulk  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. Better understanding of the size effects, temperature dependency, and alloy composition on the thermal properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> must be explored. Other strong reductions in thermal conductivity are expected to come from the creation of superlattices where strong phonon scattering from multiple interfaces will impede the heat flow. In summary, thermal property measurement that explores the material space of gallium oxide will be critical to provide accurate thermal properties for device modeling. For example, it is likely that low thermal conductivity alloy barrier layers will have an impact on any top side extraction from  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>/(Al<sub>x</sub>Ga<sub>1-x</sub>)<sub>2</sub>O<sub>3</sub> MODFET.

At present, *in situ* optical methods, such as infrared thermography, thermoreflectance imaging, and micro-Raman thermometry, are used for thermal imaging of wide-bandgap electronic devices, such as GaN high electron mobility transistors (HEMTs).<sup>199-203</sup> However, these techniques are insufficient for the thermal characterization of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device technologies. Infrared thermography is incapable of probing both the semiconductor channel (due to its transparency to infrared radiation) and the metal electrodes (due to low emissivity) and lacks the spatial resolution. Thermoreflectance imaging of the metallization structures (e.g., gate electrode) is possible at low modulation frequencies (to account for the slow transient thermal dynamics of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices). However, probing the semiconductor channel using visible to near-UV wavelength illumination sources is difficult because  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is transparent at these wavelengths. At the time being, micro-Raman thermography techniques that make use of nanomaterials as discrete (i.e., nanoparticles<sup>181</sup>) or continuous (i.e., 2D layered materials<sup>204</sup>) surface temperature transducers are most suitable for performing quantitative thermal imaging of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices. To this end, a high resolution non-invasive, non-contact method that can directly probe the surface temperature of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is yet to be developed.

### B. Device-level thermal management

A variety of materials need to be integrated with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices to provide effective pathways for heat dissipation away from the device active region. These materials will include metal contacts, solder joints, dielectric layers, underfills, and high thermal conductivity substrates (e.g., AlN, SiC, and diamond). It has been predicted in several studies that top-side/flip-chip or double-sided cooling strategies will provide the most effective thermal management strategies.<sup>11,191,194</sup> However, the execution in building these architectures remains a challenge, especially in the growth and integration of high thermal conductivity dielectric layers on top of the active region of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices, without compromising the device electrical performance. The development of growth techniques of high thermal conductivity dielectric materials, such as diamond, AlN, and BN polytypes, on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices will be important to support top-side or double-sided cooling. Overall, the impact of cooling is expected to be seen for dielectric layers with micrometer

range thickness on top of the device channel with a thermal conductivity greater than 100 W/m K.

For the bottom-side heat extraction of the device, several methods, including the integration of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> with SiC through surface activation bonding,<sup>205,206</sup> fusion bonding,<sup>207</sup> and direct growth,<sup>208</sup> have been demonstrated. However, controlling the thermal transport across numerous interfaces from heterogeneous integration is still an active area of research. Challenges arise from phonon transport and scattering near the interfaces due to intrinsic material properties and many forms of defects (e.g., voids, amorphous layers, and impurities) that may form during the various processing steps of integration. The thermal resistances originating from these interfaces can contribute a significant fraction to the total junction-to-package thermal resistance, especially when  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is integrated with high thermal conductivity substrates or dielectric materials. One major limitation in the pursuit of backside heat removal is the wafer thinning process. As the substrates have increased in size, they have also gotten more fragile. Ideally, the wafer can be thinned to less than 50  $\mu$ m for efficient heat removal. Lapping and polishing techniques will need to be explored and developed to maintain wafer yield.

Because of the complications associated with the thermal boundary resistance (TBR) at interfaces, it is important to understand and control all the related TBR properties in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices, which involve the propagation, transmission, and reflection of different thermal energy carriers governed by different transport mechanisms. Nonetheless, a key aspect of the future of device thermal management will rely upon the success of heterogeneous integration of these heat spreading and dissipating materials with high thermal conductivities and sufficiently low TBR at interfaces with  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>. The integration techniques must be solutions that can be supported by wafer scale manufacturing. In addition, additional efforts are needed in the development of high thermal conductivity dielectric underfills to help dissipate the heat from the device channel.

### C. Additional prospects

By definition, a power switch operates with high efficiency. The heat generated will be a function of the switch's duty cycle. Switch analysis has yet to be studied for this material and may heavily influence implementation. If self-heating gives an upper bound to the duty cycle, it is conceivable that vertical and lateral topologies will differentiate further in applications. Some benefit will be observed by changes in device architecture to help spread out the heat generated in the active region. Moving from lateral to vertical device structures will provide opportunities to reduce thermal energy generation densities and operate at higher voltage and power levels. It has been observed that  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> will operate at high temperatures due to its wide bandgap,<sup>21,190,209</sup> but the intrinsic limits of performance and reliability as a function of temperature have yet to be explored. Thermally aware design optimization of the layout of device interconnects, which will play a major role in the heat dissipation pathways for top side cooling, will also be an important feature that must be optimized.

Additional methods to cool high-power  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices will likely involve active cooling strategies. While air cooling is desired for low cost and high reliability strategies, active liquid cooling

methods are expected to significantly enhance the operational power densities achieved by these devices and may find their niche in high performance applications.

### D. Concluding remarks

The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> materials system offers favorable attributes in terms of creating next-frontier power electronic devices (i.e., outstanding electronic properties and low-cost substrate manufacturability). The material's low thermal conductivity resulting in overheating has become a major bottleneck to maximize the performance of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device technologies. A paradigm shift in the device design process, i.e., electro-thermal co-design, is necessary to overcome the thermal impediments. In order to implement such co-design techniques, the development of novel thermal characterization and multi-physics, multi-scale device modeling schemes are necessary. These innovations in convergent research will allow the full exploitation of the promising benefits of the ultra-wide bandgap material.

## XVII. CLOSING REMARKS

### Masataka Higashiwaki

As discussed in Secs. I–III,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has a high potential based on its extremely large bandgap as a semiconductor material following SiC and GaN for next-generation power switching and RF device applications. It is obvious that high-efficiency  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power switching devices contributing global energy conservation will be more and more demanded. Harsh-environment  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> RF FETs operating at high temperature and/or under strong radiation would pave the way for the new field of semiconductor electronics. However, it is worth noting that  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has two fundamental drawbacks originated from its physical properties: no hole-conductive p-type and poor thermal conductivity. Due to the lack of p-type material having reasonable hole conductivity,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device structures have significant design limitations. Furthermore, its low thermal conductivity that directly affects heat dissipation capacity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices is another serious issue, especially for high-power device applications. We need to accept these two shortcomings and work on developments of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices in the future.

To build up more advanced  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FET and diode technologies, there are many challenges left in all aspects of bulk melt growth, epitaxial thin-film growth, and device processing. In bulk melt growth and wafer production, it can be pointed out as a major difficulty that expensive rare metal iridium (Ir) is used as a material of crucibles. Large reduction in its amount for the crucible is required to suppress production cost of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> bulk wafers. With respect to epitaxial growth, HVPE and MOCVD have reached to a certain level that can take future mass production into consideration but needs to be much more improved and advanced. In particular, improvement of reproducibility and reliability of the n-type doping technology and exploratory research on p-type doing technology take a high priority. Developments on epitaxial growth technologies for heterostructures using (AlGa)<sub>2</sub>O<sub>3</sub> and (InGa)<sub>2</sub>O<sub>3</sub> layers should also be actively pursued. In parallel with the



developments on the bulk and epitaxial growth technologies, fundamental research on physical properties of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is important and should be conducted with the support of the academic community. In particular, more complete understanding on physical properties of point defects in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is highly required to put reliability and stability of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices in the proper perspective. Furthermore, it can be expected that intentional manipulation of the point defects would lead to creation of novel devices with new functions.

As for device processing, there are still a variety of fundamental technologies that should be developed. Ease of ion-implantation doping is one of the big features for  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>; however, the process is far from being established. The search of new elements for the ion-implantation doping and optimization of the process condition should be carried out. An etching process gains more importance for the development of vertical FETs and diodes. Currently, reactive ion etching and inductively coupled plasma etching that cause some damage on the etched surface are usually used for the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device fabrication. We should develop a new etching technology that can reduce the degree of the damage. Needless to say, the bandgap energy of over 4.5 eV is the most distinguishing feature of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>; however, this leads to an issue that gate dielectric materials are very limited to form a large energy barrier at a dielectric/ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> interface. In addition, the interface quality needs to be further improved, especially for normally off FETs. The poor heat dissipation capacity of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices remains as a crucial issue for high-power device operation. One of the effective ways to improve it is direct bonding to a foreign substrate with good thermal and electrical conductivities.

The year 2021 marks the tenth anniversary of the ground-breaking demonstration of the world's first single-crystal  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> FETs,<sup>27</sup> which galvanized intensive international research and development activities on Ga<sub>2</sub>O<sub>3</sub> into the science and engineering. Consequently, in this decade,  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has earned its citizenship within the semiconductor community, and many fundamental material and device technologies have been generated. However, the worldwide research and developments on  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> have mostly been conducted by universities and public research institutes, and the degree of corporate contributions has been little. Active participation of manufacturing companies in the development is indispensable to enhance not only the development speed of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power and RF devices but also the technology transfer from the lab to the fab. Whether  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> ends up with just a booming semiconductor material or reaches to the stage of the device practical realization and industrialization, providing valuable contributions to the global challenges and economy depends on the research and development activity in the coming decade. The community is standing at a major inflection point, and the next decade will be revolutionary for the sector.

## AUTHOR DECLARATIONS

### Conflict of Interest

The authors declare no conflict of interest.

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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