Back-illuminated voltage-domain global shutter CMOS image sensor with 3.75m pixels and dual in-pixel storage nodes

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Abstract

A 1024x800 image sensor with voltage-domain global shutter pixels and dual in-pixel storage is implemented in a 90nm/65nm back-illuminated (BSI) imaging process. The pixel has a 3.75µm pitch, achieves -80dB PLS operating in its correlated double sampling mode and has a maximum dynamic range in its high-dynamic range imaging mode of 102dB.

Introduction

A back-illuminated (BSI) global shutter (GS) image sensor containing a 1024x800 pixel array with a 10T-per-pixel architecture featuring dual in-pixel storage nodes is presented. Charge domain global shutter pixels are reliant on metal light shielding [1] [2], and are hence impractical in BSI. Voltage-domain storage, however, is capable of achieving acceptable PLS performance, even without a metal light shield [3] [4] and is therefore more suitable for BSI. Dual in-pixel storage enables correlated double sampling (CDS), high dynamic range imaging (HDR) via exposure bracketing, or fast double-snapshot imaging for motion detection. The advantages of BSI are successfully harnessed to demonstrate the smallest BSI global shutter pixel yet reported at 3.75µm pixel pitch.

Image Sensor

A simplified system block diagram of the imager is shown in Fig. 1. The image sensor comprises a 1024x800 array of 10T global shutter pixels with dual-column readout connected to two external quad-channel differential ADCs, each having 16-bit resolution and x1 gain. An annotated chip photomicrograph is shown in Fig. 2. The device measures 5.5mm(H) x 5.0mm(V) and is manufactured in STMicroelectronics' 90nm(BE)/ 65nm(FE) imaging process.

Pixel Design

Fig. 3 shows the pixel schematic and signal timing diagram for the global shutter CDS (GS-CDS) mode. The 10T global shutter architecture has dual voltage-domain storage elements C_1 & C_2, each of which is coupled to the gate of a source follower connected to the bottom (C_1) and top (C_2) analogue readout blocks. The sample capacitors are 16fF in size, and are implemented in MOS capacitances, augmented by a smaller metal fringe capacitance. Read noise is dominated by the kT/C noise of one of two sources, dependent upon the mode: in CDS mode, the sample capacitors; in the dual-capture modes, the sense node.

Fig. 4 shows the cross-section of the pixel taken through the vertically-pinned photodiode (VPPD) and sample capacitors. Back-illumination technology enables high fill factor to be achieved in the pixel, despite the high pixel transistor count. The mushroom-like shape of the VPPD serves a dual-purpose: the photodiode is able to collect photo-generated electrons from a large volume within the pixel while keeping the frontside surface area footprint minimal; the large collection volume of the VPPD increases effective fill factor to 90% and improves PLS by way of reducing the quantity of photo-generated electrons which reach the comparatively small storage nodes during the readout period. The VPPD uses in-depth charge storage [5] to increase storage density and yield a full well capacity of 8100e-. P-type lateral isolation implants surround the storage region of the photodiode to prevent leakage of collected charge to the channel of the MOS capacitors

The 10T pixel relies on several factors to reduce PLS: the vertical photodiode structure and the small fraction of pixel volume occupied by the drain diffusions connected to the gates of the MOS capacitors reduce the chance of absorbed photons being collected on the sample capacitors; the ratio of sample capacitance to sense node capacitance reduces the impact of electrons collected by the sample capacitors during storage. Finally, if using global shutter CDS mode (GS-CDS), the illumination on the sample diffusions is a common-mode signal at both storage nodes. Because the arrival of photons is a Poissonian process, the subtraction of the two signals reduces the parasitic signal by a factor of $\sqrt{2n}$, where n is the mean number of electrons collected by the storage node during the storage period. In the single-exposure global shutter mode, the sensor achieves -80dB PLS and 59dB dynamic range (DR). In the high dynamic range mode, -70dB PLS is achieved, with a maximum DR of 102dB. Full-depth deep trench isolation (DTI) provides optical and electrical isolation of each pixel, eliminating blooming from oversaturated pixels to neighbouring pixels.

Fig. 5 illustrates the correlated double sampling (CDS) and exposure-bracketed high dynamic range (HDR) modes of pixel operation, aimed at extending the dynamic range (DR) at the lower and upper ends respectively. By sampling the sense node reset level on C1, the kT/C noise of the sense node – the dominant noise source at low signal levels – can be cancelled, hence the noise floor is lowered and the DR extended. Read noise in the CDS mode is 8.5e- vs 16.8e- for delta reset sampling (DRS), representing a 6dB DR improvement. The dual-capture GS-HDR mode of 10T pixel architecture does not require an inter-exposure readout, thus the two image captures are time-contiguous, thereby circumventing the ghosting issue affecting conventional image sensors using this method of DR extension. Fig. 6 shows the two images captured in GS-HDR mode and the resulting image after HDR synthesis. There are no visible artefacts in the image from either PLS or object movement in the scene. **Table 1** Fig. 6presents a summary of the performance parameters.

References

[1] Sakakibara, M. et al; ISSCC 2012
[2] Velichko, S. et al; IISW 2013
[3] Kondo, T. et al; IISW 2015
[4] Meynants, G. et al; IISW 2011
[5] Michelot, J. et al; IISW 2011

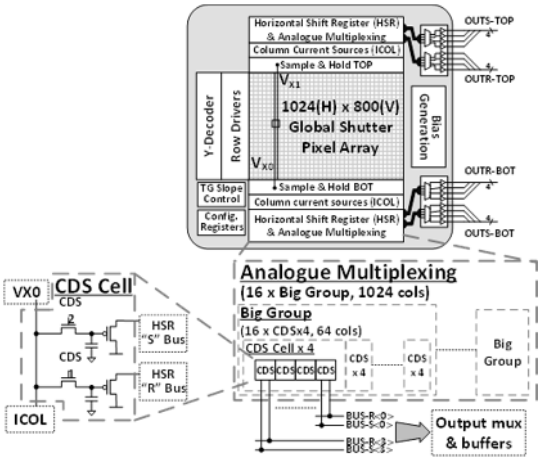

Fig. 1. Imager block diagram

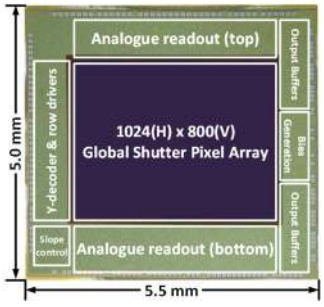

Fig. 2. Chip photomicrograph

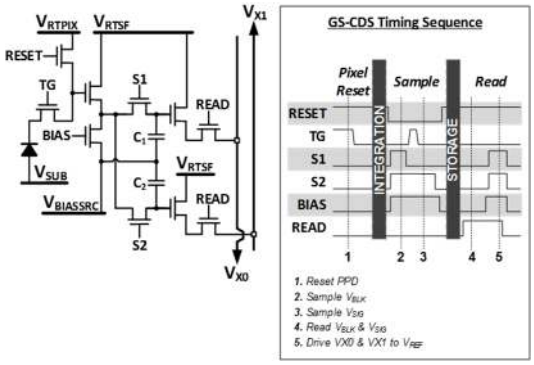

Fig. 3. Pixel schematic and timing diagram

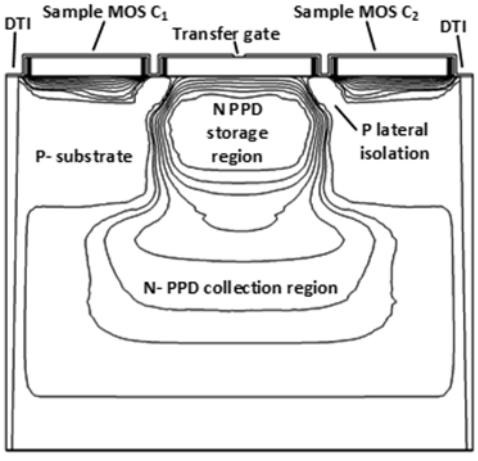

Fig. 4. Vertical photodiode cross-section from TCAD simulation

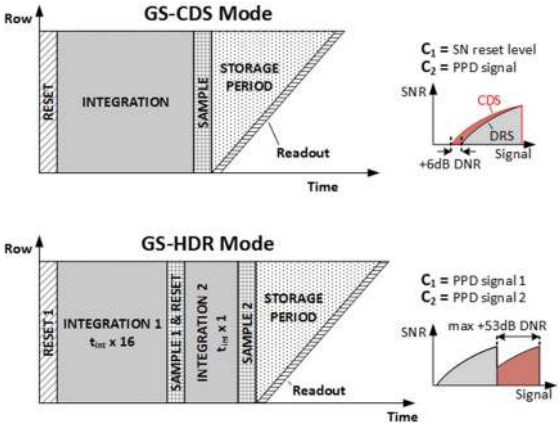

Fig. 5. Dynamic range extension modes

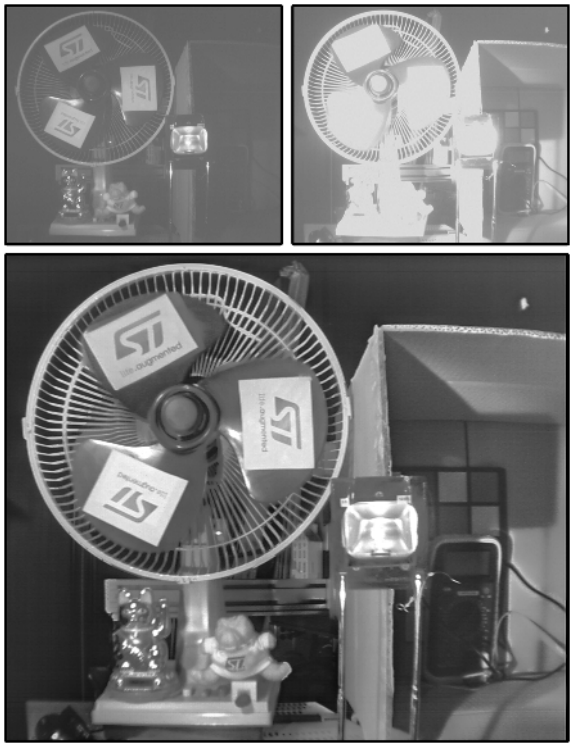

Fig. 6. HDR image (bottom) synthesised from short (top left) and long (top right) exposures. t_{int} ratio = 12:1

Parameter		Value
Pixel Array		1024(H) x 800(V)
Pixel Pitch		3.75 µm x 3.75 µm
Read Noise	RS	2.7 e-
	GS CDS	8.5 e-
	GS HDR	16.8 e-
Full Well Capacity		8100 e-
Sample Capacitors		2 x 16 fF
Parasitic Light Sensitivity	GS CDS	< -80 dB (1/10000)
	GS HDR	-70 dB (1/3000)
Dynamic Range	RS	69 dB
	GS CDS	59 dB
	GS HDR	102 dB (max)
Frame Rate		50 fps
Process Technology		BSI 90nm(BE)/65nm(FE) 1P4M

Table 1. Pixel performance summary