Background Calibration Techniques for Multistage Pipelined ADCs With Digital Redundancy

Jipeng Li, *Student Member, IEEE,* and Un-Ku Moon, *Senior Member, IEEE*

***Abstract*—The proposed digital background calibration scheme, applicable to multistage (pipelined or algorithmic/cyclic) analog-to-digital converters (ADCs), corrects the linearity errors resulting from capacitor mismatches and finite opamp gain. A high-accuracy calibration is achieved by recalculating the digital output based on each stage's equivalent radix. The equivalent radices are extracted in the background by using a digital correlation method. The proposed calibration technique takes advantage of the digital redundancy architecture inherent to most pipelined ADCs. In the proposed method, the SNR is not degraded from the pseudorandom noise sequence injected into the system. A two-channel ADC architecture with negligible overhead is also proposed to significantly improve the efficiency of the digital correlation. Simulation results confirm that 16-bit linearity can be achieved after calibration for an ADC with $\sigma = 0.1\%$ capacitor mismatches and 60 dB opamp gain.**

***Index Terms*—Analog-to-digital converter, capacitor mismatch, correlation, digital redundancy, finite opamp dc gain, multistage pipeline and algorithmic ADC, pseudorandom noise sequence, radix-based digital background calibration.**

I. Introduction

PIPELINED analog-to-digital converters (ADCs) have been used extensively in high performance digital communication systems. While the speed of state-of-the-art pipelined ADCs has exceeded 100 mega-samples per second (MSPS) in CMOS technology [1]–[4], the commonly achieved resolution is still bound within the range of 8–12 effective number of bits (ENOBs) due to the limitations set by component mismatches. Use of multibit-per-stage architecture and design optimization can achieve 14-bit performance as demonstrated in [5], but most pipelined ADCs with more than 12-bit resolution will usually require some kind of linearity enhancement techniques. Trimming is one such method, but it cannot track variations over time caused by component aging and temperature changes despite the high cost implementation. Self-calibration techniques, which measure errors by the converter itself and subtract the code error during the normal operation, can be used to improve the accuracy of high resolution ADCs. In many of the self-calibration techniques, although the code errors are calculated in the digital domain, they are actually subtracted in the analog domain using a separate calibration digital-to-analog converter (DAC) [6], [7]. More recently, digital self-calibration techniques, which subtract the code errors in the digital domain, have been introduced to relieve the accuracy requirements of analog calibration circuits [8]–[11]. While digital self-calibration has the advantage of low complexity and high accuracy, most implementations are calibrated in the foreground. That means the normal operation has to be interrupted to start the calibration cycle. Although the calibration can be done during the system power-up or standby, it is desirable to run the calibration at all times to track device and environmental variations.

To avoid the foreground interruptions, several background calibration schemes that are transparent to the normal operation have been proposed. A resistor-string DAC instead of a capacitor DAC was used in a 13-bit ADC, so that it could be calibrated in the background by a slow-but-accurate delta–sigma ADC [12]. This scheme can only be applied to an ADC with resistor-string DAC. Redundant pipeline stages can be added to substitute the stages under calibration as shown in [13], so that the normal operation need not be stopped during calibration. This results in a large overhead for die area and power dissipation. To create the needed time slots for calibration, a skip-and-fill algorithm was proposed [14], [15]. In this algorithm, the conversion of input samples is occasionally skipped, and a sample of calibration signal is converted instead. The missing input samples are later filled in digitally via nonlinear interpolation of data. The skip-and-fill method is relatively simple and accurate for implementation, but the input-signal bandwidth has to be limited to avoid performance degradation due to interpolated regeneration of skipped samples. In order to minimize this effective bandwidth reduction, a similar queue-based calibration scheme was used in an algorithm ADC design [16].

Several correlation-based methods have been proposed for background calibration in pipelined ADCs [17]–[21]. These methods modulate the calibration signal or capacitor DAC errors with a pseudorandom noise sequence in the analog domain and then demodulate them in the digital domain to extract the errors from the processed input signal. The input-signal bandwidth limitation and/or redundant analog hardware can be avoided using this method. Despite the added advantages, the previously reported correlation-based schemes are quite complex and slow to converge.

In the following, we present the details of a fast and accurate correlation-based background digital calibration scheme in the context of a 1.5-bit-per-stage pipelined or cyclic ADC architecture. The input-signal magnitude need not be reduced to allow the injection of pseudorandom calibration signal. The minimal addition of analog hardware for calibration keeps the original ADC design essentially unchanged. The correlation algorithm

Manuscript received January 3, 2003; revised May 21, 2003. This work was supported by the Center for Design of Analog-Digital Integrated Circuits (CDADIC) under National Science Foundation CAREER Grant CCR-0133530, and by Analog Devices. This paper was recommended by Associate Editor F. Duque-Carrillo.

The authors are with Department of Electrical and Computer Engineering, Oregon State University, Corvallis, OR 97331-3211 USA (e-mail: lijip@ece.orst.edu; moon@ece.orst.edu).

Digital Object Identifier 10.1109/TCSII.2003.816921

1057-7130/03$17.00 © 2003 IEEE

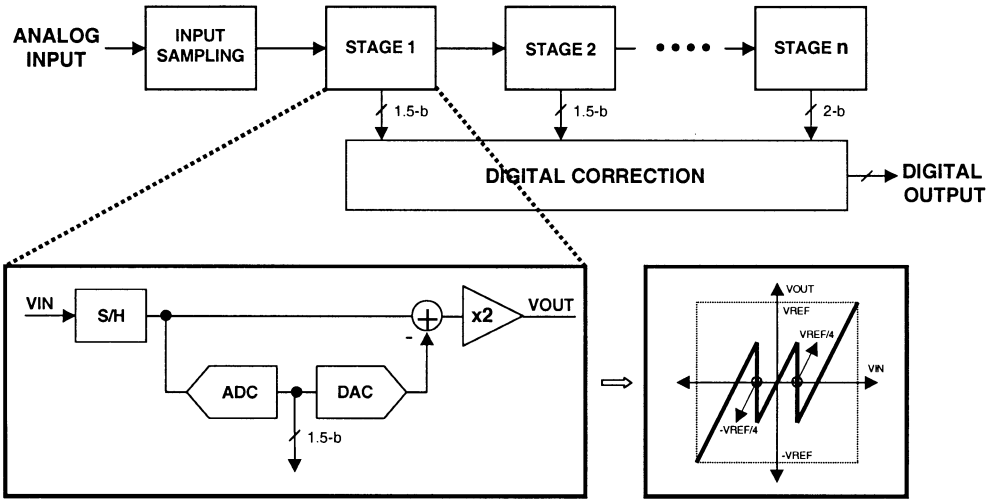


Fig. 1. 1.5-bit-per-stage pipeline ADC.

converges very quickly in the proposed two-channel ADC architecture because of the interference cancelling scheme employed. The rest of this paper is organized as follows. Section II describes the proposed calibration scheme; Section III provides the simulation results for verification; and final comments and conclusions are given in Section IV.

II. Proposed Digital Background Calibration

In the proposed calibration scheme, the errors due to capacitor mismatches and finite opamp gain are corrected by re-calculating the digital output based on the equivalent radix value of each stage. The equivalent radices are extracted on-line using a correlation-based algorithm. To minimize the interference from the input signal in the correlation-based radix extraction, a two-channel ADC architecture (with the same total capacitance and small power consumption overhead) is also proposed.

A. Radix-Based Digital Self-Calibration Concept

Fig. 1 shows the block diagram of a typical pipelined ADC with 1.5-bit-per-stage structure. This architecture is commonly used to maximize the conversion rate at a reasonable power consumption [22]. It consists of multiple cascaded stages. In each stage (except the last stage which has only a 2-bit flash ADC), the input signal is first quantized by a sub-ADC (flash ADC), then the output digital code is converted back to an analog signal by a sub-DAC. This quantized analog signal is then subtracted from the input signal, resulting in a *residue* that is amplified by two and then passed onto the next stage. In switched-capacitor implementations, the functions of sub D/A conversion, subtraction, and amplification are usually combined together and referred to as the multiplying digital-to-analog converter (MDAC). A widely used "capacitor-flip-over" MDAC is shown in Fig. 2. Assuming that the ADC is ideal, the analog output of each stage is given by

$$\begin{aligned} V_o &= 2V_i - D \cdot V_{\text{ref}} \\ &= 2\left(V_i - D \cdot \frac{V_{\text{ref}}}{2}\right) \end{aligned} \tag{1}$$

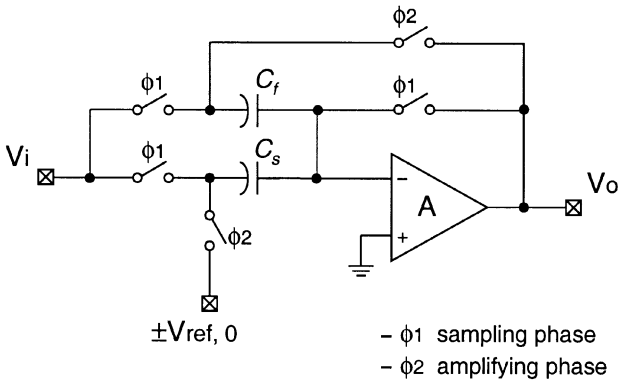


Fig. 2. "Capacitor-flip-over" MDAC.

where D is ± 1 or 0 depending on the input voltage level (i.e., the sub-ADC output). In the transistor level circuit implementation, the nonideal effects such as capacitor mismatches and finite opamp gain will add errors to the conversion. Fig. 3 shows the functional diagram of a pipeline ADC in the presence of nonideal terms, α_i, β_i, and δ_i, denoting the errors caused by capacitor mismatches and finite opamp gain. Since signal-independent charge injection and opamp offset only result in an equivalent overall offset to the pipeline ADC, they are not shown in Fig. 3. The resulting analog output of an MDAC is

$$V_o = (1+\delta)\big((2+\alpha)\cdot V_i - D\cdot(1+\beta)\cdot V_{\text{ref}}\big). \tag{2}$$

For a nonideal pipeline ADC with the error terms mentioned above, the conversion will be inaccurate and calibration is needed for an improved performance.

For a single-stage cyclic/algorithmic ADC, we can rewrite (2) as

$$V_o = (1+\delta)(2+\alpha)\left(V_i - D\cdot\frac{1+\beta}{2+\alpha}\cdot V_{\text{ref}}\right). \tag{3}$$

Note that (3) is equivalent to (1) if we take $(1+\delta)(2+\alpha)$ as the new radix (instead of 2) and $(2(1+\beta)/2+\alpha)\cdot V_{\text{ref}}$ as the redefined reference voltage. The correct digital output of the

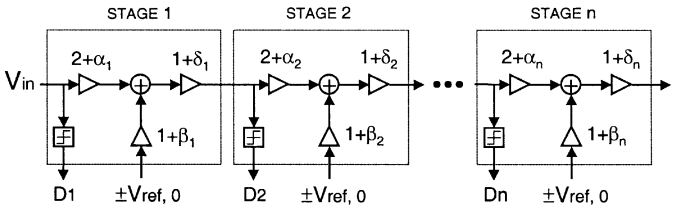


Fig. 3. Functional diagram of a pipeline ADC (1.5-bit-per-stage).

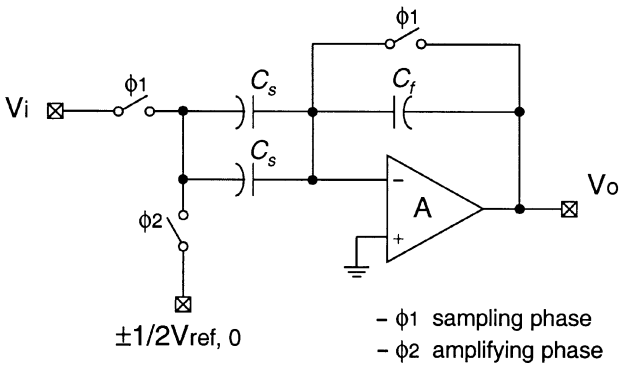


Fig. 4. "Noncapacitor-flip-over" MDAC.

ADC can now be obtained by using a simple radix calculation based on the modified radix value [16]

$$D_{\text{out}} = D_n + D_{n-1}\cdot(ra) + D_{n-2}\cdot(ra)^2 + D_2\cdot(ra)^{n-2} + D_1\cdot(ra)^{n-1} \tag{4}$$

where ra is the modified radix number (which is ideally equal to 2) taking into account the effects of all error terms. While the single-stage algorithm ADC displays this favorable feature, this algorithm can not be applied to a multistage ADC, because the redefined reference voltages (function of capacitor mismatches and finite opamp gain) will be different from stage to stage. To solve this problem, a "noncapacitor-flip-over" MDAC shown in Fig. 4 was used in [23]. In this modified MDAC scheme, the analog input V_i and the reference V_{ref} will see identical error terms, so the analog input and output relation can be written as [23]

$$V_o = ra\cdot\left(V_i - D\cdot\frac{V_{\text{ref}}}{2}\right). \tag{5}$$

Note that the radix number ra varies from stage to stage but the reference voltages ($V_{\text{ref}}/2$) are same for all stages. The correct digital output of the ADC can be calculated by [23]

$$D_{\text{out}} = D_n + D_{n-1}\cdot ra_{n-1} + D_{n-2}\cdot(ra_{n-1})(ra_{n-2}) + D_{n-3}\cdot(ra_{n-1})(ra_{n-2})(ra_{n-3}) + \cdots + D_1\cdot(ra_{n-1})(ra_{n-2})\cdots(ra_2)(ra_1). \tag{6}$$

Despite the simplicity found in the "noncapacitor-flip-over" MDAC of Fig. 4, the conventional "capacitor-flip-over" MDAC has the speed advantage due to the large feedback factor in the loop settling. Thus, it would be desirable to find a solution which can be applied to both MDAC structures.

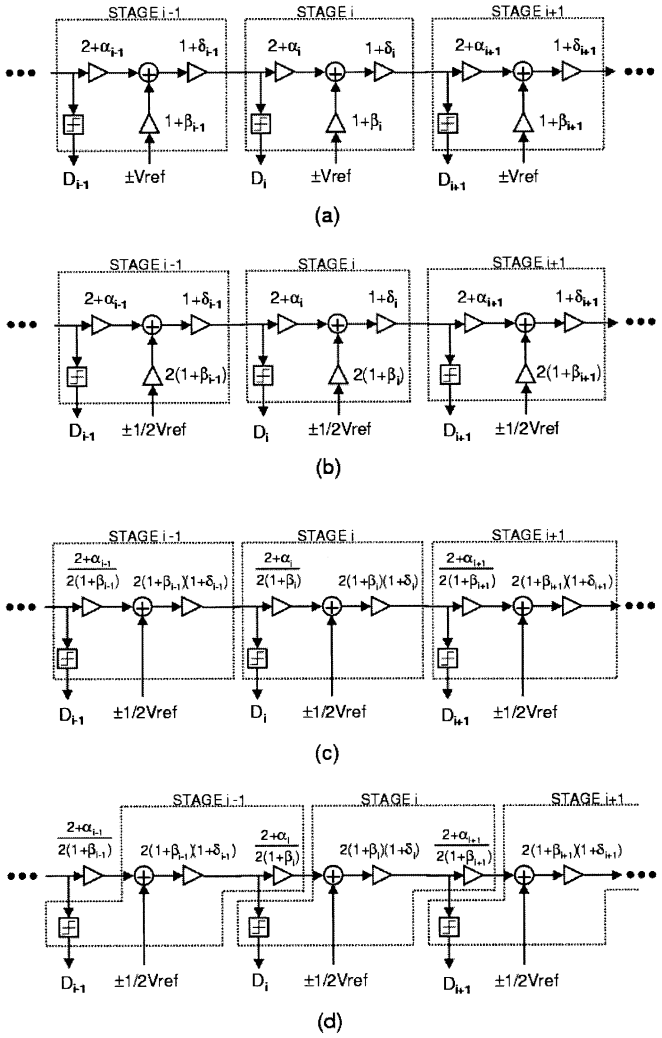


Fig. 5. Equivalent transformation of a pipeline ADC.

Such a solution indeed exists and can be achieved easily after some systematic manipulations. To understand how this general solution works, we can apply some equivalent transformations to the pipeline ADCs functional diagram of Fig. 3. The transformation procedure is shown in Fig. 5. Fig. 5(a) represents the functional diagram of a pipeline ADC with all error terms. If we change V_{ref} to $V_{\text{ref}}/2$ and adjust the gain factor of the reference voltage accordingly, we get the equivalent block diagram Fig. 5(b). Then, we merge the gain factor of the reference voltage into the gain factors of the input and the output to arrive at Fig. 5(c). Now, we simply redefine the stage's input and output so that each stage's input gain factor is merged into its previous stage's output gain factor, and the next stage's input gain factor is merged into output gain factor. The resulting equivalent ADC is shown in Fig. 5(d). Note that Fig. 5(d) is equivalent to the functional block diagram of a pipeline ADC where the MDACs input and output relationship can be written in the form of (5). The equivalent radix of each stage is now given by

$$ra_i = (1+\beta_i)(1+\delta_i)\left(\frac{2+\alpha_{i+1}}{1+\beta_{i+1}}\right). \tag{7}$$

This means we can now use (6) to calibrate multistage ADCs with "capacitor-flip-over" MDAC. As a result this radix-based digital calibration scheme becomes a general calibration technique and can be applied to any 1-bit-per-stage pipelined or algorithmic/cyclic ADC without the limitation on the structure of MDAC. The key point in the "capacitor-flip-over" MDAC was to redefine the stage's input and output so that the desired form of equivalent radix can be achieved. One resulting issue with this redefinition is that the comparators (sub-ADC) still see the original input voltage before the redefinition took place. It equivalently adds signal-dependent offset to the comparator (sub-ADC) input. Fortunately, this is not a problem because the added offset is small and can be compensated by the digital redundancy of the pipeline ADC without any performance degradation.

Although this kind of radix-based digital calibration scheme prefer 1-bit-per-stage ADC architecture for its simplicity, it can easily be applied to the 1.5-bit-per-stage architecture with little modification. We can still use (6) to recalculate the ADCs digital output. The digital output of each stage is now a three-level value (± 1 or 0) instead of the two level value (± 1) of the 1-bit-per-stage ADC. This is the only modification that we need to make in order for this radix-based calibration scheme to be adapted from the 1-bit-per-stage ADC to the 1.5-bit-per-stage ADC. In an uncalibrated 1.5-bit-per-stage ADC where all radices are "2," (6) is equivalent to a commonly used digital correction logic.

B. Background Equivalent Radix Extraction

In [23], radix extraction/measurement was employed in the foreground to obtain the equivalent radices in a nonideal pipeline ADC. The ADC operation has to be interrupted to perform this radix extraction/measurement. Because of this drawback, it is highly desirable to develop a background radix extraction scheme.

Among various background calibration techniques, the correlation-based schemes [17]–[21] are most promising because they involve minimum additional analog circuitry. In the calibration system, the small error terms resulting from capacitor mismatches and finite opamp gain are modulated by a pseudorandom sequence in the analog domain. Then, they are converted to a digital code along with the input signal to the ADC. These small error terms are detected in the digital domain by correlating the ADC digital output with the same pseudorandom sequence. Applying the correlation algorithm to the radix-based calibration described in the previous Section II-A, we can develop a simple and robust background digital calibration technique to pipelined ADCs.

Fig. 6 illustrates one possible (not optimum) background equivalent radix extraction scheme based on correlation. This calibration scheme incorporates a ± 1 pseudorandom noise sequence, which is scaled by a constant (1/4 in this example) and then added to the input of the sub-DAC. This pseudorandom noise travels through the interstage gain block which contains the actual radix number. Then, it is quantized by the back-end ADC. Finally, to maintain the same SNR, this added pseudorandom noise is subtracted from the back-end ADC's

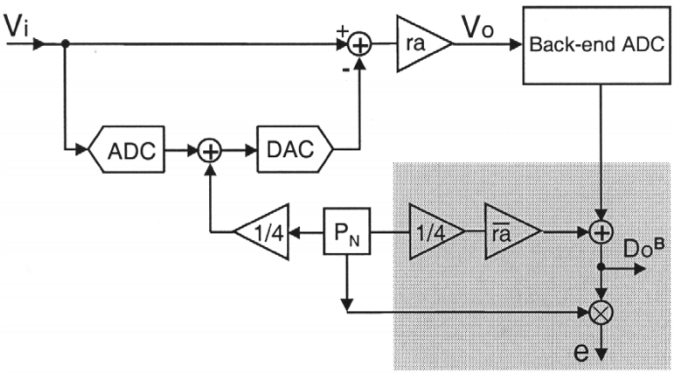


Fig. 6. Background equivalent radix-extraction scheme 1.

output in the digital domain. An estimated radix number has to be provided to do this pseudorandom noise cancellation. The resulting final digital output of the back-end ADC is given by

$$\begin{aligned} D_o^B &= \left(\frac{1}{4}\right) P_N \cdot \overline{ra} - \left(Q_N + \left(\frac{1}{4}\right) P_N\right) \cdot ra + O_N \\ &= -Q_N \cdot ra + \left(\frac{1}{4}\right) P_N \cdot (\overline{ra} - ra) + O_N \end{aligned} \tag{8}$$

where D_o^B is the final digital output of the back-end ADC, P_N is the pseudorandom noise sequence, ra is the actual radix, $\overline{ra}$ is the estimated radix, Q_N is the quantization noise of this stage, and O_N includes all other noise sources such as thermal noise and quantization noise of the back-end ADC. Note that the sub-DACs error has been merged into the actual radix from the radix-based calibration concept described earlier, so it can be seen as an error-free block. Also, if the estimated radix $\overline{ra}$ is not equal to the actual radix ra, the added pseudorandom noise will not be cancelled completely. If we now correlate the back-end ADC digital output with the same pseudorandom sequence, we can get the difference between the actual radix and the estimated radix

$$e = \left(\frac{1}{4}\right)(\overline{ra} - ra) - P_N \otimes (Q_N \cdot ra - O_N) \tag{9}$$

where e is the result of the correlation and $\otimes$ is the symbol for correlation. Ideally, since P_N is uncorrelated with Q_N or O_N, their correlation products will approach zero as we increase the length of the pseudorandom sequence.[1] Given a pseudorandom sequence that is long enough, the actual radix can be calculated as

$$ra = \overline{ra} - 4e. \tag{10}$$

Similar schemes can be found in [17], [18], and [20], in a slightly different context.

There are some practical issues about the correlation scheme described in the above. The first issue is that the amplitude of the ADCs input signal has to be reduced when injecting this pseudorandom noise. The reason is that each stage's analog

[1]To be precise, the quantization noise of the back-end ADC O_N contains a portion that is correlated to the pseudorandom sequence P_N, as all ADC quantization noise is finitely correlated to its input signal. The resulting estimation of radix error term will be limited due to this finite amount of correlation between P_N and O_N.

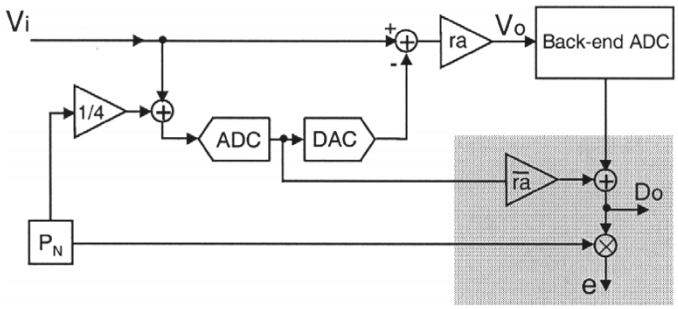


Fig. 7. Background equivalent radix-extraction scheme 2.

output has a maximum full signal range. Therefore the adding of pseudorandom noise can make the ADC stage's analog output to go out of the full-scale signal range if the input signal's magnitude is not reduced. The second issue is how to inject a *scaled* pseudorandom noise sequence in the analog domain with a very accurately known magnitude (i.e., the accuracy of 1/4 in the analog domain). This is not a trivial task in a practical integrated circuit (IC) implementation. The methods proposed in [17], [18], [20] add quite a bit of complexity to resolve this issue. For example, a slow-but-accurate delta–sigma ADC was employed to measure the changed reference voltage after injecting pseudorandom sequence [18]. Finally, beyond these two issues, any uncorrected (incompletely cancelled) pseudorandom sequence injected into the system directly degrades the SNR of the ADC under calibration.

In pipelined ADCs which incorporate digital redundancy, there is another way to do the background radix detection. This proposed method is illustrated in Fig. 7. Here, the scaled (by approximately 1/4) pseudorandom noise sequence is injected at the input of the sub-ADC instead of the sub-DAC. The resulting ADC digital output (combining this stage ADC and its back-end ADC) is

$$D_o = \left(V_i + Q_N + \left(\frac{1}{4}\right)P_N\right)\cdot \overline{ra} - \left(Q_N + \left(\frac{1}{4}\right)P_N\right)\cdot ra + O_N$$
$$= V_i \cdot \overline{ra} + Q_N \cdot (\overline{ra} - ra) + \left(\frac{1}{4}\right)P_N \cdot (\overline{ra} - ra) + O_N. \quad (11)$$

If we correlate the ADC digital output with the same pseudorandom sequence, we get

$$e = \left(\frac{1}{4}\right)(\overline{ra} - ra) + P_N \otimes \left(V_i \cdot \overline{ra} + Q_N \cdot (\overline{ra} - ra) + O_N\right). \quad (12)$$

By similar theoretical reasoning, since V_i, Q_N and O_N are uncorrelated with P_N, we can ignore their correlation products if the pseudorandom sequence is long enough.[2] And the actual radix can be calculated using (10).

It may be seen that the second equivalent radix detection scheme is similar to the first one. The key modification here is to inject the pseudorandom sequence at the input of the sub-ADC instead of the sub-DAC. This change gives us many advantages as we do not suffer from the practical issues mentioned in the first scheme (Fig. 6). First, the injected pseudorandom noise can be seen as being equivalent to time-varying (but limited/bounded) comparator offsets, thus it can be compensated by the digital redundancy of the pipeline ADC without any performance degradation. Therefore, it is unnecessary to reduce the input-signal magnitude when injecting the pseudorandom noise. Second, we do not need to face the complications of needing an accurate scaling (1/4 value) in the analog domain.[3] Third, in the circuit implementation, the injection of pseudorandom noise can be done by randomly varying the comparator threshold level (comparator dithering), as long as this variation/dithering does not exceed the bounds of digital redundancy. There is no change to the MDAC, which is the most critical and sensitive block in the pipeline ADC design. As a result, we can expect faster operation and less noise coupling from this radix detection scheme compared to the radix extraction scheme 1 shown in Fig. 6 which needs to modify the MDAC to inject the pseudorandom noise at the input of sub-DAC. Because of these advantages, this "comparator dithering" equivalent radix detection scheme is proposed as the most preferred digital background calibration scheme. Recently, a very similar calibration technique was developed independently by Murmann and Boser to correct the linear and nonlinear gain errors in the residue amplifier of a multibit gain stage in a pipeline ADC [21]. While both calibration techniques take advantage of the digital redundancy in pipelined ADCs for error detection, the proposed scheme in this paper uses a 1.5-bit/stage architecture to also correct for the DAC nonlinearity (due to capacitor mismatches).

C. Interference Cancelling in Calibration

Although the proposed correlation-based algorithm of Fig. 7 can be employed "as is" to extract the equivalent radix, the process would be slower and less accurate than the foreground algorithm in [23]. The main reason is the strong interference from the input signal to the ADC. Specifically, when we correlate the ADCs digital output with the pseudorandom sequence to detect the radix error, the input signal is transformed into noise at the same time (because the input signal is uncorrelated to the pseudorandom sequence). This input-signal transformed noise will interfere with the radix error detection, making it less accurate or very slow. This situation is illustrated in Fig. 8. As shown in the figure, e is the small radix error that needs to be extracted. It is first modulated by a pseudorandom sequence P_n, then added to the ADCs input signal V_{in}. After A/D conversion, it is demodulated in the digital domain. This illustration directly represents Fig. 7 with (11) and (12). Comparing the spectrum before and after demodulation, we can observe an obvious rise of the noise floor that is due to the input signal being transformed into noise. Although other noise sources such as thermal noise, $1/\text{f}$ noise, and back-end ADCs quantization noise also affect the detection, the signal transformed noise is the dominant

[2]We note once again that the quantization noise of the back-end ADC O_N is finitely correlated to the pseudorandom sequence P_N. Higher the effective resolution of the back-end ADC, lower this finite amount of correlation which limits the overall accuracy of the radix error estimation.

[3]Even though we loosely use a scaled value of approximately 1/4 in the discussion, a practical implementation would need a value closer to 1/8 so that the digital redundancy would accommodate for actual circuit-level offsets as well as the pseudorandom signal.

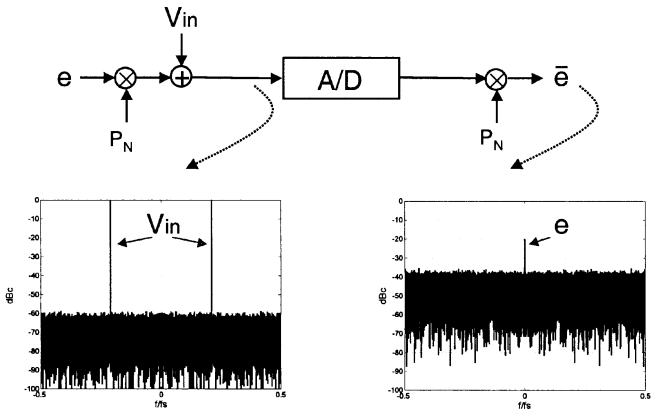


Fig. 8. Interference in the radix-error detection.

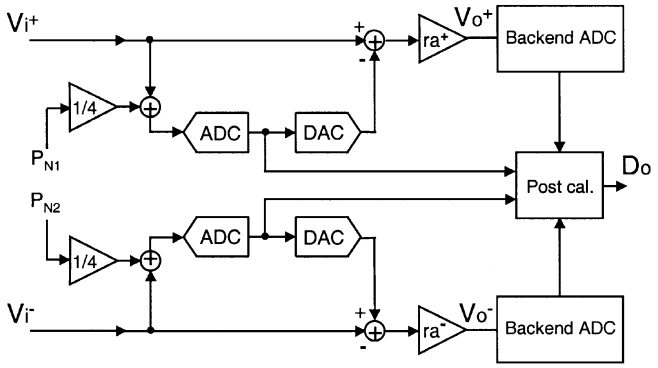


Fig. 9. Two-channel ADC architecture.

interference because the signal is usually strong (e.g., full scale input), and other noise sources are much smaller in comparison. This interference issue is common to all correlation-based calibration techniques. And it will limit the calibration accuracy. This problem is usually minimized by increasing the length of the pseudorandom sequence, but it is not very effective because the noise level only goes down by a 3 dB for each doubling of the sequence length.

To mitigate this problem, we propose a two-channel ADC architecture shown in Fig. 9. Instead of a single-channel ADC, we put two identical ADCs in parallel to build a two-channel ADC. The two ADC channels are not time-interleaved. Instead, they take the same input signal but with opposite polarity. The final digital output of this two-channel ADC is given by

$$D_o = D_o^+ - D_o^- \tag{13}$$

where D_o^+ is the positive (P) channel ADCs digital output and D_o^- is the negative (N) channel ADCs digital output. When we apply the proposed background radix extraction algorithm to this two-channel ADC, we can use two uncorrelated pseudorandom sequences to extract both radices in P channel and N channel at the same time. Despite this overhead, the ADCs input signal can be cancelled by adding the two channels' digital output together when we do the equivalent radix extraction using correlation. The computational efficiency of the proposed background radix extraction process can be improved dramatically because the majority of input-signal component is removed in the correlation process. If the two ADC channels are perfectly matched, the efficiency of this background radix extraction algorithm could be as good as a foreground algorithm that is performed in the absence of the input signal. In practical designs, channel mismatches such as offset mismatch and gain mismatch will limit performance. While these mismatches can severely degrade the SNDR in *time-interleaved* two-channel ADCs, here they only mildly reduce the efficiency of the background radix extraction algorithm because of the incomplete cancelling of the ADCs input signal in the correlation process. No tones will be produced because the operations of these two ADC channels are parallel and synchronized, not time-interleaved. To speed up the radix detection algorithm even more, some channel mismatch calibration methods could also be employed with added circuitry. If necessary, in this proposed two-channel ADC architecture, the mismatches can also be calibrated out easily in the background as the two ADC channels are essentially processing the same signal but opposite polarity.

At first glance, it would seem that the two-channel ADC architecture will double the die area as well as power dissipation. But in reality, it just increases the die area taken up by the comparators and the digital calibration circuitry. The reason is similar to why fully-differential design will not double the die size in comparison to a single-ended design given the same SNR requirement. In high-accuracy switched-capacitor circuits, the die size is dominated by the total capacitor area. And the capacitor size is determined by the kT/C noise requirement. Given the same SNR requirement and the same input-signal magnitude, we can reduce each ADC channel's capacitor size by half, so the total capacitor size of this proposed two-channel ADC is equal to the total capacitor size of a conventional single-channel ADC. Although the resulting noise power would be four times higher in the proposed two-channel ADC, the equivalent input-signal power is also four times higher since the equivalent input-signal magnitude is doubled (we take both ADC channels' digital output). Thus the SNR will not change. The main die size overhead is due to the fact that the number of comparators and digital calibration hardware is doubled (the number of opamps is also doubled but each opamp is smaller) in the proposed two-channel ADC architecture. Fortunately, these additional circuit blocks can be made small and maintain a low additional power consumption.

Fig. 10 shows the overall ADC with proposed background calibration scheme using two uncorrelated pseudorandom sequences P_{N1} and P_{N2} to calibrate both channels simultaneously. To achieve a very robust operation, we use an iterative approach to extract the equivalent radix instead of using (10). First, we give an initial value to the estimated radix. Then, we start an iteration to approach the actual radix value. The radix update equations are

$$\begin{aligned}\overline{ra^+}[n+1] &= \overline{ra^+}[n] - \Delta \cdot \left((Do^+ + Do^-) \otimes P_{N1}\right) \\ \overline{ra^-}[n+1] &= \overline{ra^-}[n] - \Delta \cdot \left((Do^+ + Do^-) \otimes P_{N2}\right)\end{aligned} \tag{14}$$

where $\overline{ra^+}$ and $\overline{ra^-}$ are the estimated radices of P and N channel ADC stages, respectively; P_{N1} and P_{N2} are the two pseudorandom noise sequences used in radix extraction; n is the iteration index; and Δ is the step size. After a certain

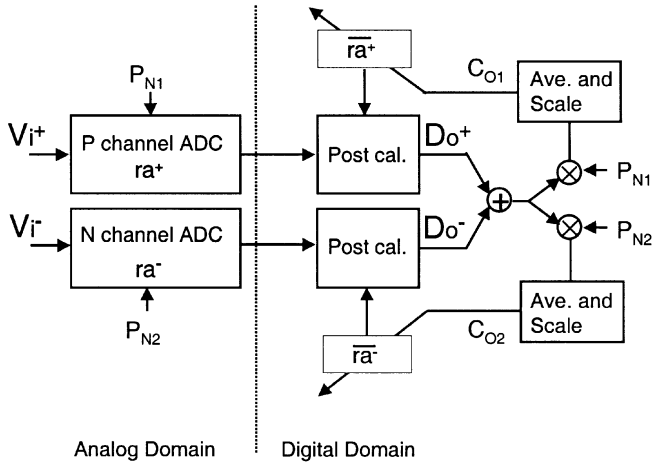


Fig. 10. Overall ADC with proposed background digital calibration.

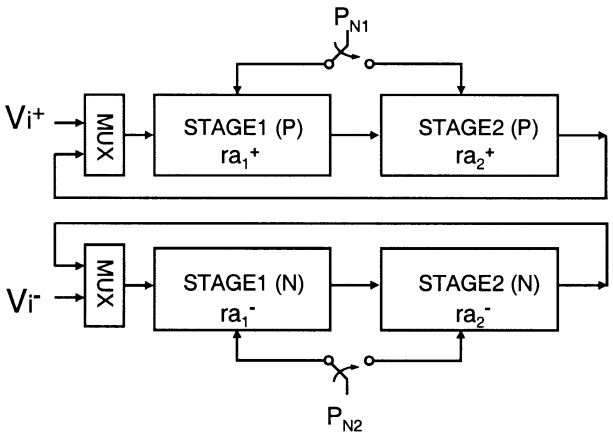


Fig. 11. Prototype two-stage cyclic ADC applying proposed calibration.

number of steps, the estimated radix will converge to the actual equivalent radix. The main advantage of this iterative method is that the calibration of each stage is insensitive to the errors of its back-end ADC. That makes it very accurate, robust, and easy to implement.

When there are multiple stages that need to be calibrated, we can choose to use more pseudorandom noise sequences to extract the radices simultaneously. To reduce the number of pseudorandom noise sequences, we can share the same pseudorandom noise sequence among different stages and do the multistage ADC calibration by stepping through one stage at a time. Pushing this to the extreme, ultimately only one pseudorandom sequence is required, which can then be stepped through one block at a time (shared among channels as well as stages).

III. Simulation Results

Some behavioral simulations have been performed to verify the proposed calibration scheme. The prototype ADC in simulation was a 17-bit two-stage cyclic/algorithmic ADC as shown in Fig. 11. Note that the pseudorandom sequences are shared between two stages in this example to reduce the number of pseudorandom sequence generators. Gaussian distributed random capacitor mismatches of $\sigma = 0.1\%$ and 60 dB opamp gain were assumed for this ADC. The two ADC channels were

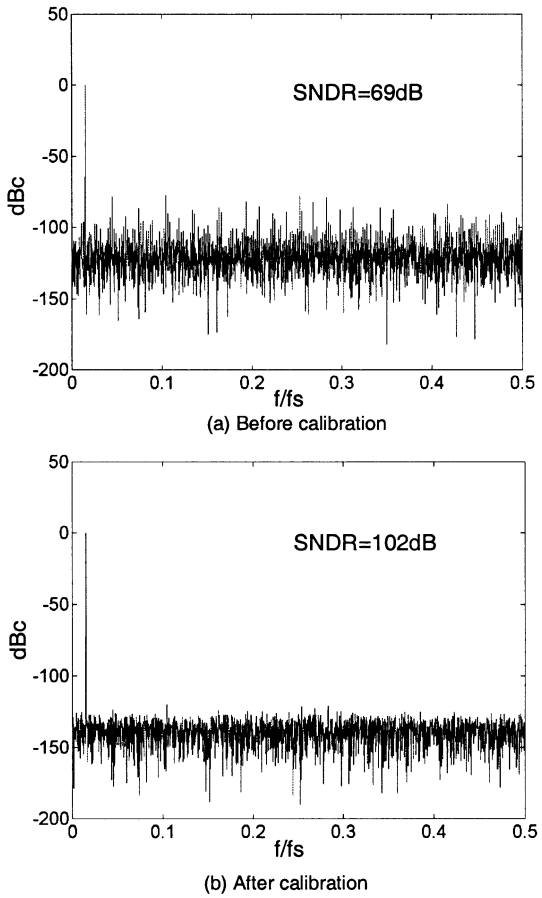


Fig. 12. Output spectrum of the prototype ADC before and after calibration.

also given a fixed $1\%V_{\rm ref}$ offset and 1% gain mismatches. In the equivalent radix extraction, the number of total samples was 2^{20}, and the radix update step size Δ was 2^{-24}. One typical output spectrum of the prototype ADC is shown in Fig. 12. In this case, the equivalent radices calculated by using (7) were 2.002 and 1.996 for the P channel, and 2.004 and 1.998 for the N channel. The values extracted by applying the proposed algorithm were 2.001 990 and 1.996 029 for the P channel, and 2.003 979 and 1.998 014 for the N channel. Fig. 12(a) shows the output spectrum of the prototype ADC before calibration. The SNDR before calibration is 69 dB. Fig. 12(b) shows the simulation results of the same ADC after the proposed background calibration is applied. The SNDR is improved to 102 dB.

IV. Conclusion

A background digital self-calibration technique for multistage pipelined or cyclic/algorithmic ADCs has been described. This technique can correct the errors resulting from capacitor mismatches and finite opamp gain. An accurate calibration is achieved by re-calculating the digital output based on each stage's equivalent radix. These equivalent radices are extracted in the background by applying a correlation process using pseudorandom noise sequence. The pseudorandom noise sequence is injected at the input of the sub-ADC such that the input signal is unaltered by the added noise. The inherent digital redundancy of the pipelined ADC architecture compensates for the

added pseudorandom noise without reducing the input-signal range and without degrading the SNR of the ADC system. The efficiency of the correlation algorithm can be improved significantly by using a two-channel ADC architecture with small die area and power consumption overhead. Simulation results indicate that a significant SNDR improvement can be achieved by using the proposed calibration technique. Although the 1.5-bit-per-stage architecture is chosen to demonstrate the operation of the proposed calibration technique, the proposed technique can be generally applied to other multibit-per-stage architectures. In the case of a multibit-per-stage architecture, a binary-weighted DAC (instead of thermometer DAC) can be used to reduce the number of variables in calibration.

ACKNOWLEDGMENT

The authors would like to thank the anonymous reviewers for their valuable comments which have been incorporated into the final version of this manuscript.

REFERENCES

[1] K. Kim, N. Kusayanagi, and A. Abidi, "A 10-b 100MS/s CMOS A/D converter," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1996, pp. 419–422.

[2] D. G. Nairn, "A 10-b, 3V, 100MS/s pipelined ADC," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 2000, pp. 257–260.

[3] Y. Park, S. Karthikeyan, F. Tsay, and E. Bartolome, "A 10-b 100MS/s CMOS pipelined ADC with 1.8V power supply," *In ISSCC Dig. Tech. Papers*, pp. 130–131, Feb. 2001.

[4] S. Yoo, T. Oh, J. Moon, S. Lee, and U. Moon, "A 2.5V 120 MSample/s CMOS pipelined ADC with high SFDR," *In. Proc. IEEE Custom Integrated Circuit Conf.*, vol. 23, pp. 441–444, May 2002.

[5] W. Yang, D. Kelly, I. Mehr, M. Sayuk, and L. Singer, "A 3-V 340 mW 14-b 75 Msample/s CMOS ADC with 85-dB SFDR at Nyquist input," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1931–1936, Dec. 2001.

[6] H. Lee, D. Hodges, and P. Gray, "A self-calibrating 15-b CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 813–819, Dec. 1984.

[7] Y. Lin, B. Kim, and P. Gray, "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3u CMOS," *IEEE J. Solid-State Circuits*, vol. SC-26, pp. 628–636, Apr. 1991.

[8] S. Lee and B. Song, "Digital-domain calibration of multistep analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1679–1688, Dec. 1992.

[9] A. Karanicolas and H. Lee, "A 15-b 1-Msample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, pp. 1207–1215, Dec. 1993.

[10] S. Lee and B. Song, "Interstage gain proration technique for digital-domain multistep ADC calibration," *IEEE Trans. Circuits Syst. II*, vol. 41, pp. 12–18, Jan. 1994.

[11] H. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE J. Solid-State Circuits*, vol. 29, pp. 509–515, Apr. 1994.

[12] T. Shu, B. Song, and K. Bacrania, "A 13-b, 10-Msample/s ADC digitally calibrated with oversampling delta–sigma converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1866–1875, Dec. 1997.

[13] J. Ingino and B. Wooley, "A continuously calibrated 12-b 10-Ms/s 3.3-V A/D converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1920–1931, Dec. 1998.

[14] U. Moon and B. Song, "Background digital calibration techniques for pipelined ADCs," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 102–109, Feb. 1997.

[15] S. Kwak, B. Song, and K. Bacrania, "A 15-b, 5-Msample/s low-spurious CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1866–1875, Dec. 1997.

[16] O. Erdogan, P. Hurst, and S. Lewis, "A 12-b digital-background-calibrated algorithmic ADC with -90-dB THD," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1812–1820, Dec. 1999.

[17] R. Jewett, K. Poulton, K. Hsieh, and J. Doernberg, "A 12-b 128 Msamples/s ADC with 0.05LSB DNL," in *Proc Int. Solid-State Circuits Conf.*, Feb. 1997, pp. 138–139.

[18] J. Ming and S. Lewis, "An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration," *IEEE J. Solid-Sate Circuits*, vol. 36, pp. 1489–1497, Oct. 2001.

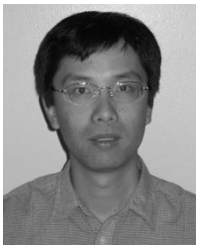
[19] I. Galton, "Digital cancelation of D/A converter noise in pipelined A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 185–196, Mar. 2000.

[20] E. Siragusa and I. Galton, "Gain error correction technique for pipelined analog-to-digital converters," *Electron. Lett.*, vol. 36, pp. 617–618, 2000.

[21] B. Murmann and B. Boser, "A 12-b 75MS/s pipelined ADC using open-loop residue amplifier," *ISSCC Dig. Tech. Papers*, pp. 330–331, Feb. 2003.

[22] S. Lewis, "Optimizing the stage resolution in pipelined, multistage, analog-to-digital converters for video-rate applications," *IEEE Trans. Circuits Syst. II*, vol. 39, pp. 516–523, Aug. 1992.

[23] D. Chang and U. Moon, "Radix-based digital calibration technique for multistage ADC," in *Proc. IEEE Int. Symp. Circuits Systems*, vol. II, May 2002, pp. 796–799.



Jipeng Li (S'01) received the B.S.E.E. degree and the M.S.E.E. degree from Fudan University, Shanghai, China, in 1995 and 1998, respectively. Since September 1999, he has been with Oregon State University, Corvallis, where he is working toward the Ph.D. degree in electrical engineering.

From July 1998 to July 1999, he worked with the ZTE corporation, Shanghai, China, designing RF transceivers for GSM base station system. His doctoral research focuses on accuracy enhancement techniques in low-power and high-speed pipelined analog-to-digital converter design. During the summer of 2001, he was with Analog Devices Inc., Beaverton, OR, designing bipolar junction transistor mixers for 3–6-GHz wireless communication. His current research interests include analog and mixed signal integrated-circuit design for broadband digital communication systems.

Un-Ku Moon (S'92–M'94–SM'99) received the B.S. degree from University of Washington, Seattle, the M.Eng. degree from Cornell University, Ithaca, NY, and the Ph.D. from University of Illinois, Urbana-Champaign, all in electrical engineering, in 1987, 1989, and 1994, respectively.

From February 1988 to August 1989, he was a Member of Technical Staff at AT&T Bell Laboratories, Reading, Pennsylvania, and during his stay at the University of Illinois, Urbana-Champaign, he taught a microelectronics course from August 1992 to December 1993. From February 1994 to January 1998, he was a Member of Technical Staff at Lucent Technologies Bell Laboratories, Allentown, Pennsylvania. Since January 1998, he has been with Oregon State University, Corvallis. His interest has been in the area of analog and mixed analog-digital integrated circuits. His past work includes highly linear and tunable continuous-time filters, telecommunication circuits including timing recovery and analog-to-digital converters, and switched-capacitor circuits.