Backside illuminated SPAD image sensor with 7.83m pitch in 3D-stacked CMOS technology

Backside Illuminated SPAD Image Sensor with 7.83µm Pitch in 3D-Stacked CMOS Technology

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***Abstract*—**We present the first 3D-stacked backside illuminated (BSI) single photon avalanche diode (SPAD) image sensor capable of both single photon counting (SPC) intensity, and time resolved imaging. The 128×120 prototype has a pixel pitch of 7.83µm making it the smallest pixel reported for SPAD image sensors. A low power, high density 40nm bottom tier hosts the quenching front end and processing electronics while an imaging specific 65nm top tier hosts the photo-detectors with a 1-to-1 hybrid bond connection [1]. The SPAD exhibits a median dark count rate (DCR) below 200cps at room temperature and 1V excess bias, and has a peak photon detection probability (PDP) of 27.5% at 640nm and 3V excess bias.

I. Introduction

The integration of SPADs in CMOS processes more than a decade ago spurred the development of a variety of low light and time correlated sensors utilizing the SPAD's sensitivity and timing performance. Several time-gated SPAD image sensors have been published highlighting the main tradeoff between pixel complexity, sensitivity and silicon area. Digital approaches tend to have large pixels due to the size of logic gates implemented in older technology nodes [2]. Other single bit digital pixels alleviate this limitation at the cost of full well capacity and high data rates [3]. Analog approaches have managed to shrink the pixel down to an 8µm pitch while maintaining a relatively high fill factor but at the cost of temporal resolution and added noise from analog counters and readout [4]. Such tradeoffs have constrained SPAD image sensors to spatial resolutions of QVGA or lower and limited their adoption in applications such as endoscopy, where the miniature sensor form factor is a key requirement.

While realizing such designs in planar processes is challenging, the advent of 3D-stacking enables new possibilities in terms of sensor architectures and process nodes. Although a time resolved stacked BSI Geiger-mode APD image sensor has been reported in [5], it had a large pixel pitch of 50µm and lacked the ability to count photons within an exposure period. Hence we present the first 3D integrated BSI SPAD image sensor capable of both intensity and time resolved imaging. Combining an advanced 40nm bottom tier which enables high integration density and a 65nm imaging specific top tier, the sensor achieves the smallest SPAD pixel pitch to date at 7.83µm with 45% fill factor, peak PDP of 27.5% at 640nm, temporal aperture ratio (TAR) of 1 and full well capacity of 4095 photons.

High TAR and fill factor allows the sensor to attain the highest effective quantum efficiency (EQE) possible for its operation. The low noise floor and noiseless digital frame summation permit a high dynamic range (80.88dB) towards shot-noise limited photon counting imaging. Nanosecond temporal binning and gating offer additional capabilities over other comparable low-light sensitive BSI image sensor technologies.

II. Architecture

The fabricated die has an area of 2.4mm by 2.4mm and is divided into 4 completely independent 1.2mm by 1.2mm chips or trials within one seal ring and one pad ring as shown in Fig. 1. All of the trials are identical in terms of their system blocks (Fig. 2) but with slight variations to the in-pixel quenching front end or the SPAD structure. All results presented herein refer exclusively to the main trial.

As the aim of this work is to evaluate what could be integrated in such a small area image sensor targeting biomedical applications, the system was kept as simple as possible while focusing on the optimization of the pixel array. Hence, all voltages, controls and timing signals are generated externally. The readout implemented is a two channel serial interface, one per sixty rows, operating at 50MHz allowing a frame rate of 500fps in global shutter (GS) mode assuming an exposure time of 155µs.

III. Pixel

In this work the pixel constituents are split between the two tiers with a 1-to-1 hybrid bond connection [1]. Only the photo-detector is implemented on the top tier to maximize fill factor while the bottom tier contains all the circuitry.

A. SPAD

The SPAD multiplication junction is formed between a p-well implant and a deep n-well implant with a virtual retrograde guard ring as in [6]. The detector array on the top tier is formed from closely packed SPADs at 7.83µm pitch all sharing the same deep n-well yielding a drawn fill factor of 45%. While this is a BSI technology, the effective fill factor is unlikely to be greater than the drawn as this is an isolated SPAD structure. The common deep n-well is reverse biased to the excess bias voltage above the 12V breakdown of the device to operate it in Geiger-mode. Individual p-well anodes act as moving nodes and are connected to their corresponding processing pixels on the bottom tier through a vertical metal stack. Fig. 4 shows a layout cross section of the array. On the

top tier, a metal 2 plate is fabricated over the p-well region to act as a reflector that enhances PDP at longer wavelengths.

B. Pixel Circuitry

Fig. 5 shows the circuit diagram of the implemented pixel. A thick oxide front end allows the SPAD to be biased with an excess voltage up to 3.3V. The SPAD pulse is then level shifted to low voltage levels compatible with the low power 40nm process thin oxide logic. The pixel has two GS modes of operation; (1) SPC intensity imaging and (2) time-gated imaging. The required mode of operation is selected by the global mode control signal.

In intensity mode, a bank of toggle flip flops comprises a 12-bit ripple counter triggered by the SPAD's asynchronous pulses giving a full well capacity of 4095 photons with zero parasitic light sensitivity (PLS). Fig. 3 shows a single shot intensity image captured by the sensor. In time-gated mode, the counter is split into two 6-bit banks or bins operating in parallel. When the in-pixel gating logic detects a photon within the globally broadcasted time gates, the corresponding bin is incremented. Figs. 6 and 7 show an indirect time of flight depth map resolved in gating mode and various time gate profiles of the first bin of a selected pixel.

Rolling shutter (RS) intensity imaging is also possible. As discussed in [7], a sensor's TAR is dependent on its deadtime period throughout a measurement. RS permits zero deadtime readout by instantaneous sampling of the digital counter values into the serial interface, and by allowing the counters to wraparound without an active reset period where the integrated signal can be recovered by frame differencing. At low light levels, the probability of at least two photons hitting the SPAD within a typical 20ns deadtime is negligible (Fig. 8) rendering pile-up effects insignificant. Hence, the sensor is capable of continuous SPC with TAR of 1 and the maximum attainable EQE of 12.38%.

IV. Characterization Results

Characterization results, mainly of the photo-detector, are presented in order to evaluate its performance in a BSI implementation. DCR was measured at room temperature for different excess bias voltages as shown in Fig. 9. At 1V excess bias, the SPAD exhibits a median DCR below 200cps which increases exponentially with the applied voltage.

The timing performance or jitter of the SPAD was measured with a LeCroy WaveRunner 4GHz oscilloscope which timed the interval between the sync signal of a Hamamatsu PLP10 laser and the pulse of a buffered SPAD output of an edge pixel. A neutral density filter was used to ensure that no more than 5 SPAD pulses were observed for every 100 laser repetitions and more than 30k hits were recorded per measurement. Fig. 10 shows the results at different excess bias voltages without correcting for the laser pulse width of 53ps and 56ps FWHM at 443nm and 773nm respectively, or the output buffer chain jitter contributions. At excess bias voltages higher than 2V the jitter does not reduce any further.

To evaluate the sensor's photo response non-uniformity (PRNU), 5000 frames were captured under fixed illumination level and 25% of full well. The mean frame is shown in Fig. 11. After excluding the 4 rightmost columns without metal reflectors, the normalized array histogram was plotted (inset) and a PRNU less than 2% was calculated without correcting for high DCR pixels.

PDP results for pixels with metal reflectors at different excess bias voltages are shown in Fig. 12 with a peak of 27.5% at 640nm. Fig. 13 compares the PDP of pixels with and without reflectors at 3V excess bias demonstrating an improvement up to 6% at 820nm. Compared to an equivalent implementation in a front side illuminated (FSI) technology, the BSI SPAD PDP response heavily attenuates the blue region of the spectrum. This is due to the absorption of short wavelengths near the top of the backside far from the reach of the deep isolated multiplication junction.

To demonstrate the sensor's noiseless SPC capability, 5000 frames were captured under constant illumination at each exposure setting for exposure times ranging from 20ns to 1ms. For a randomly selected pixel, the standard deviation and mean signal at each of the settings were plotted as shown in Fig. 14. The data matches with ideal Poisson statistics demonstrating shot-noise limited SPC with zero read noise. Similarly, the standard deviation and mean signal for a random frame were plotted showing a similar behavior but with noticeable deviation from the ideal curve at higher signal levels due to PRNU.

V. Conclusion

We have demonstrated and characterized the first BSI 3D-stacked SPAD image sensor capable of both intensity, and time resolved imaging. The sensor's performance parameters are summarized in Table I.

Acknowledgment

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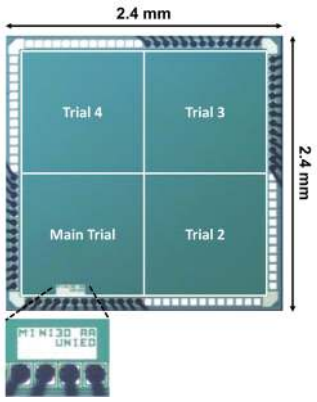

Fig. 1. Micrograph of top tier showing the 4 independent trials and the line name.

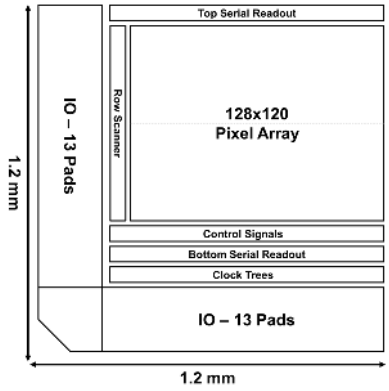

Fig. 2. Individual trial block diagram.

Fig. 3. Single shot grayscale intensity image with no post processing. White dots are high DCR pixels.

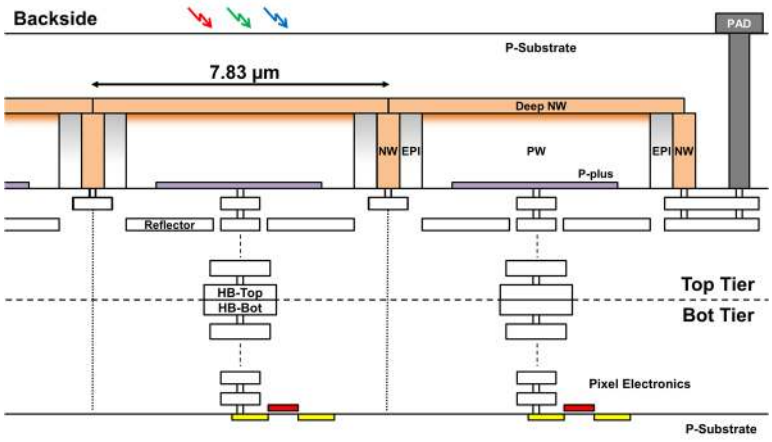

Fig. 4. Array layout cross section.

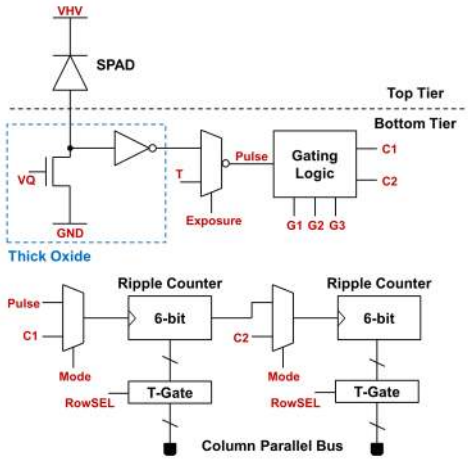

Fig. 5. Pixel circuit diagram.

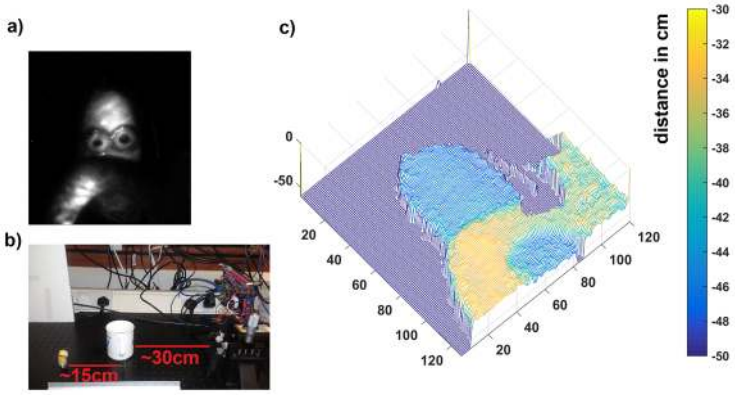

Fig. 6. Indirect time of flight experiment with 4ns laser pulse width, a) is intensity image of sensor's field of view, b) is bench setup and c) is resolved depth map with median filter applied showing a toy behind a mug's handle.

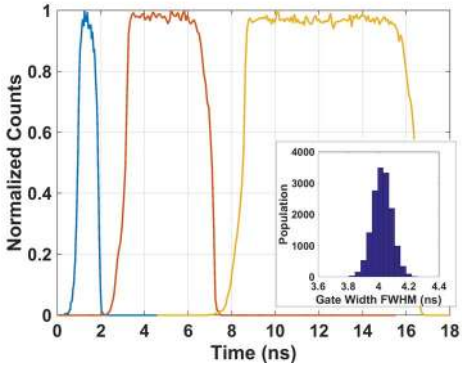

Fig. 7. 1ns, 4ns and 8ns FWHM time gate profiles of bin1 of a selected pixel. Inset is histogram of the 4ns gate width across the array with 64ps standard deviation.

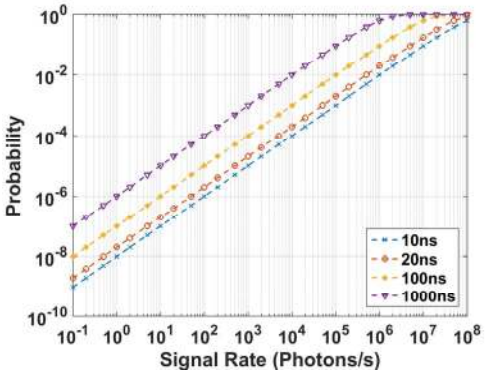

Fig. 8. Modeled probability of at least two photons hitting the SPAD within a given detector deadtime (legend) at different photon rates.

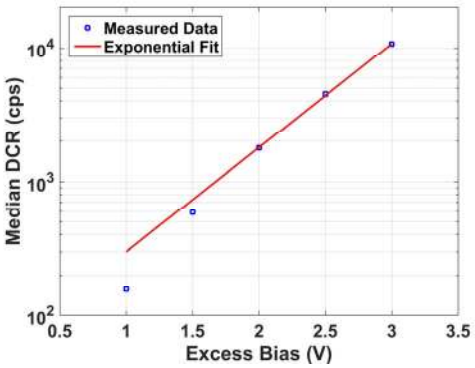

Fig. 9. Median DCR in counts per second versus excess bias voltage.

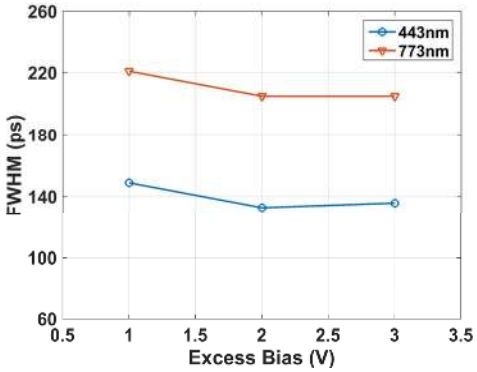

Fig. 10. SPAD jitter versus excess bias voltage at 443nm and 773nm.

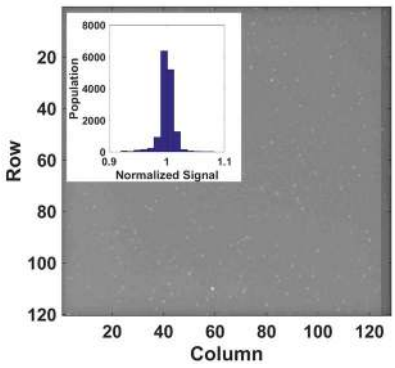

Fig. 11. Mean frame of 5000 captures under fixed illumination. Inset is histogram of normalized signal response excluding the 4 rightmost columns without metal reflectors

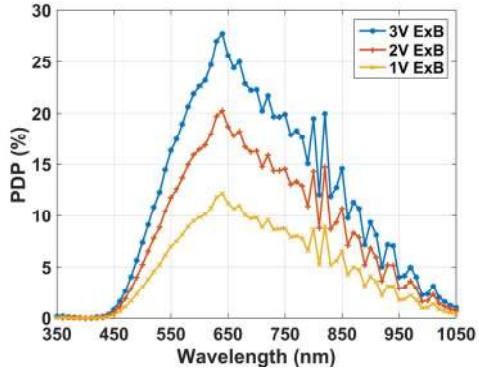

Fig. 12. PDP versus wavelength at different excess bias voltages for pixels with metal reflector.

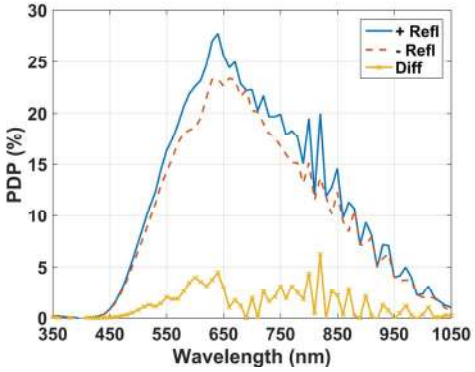

Fig. 13. PDP comparison of pixels with and without metal reflector at 3V excess bias.

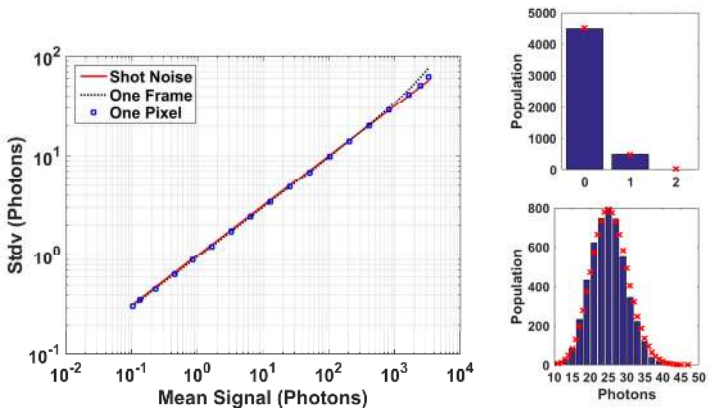

Fig. 14. Photon transfer curve of a selected pixel and a selected frame showing shot-noise limited response. Right are histograms of the selected pixel signal values at 20ns exposure (top) and 8µs exposure (bottom) with Poisson fit overlaid as crosses.

Parameter	Note	Value		Unit
Chip				
Resolution	Col x Row	128 x 120		
3D CMOS Technology	Top tier (BSI)	65nm (Imaging)		
	Bottom tier	40nm		
Chip Area	One independent trial	1.2 x 1.2		mm²
Pixel Pitch		7.83		µm
Fill Factor	Drawn	45		%
PRNU	Without DCR correction	<2		%
Full Well	Intensity mode	4095		photons
	Time gated mode	64 (per bin)		
Dynamic Range	Rolling shutter, 1V excess bias	80.88		dB
TAR	Rolling shutter, low light	1		
Maximum Frame Rate	Global shutter assuming 155µs exposure time	500		fps
Minimum Time Gate	93ps σ across array	1		ns
Power Consumption	Including IO and SPADs at 14V	70		mW
SPAD				
Excess bias voltage		*1*	*3*	*V*
Median DCR		<200	<11000	cps
Peak PDP (at 640nm)	Without metal reflector	10.5	23	%
	With metal reflector	12	27.5	
Jitter	443nm	149	136	ps
	773nm	221	205	
Breakdown Voltage		12		V

Table I. Sensor performance summary.