Open access • Journal Article • DOI:10.1109/LED.2008.919377

Barrier-Layer Scaling of InAlN/GaN HEMTs — Source link

Farid Medjdoub, Mohammed Alomari, J.-F. Carlin, M. Gonschorek ...+4 more authors

Institutions: University of Ulm, École Polytechnique Fédérale de Lausanne

Published on: 22 Apr 2008 - IEEE Electron Device Letters (IEEE)

Topics: Barrier layer, Gallium nitride, High-electron-mobility transistor and Electron mobility

Related papers:

- Power electronics on InAlN/(In)GaN: Prospect for a record performance
- Analysis of degradation mechanisms in lattice-matched InAlN/GaN high-electron-mobility transistors
- Can InAlN/GaN be an alternative to high power / high temperature AlGaN/GaN devices?
- Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices
- High electron mobility lattice-matched AlInN∕GaN field-effect transistor heterostructures

Share this paper:

View more about this paper here: https://typeset.io/papers/barrier-layer-scaling-of-inaln-gan-hemts-44rqdcb68q

Barrier layer scaling of InAlN/GaN HEMTs

F Medjdoub, M Alomari, J.-F Carlin, M Gonschorek, E Feltin, M Py, N Grandjean, E Kohn

► To cite this version:

F Medjdoub, M Alomari, J.-F Carlin, M Gonschorek, E Feltin, et al.. Barrier layer scaling of InAlN/GaN HEMTs. IEEE Electron Device Letters, Institute of Electrical and Electronics Engineers, 2008. hal-03281203

HAL Id: hal-03281203

https://hal.archives-ouvertes.fr/hal-03281203

Submitted on 8 Jul 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Barrier layer scaling of InAlN/GaN HEMTs

F. Medjdoub[1], M. Alomari[1], J.-F. Carlin[2], M. Gonschorek[2], E. Feltin[2], M.A. Py[2], N. Grandjean[2] and E. Kohn[1]

[1]University of Ulm, Inst. of Electron Devices and Circuits, Albert Einstein Allee 45, 89081 Ulm, Germany.

Email: farid.medjdoub@uni-ulm.de

[2]Ecole Polytechnique Fédérale de Lausanne (EPFL), CH 1015 Lausanne, Switzerland

Index terms: InAlN barrier, HEMT, GaN-based, scaling, Microwave devices

Abstract.

We discuss the characteristics of $In_{0.17}Al_{0.83}N$/GaN High Electron Mobility Transistors (HEMTs) with barrier thicknesses between 33 nm and 3 nm, grown on sapphire substrates by MOCVD. The maximum drain current (at V_G = +2.0 V) decreased with decreasing barrier thickness due to the gate forward drive limitation and residual surface depletion effect. Full pinch-off and low leakage is observed. Even with 3nm ultra thin barrier the heterostructure and contacts are thermally highly stable (up to 1000°C).

I. INTRODUCTION

Many high speed applications require devices with high power, high efficiency and high linearity at mm-wave frequencies and beyond. In this field, GaAs and InP-based HEMTs with gatelengths below 100 nm have been used employing gate recess [1-2], however limited in power by their breakdown strength. On the other hand GaN-based HEMTs with AlGaN barriers have enabled more than 1 order of magnitude higher power densities. Nevertheless, it has been difficult to extend the frequency of operation into V-band (50-75 GHz) [3] and W-band (75-111 GHz) [4] due to their difficult technology. To obtain very high frequency performance, it is necessary to shrink the gate length while maintaining the structural aspect ratio of gate length to gate to channel separation [5-6]. However in planar AlGaN/GaN devices, the channel sheet carrier density starts to decrease already at a barrier thickness of around 20 nm [7-8]. Consequently, surface depletion of the interfacial induced polarization occurs for thin barriers due to the location of the polarization dipole countercharge on the surface in a deep level (often referred as surface donor [9]). This level is approx. 1.6 eV below the conduction band edge in the case of AlGaN/GaN with 30 % Al-content. The deep surface donor level can only be removed by surface passivation like with Si-Nitride [10] and indeed 10 nm barrier thickness AlGaN/GaN MISHEMTs have been demonstrated using a 2 nm SiN dielectric [11]. Recently, 3.5 nm barrier highly strained AlN/GaN MISHEMTs have been demonstrated with an extremely high current level [12]. However, these approaches rely on the deposition of an amorphous defect free dielectric overlayer with high dielectric strength and are therefore difficult to realize. These problems have prevented the use of gate lengths smaller than 100 nm in planar devices without apparition of short channel effects. Another possibility to obtain a high HEMT aspect ratio is the use of a gate recess. However, AlGaN possesses a ceramic-like stability and cannot easily be etched with wet solutions. However, dry etching of the strained barrier layer may generate defects. In fact defects in the strained barrier layer have been found one of the main limiting factors in reliability [13]. Thus, although AlGaN/GaN recess techniques have been developed [14], planar approaches may still be more robust.

Recently, $In_{0.17}Al_{0.83}N$ has been proposed as an alternative to AlGaN barrier layers [15]. In this case a high interfacial sheet charge density of 2.8 x 10^{13} cm^{-2} has been predicted and has indeed been verified by CV and Hall measurements [16] and by the analysis of HEMT devices with output current densities above 2 A/mm [17]. Hall measurements on heterojunctions with various barrier thicknesses have indicated a constant sheet charge density down to approx. 10 nm barrier thickness and even at a barrier thickness of 5 nm a sheet charge density of 1.6 x 10^{13} cm^{-2} is observed [18]. These results have encouraged this investigation of barrier thickness scaling of InAlN/GaN HEMT structures.

II. MATERIAL GROWTH AND DEVICE FABRICATION

The heterostructures were grown by Metal Organic Chemical Vapor Deposition on sapphire substrates. The structures consisted of a 2 µm thick GaN buffer, a 1.0 nm thick AlN spacer and various $In_{0.17}Al_{0.83}N$ barrier layer thicknesses. The total barrier thicknesses (InAlN barrier and AlN spacer) have been between 33 nm and 3.0 nm. The heterostructures have been characterized by HRXRD (High Resolution X-Ray Diffraction). The 3.0 nm barrier thickness is not detectable by HRXRD, which on the other hand indicates the growth of an extremely thin InAlN film. The sheet carrier densities ($N_{S\ Hall}$) of the different layers resulting from Hall measurements are shown in Fig. 1. The HEMT structures were fabricated as follows: Mesa isolation was performed by dry etching using argon plasma. Ti/Al/Ni/Au metal stack annealed at 870°C for 30 s has been used for the ohmic contacts. The drain-source distance was 3 µm. Ni/Au Schottky gates with 0.25 µm footprint were defined by e-beam lithography and placed asymmetric between source and drain, 1 µm apart from source contact.

III. SURFACE BARRIER PROPERTIES

The Hall measurements indicate a reduction in channel sheet charge density below 10 nm barrier thickness. To understand this behaviour, a model of the InAlN surface properties has been developed, especially the location and density of surface traps. The Atlas simulation tool was used to simulate the sheet charge density as a function of the barrier thickness, not distinguishing between the 1 nm AlN spacer layer and the InAlN barrier layer to simplify modelling (no influence of the AlN smoothing layer on the sheet charge density has been observed experimentally). We have considered three cases: (1) a high (infinite) density of surface traps comparable to the case of the GaAs surface, (2) a deep donor sheet charge density located near the surface equal to the interfacial polarization dipole charge corresponding to the surface donor model of AlGaN [9] and (3) a fully ionized surface sheet charge density equal to the interfacial polarization dipole charge in combination with a discrete surface state level (donor-like traps) of identical density, located on the surface. Case (1) would result in an accessible channel sheet charge density decreasing with barrier thickness. This is not observed. Case (2) only results in the full undepleted sheet charge density for thin barriers, if the surface donor level is located within the conduction band. In this case the polarization countercharge would fully obey the semiconductor carrier distribution statistics, which is not obvious for example for adsorbed molecules. In case (3) the surface potential is only dominated by the surface state properties, where this state could be also considered as a chemical redox couple on the free surface. This third case is illustrated with Fig. 1. Fitting the surface potential (φ_s) dependence on barrier thickness with the experimental data, reveal a surface state level between 0.4 and 0.6

eV below the conduction band edge (in this case 0.6 eV). This value is considerably lower than the one discussed in [9]. In consequence planar InAlN/GaN HEMTs can be fabricated with barrier thicknesses down to the tunnelling thickness in a well controlled way and can be evaluated even before passivation.

IV. DEVICE CHARACTERISTICS

The dependence of maximum HEMT output current (I_{DSS}) on barrier thickness shown in fig. 2 follows the trend observed for the sheet charge density obtained from Hall-measurements $N_{S\ Hall}$ shown in fig. 1. However, the correlation between I_{DSS} and $N_{S\ Hall}$ for the free surface is only indirect. Underneath the gate no reduction in sheet charge density with thinner barrier is expected, if no stress is added by the gate metal. The surface potential of the free surface can only act in the source/gate and gate/drain access regions mainly as parasitic current limiter on the FET open channel current. In this first analysis the open channel current has been approximated by the saturated output current I_{DSS} obtained at V_G = + 2.0 V, and the correlation with $N_{s\ Hall}$ cannot be quantitative. At this gate bias gate leakage becomes noticeable, which is consistent with a Schottky barrier height of approx. 1.7 V as can be extracted from the extrapolation in fig. 3. In the insert (Fig. 2) the FET output characteristics are shown for the 0.25 µm gatelength FETs (w = 50 µm) with 15 nm and 3.0 nm total barrier thicknesses. For thick barriers I_{DSS} is approx. 1.8 A/mm and decreases to 0.6 A/mm for the 3.0 nm barrier. It can be seen that current compression is not seen in the thin barrier device prior to forward gate breakdown. Thus, for thin barriers I_{DSS} is gate barrier limited and not N_S limited. After passivation by PECVD Si_3N_4 at 300 °C the saturation current I_{DSS} at V_G = +2 V is increased, especially for the thin barrier devices. This may again be a consequence of a reduction or removal of the surface potential φ_s in the access regions together with a modification of the field redistribution at the point where the gate metal, the barrier layer surface and the passivation layer meet.

Scaling of the barrier thickness could not easily be controlled down to 3 nm by HRXRD and verification would be needed by TEM. However, scaling the FET pinch-off voltage as shown in Fig. 3 results in a linear relationship for all data points, confirming the growth data. After passivation, a maximum output current of 0.9 A/mm has been obtained in conjunction with pinch-off voltage of V_P = -1.0 V for the 3.0 nm barrier device. Enhancement mode of operation would be reached for a total barrier thickness of 2.0 nm.

V. THIN BARRIER THERMAL STABILITY

Even at the smallest barrier thickness the stability of the barrier layer and contact/barrier layer interfaces can tolerate high processing temperatures up to 1000 °C, promising potentially high robustness of these ultra thin barrier devices. In the stress experiment (in vacuum), the samples have been heated in intervals of 100°C and

kept at each temperature for 30 min. The temperature has been determined as described earlier [15]. At each temperature step the sample has been cooled down to Room Temperature (RT) and data were taken to evaluate permanent degradation. Temperatures above 1000°C were not possible because of Au-melting. The room temperature DC characteristics after cycling and final heating for 30 min at 1000°C are shown in Fig. 4. In spite of the extensive thermal stressing, the gate forward drive capability, the open channel current and pinch voltage are preserved. No gate sinking has occurred. Thus, the metallurgical interface properties and the properties of the InAlN/AlN barrier layer stack have not been degraded and ohmic as well as Schottky contacts have also not suffered. Thus, stable interface compounds have been formed. Their analysis will have to be subject of an additional materials oriented investigation. As shown in fig. 4, the reverse Schottky barrier leakage after temperature stress is almost identical to the virgin one. In contrast, Ni/Au Schottky barrier contact on $Al_{0.3}Ga_{0.7}N$/GaN devices with 25 nm barrier thickness show ohmic behaviour after such a temperature stress experiment.

VI. CONCLUSION

Barrier layer scaling of InAlN/GaN HEMTs has been studied for the first time down to 3 nm. The results indicate that InAlN/GaN HEMT device structures can be reliably designed and fabricated with barrier layer thicknesses approaching the tunnelling thickness and approaching enhancement mode characteristics. The thermal stability of 3 nm barrier thickness InAlN/GaN devices has been also evaluated up to 1000°C. No degradation of the InAlN/GaN interface towards the GaN buffer and the surface metals occurred at such high temperatures, which is promising for highly reliable ultra short, ultra high frequency GaN-based devices. Semi-enhancement mode of operation (V_P = -1.0 V) with 0.9 A/mm has been obtained. Improving the gate breakdown characteristics further, would enable enhancement mode of operation with channel current densities well above those, which can be obtained by the conventional AlGaN/GaN counterparts.

ACKNOWLEDGMENT

This work was carried out in the frame of the European project UltraGaN (contract 6903). Thus, sincere thanks go to all members of this consortium for many stimulating, fruitful and helpful discussions. The growth material of this work is supported by the Swiss National Science Foundation. The authors would like to acknowledge Mr. Y. Men for e-beam processing.

References

[1] D. C. Streit, K. L. Tan, R. M. Dia, A. C. Han, P. H. Liu, H. C. Yen and P. D. Chow, "High performance W-band InAlAs-InGaAs-InP HEMT," *Electronic Lett.*, vol 27, pp. 1149-1150, 1991

[2] F. Medjdoub, M. Zaknoune, X. Wallart, C. Gaquière, F. Dessenne, J.L. Thobel and D. Theron, "InP HEMT downscaling for power applications at W band," *IEEE Trans. Electron Devices*, vol. 10, pp. 2136-2143, 2005

[3] R. Quay, A. Tessmann, R. Kiefer, R. Weber, E. van Raay, M. Kuri, M. Riessle, H. Massler, S. Muller, M. Schlechtweg, and G. Weimann, "AlGaN/GaN HEMTs on SiC: towards power operation at V-band," in *Proc. IEDM Tech. Dig,* Washington, DC, 2003, pp. 567–570

[4] M. Micovic, P. Kurdoghlian, P. Hashimoto, M. Hu, M. Antcliffe, P. J. Willadsen, W. S. Wong, R. Bowen, M. Wetzel, and D. H. Chow, "GaN HFET for W-band power applications," in *Proc IEDM Tech. Dig.*, San Francisco, CA, 2006, pp.425-427

[5] Y. Awano, M. Kosugi, K. Kosemura, T. Mimura, M. Abe, "Short-channel effects in subquarter-micrometer-gate HEMTs: simulation and experiment," *IEEE Trans. Electron Devices,* vol. 36, pp. 2260-2266, 1989

[6] G. H. Jessen, R. C. Fitch, J. K. Gillespie, G. Via, A. Crespo, D. Langley, D. J. Denninghoff, M. Trejo, and E. R. Heller, "Short-Channel Effect Limitations on High-Frequency Operation of AlGaN/GaN HEMTs for T-Gate Devices," *IEEE Trans. Electron Devices, vol.* 54, pp. 2589-2597, 2007

[7] V. Tilak, B. Green, V. Kaper, H. Kim, T. Prunty, J. Smart, J. Shealy, and L. Eastman, "Influence of Barrier Thickness on the High-Power Performance of AlGaN/GaN HEMTs," *IEEE Electron Device Lett.,* vol. 22, pp. 580-582, 2001

[8] M. Higashiwaki and T. Matsui, "Barrier Thickness Dependence of Electrical Properties and DC Device Characteristics of AlGaN/GaN Heterostructure Field-Effect Transistors Grown by Plasma-Assisted Molecular-Beam Epitaxy," *Jap. J. Appl. Phys.,* Vol. 43, pp. L1147-L1149, 2004

[9] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBars, J. S. Speck, and U. K.Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Appl. Phys. Lett.* Vol. 77, pp. 250-252, 2000

[10] K. Hyungtak, R.M. Thompson, V. Tilak, T.R. Prunty, J.R. Shealy, L.F. Eastman, "Effects of SiN passivation and high-electric field on AlGaN-GaN HFET degradation," *IEEE Electron Device Lett.,* Vol. 24, pp. 421-423, 2003

[11] M. Higashiwaki, T. Matsui, T. Mimura, "AlGaN/GaN MIS-HFETs with f_T of 163 GHz using cat-CVD SiN gate-insulating and passivation Layers," *IEEE Electron Device Lett*., Vol. 27, pp. 16-18, 2006

[12] Y. Cao, T. Zimmermann, D. Deen, J. Simon, J. Bean, N. Su, J. Zhang, P. Fay, H. Xing, D. Jena, "Ultrathin MBE-Grown AlN/GaN HEMTs with record high current densities," in *Proc. Int. Semicond. Device Research Symp.,* Maryland, MD, 2007

[13] J. Joh and J. del Alamo. "Mechanism for electrical degradation of GaN High Electron Mobility Transistor," in Proc. *IEEE IEDM Tech. Digest*., p. 415, 2006

[14] A. Chini, D. Buttari, R. Coffie; L. Shen, S. Heikman, A. Chakraborty; S. Keller; U.K. Mishra, "Power and linearity characteristics of field-plated recessed-gate AlGaN-GaN HEMTs," *IEEE Electron Device Lett.,* Vol. 25, pp. 229-231, 2004

[15] J. Kuzmik, "Power Electronics on InAlN/(In)GaN: Prospect for a Record Performance," *IEEE Electron Device Lett*., Vol. 22, pp. 510-512, 2001

[16] M. Gonschorek, J.-F. Carlin, E. Feltin, M. A. Py, and N. Grandjean, "High electron mobility lattice matched AlInN/GaN field-effect transistor heterostructures," *Appl. Phys. Lett.* Vol. 89, 062106, 2006

[17] F. Medjdoub, J.-F. Carlin, M. Gonschorek, E. Feltin, M.A. Py, D. Ducatteau, C. Gaquière, N. Grandjean and E. Kohn, "Can InAlN/GaN be an alternative to high power / high temperature AlGaN/GaN devices?," in *Proc. IEDM Tech. Dig*, San Francisco, CA, 2006, pp. 927-930

[18] F. Medjdoub, J.-F. Carlin, M. Gonschorek, E. Feltin, M.A. Py, M. Knez, D. Troadec, C. Gaquière, A. Chuvilin, U. Kaiser, N. Grandjean and E. Kohn, "Barrier layer downscaling of InAlN/GaN HEMTs," in *Proc*. *IEEE DRC Conf. Dig.,* South Bend, IN, 2007 pp. 109-111

Figure captions

Figure 1: Simulated $N_{S\ Hall}$ data as a function of the $In_{0.17}Al_{0.83}N$/GaN HEMT barrier thickness. The experimental results are indicated by the squares. Corresponding electron mobility are approx. 1000 cm^2/Vs down to 9 nm barrier thickness and 600 cm^2/Vs for the 6 nm and 3 nm barrier thicknesses.

Figure 2: DC maximum output current density (I_{DSS}) at V_G = + 2V as function of barrier thicknesses of $In_{0.17}Al_{0.83}N$/GaN HEMTs at room temperature. The inserts show the DC output characteristics of a 15 nm (V_{GS} swept from +2 V to -10 V by step of 2 V) and 3.0 nm barrier thickness (V_{GS} swept from +2 V to -1 V by step of 1 V) 0.25×50 μm^2 $In_{0.17}Al_{0.83}N$/GaN HEMT.

Figure 3: Pinch-off voltage dependence on barrier thicknesses of $In_{0.17}Al_{0.83}N$/GaN HEMTs.

Figure 4: DC output characteristics of a 3.0 nm $In_{0.17}Al_{0.83}N$/GaN HEMT after 30 min 1000°C thermal stress. The corresponding R.T. characteristics are shown in the insert of fig. 2. V_{GS} swept from +2 V to -1 V by step of 1 V. The insert shows the Schottky diode characteristics at R.T. and after 30 min 1000°C thermal stress.

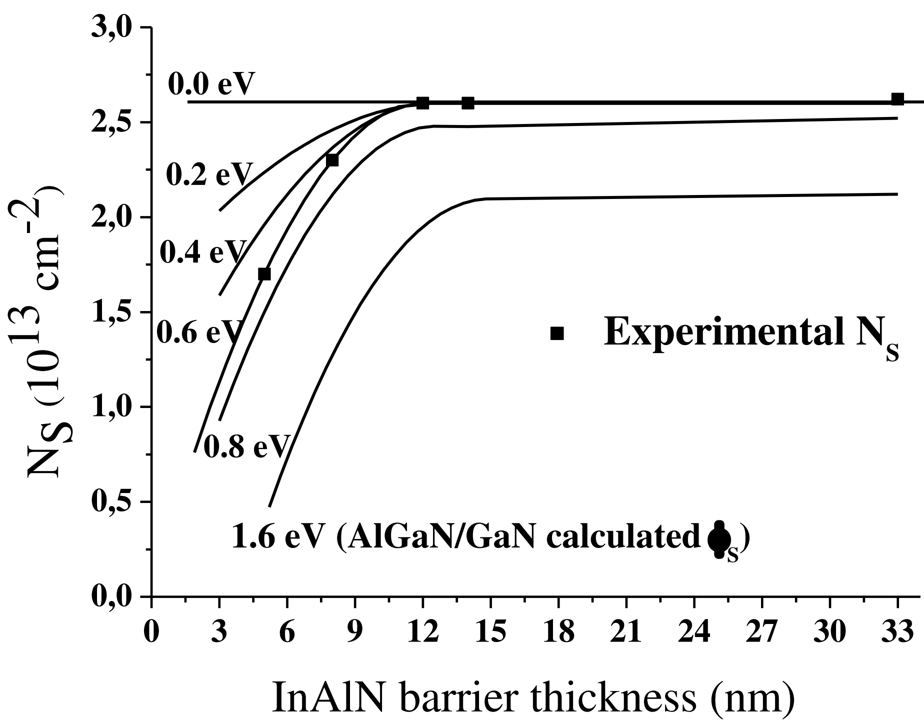

Fig. 1 : F. Medjdoub et al.

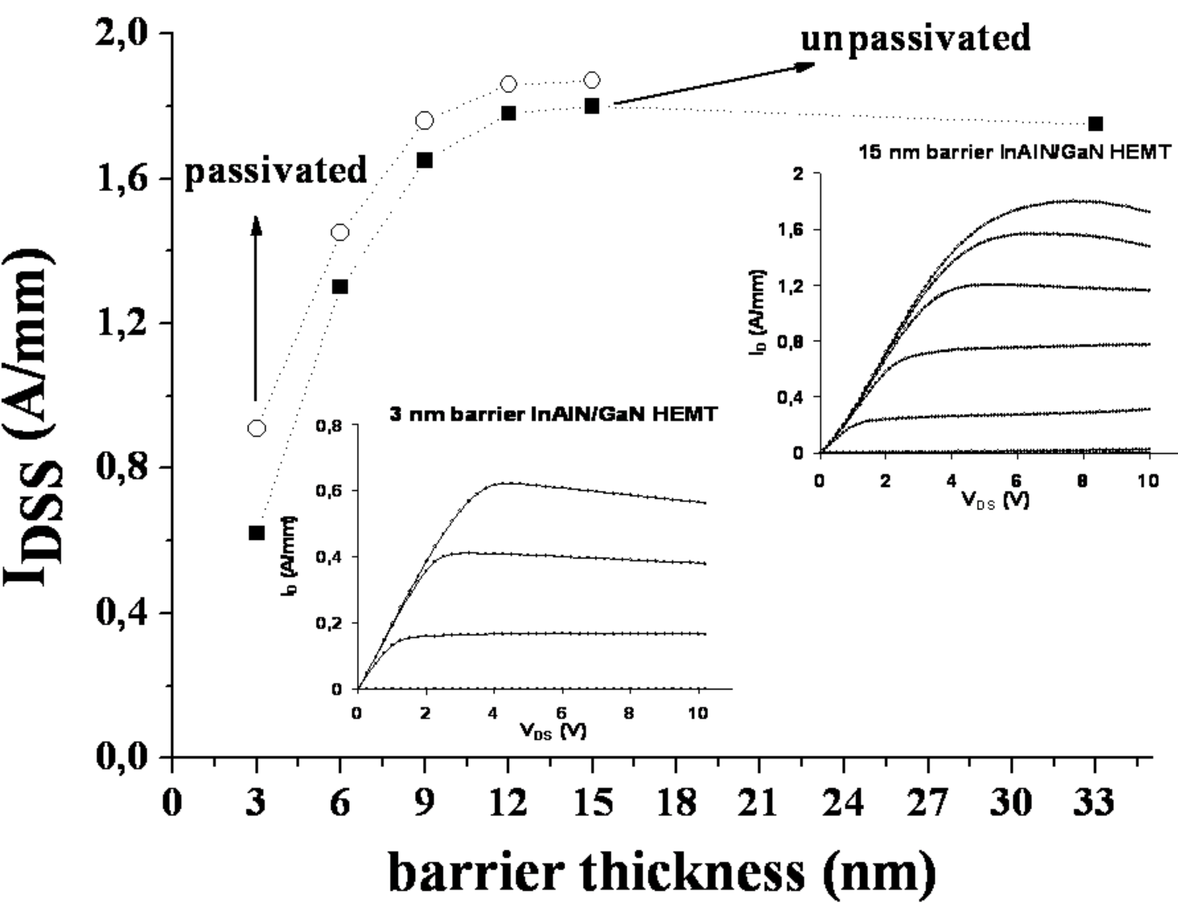

Fig. 2 : F. Medjdoub et al.

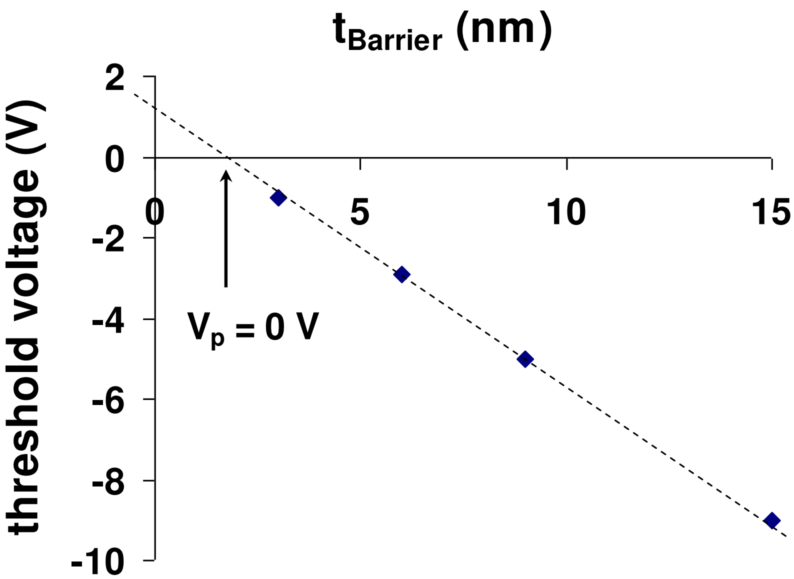

Fig. 3 : F. Medjdoub et al.

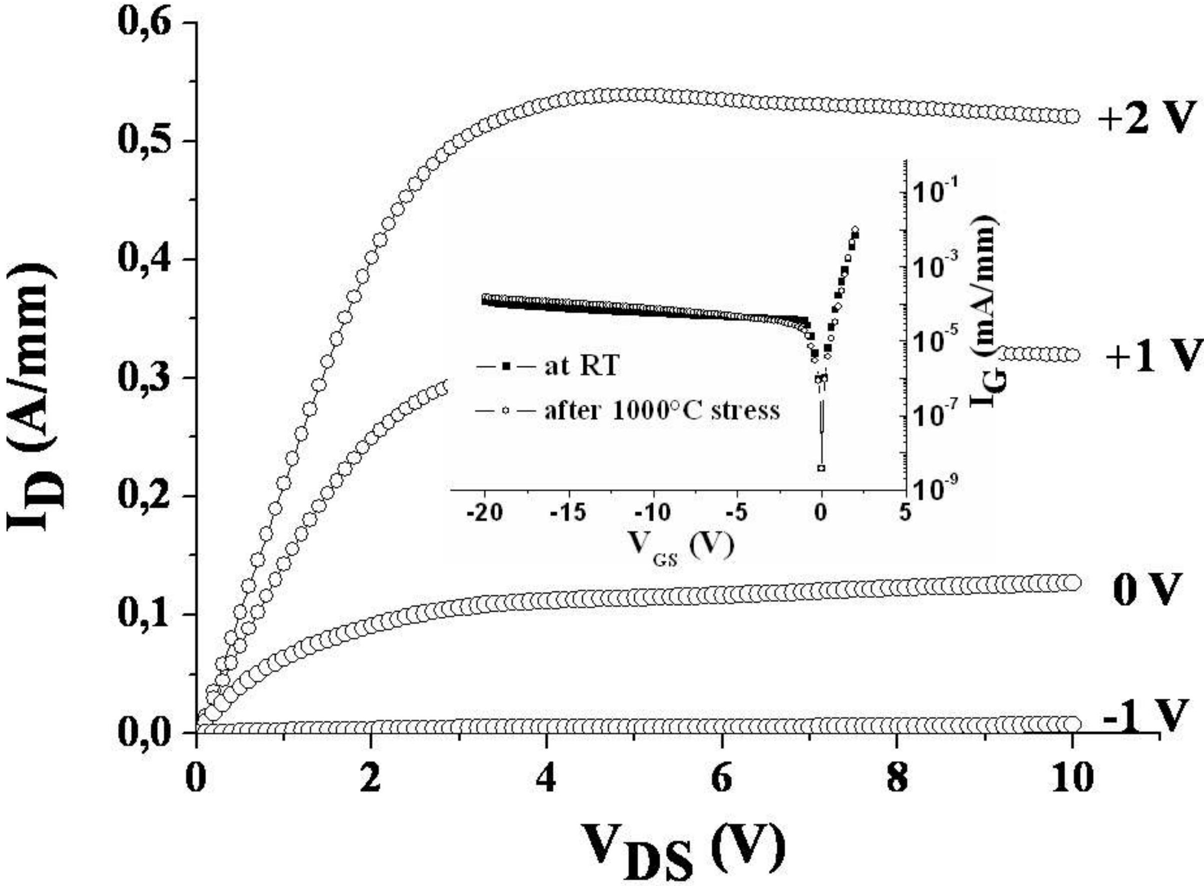

Fig. 4 : F. Medjdoub et al.