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Basic Analog and Digital Circuits with a-IGZO TFTs

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***Abstract*—This paper presents the characterization of fundamental analog and digital circuits with a-IGZO TFTs from measurements performed at normal ambient. The fundamental blocks considered in this work include digital logic gates, a low-power single stage high-gain amplifier with capcacitive bootstrapping and a level shifter/buffer. These circuits are important functional blocks in analog/Mixed signal IC design with oxide TFTs. Being fabricated at low temperature ($< 200\,^{\circ}$C), they can find potential applications in low-cost large-area flexible systems.**

***Index Terms*—Low-power circuits, high-gain amplifier, a-IGZO TFT.**

I. Introduction

Transparent conductive oxides (TCO), especially amorphous indium gallium zinc oxide (a-IGZO), as a semiconductor in thin-film-transistors (TFTs), is gaining considerable attention, because of its higher mobility compared to a-Si:H and organic TFTs and low-temperature fabrication [1], [2]. Though a-IGZO TFT technology is mainly meant for displays [3], its applications are extending to other low-cost large-area systems including wearable technology and RFIDs [4]. Consequently, analog/mixed signal design with this technology is gaining significant interest.

In spite of several advantages it offers, the technology imposes few limitations on circuit design, mainly due to:

- Lack of reliable complementary (p-type) transistor: Forming p-type oxide semiconductors [5], [6] is showing to be very difficult to accomplish, and those reported present a very poor hole-mobility [7]. Copper and tin based semiconductor oxides are gaining supporters as a possible basis for p-type oxide material [8]. However, p-type devices with good electrical characteristics, closer to the n-type have not yet been reported .
- Device electrical mobility is orders of magnitude lower when compared to the crystalline silicon.

Nevertheless, some work has already been reported towards basic digital circuit design, such as the transparent two-input logic gates operating up to 5 kHz and fabricated at high temperature (600 °C) [9]. However, this work presents the characterization of logic gates with frequency of operation that goes up to 10 kHz and fabricated at low temperature ($< 200\,^{\circ}$C). An operational amplifier reported in [10] has 16 TFTs to accomplish a gain of 18.7 dB with a power consumption of 0.9 mW. This paper presents a single-stage bootstrap amplifier based on a topology with three TFTs and a capacitor. It is showing a similar gain (18.6 dB) but much lower power consumption (0.3 mW). Consequently this circuit could find potential applications in wearable technologies or in battery assisted systems, where low power consumption is required. In addition to these circuits a level shifter is also characterized, which can also function as a buffer. This circuit is formed with four transistors. It can act not only as a driving circuit but also to lower the DC level of the signal by a significant amount, if needed. Note that all the circuits reported in this paper are confined to n-type TFTs.

II. Circuit Design and Fabrication

Logic Gates

An inverter, two-input NAND and NOR gates circuit schematics are shown in Fig. 1. The NAND gate is formed by a series connection of two driving transistors (width: 480 μm) with a diode connected load (width: 40 μm). On the other hand, a NOR gate is designed with a parallel connection of two driving transistors and a diode connected load. A NAND gate and a single TFT micrograph with wire-bonding are presented in Fig. 2. For an inverter, when the input is low, T1 turns 'off'

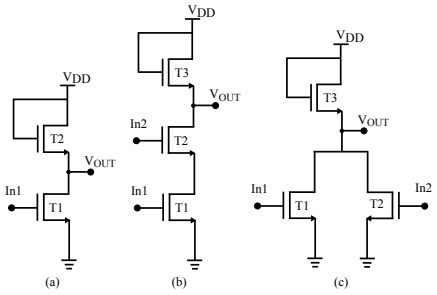

Fig. 1. Logic gate schematics (a) Inverter (b) Two-input NAND (c) Two-input NOR.

and no current flows in the circuit, resulting in a high output state, close to V_{DD} - V_{TH}. On the other hand, when the input is high T1 turns 'on' and causes a current flow that leads to a voltage drop on the diode connected transistor (T2). The output will be low, but not exactly zero due to the voltage drops on

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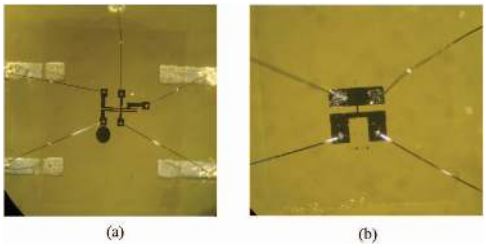

Fig. 2. (a) Two input NAND gate (b) An isolated TFT with wire-bonding

the conducting transistors. For the NAND gate, when any of the inputs is low at least one of the transistors will be 'off' and no current flows in the circuit. The output becomes high, otherwise the output becomes low but not exactly to ground for the same reasons of the inverter. A similar reasoning can be applied to the NOR gate.

Capacitive bootstrap amplifier (Amplifier1)

A high-gain topology only with n-type enhancement transistors is shown in Fig. 3a, where A_f is the feedback factor. Its small signal equivalent is shown in Fig. 3b. When A_f is one, signal levels at gate and source of T2 become equal.

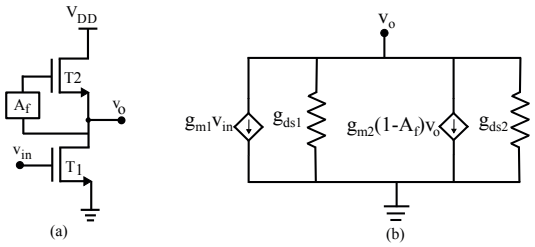

Fig. 3. High-gain amplifier topology employing positive feedback, only with n-type transistors (a) Schematic (b) Small signal equivalent

By applying KCL at v_o in Fig. 3b,

$$A = \frac{v_o}{v_{in}} = \frac{-g_{m1}}{(1-A_f)g_{m2} + g_{ds2} + g_{ds1}} \quad (1)$$

$$A = -g_{m1}(R_L//r_{ds1}) \quad (2)$$

where,

$$R_L = \frac{1}{(1-A_f)g_{m2} + g_{ds2}} \quad (3)$$

By making A_f close to unity, the effective active load resistance sets to $R_L \approx \frac{1}{g_{ds2}} = r_{ds2}$, this results in

$$A \approx -g_{m1}(r_{ds1}//r_{ds2}) \quad (4)$$

In order to guarantee a stable behavior, A_f must always be kept below unity. Based on the topology shown in Fig. 3a, a high-gain amplifier circuit schematic is presented in Fig. 4a. This circuit is referred to as Amplifier1 from here on. In this circuit, the active load (R_L) is formed by T2, T3 and C. Transistor T3 is in cutoff, hence, its effective off resistance is significantly high. Due to the transistor intrinsic capacitance, T3 can be viewed as a parallel combination of a resistor and capacitor

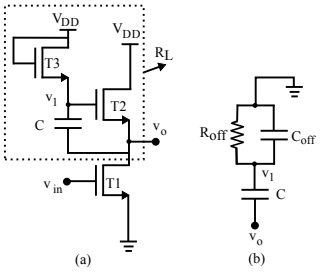

Fig. 4. (a) High gain amplifier with capacitive bootstrapping (Amplifier1) (b) Feedback path (C and T3)

as shown in Fig. 4b. On the other hand, T1 and T2 are in saturation. For high frequency signals, capacitor (C) acts as a short-circuit so the feedback factor (A_f) is supposed to be unity. However, A_f depends on the aspect ratio of the transistor T3 (C_{off} is a function of the transistor aspect ratio due to the considerable overlap areas between the gate and source/drain) and C. From Fig. 4,

$$v_1 = A_f v_0 \quad (5)$$
$$= v_0 \frac{1}{1 + \frac{1}{sC}(\frac{1}{R_{off}} + sC_{off})}$$

since R_{off} is very high, it can be simplified as

$$A_f = \frac{v_1}{v_0} = \frac{1}{1 + \frac{C_{off}}{C}} \quad (6)$$

From (6), making $C >> C_{off}$, A_f can be made close to one to promise high gain. Consequently, transistor T3 should be made small. The fabricated circuit micrograph with wire-bonding is shown in Fig. 5. Because of the positive feedback path (Fig. 4b), a high-pass filter action can be noticed, though the lower cutoff frequency is very small. In this circuit, T1 and T2 widths are 160 μm and T3 width is 40 μm. A channel length of 20 μm is used for all the TFTs, which is a reasonable value comparing to the total gate to source and drain overlap of 10 μm.

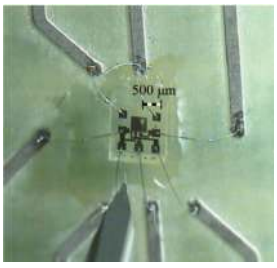

Fig. 5. Capacitive bootstrap amplifier micrograph with wire-bonding

Level Shifter:

The circuit is realized with four transistors. Its schematic and respective micrograph are shown in Fig. 6. Diode connected transistors (T2 and T3) are used to lower the DC level of the input signal, which is controlled by the bias voltage

(V_B) applied at the gate of T1. With all transistors having the same dimensions (width = 80 μm and length = 20 μm) and biased in saturation region, then:

$$v_{OUT} \approx K.v_{IN} - 3V_B \tag{7}$$

Since this circuit is fabricated on glass, which is a good insulator, body-effect is negligible unlike conventional CMOS devices, hence "K $\approx$ 1" can be achieved.

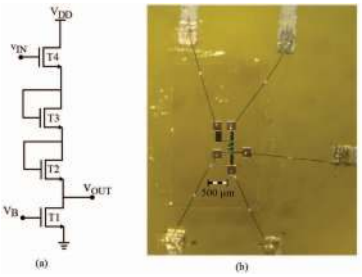

Fig. 6. Level shifter (a) schematic (b) Fabricated circuit with wire-bonding with Mo as source/drain metal

Fabrication

Fabrication process of circuits and transistors in this work follow the same method as [12] with fabrication temperature $< 200\,^{\circ}$C, where the a-IGZO layer is deposited with RF magnetron sputtering. Though transparent devices can be achieved with TCO (e.g. IZO) source/drain electrodes, Mo is employed in this work, as it facilitates wire-bonding for easier circuit testing.

III. Results and Discussion

All circuits were simulated with an in-house model developed from the device measurements [12]. Meyer model was adopted for the bias dependent capacitance. Circuit simulations were carried out in the Cadence Virtuoso Analog Design Environment. In-house technology libraries were used to support the custom IC design flow. Circuits measurements took place at room temperature. Logic gates and Amplifier1 were characterized with the help of a buffer, which is formed by an external IC showing an equivalent load capacitance of 4 pF. On the other hand, the level shifter circuit is directly tested with an oscilloscope in order to determine the circuits driving ability.

Logic gates

Inverter voltage transfer characteristics (VTC) is shown in Fig. 7a, when the input ('In1') is swept between 0 to 5 V in steps of 0.25 V for two different power supply voltages (V_{DD}) of 5 and 10 V. It can be noticed that almost full swing (high level $\approx$ V_{DD} and low level $\approx$ 0.15 V) results at the output. NAND and NOR gates VTCs are also presented in Fig. 7b and 7c with a V_{DD} of 5 V, when 'In2' is low and high, by sweeping 'In1', similar to the inverter.

Logic gates (inverter, NAND and NOR) dynamical behavior at V_{DD} = 5 V is also characterized. Their responses for an

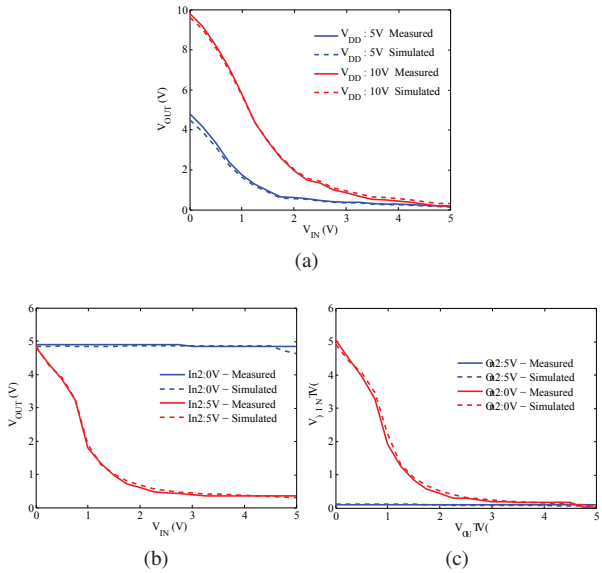

Fig. 7. Logic gates VTC: (a) Inverter: $\left(\frac{W}{L}\right)_{T2} = \frac{40\,\mu m}{20\,\mu m}$, $\left(\frac{W}{L}\right)_{T1} = \frac{480\,\mu m}{20\,\mu m}$ and V_{DD} 5 V and 10 V (b) NAND (c) NOR, where $\left(\frac{W}{L}\right)_{T3} = \frac{40\,\mu m}{20\,\mu m}$, $\left(\frac{W}{L}\right)_{T2} = \left(\frac{W}{L}\right)_{T1} = \frac{480\,\mu m}{20\,\mu m}$ and V_{DD} 5 V, for both the logic gates.

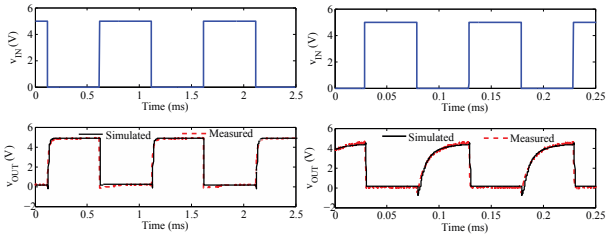

Fig. 8. Inverter response, when the input signal frequency is (a) 1 kHz (b) 10 kHz.

input signal with different frequencies of 1 kHz and 10 kHz are presented in Fig. 8, 9 and 10. At transitions of the input signals, small spikes in the output waveforms can be noticed, mainly at high frequency (10 kHz) due to the charge injection from the transistor capacitance that couple the input to the output. Both load and transistor capacitance are responsible for the charging and discharge effect in the output signals. It can also be observed that the output signal rise time is much

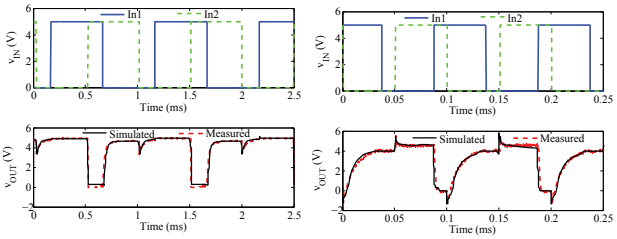

Fig. 9. NAND response, when the input signal frequency is (a) 1 kHz (c) 10 kHz.

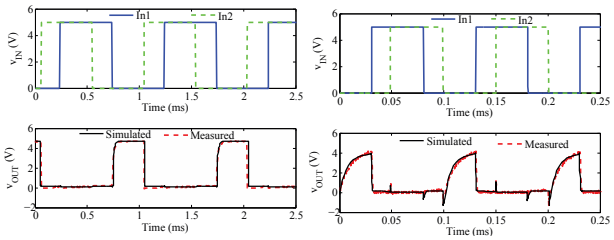

Fig. 10. NOR response, when the input signal frequency is (a) 1 kHz (c) 10 kHz.

higher than the fall time. This is because the load capacitor charges through a small load transistor and discharges through a wider driver transistor(s).

Amplifier1: Frequency response of Amplifier1 is shown in Fig. 11 for a load of 4 pF with a V_{DD} of 6 V. With an on-chip capacitance (C) of 47 pF, the circuit measurements result in a bandwidth of 20 kHz, a gain of 18.6 dB and a power consumption of 345 μW.

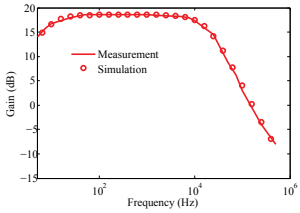

Fig. 11. Amplifier1 response from simulation and measurements

Level shifter: Circuit response is shown in Fig. 12a, for an input defined as 9.5 + 0.5sin(ωt) and $V_B = 2$ V from simulations (transient analysis) and measurements. Fig. 12b shows the frequency response of the circuit, when it drives a load of (10 MΩ//16 pF). Resulted gain is $\approx$ 1, as expected and also the functional verification from (7) can be noticed in Fig. 12a. 3 dB bandwidth is $\approx$ 80 kHz and power consumption is 24 μW. Performance metrics of the reported circuits (Amplifier1 and Level shifter) are compared with literature in Table. I.

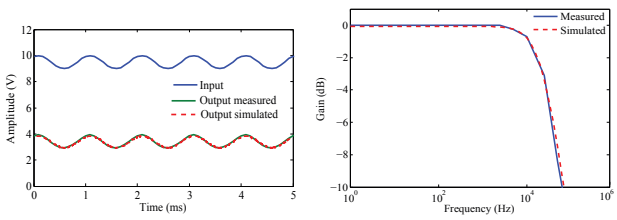

Fig. 12. Level shifter response from simulations and measurements (a) Transient response (b) Frequency response

IV. Conclusions

This paper presented the characterization of basic analog and digital circuits both from simulations and measurements. Circuit simulations are in very good agreement with the measured response. As these circuits were fabricated at low temperature they would find potential applications in large-area wearable electronics.

TABLE I
Performance comparison

Circuit	No. of TFTs	Power (mW)	Bandwidth (KHz)	Gain (dB)	Load
Source follower	4	0.024	80	0	10 MΩ//16 pF
Amplifier1	3	0.345	20	18.6	4 pF
[10]	16	0.9	54	18.7	1 MΩ//2 pF

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