Basic Concepts of Power Distribution Network Design for High-Speed Transmission

F. Carrió*, V. González and E. Sanchis

Department of Electronic Engineering, University of Valencia, Spain

Abstract: This paper tries to gather the Power Distribution Network (PDN) techniques used to preserve power integrity in PCB designs when transmitting data rates over 6 Gbps using the newest commercial optical modules.

The PDN design described allows for proper impedance control of the power supply with the appropriate choice of the number, location and values of capacitors. This method needs the knowledge of the electrical RLC model of the regulators, copper planes, capacitors and vias used in the PCB.

A particular case of PDN design will be presented for a module using one SNAP12 optical transmitter and one receiver connected to an Altera Stratix II GX FPGA. This board is designed to work with data rates up to 75 Gbps for a high-energy physics application.

Keywords: Power integrity, signal integrity, power distribution system, power distribution network, decoupling capacitors, power supply noise, high-speed design, multigigabit.

1. INTRODUCTION

In the last years the need to increase data rates of electronic systems has produced the development of optical devices for high-speed communications. Nowadays, high-speed optical modules have become indispensable devices for communication system designs. High speed optical modules transduce light in electrical signals via Vertical Cavity Surface Emitting Laser (VCSEL) arrays for drivers and PIN photodiode arrays for receivers, both of them using a nominal wavelength of 850 nanometers. This optical technology implies electrical signal rise times of about few tens of picoseconds. These short rise times involve fast electrical current transients that degrade signal integrity and produce new problems related with power integrity in Printed Circuit Boards (PCBs).

We have to strongly consider that the interconnection between power supply and the device (i.e. a processor) acts as an inductance in series with a resistance. So when fast current transients are present in power connections, power supply cannot hold constant voltage in the entire power connection and voltage fluctuations appear on it.

These fluctuations cause malfunction of devices and even can decrease their lifetime [1]. Equation 1 determines roughly the voltage fluctuation value due to interconnection:

$$V_{drop} = R \cdot I + L \cdot \frac{dI}{dt} \quad (1)$$

It is necessary to have a proper PDN design to maintain voltage fluctuations inside noise boundaries where devices work without problems.

*Address correspondence to this author at the Campus Burjassot – Paterna, Avenida de la Universitat s/n - 46100 Burjassot (Valencia), Spain;
Tel: +34 96354039; Fax: +34 9635 44353;
E-mail: fernando.carrio@uv.es

Power connection behaves as an inductor in series with a resistor, and it can be defined with the lumped element model shown in Fig. (**1**):

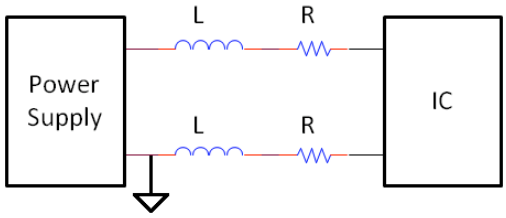

Fig. (1). Interconnections between power supply and device.

Fig. (**2**) shows the impedance profile of a typical power connection:

As we can see in Fig. (**2**) the impedance increases with frequency due to power connection reactance. It causes that voltage fluctuations appear in power supply distribution when devices switch their input and outputs and fast current transients occur.

2. POWER DISTRIBUTION NETWORK DESIGN

There are two essential parameters for PDN design: f_{knee} and Z_{target}.

2.1. Knee Frequency (f_{knee})

The bandwidth of signals used to transmit information is a basic parameter for PDN design. The bandwidth is a term used to quantify the highest frequency component of importance in our electronic system. So, it provides the maximum frequency which is important to not distort in order to keep an adequate signal waveform in time domain. Equation 2 gives the relationship between the signal rise time and the bandwidth [2]:

1874-3285/11

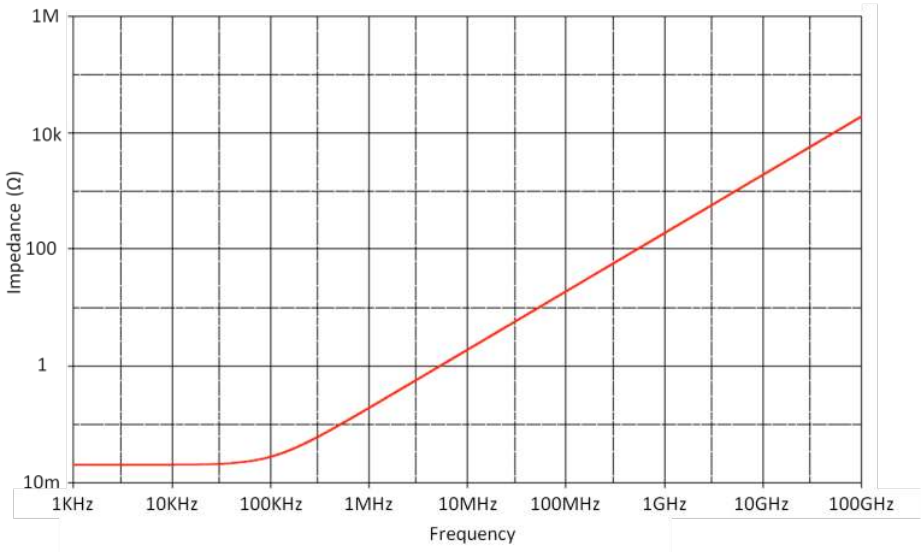

Fig. (2). Impedance profile of interconnections shown in Fig. (**1**).

$$BW = \frac{0.35}{T_r} \quad (2)$$

where T_r indicates the rise time of a square wave and BW the bandwidth of the square wave.

Fig. (**3**) shows the Fourier Transform of a pulse train with rise time T_r:

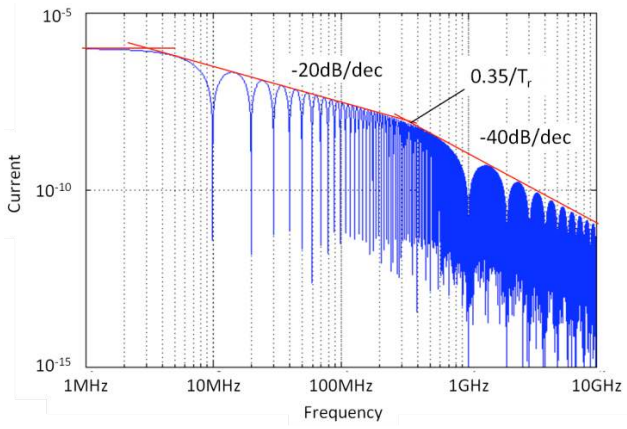

Fig. (3). Spectrum of a pulse train.

As it can be seen, most of frequency components which determine the waveform in time domain are included in the range between 0 Hz and $0.35/T_r$ Hz. The frequency corresponding to $0.35/T_r$ is known as the knee frequency (f_{knee}).

2.2. Target Impedance (Z_{target})

Z_{target} has dimensions of impedance and represents the maximum impedance value that power pins of a device must see from the power supply (Z_{board}). To avoid distorting important frequency components, Z_{board} profile must not overpass Z_{target}, maintaining voltage fluctuations inside the allowable noise margin.

Z_{target} relates the maximum voltage fluctuation allowed to the dynamic current consumed by the device. It is determined by the following equation [3, 4]:

$$Z_{target} = \frac{V_{dd} \cdot \Delta V(\%)}{0.5 \cdot I_{max}} \quad (3)$$

where:

V_{dd} is the power supply voltage

$\Delta V(\%)$ is the maximum V_{dd} tolerance allowed

I_{max} is the maximum current consumed by the device. We assume that dynamic current is a 50% of I_{max}.

Therefore, the goal of the PDN design is to maintain the impedance profile of power interconnections, Z_{board}, below Z_{target} from 0 Hz up to f_{knee} as it is indicated in the Fig. (**4**). In this way, we will be able to meet manufacturer specifications about voltage noise.

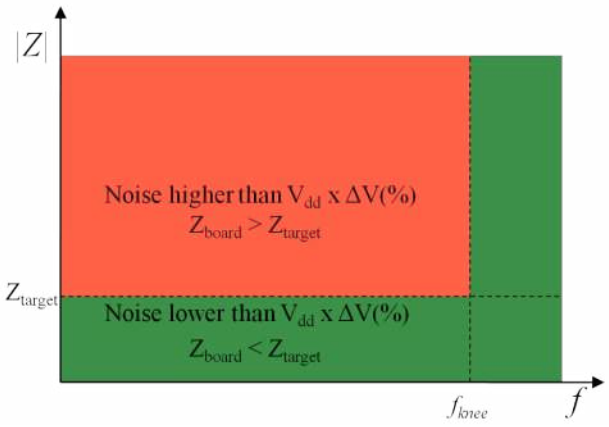

Fig. (4). The green zone represents where Z_{board} must keep in.

3. PDN DESIGN ELEMENTS

We need to obtain all lumped circuit models of the PDN components to design it. The main components we have to consider in a PDN are:

- Voltage Regulator Modules (VRMs)
- Capacitors

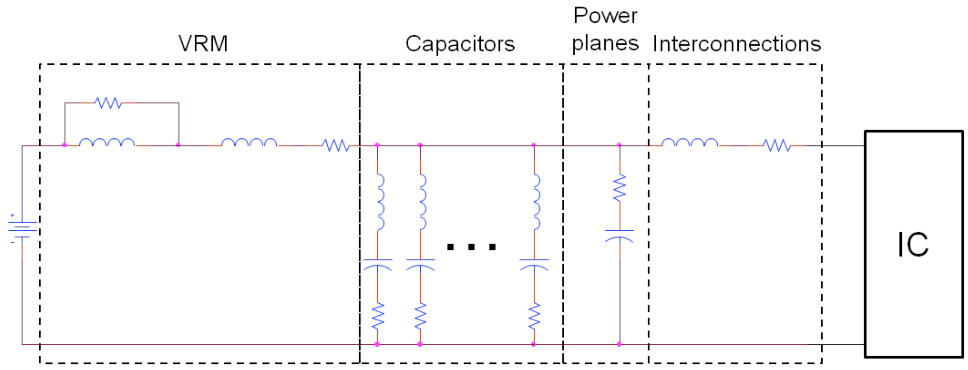

Fig. (5). Lumped circuit model of a PDN.

- Power plane capacitance
- Interconnection inductance

All of them are schematically represented in Fig. (**5**).

3.1. Voltage Regulator Modules (VRMs)

VRMs are devices that convert one voltage level to another. They can provide a low Z_{board} between 0 Hz and several hundred of kHz.

Although VRM is a nonlinear element its behavior can be defined by the next model made of four lumped elements [3]:

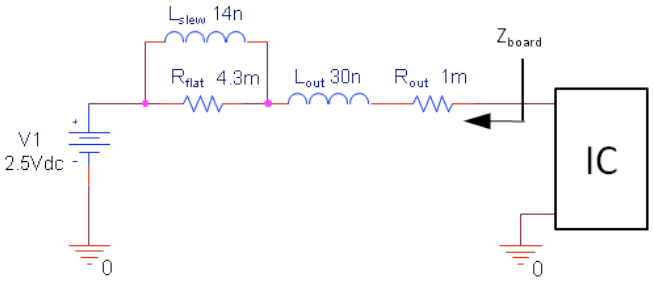

Fig. (6). Lumped circuit model of a VRM.

where:

R_{out} is the value of the resistor between the VRM output and the device and is usually around few mΩ.

L_{out} is the value of the inductance between the VRM output and the device. This value depends on the quality of the interconnection: thin traces present a higher inductance than direct connections to power planes.

R_{flat} is the Equivalent Series Resistance (ESR) of the bulk capacitor associated with the VRM output and can be obtained from the capacitor datasheet.

L_{slew} determines the total amount of time that VRM needs to ramp up the transient current. It can be calculated by the following equation:

$$L_{slew} = V_{drop} \cdot \frac{dt}{dI} \quad (4)$$

where V_{drop}, dt and dI can be obtained from the manufacturer datasheet. V_{drop} is the amount of voltage that drops when VRM gives a current of dI in a time of dt.

Fig. (**7**) shows the impedance profile of the VRM model from Fig. (**6**):

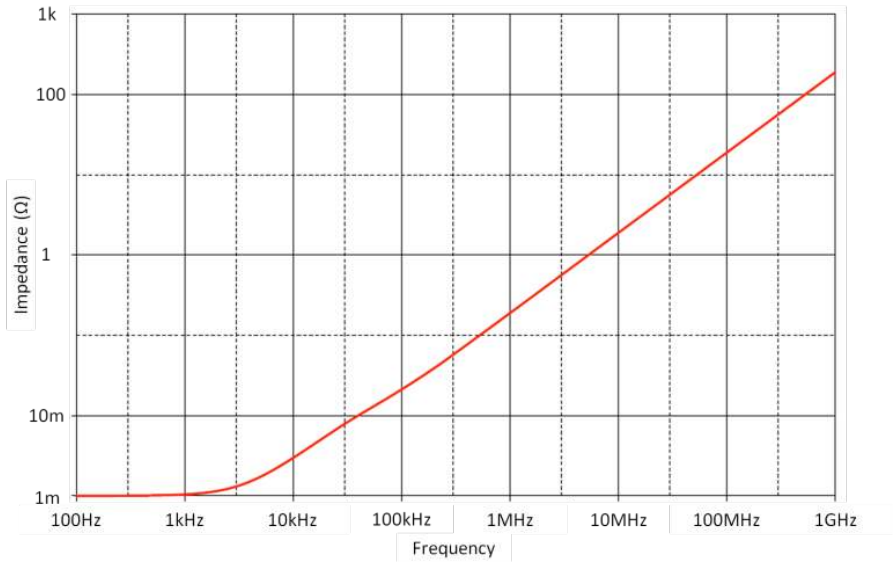

Fig. (7). Impedance profile of VRM model from Fig. (**6**).

3.2. Capacitors

Capacitors provide the current needed at those frequencies where VRM can't do it. Capacitors are used to keep Z_{board} below Z_{target} from the first hundreds of kHz up to the first hundreds of MHz.

It is important to know their impedance profile because their behavior isn't ideal. Fig. (**8**) shows the lumped circuit model of a capacitor:

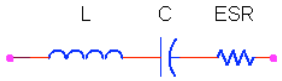

Fig. (8). Lumped circuit model of a capacitor.

where:

L is the inductance value which depends on the capacitor Equivalent Series Inductance (ESL) and the mounting inductance (L_{mount}).

C is the capacitance value.

ESR is the capacitor Equivalent Series Resistance which depends on capacitor geometry.

Thus, the capacitor impedance profile in the frequency domain depends on its ESR, L and capacitance. Fig. (**9**) shows an example of the impedance profile of a capacitor:

The resonance frequency f_o of a capacitor can be determined by the following equation:

$$f_o = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (5)$$

Two kinds of capacitors are used in PDN design: bulk capacitors and *MultiLayer Chip Capacitor* (MLCC). Bulk capacitors are used at lower frequencies than MLCC capacitors. They provide low impedance at those frequencies where VRM and MLCC capacitors cannot; between a few hundred of kHz and a few MHz. Bulk capacitors have high

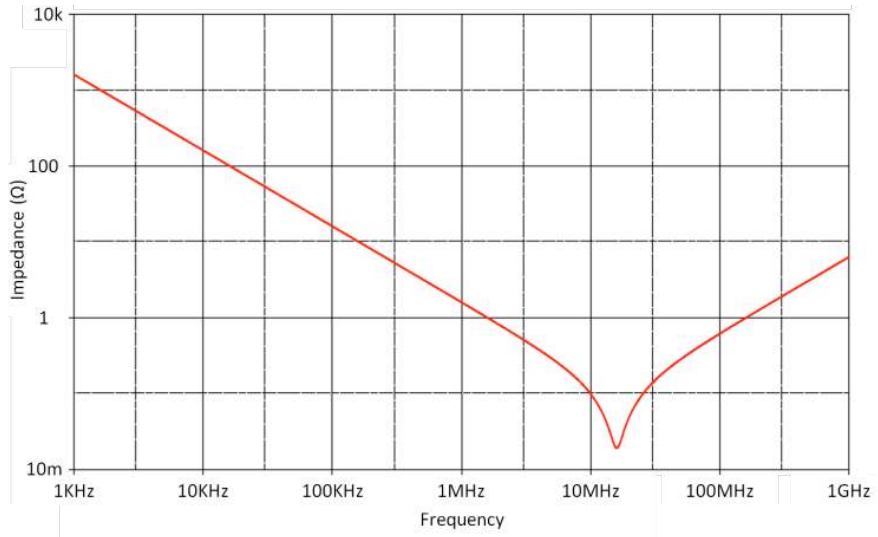

Fig. (9). Impedance profile of capacitor model.

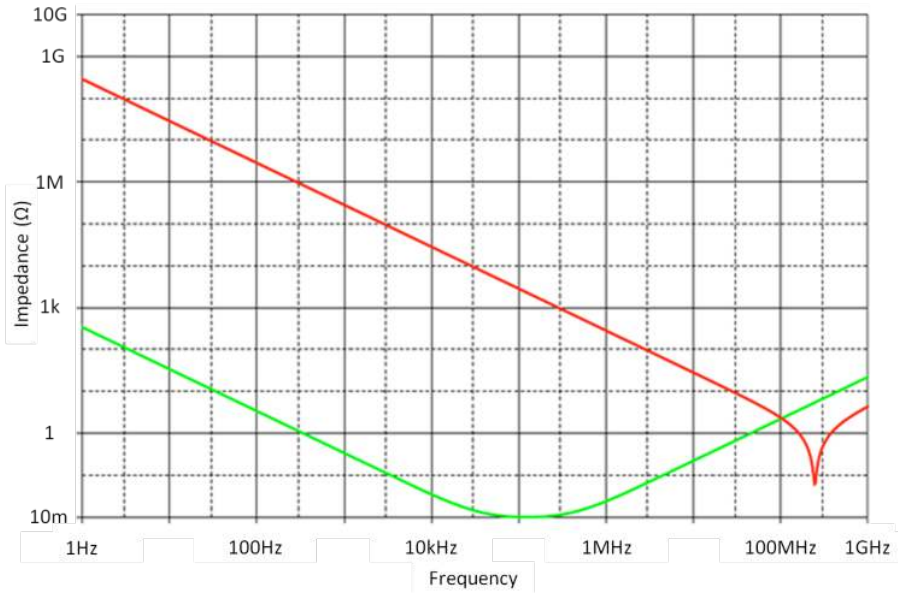

Fig. (10). Impedance profile of bulk capacitor (green) and MLCC capacitor (red).

capacitance and inductance values due to their big geometry compared to MLCCs.

Moreover, MLCC capacitors have low capacitance and inductance values, so its resonance frequency is higher than bulk capacitor ones. They work from few MHz up to few hundreds of MHz.

Fig. (**10**) shows a comparison between the impedance profile of a bulk capacitor and a MLCC capacitor.

3.3. Plane Capacitance

Power planes act as capacitors with a very low resistance and with a negligible inductance so they behave as nearly perfect capacitors at high frequencies. Power plane capacitances start working from around 100 MHz.

We can consider the geometry shown in Fig. (**11**) to estimate the plane capacitance value. Therefore the plane capacitance can be expressed with equation 6 [5]:

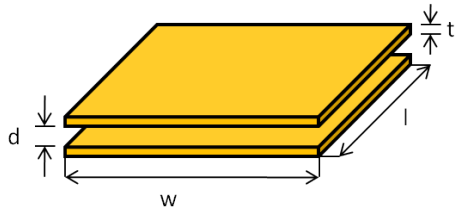

Fig. (11). Power planes.

$$C = \varepsilon_o \varepsilon_r \frac{w \cdot l}{d} = \varepsilon_o \varepsilon_r \frac{A}{d} (F) \quad (6)$$

where:

ε_o is the vacuum permittivity.

ε_r is the dielectric constant.

d is the distance between power planes.

A is the area of the power planes.

Fig. (**12**) shows the typical impedance profile in the frequency domain of a power plane conforming to equation 6.

According to equation 6, we would rather have large areas (A) avoiding plane cuts or split planes to obtain the maximum capacitance value, decreasing as much as possible the thickness of the dielectric (d) between power planes and select a dielectric with a ε_r as high as possible.

3.4. Interconnection Inductance

The interconnection inductance comprises the plane spreading inductance and the via inductance [2].

The spreading inductance value varies as a function of the dielectric thickness between power planes and the spatial distance between decoupling capacitors and load. Spreading inductance is directly proportional to the size of loop 2 in Fig. (**13**). Moreover, via inductance varies as a function of their separation and their height. Via inductance is directly proportional to the size of loop 3 in Fig. (**13**).

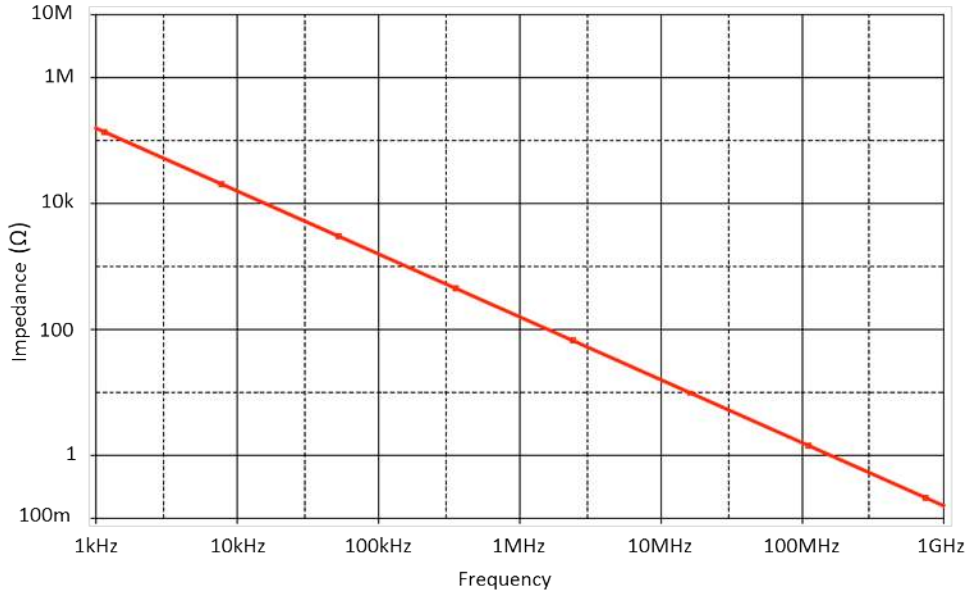

Fig. (12). Impedance profile of plane capacitance model.

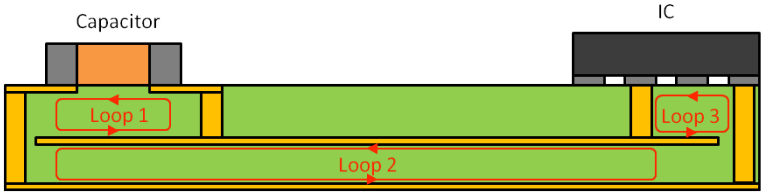

Fig. (13). Interconnection between capacitor and device.

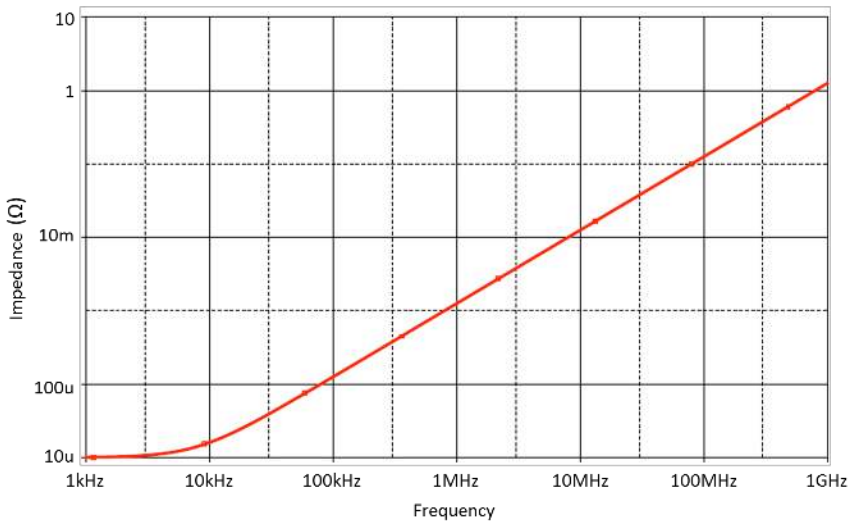

Fig. (14). Impedance profile of interconnection model.

Interconnection inductance is usually around few hundreds of picohenries, but it depends on how the decoupling capacitors connect to the load. Fig. (**14**) shows an example of the impedance behavior of interconnections.

It is very important to estimate the interconnection inductance value and maintain this value very low as it cannot be cancelled by decoupling capacitors. The maximum allowable inductance value is given by equation 7:

$$L_{int} < \sqrt{\frac{Z_{target}^2 - R_{int}^2}{2\pi \cdot f_{knee}}} \quad (7)$$

where:

L_{int} is the interconnection inductance.

R_{int} is the interconnection resistance. This value is usually negligible.

A good practice to decrease spreading inductance is to use power planes as near to the load as possible, to decrease via height and to use low separation between power and ground planes. On the other hand, a good practice is to minimize the separation between via pairs and use vias as short as possible to decrease via inductance.

4. EFFECTIVENESS OF CAPACITORS

Effectiveness of capacitors, understood as the bandwidth where a single capacitor can keep Z_{board} below Z_{target}, depends on L value, shown in section III and the distance to the load.

The following figure shows how to change the impedance profile of a capacitor as a function of C, ESR and L:

As we can see in Fig. (**15**) and in equation 8, capacitance and inductance values determine the resonance frequency as well as the quality factor, Q, which is a relation between the bandwidth and the resonance frequency. The Q factor for a series RLC circuit can be defined as follows:

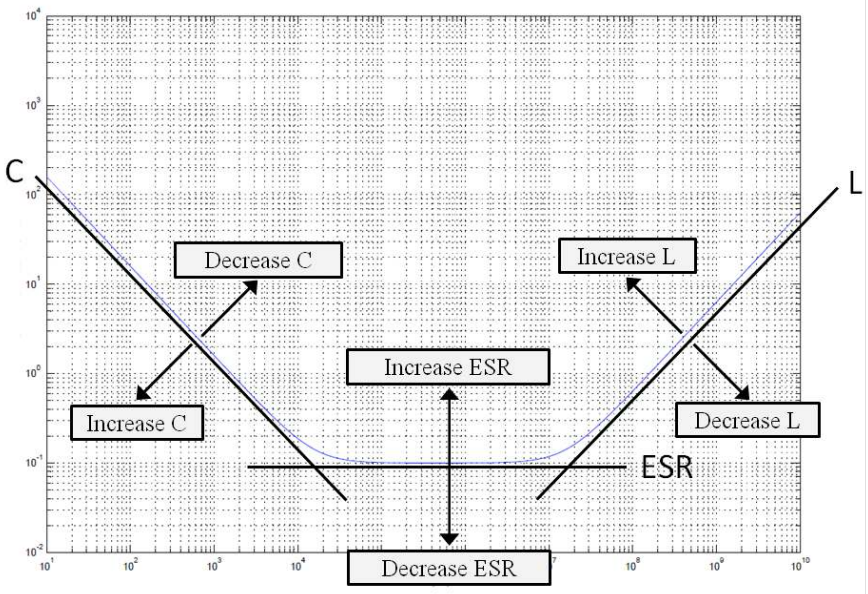

Fig. (15). Relation between impedance profile and L, ESR and C values.

$$Q = \frac{\omega_o}{BW} = \frac{\omega_o L}{ESR} \quad (8)$$

Replacing equation 5 in equation 8, we can obtain the next equation:

$$Q = \frac{1}{ESR}\sqrt{\frac{L}{C}} \quad (9)$$

If L value increases, ESR decreases or C value decreases, the bandwidth of frequencies that the capacitor covers decreases, reducing the effectiveness of capacitor.

As a conclusion, to cover the maximum bandwidth per capacitor, we must use capacitors with high capacitance values (C) and low ESR and inductance values (L).

4.1. L Value

L value is related to the geometry of the capacitor (ESL) and its mounting inductance (L_{mount}). Higher values of capacitance, C, imply bigger geometries and therefore higher L values.

How capacitors are connected to power planes plays also an important role in PDN design. Even we cannot modify the ESL value, we can decrease the amount of inductance due to mounting process of capacitor, L_{mount}. Fig. (**16**) shows five different footprints to mount decoupling capacitors.

The key is to minimize current loops below the capacitor, so traces have to be short and wide.

In the same way, it is important to place capacitors as near as possible to power planes, decreasing current loops and therefore the L_{mount} value [6]. Fig. (**17**) shows an example of this placement.

4.2. Distance to Load

Capacitors have to be placed as close as possible to load due to two main reasons [7]. The first reason is that increasing the distance of the capacitor to the load, increases the spreading inductance value decreasing the effectiveness of the capacitor.

The second reason deals with power planes behaving as transmission lines at high frequency, so there is a time delay from the moment the voltage fluctuation occurs in the device pins to the moment the capacitor current reaches the device pins. The placement of the capacitor is related to the resonance frequency as it is the frequency where capacitor is effective.

A good practice is to place capacitors at a distance less than a tenth of a quarter wavelength of their resonance frequency. This distance is known as effective distance:

$$d_{eff} \leq \frac{\lambda}{40} \quad (10)$$

5. METHODOLOGIES FOR PDN DESIGN

In this section we compare the four most popular methodologies used in PDN design to maintain a correct Z_{board} profile below Z_{target} [8]. These methods are:

- "Big-V"
- "Capacitors-by-the-decade" (CBD)

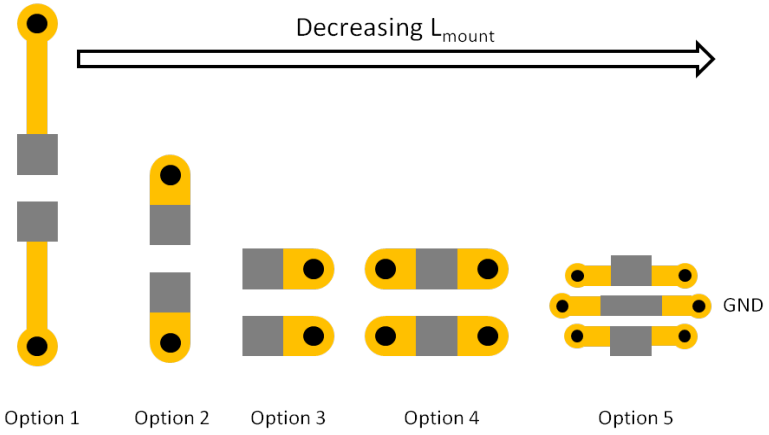

Fig. (16). Examples of capacitor footprints.

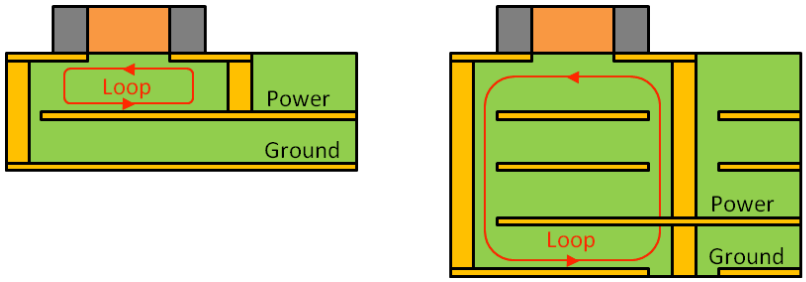

Fig. (17). Low L_{mount} value (left) and high L_{mount} value (right).

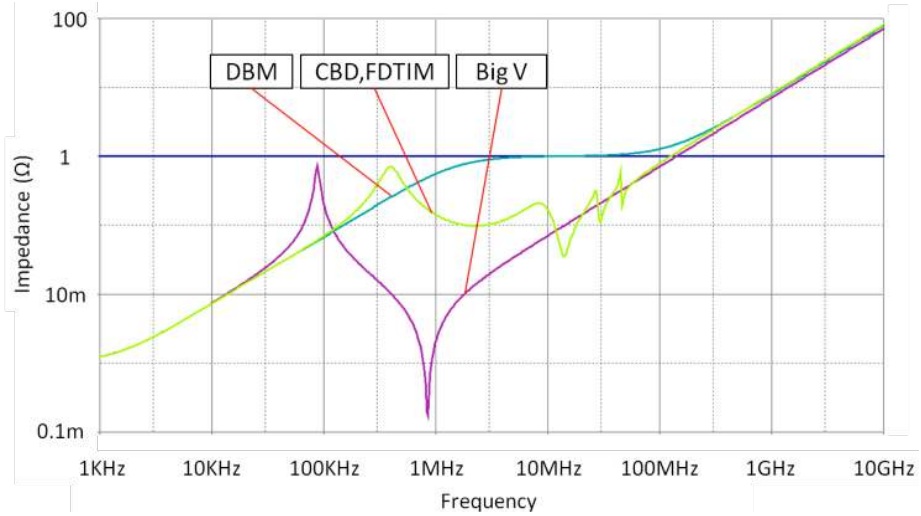

Fig. (18). Comparison between different methodologies.

- "Frequency Domain Target Impedance Method" (FDTIM)
- "Distributed Matched Bypassing" (DMB)

Big V method aims to reduce Z_{board} in the desired frequency range using a single value of capacitance and placing as many capacitors of that value as needed, so that the impedance profile often takes the form of a big "V".

CBD method is similar to Big V method but it only uses few different values of capacitors per decade to maintain a proper Z_{board} value.

FDTIM method is like the CBD method but there is no limit to the different number of capacitors that can be used per decade. FDTIM method involves placing a capacitor at that frequency where Z_{board} exceeds Z_{target}.

Finally, DBM method is an improvement of Big V method where the result is adjusted controlling ESR value of capacitors through an external resistor. DBM method provides a flat impedance profile in frequency domain. Fig. (**18**) shows an example of these methods.

The following Table **1** shows a comparison between the four methods:

Table 1. Comparison between PDN Design Methods

	Big-V	**CBD**	**FDTIM**	**DMB**
Transient	Hard	Medium	Soft	Very soft
Number Caps	Low	High	Medium	Low
Sensitivity	Low	High	High	Low
Portability Design	High	Low	Low	High
Complexity Design	Low	Low	High	Very high
Cost	Low	Low	Low	High

6. AN EXAMPLE OF PDN DESIGN: A 75GBPS MULTIFIBER DATA PROCESSING MODULE

This section shows a real example of PDN design for a 75 Gbps multifiber data processing module [9]. Fig. (**19**) shows a picture of this module.

Fig. (19). 75Gbps multifiber data processing module.

This module consists of a FPGA device as processing core and two SNAP12 connectors (one as a receiver and one as transmitter).

The FPGA used is an Altera Stratix II GX device. More precisely it's an EP2SGX60E which includes 12 high-speed transceivers capable of input and output data at up to 6.375 Gbps. Moreover, SNAP12 connectors are designed to transmit and receive 12 optical channels with a maximum data rate of 10 Gbps per channel. In the present implementation we use 6.25 Gbps per channel for a total data bandwidth of 75 Gbps per connector.

The implementation of this module needs a high degree of specialization. The main reason for this is the high frequency signals used to achieve the high data rate devised. Particularly, power distribution network design is a big concern in this design due to FPGA manufacturer requirements to get the maximum speed in the transceivers.

The result is a mezzanine board (120 mm x 174 mm) with 12 layers (6 routing and 6 power/ground planes). Different copper thickness (15µm and 30µm) is used for routing and power planes for better signal quality. Also, different dielectric thickness (63.5µm, 101.6µm and 152.4µm) is used between the planes to assure impedance values as well as enough capacitance for signal switching current demands.

The main purpose of this module is the study of high data rate optical and processing technology for particle physics experiments.

The global PDN of this module includes seven different PDNs. PDNs have been designed modeling vias with mathematical approximations, VRMs with four-elements model shown in section III, capacitors with datasheets and *FastHenry* [10] software and copper planes with Transmission Matrix Model [11-13]. For these PDN designs FDTIM method shown at section V has been applied.

The PDN design has been performed using the software *PDN Selector* tool developed at the University of Valencia [14, 15]. The result of the PDN design is a total of 134 capacitors which occupy around the 30% of the board surface.

For example, V_{CCH} power supply is one of the high-speed transceiver power supplies of the FPGA and it needs a proper PDN design. Table **2** shows the V_{CCH} power supply specifications where I_{max} has been estimated through software from FPGA manufacturer [16]:

Table 2. Specifications for V_{CCH} Power Supply

Name	V	ΔV	I_{max}	ΔI	f_{max}	Z_{target}
V_{CCH}	1.5V	2%	290mA	50%	200MHz	206.896mΩ

This FPGA uses signal rise times around 35ps [17] and, according to equation 2, these signals have a bandwidth around 10 GHz. But, for this case, FPGA manufacturer specifies that we only have to design the PDN up to 200 MHz because above this frequency on-chip capacitors carry out the necessary decoupling.

Table **3** shows the value, number of capacitors and the associated maximum distance to the load for the V_{CCH} PDN design.

This result has been simulated with Cadence Allegro SPB 16.2 PI [18]. Fig. (**20**) shows the impedance profile of V_{CCH} PDN. As it's shown, it remains below Z_{target} up to 200 MHz.

A current step with a rise time according to a bandwidth of 200 MHz has been simulated to verify that noise levels are not exceeded with this PDN design. As Fig. (**21**) shows,

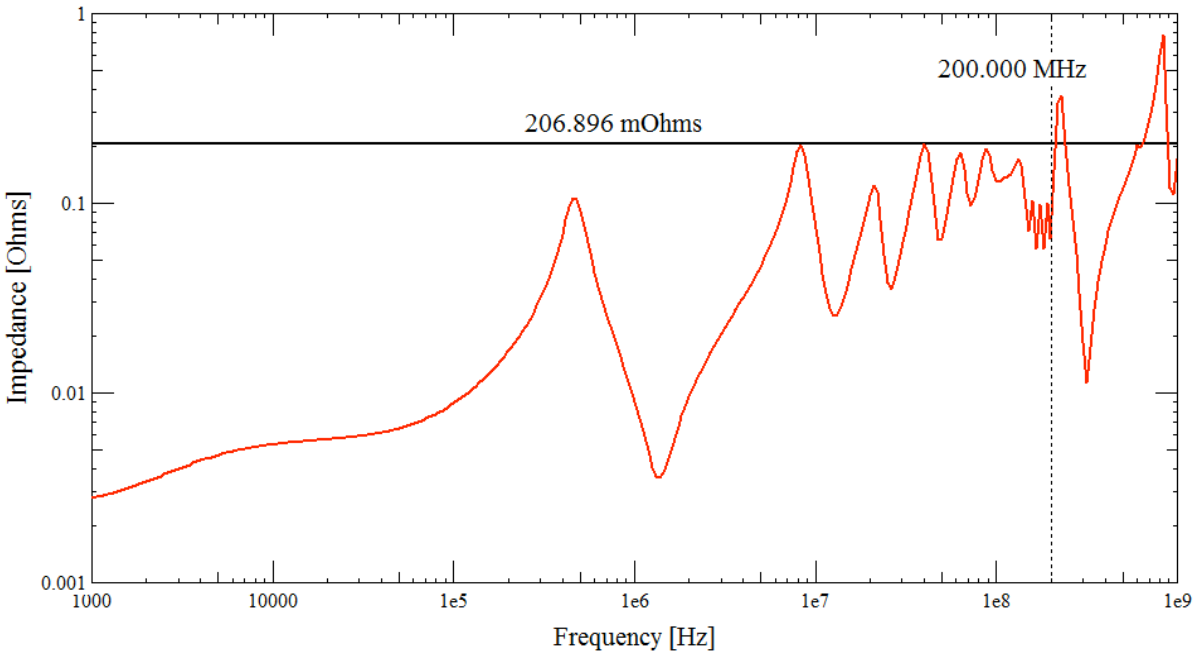

Fig. (20). Z_{board} profile for V_{CCH} with a proper PDN design.

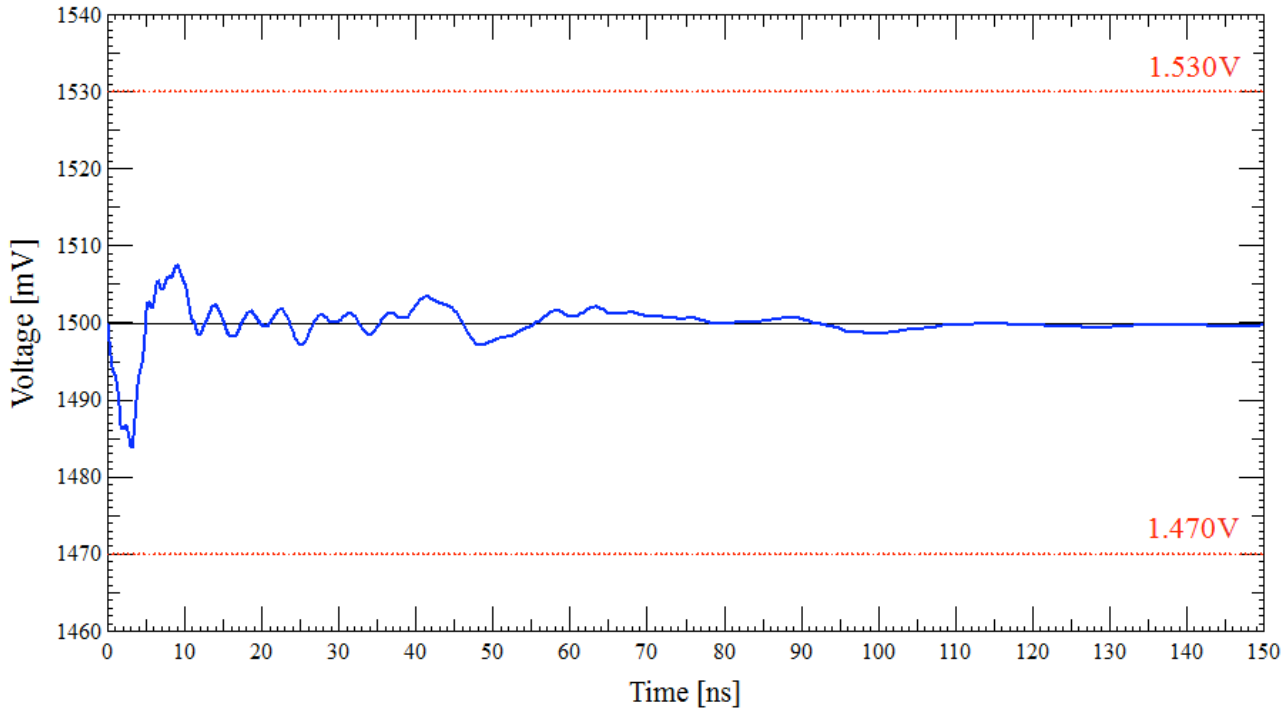

Fig. (21). Voltage response to current step for V_{CCH}.

voltage noise levels are not exceeded confirming that the designed PDN works properly.

Table 3. Value, Number and Effective Distance of Capacitors for the V_{CCH} PDN Design

Capacitor Value	Number	D_{eff} (mm)
10uF	1	1949.76
150nF	1	222.81
33nF	1	112.55
10nF	1	58.89
4.7nF	1	38.81
2.2nF	1	28.45
1.5nF	2	23.66
1nF	1	18.91
820pF	1	17.5
680pF	1	16.04
560pF	1	14.76
Total	12	

CONCLUSIONS

An explanation about PDN design for electronic designs with newest optical modules has been presented. It describes the design process, needed models and how to improve the effectiveness of PDN using less number of capacitors and obtaining cleaner voltage power supplies. Finally, a real example of PDN design of a 75 Gbps multifiber data processing module used for particle physics experiments is shown.

CONFLICT OF INTEREST

None declared.

ACKNOWLEDGEMENT

None declared.

REFERENCES

[1] Livshits P, Gurfinkel M, Fefer Y. VLSI MOSFETs lifetime reduction caused by impedance mismatch. Microelectron Eng 2011; 88(1): 28-31.

[2] Bogatin E. Signal and Power Integrity - Simplified. 2nd ed. Indianapolis: Prentice Hall Oxford, England 2009; 555-613.

[3] Smith L, Anderson R, Roy T. Power distribution system design methodology and capacitor selection for modern CMOS technology. IEEE Trans Adv Packag 1999; 22: 284.

[4] Altera. High-Speed Board Design Advisor - Power Distribution Network. TB-092-1.0. 2007.

[5] Knighten J, Archambeault B, Fan J, Selli J, Xue L, Connor S, Drewniak J. PDN Design Strategies: III. Planes and Materials – Are They Important Factors in Power Bus Design?. IEEE EMC Soc Newslett 2006; No. 210: 58-69.

[6] Archambeault B. Designing with Decoupling Capacitors. Printed Circuit Design & Fab 2001. Available from: http://pcdandf.com/cms/magazine/95/3410

[7] Xilinx. Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors. XAPP623. 2005.

[8] Novak I. Comparison of power distribution network design methods: bypass capacitor selection based on time domain and frequency domain performances. TF-MP3 at DesignCon 2006, Santa Clara, CA, Feb 6-9, 2006.

[9] Carrió F, Castillo V, Ferrer A, *et al*. Optical link card design for the phase ii upgrade of tilecal experiment. IEEE Trans Nucl Sci 2011; 58(4): 1657-63.

[10] Fast Field Solvers. Available from: http://www.fastfieldsolvers.com/

[11] Smith L, Anderson R, Roy T. Power plane SPICE models and simulated performance for materials and geometries. IEEE Trans Adv Packag 2011; 24: 277-87.

[12] Smith L, Roy T, Anderson R. Power plane SPICE models for frequency and time domains. IEEE Conference on Electrical Performance of Electronic Packaging; Palo Alto, CA, USA: Sun Microsyst. Inc. 2000; pp. 51-4.

[13] Swaminathan M, Engin AE. Power integrity modeling and design for semiconductors and systems. NY: Prentice Hall Signal Integrity Library Oxford, England 2008.

[14] Carrió F, González V, Sanchis E, Barrientos D, Blasco JM, Egea FJ. A Capacitor selector tool for on-board PDN designs in multigigabit applications. IEEE International Symposium on Electronic Compatibility (EMC), Rome, Italy 2011; pp. 367-72.

[15] Carrió F. Power Distribution Network Design Tool for Multigigabit Applications. Master diss., Department of Electronic Engineering, University of Valencia 2011.

[16] Stratix II, Stratix II GX, and HardCopy II PowerPlay Early Power Estimator. Available from: http://www.altera.com/

[17] Altera. DC and switching characteristics. Stratix II GX Device Handbook. Vol. 1, 4: p. 8, 2009.

[18] Cadence Design Systems. Allegro PCB PI User Guide. 2008.

Received: May 15, 2011 Revised: September 29, 2011 Accepted: November 20, 2011