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T.S. Latos

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A BATTERY CHARGER AND STATE OF CHARGE INDICATOR

Final Report

By
Thomas S. Latos

April 15, 1983

Work Performed Under Contract No. AI01-78CS54209

Gould Research Center
Rolling Meadows, Illinois

Technical Information Center
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United States Department of Energy

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To:
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

Final Report
A BATTERY CHARGER
AND
STATE OF CHARGE INDICATOR

Date:
15 April 1983

Prepared By:

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Executive Brief

Contract No. 955782 was a research contract performed by Gould, Inc. for the Jet Propulsion Laboratory, California Institute of Technology. It was sponsored by the U.S. Department of Energy through an agreement with the National Aeronautics and Space Administration. The objective was to design, fabricate, test and deliver a state-of-the-art Battery Charger and State-of-Charge Indicator (BC/SCI) for use in electrically powered vehicles. The BC/SCI system was designed with primary emphasis on attaining 90 percent or better overall energy efficiency, low weight, low input line noise generation, near unity power factor, state-of-charge indication accuracy of 0% to -10% and weight and volume as small as possible.

The battery charger employs a full-wave rectifier in series with a transformer isolated 20kHz dc-dc converter whose high frequency switches are programmed to actively shape the input ac line current to be a mirror image of the ac line voltage. The power circuit is capable of operating at 2kW peak and 1kW average power. The BC/SCI has two major subsystems; 1) the battery charger power electronics with its controls and 2) a microcomputer subsystem which is used to acquire battery terminal data and exercise the state-of-charge software programs. The state-of-charge definition employed is the energy remaining in the battery when extracted at a 10kW rate divided by the energy capacity of a fully charged new battery.

The battery charger circuit is an isolated boost converter operating at an internal frequency of 20kHz. The switches selected for the battery charger are the single most important item in determining its efficiency. The combination of voltage and current requirements dictated the use of high power NPN Darlington switching transistors. The power circuit topology developed is a three switch design utilizing a power FET on the center tap of the isolation transformer and the power Darlington on each of the two ends. An analog control system is employed to accomplish active input current waveshaping as well as the necessary regulation.

The battery state-of-charge (SOC) and recharge algorithms implemented in the BC/SCI are based on a phenomenological battery model which is an adaptation of both the Martin and Shepherd equations for battery voltage under dc discharge conditions. An MC6809 microprocessor provides the basic nucleus of the low-power electronics. A remote display (SCI) is connected to the system using a simple serial communications path. The software for the BC/SCI employs both assembly and Fortran languages.

Testing of the completed BC/SCI hardware indicated that most of the original performance target goals were met. Some of the targets were revised during the program due to state-of-the-art limitations and JPL's decision to rescope Gould's developmental efforts in the contract extension. Overall efficiency of the charger is 87% at an output power level of 1kVA. The weight of the entire BC/SCI system is under 35 lbs. The charger introduces a Total Harmonic Distortion of only 5% on the utility grid at the 1kW operating point. The power factor of the charger is at the targeted goal of 0.94.

The battery SOC algorithm implemented in the BC/SCI is capable of the desired +5% accuracy only when equipped with accurate battery parameters. The feasibility of tracking these battery parameters as the battery ages was demonstrated under laboratory conditions, however this capability was not included in the BC/SCI software due to the aforementioned rescoping of the contract extension. However, a follow-on contract from JPL addresses the software development of an 'adaptive algorithm'. This follow-on activity is not discussed in this report.

The battery recharge algorithm incorporates depth-of-discharge information obtained while calculating the SOC. Knowledge of this charge information prolongs the life of the propulsion batteries since the amount of overcharge is carefully controlled.

Some recommendations are suggested for future high performance EV battery chargers. These include alternate means for electrical isolation, increasing the line distortion specification limits and including an adaptive algorithm to ensure accurate SOC indication.

1. Introduction

This report discusses a program to design, fabricate, test and deliver a state-of-the-art Battery Charger and State-of-Charge Indicator (BC/SCI) for use in electrically powered vehicles. This work was performed by Gould, Inc. under Contract No. 955782 for Jet Propulsion Laboratory, California Institute of Technology. It was sponsored by the U.S. Department of Energy through an agreement with the National Aeronautics and Space Administration.

The BC/SCI system was designed with emphasis on attaining 90 percent or better overall energy efficiency, low weight, input power line noise generation of less than 100 ma, power factor between 1.0 and 0.94, state-of-charge indication accuracy of +0% to -10%, maximum battery life, minimum battery maintenance, safe installation and high reliability. The maximum power output of the battery charger was targeted at 3kVA. Semiconductors with sufficiently high voltage ratings were not available, hence this power requirement was lowered to 1kVA.

The BC/SCI system which was designed and constructed during this contract is a sophisticated piece of hardware aimed directly at mating with a 54-cell lead-acid battery, specifically a string of Gould PB-220, 3 cell golf-cart style batteries. The battery charger employs a full-wave rectifier in series with a transformer-isolated 20kHz dc-dc converter whose high frequency switches are programmed in such a manner to actively shape the ac line current to be a mirror image of the ac line voltage. The power circuit is capable of operating at peak powers of 2kW and average powers of 1kW. The ac-dc charging system dissipates only 120W measured during full power (1kW) operation. To minimize loss, circuit components were designed or selected to be nearly ideal, especially the 20kHz isolation transformer.

The original BS/SCI performance goals were relaxed due to the costs associated with solving the technical problems which arose during the initial contract. Resource limitations at JPL precluded their ability to fund all the work needed to resolve these problems. As such, Gould was not permitted to address all of the problems, during the contract extension, needed to satisfy

the original goals. However, the ability of the SOC algorithm to 'adopt' to aging batteries is the subject of another follow-on contract from JPL. This 'adaptive' algorithm is not discussed in this report.

2. Battery Charge/State-of-Charge Indicator System

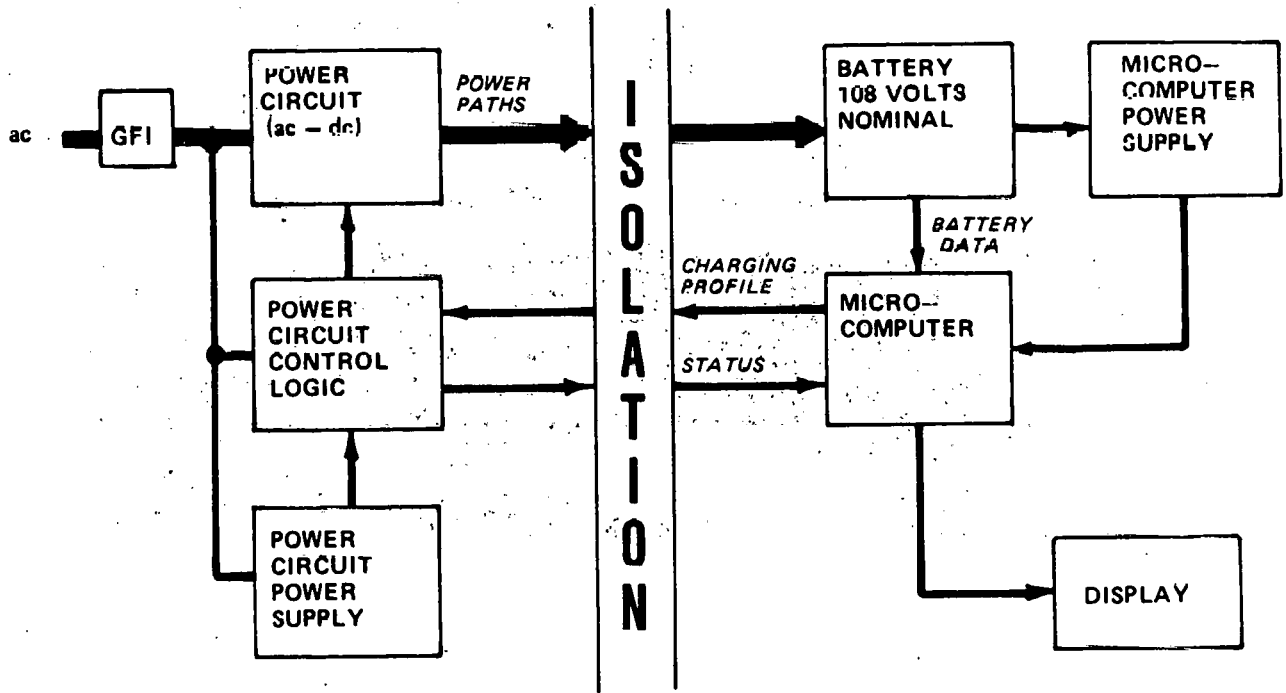
2.A System Description

The Battery Charger/State-of-Charge Indicator (BC/SCI) has two major subsystems, those being the battery charger power electronics with its controls and a microcomputer subsystem which is used to acquire battery terminal data and exercise the state of charge software programs. These two electrical subsystems are completely independent; the power circuitry is referenced to the ac line and the microcomputer is electrically referenced to the propulsion battery. Galvanic isolation between the two systems is achieved with a transformer integral to the battery charger and opto-isolated data communication paths. These major subsystems communicate with each other only during battery charging.

Figure 2.A.1 is a schematic block diagram of the complete BC/SCI. As shown in the figure, there are two independent subsystems, each with their own power supply and control electronics. A ground-fault-interruptor (GFI) is included in series with the ac line for user safety. Figure 2.A.2 is a photograph of the BC/SCI system. The major blocks in Figure 2.A.1 are all contained in the main enclosure with the exception of the GFI and the display. Battery data is obtained by inserting the junction box between the battery and the vehicle controller.

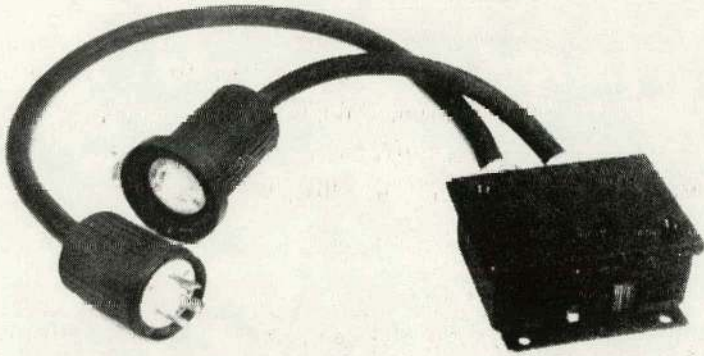
The BC/SCI system has four distinct operational modes, although only two are readily apparent to a user. The modes are; 1) Discharge Monitoring, 2) Charging, 3) Wake-up, and 4) Thinking.

The Discharge Monitoring Mode is operational while the electric vehicle (EV) controller is on. In this mode, the battery parameters of voltage, current and electrolyte temperature as well as time of day are measured.

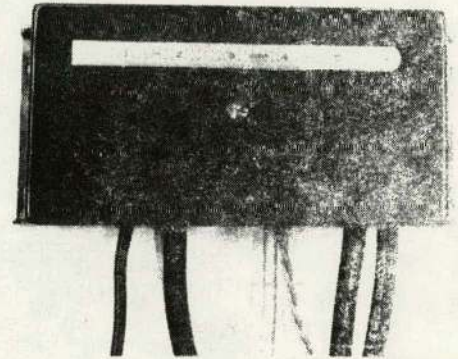


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Figure 2.A.1 Battery Charger/State of Charge Indicator (BC/SCI)



(a)



(b)



(c)

Figure 2.A.2 BC/SCI System

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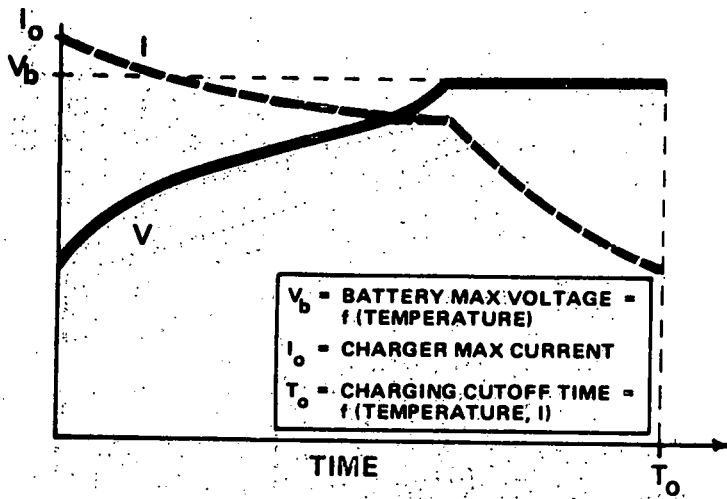
- (a) GFI module and pigtails
- (b) interface module
- (c) front view of main enclosure and display module

Using these parameters, battery state-of-charge is calculated and displayed on the display's bar graph. The state-of-charge definition employed is the energy remaining in the battery if extracted at a 10kW rate divided by the energy capacity of (again at the 10kW rate) a fully charged new battery. The state-of-charge is displayed in 10% increments.

The Charging Mode will be obvious to the user. During this mode, the battery is charged with a charging profile selected by the microcomputer system. The charging profile can be thought of as a temperature-compensated modified-constant-potential profile, shown in Figure 2.A.3. An equalize recharge profile is automatically commanded by the microcomputer periodically. It can be deferred by the operator but not requested.

The third mode, the Wake-up Mode, is one which is self-commanded by the microcomputer subsystem. This mode is exercised only after a battery discharge and two hours have elapsed. During this mode, the value of the battery terminal voltage is measured and used as a measurement of the battery's equilibrium voltage. The measurement is used to assist in determining the actual ampere-hours and amount of charge extracted from the battery.

The fourth mode, the Think Mode, has been provided to give the BC/SCI the capability of adjusting the battery model as the battery changes its characteristics during its useful life. In the present system, the fourth mode is unused.



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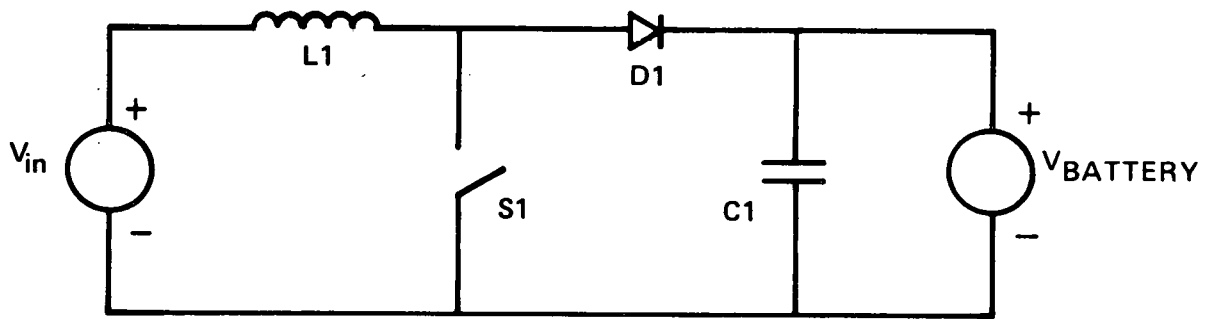
Figure 2.A.3 Temperature – compensated modified constant – potential charging profile

2.B. Power Conversion Electronics

The design selected for the charger section of the BC/SCI stems from it being an on-board electric vehicle charger and the potential impact of widespread vehicle charging on the electrical distribution grid. The charger's electrical efficiency directly impacts the operating cost of an electric vehicle and the time required to recharge the propulsion battery. Therefore it is desirable to obtain high ac-dc conversion efficiency. The weight of the charger affects the useful range and payload of present electric vehicles. A final charger design requirement is that the propulsion battery be isolated from the ac power source.

The concerns of the utility industry are directed towards line distortion and power factor. Many battery chargers in operation simultaneously having poor power factor reduces the capacity of the transmission network and decreases its efficiency. Line distortion can adversely influence the performance of loads which are common to the transmission line. The combination of the attributes of high efficiency, line isolation, high power factor, and low weight suggested a battery charger which contains a high-frequency transformer link to reduce the size and weight of the isolation magnetics. Furthermore, absence of 60Hz energy storage elements to achieve high power factor is essential. Active waveshaping control of the input line current is needed to minimize line distortion.

The battery charger circuit which was selected to meet these requirements is an isolated boost converter operating at an internal frequency of 20kHz. The general topology of a boost converter is shown in Figure 2.B.1. It contains a dc voltage source, a "boost" inductor, a switch, an output diode and a filter capacitor which is connected across the battery. During operation, S1 is toggled at high frequency and transfers energy from the source to the boost inductor, L1, when S1 is closed, then to the battery from the boost inductor when S1 is opened. Boost converters are characterized by the qualities of continuous input current, discontinuous output current, and output voltages higher than the source voltage.



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Figure 2.B.1 Simple boost converter topology. Energy is transferred from the source to $L1$ when the switch is closed, then to the battery when the switch is opened.

The following definitions are useful in order to understand the operational characteristics of the simple boost converter of Figure 2.B.1

$f_s \equiv$ switching frequency of S1

$d \equiv$ time fraction of switching period during which S1 is closed

$V_{in} \equiv$ source voltage

$I_0 \equiv$ boost inductor current at start of first period

$I_0' \equiv$ boost inductor current at start of second period.

$V_{bat} \equiv$ battery terminal voltage

$I_{L1} \equiv$ boost inductor current

At the end of the time interval when S1 is closed, the current which flows in the boost inductor L1 is

$$I_{L1} = I_0 + \frac{V_{in}}{L1} \left(\frac{d}{f_s} \right) \quad (1)$$

Similarly, at the end of the interval when S1 is open

$$I_{L1} = I_0' + \frac{(V_{in} - V_{bat})}{L1} \frac{(1-d)}{f_s} \quad (2)$$

Examination of equations (1) and (2) reveal that the control variable d does not uniquely determine the current in the boost inductor L_1 , but only its rate of change. There is only one value of d which causes the boost inductor current to remain unchanged and the converter to be in equilibrium. Equating (1) and (2), and solving for d assuming I_{L1} is unchanged ($I_o - I_o' = 0$) after a complete switching period, $\frac{1}{f_s}$, yields:

$$\frac{V_{bat}}{V_{in}} = \frac{1}{(1-d)} \quad (3)$$

For equilibrium operation, that is constant I_{L1} , d is uniquely determined by the input and output voltages.

Again combining equations (1) and (2) and solving for the change in I_{L1} , Δi , as a function of d ,

$$\Delta i = V_{in} - V_{bat} (1-d) \frac{1}{f_s L_1} \quad (4)$$

Equation (4) shows that by modulating d , it is possible to shape Δi , and hence I_{L1} . This is the fundamental concept employed in the BC/SCI charger to extract sine waves of current from the ac line. In the charger, $V_{in} = \sqrt{2} V_{ac} \sin \omega t$ and $d = 1 - \sin \omega t$. The input current of the charger is controlled to follow the input voltage so that $I_{in} = \sqrt{2} I_{ac} \sin \omega t$. The power into the charger is then $P = V_{in} I_{in} = 2 V_{ac} I_{ac} \sin^2 \omega t$. The output power is very nearly equal in the input power so that $P_{out} = V_{bat} I_{bat} = 2 V_{ac} I_{ac} \sin^2 \omega t$. The output current, I_{bat} , is therefore proportional to $\sin^2 \omega t$ since the battery voltage, V_{bat} , is constant.

2.B.1 Power Circuit Description

The BC/SCI power circuit consists of an input diode bridge to convert the ac input power to dc and a transformer isolated boost converter. A detailed electrical schematic of the power circuit is shown in Figure 2.B.2.

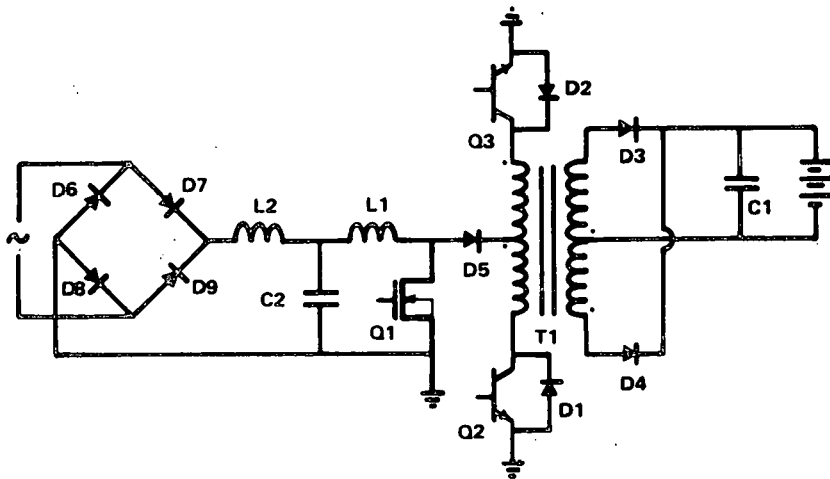
The output voltage is held to a value determined primarily by the terminal voltage of the battery.

Diodes D6-D9 form the input bridge, L2 and C2 form a high frequency low-pass filter, and L1 is the main boost inductor. Q1 is a field-effect transistor. Q2 and Q3 are used to alternately ground each half of the primary winding. D1 and D2 are diodes incorporated into Q1 and Q2. Finally D3, D4 and the secondary transformer windings form a full-wave rectifier which is connected to the battery terminals. C1 is employed as an output filter to shunt the inductive impedance of the battery cables.

The resemblance of the actual circuit incorporated in the BC/SCI to the simple circuit in Figure 2.B.1 is evident. The simple source voltage V_{in} has been replaced with a full-wave diode bridge, a high-frequency filter shunts the inductor ripple current from the ac line, and an isolation transformer has been included. The inductor discharge path includes transistors Q2 or alternately Q3.

Since high power conversion efficiency was the primary design goal, it strongly influenced the design and selection of the power circuit components. The circuit switching sequence is presented as an introduction to both the active and passive component requirements.

A current I_0 initially flows in L1, the boost inductor. This current increases during the interval $d/2f_s$ where f_s is the isolation transformer frequency of operation and d is the time fraction of the period Q1 is closed. During this interval the current slews to a new value of $I_0 + \Delta i$. Base drive is supplied to Q2 (or alternately Q3) momentarily before opening Q1. Q2 is gated on for the time period $(1-d)/2f_s$, after which time Q1 is again closed. The storage time of Q2 insures overlap between Q1 and Q2 (Q3). The circuit timing diagram is illustrated in Figure 2.B.3. The resulting switching action occurring between Q1, Q2 and Q3 alternately transfers the current flowing thru L1 between the two primary windings of T1 and Q1. This action soft switches Q2 and Q3 with Q1 as illustrated in Figure 2.B.3. The voltage requirements of Q2 and Q3 will be $2V'_{bat}$ where V'_{bat} is the battery voltage transformed to the primary side across Q1.



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Figure 2.B.2 Battery charger power stage topology. The power circuit consists of a boost chopper driving a toggled transformer.

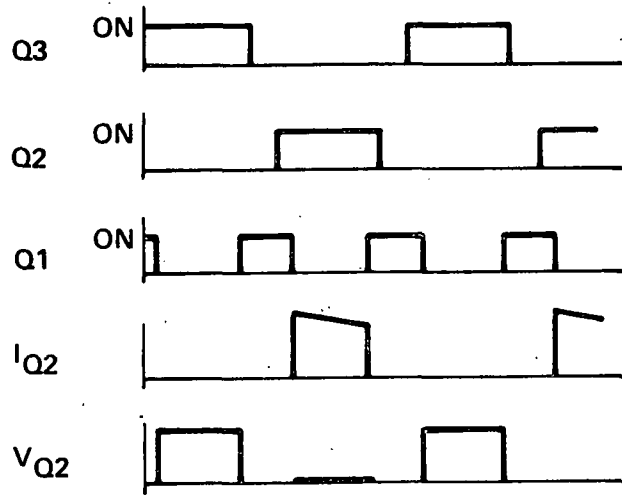
The addition of Q1 and D5 in the circuit topology are apparently redundant, as the same switching action on L1 can be achieved with an appropriate gating sequence on Q2 and Q3 (Reference 1). Efficiency penalties associated with suitable transistors for Q2 and Q3, however, justify the addition of Q3 and D5 as is discussed in a following section.

2.B.2. Design Strategy

As discussed earlier, the primary emphasis during the design phase was to achieve high efficiency operation. This section examines the component requirements and summarizes the selection/design decisions. This design iteration concentrated on a 108V lead-acid battery and a power rating of 3kW.

Input Rectifier Bridge

The input rectifiers must have a V_{RRM} rating of 400V and will conduct an average current of 11.25A. The dissipation of 25A, 50A, and 100A rectifiers was measured and compared to determine the effects of current density and manufacturing processes on the diode terminal V-I characteristics. Device dissipation was obtained from the measured V-I terminal relationship integrated over 60Hz when conducting half wave current sinusoids with an average value of 11.25A. Table 2.B.1 summarizes the results and also the diode costs.



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Figure 2.B.3 Switching sequence used to coordinate Q1, Q2, and Q3. As illustrated above, Q1 soft switches Q2 (or Q3). The maximum duty cycle required for Q2 or Q3 is 0.5.

Table 2.B.1

Input Rectifier Dissipation at Rated Input Current

| <u>Device</u> | <u>Rating</u> | <u>Dissipation (T_j)</u> | <u>Cost</u> |
|---------------|---------------|---------------------------------------|-------------|
| 1N2158 | 25A/400V | 9.3W (100°C) | 4.50 |
| UT7207 | 25A/300V | 8.9W (85°C) | 8.00* |
| MR5040 | 50A/400V | 9.4W (106°C) | 3.80 |
| 1N3291 | 100A/400V | 8.3W (86°C) | 14.10 |

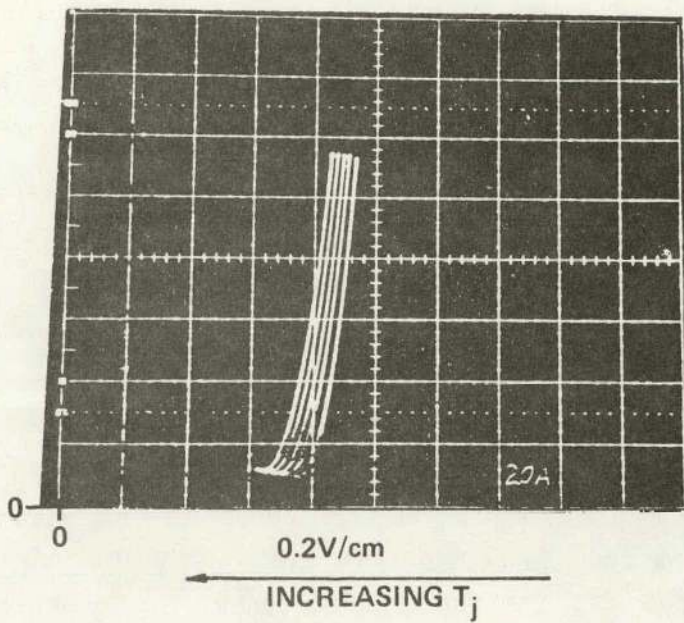
* Estimate

MR5040 diodes were selected based on their low cost since the dissipation of all diodes evaluated was nearly identical. Figure 2.B.4 shows the terminal V-I characteristics of this diode as a function of junction temperature for average currents of 11.25A and 9.0A. These currents correspond to BC/SCI line charging currents of 25A and 20A respectively.

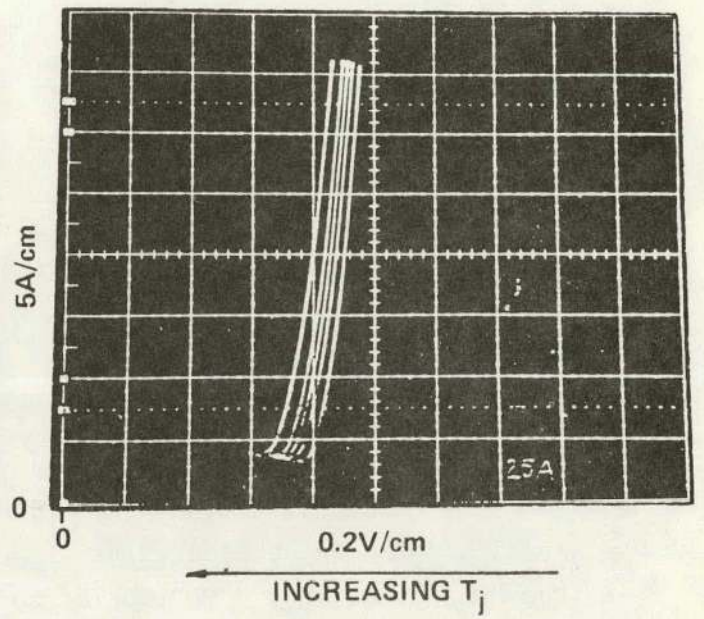
Boost Inductor/Input Filter

The boost inductor can be designed to have an inductance value ranging from approximately 0.2mH to a maximum value of 2.6mH. These limits are determined by the allowable power factor (0.94 min) and the additional stresses imposed by the high frequency ripple current upon the switching semiconductors. The upper limit on L_1 can be expressed in terms of the minimum power factor (PF), the input current slew rate, and the maximum duty cycle of Q_1 , d_{max} in the following relationship.

$$L_1 < \frac{V_{ac} \sin(\cos^{-1}PF)d_{max}}{377 I_{ac}} \quad (5)$$



$T_j = 23^\circ\text{C}$
 45°C
 60°C
 75°C
 91°C



$T_j = 23^\circ\text{C}$
 45°C
 60°C
 75°C
 106°C

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Figure 2.B.4 MR5040 V-I Characteristics

This follows from $V = L \, dI/dt$ and $L < V \, dt/dI$ where $V = V_{ac} \sqrt{2} d_{max} \sin(\cos^{-1}PF)$ and $I = I_{ac} \sqrt{2} \sin \omega t$. V_{ac} is the rms of the line voltage and I_{ac} is the rms of the line current.

Equation 5 results from the need for a sufficient line voltage to obtain the desired current slew rate in the boost inductor. The power factor angle, the line voltage, and the maximum duty cycle determine the voltage at the time of the maximum required current slew rate. The lower design bound can be determined by selecting the maximum ripple current desired. Limiting this to 10% ($dI = 0.1 I_{ac} \sqrt{2}$ and $dt = 1/4f_s$) implies:

$$L1 > \frac{V_{ac} \, d_{min}}{0.4f_s \, I_{ac}} \quad (6)$$

where f_s is the Q2 or Q3 switching frequency and d_{min} is the minimum conduction of Q1.

The RMS input current at the switching frequency was calculated assuming the maximum value of inductance, 2.6mH, and found to exceed the 100mA_{RMS} line distortion goal by a factor of 2, thus an input filter was necessary for any chosen value of boost inductance. Figure 2.B.5 is a plot of the high frequency RMS ripple current vs. the boost inductance. A boost inductance of 0.8mH was selected which places it at the knee of the curve of Figure 2.B.5. Figure 2.B.6 shows the sensitivity of the ripple current to variations in line voltage and battery terminal voltage. It is noteworthy that the ripple current magnitude is only a function of d , V_{ac} , and V_{bat} for a given value of boost inductance.

The boost inductor was fabricated with a 2 mil selectron C core (AL-100-Arnold) and square No.7 AWG wire, 82 turns, distributed on both legs to reduce the mean-turn-length. A gap of 0.15" limits the peak flux to 1.1 Tesla (T) at the peak current of 40A. Dissipation at rated power was projected to be 20W.

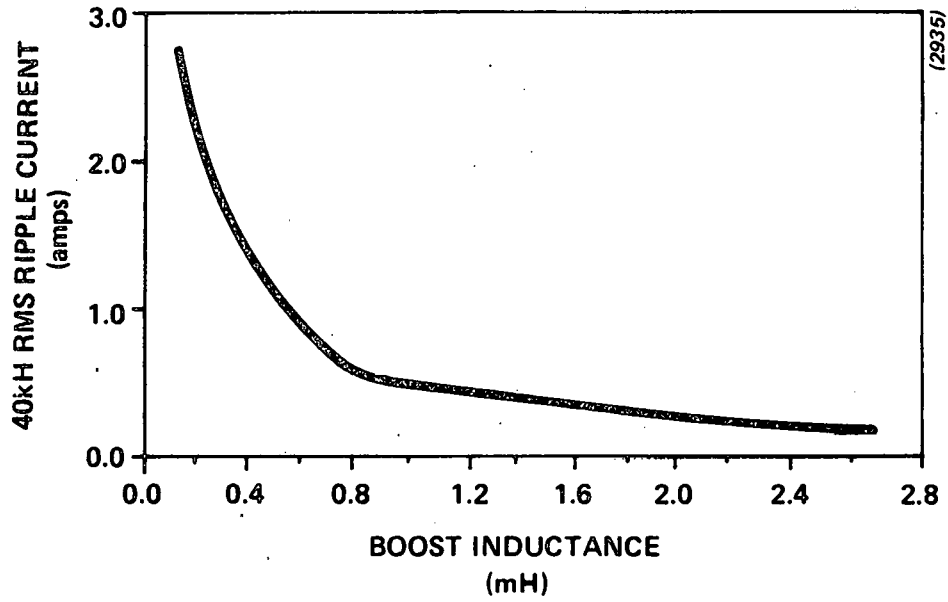
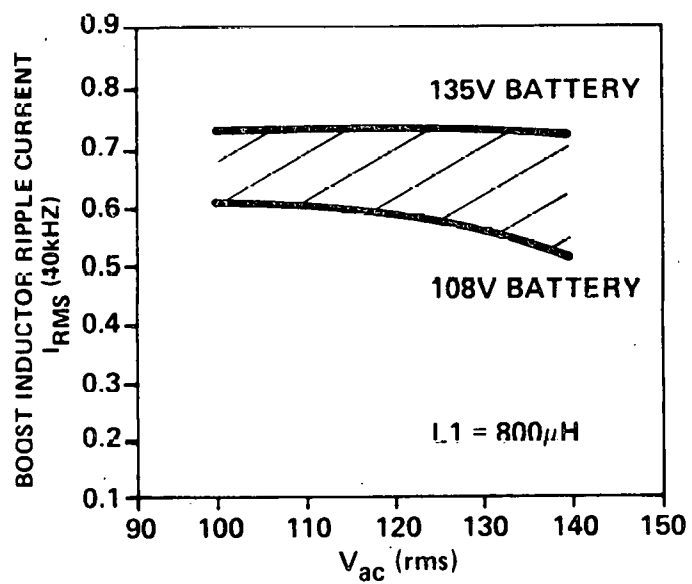


Figure 2.B.5 High frequency ripple current flowing in the boost inductor as a function of the inductance



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Figure 2.B.6 Ripple current as a function of line voltage and the battery voltage

Although ferrite material could be employed in the construction of the boost inductor, its low flux density, 0.25 Tesla, and limited core geometries requires a large number of turns and hence almost equal copper loss to the total dissipation of the selectron-based design.

The input filter was selected to shunt the 40kHz ripple current to keep it from appearing on the ac line. The magnitude which would appear on the line side of the two-pole filter can be expressed as

$$I_{ac}(40kHz) = \frac{I_{RMS}(40kHz)}{1 + \omega_s C_f (\omega_s L_f + R_l)} \quad (7)$$

where, $I_{ac}(40kHz)$ is the high frequency current injected into the ac line,
 $I_{RMS}(40kHz)$ is the boost inductor ripple current,
 R_l is the line impedance
 C_f is the filter capacitance
 L_f is the filter inductance
 ω_s is the angular switching frequency

Solving (7) for the minimum value of L_f to meet the 100mA distortion-requirement yields a filter inductance of $18\mu H$ with $R_l = \phi$ and $C_f = 5\mu F$. A filter inductor of $35\mu H$ was designed with a 4-mil C-core, Arnold AH-407, using 8 turns of No.9 AWG with a gap of 10.5mil to limit the peak flux to 1.5T.

Semiconductor Switch Requirements

The switches selected for the battery charger are the single most important item in determining its efficiency. The devices must have a V_{ce0} rating sufficient to withstand the transformed battery voltage, low conduction loss, and fast switching speed for minimum switching loss. The peak switch currents at full power operation approach 40A and the transformed battery voltage across the center-tapped primary could range from approximately 366V to 600V depending on the primary-secondary turns ratio and the battery voltage. The combination of the voltage and current requirements indicated

that there were only two possible choices for the transistors in series with the transformer windings, Q2 and Q3 in Figure 2.B.2. Characteristic of both of the available devices, Motorola MJ10024 and Power Tech PT3526, were inductive load switching times of $1\mu\text{s}$ or longer and the requirement of parallel devices/switch to achieve the current requirement.

Figure 2.B.7 shows the impact of the battery voltage and the turns ratio N_p/N_s of the isolation transformer on the V_{ce0} rating of Q2 and Q3. An examination of Figure 2.B.7 suggests that a minimum turns ratio which satisfies the equation

$$N_p/N_s > \frac{V_{ac} \sqrt{2}}{V_{hat}} \quad (8)$$

be employed to minimize the V_{ce0} requirements. For the range of expected line voltage and battery voltage, this suggests $N_p/N_s > 1.7$. However the efficiency of the power circuit is also directly impacted by the leakage inductance of the isolation transformer which can be minimized by employing an integer turns ratio. Since the MJ10024 V_{ce0} rating was 750V, a N_p/N_s ratio of 2 was selected thus determining the voltage stresses. Four parallel transistors per switch were specified to reduce conduction loss and maintain acceptable collector-base current gains.

The feasibility of using a different transformer isolated boost converter, shown in Figure 2.B.8 and operationally described in (1), was originally examined with the switching performance of the MJ10024 devices. Assuming a $1\mu\text{s}$ fall time, an average current of $\frac{I_{dc} \sqrt{2}}{\pi}$, a voltage of 480, the estimated turn-off losses for both switches exceeded 100W. This circuit topology was therefore rejected based on efficiency arguments. The inclusion of Q1 in Figure 2.B.2, a FET, reduced the switching loss projection to 11 W assuming a $0.1\mu\text{s}$ fall time, an average current of $\frac{2I_{ac} \sqrt{2}}{\pi}$, and a voltage of 240V. The FET needs only to have a V_{ds} rating of 1/2 the V_{ce0} rating of the transistors since it is only subjected to the voltage across the primary center tap. The inclusion of this third switch however, necessitated the inclusion of a diode in series with the transformer center tap because of the

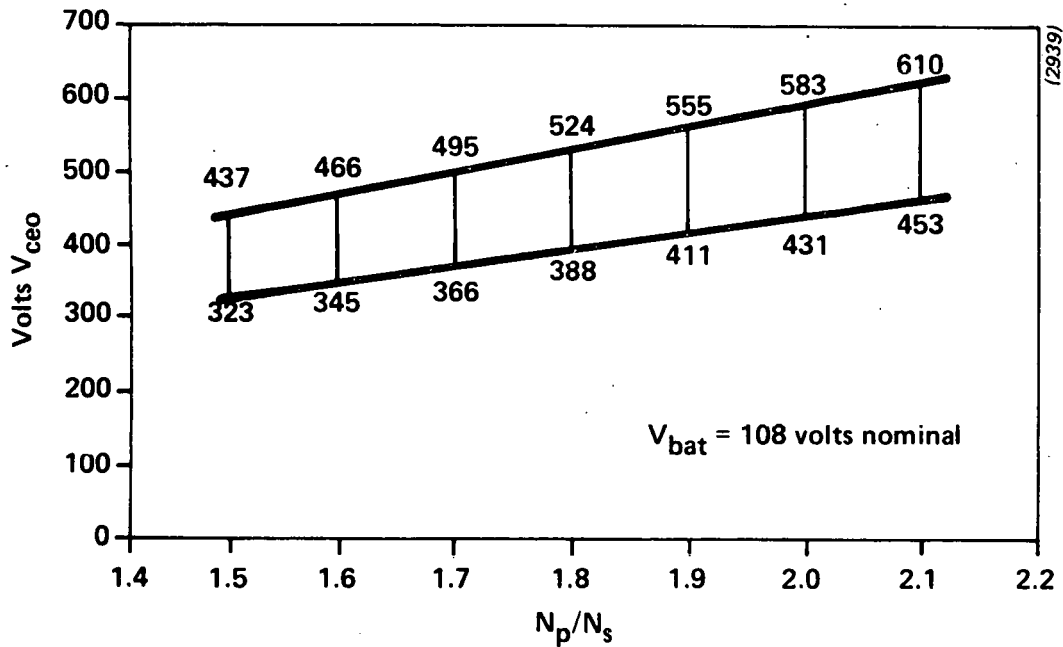
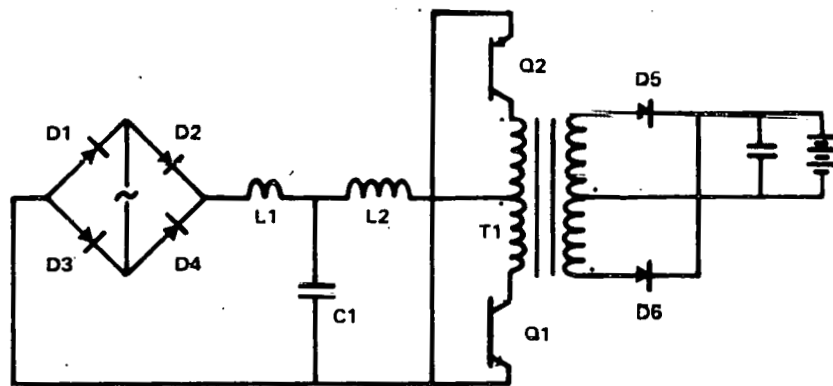


Figure 2.B.7 The influence of the changing battery voltage and the isolation transformer turns ratio on the V_{ce0} requirements of Q2 and Q3. 1.7:::1 is the minimum ratio which satisfies the constraints of the boost circuit topology. Top curve represents a fully charged battery; bottom curve represents beginning of charge.



(2941)

Figure 2.B.8

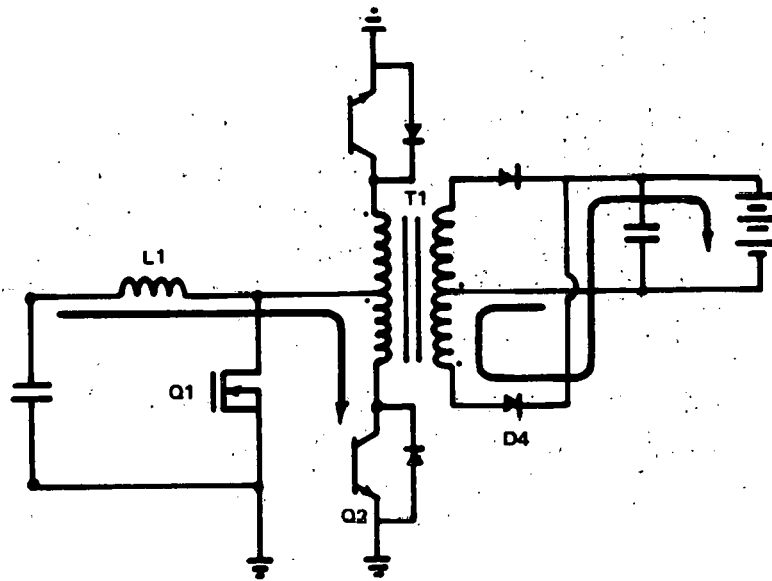
Two Switch Power Circuit Topology

During the inductor charging mode, both Q1 and Q2 are conducting, alternately opening Q1 or Q2 to discharge the boost inductor. Each transistor has a duty cycle ranging from 0.5 to 1.0.

finite recovery time of the secondary diodes D3 and D4. The reverse recovery current in these diodes, coupled with the antiparallel diodes on each darlington transistor, complete a path for a circulating current to flow in the transformer primary windings, the antiparallel diodes, and the FET (Q1), substantially increasing the conduction losses in Q1. This situation is illustrated in Figure 2.B.9 and is initiated by the closing of Q1.

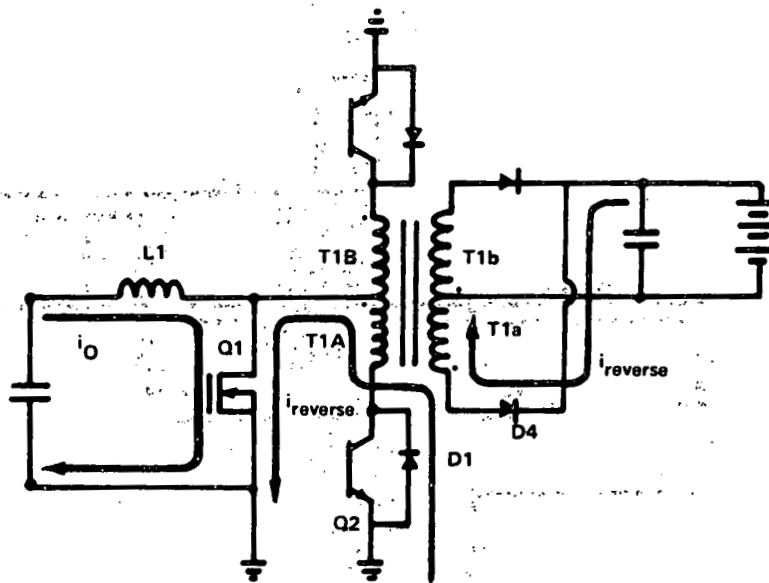
Assume an initial current is flowing through L1 into the center-tap of T1 and returning through Q2 to ground. D4 is forward biased and power is being supplied to the battery. At the moment Q1 closes, the inductor current will be transferred to Q1 at a rate dependent on the leakage inductance between the T1a and T1A transformer windings and the battery voltage impressed on C1. Current will decay to zero and reverse through the shorted D4. This current will be reflected to the primary side switch until D4 recovers. At the moment of recovery, current is flowing in T1A and T1a. Since the current in T1a is driven to zero when D4 recovers and the voltage at the center tap is constrained to be on-state voltage of Q1, the amp-turn imbalance in T1 forward biases the antiparallel diode across Q3 and a matching current flows through T1B. This current will decay at a rate proportional to the on-voltage of Q1 and the leakage inductance between T1A and T1B. Since the on-voltage of Q1 is small, the current continues to circulate for the entire conduction interval of Q1. The inclusion of D5 (Figure 2.B.2) blocks this circulating current.

Several less obvious advantages are obtained by the introduction of Q1 in the boost power stage topology. As illustrated in Figure 2.B.3, it is possible to adopt a gating strategy for Q2 and Q3 where each of their duty cycles ranged from 0 to a maximum of 50%. This allows the use of a standard proportional-feedback base drive to reduce base drive power supply requirements. Secondly, since the current in the transformer T1 is never required to transfer instantaneously to both primary windings, the leakage inductance between the T1 primary windings is not a critical winding design parameter.



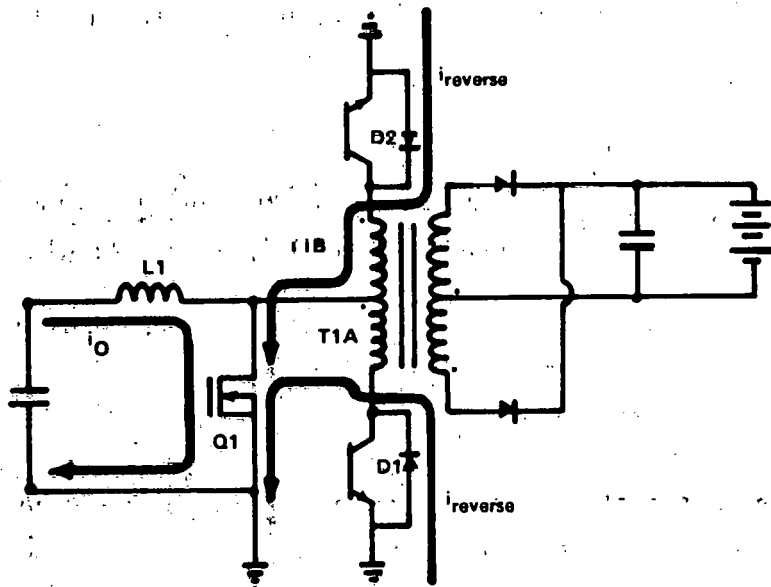
(2943)

Figure 2.B.9A Initial current path. The primary side current flows through T1 and Q2. Secondary current flows through D4 into the battery.



(2944)

Figure 2.B.9B Current path showing the effect of reverse recovery current of D4. The reverse recovery current flows into the winding T1a and is transformed into winding T1A. This current adds to the current i_0 flowing in Q1.



(2945)

Figure 2.B.9C Recirculation current established. The current flowing through Q1 is now the sum of $i_O + 2i_{reverse}$.

The switch losses, switching (P_S) and conduction (P_C) predicted at full power operation were calculated with the aid of equations (9) - (13).

$$P_{Q2,Q3} = P_C \quad (9)$$

$$P_{Q1} = P_C + P_S \quad (10)$$

where $P_C = V_{ce(sat)} (I_{ave}) \quad (11)$

for each Darlington Transistor and

$$P_C = I_{rms}^2 r_{ds} \quad (12)$$

for the FET. P_S , the switching loss for the Darlington Transistor, is zero with the adopted gating strategy. P_S for the FET is approximated by

$$P_S = 1/2 V_{ds} \cdot I_{ave} \cdot f_s \cdot t_s \quad (13)$$

where f_s is 40kHz. Table 2.8.2 contains the loss estimates for each switch type. As shown in the table, the switching loss is only 22% of the switch dissipation, the dissipation being dominated by conduction loss in each darlington (13W) and in the 2 parallel MTM15N40 FET's (18W).

Table 2.8.2

Switch Loss Projection at Rated Charger Power of 3kW

| <u>Device</u> | <u>P_C(W)</u> | <u>P_S(W)</u> | <u>$P_C + P_S$(W)</u> |
|---------------|----------------------------|----------------------------|----------------------------------|
| MJ10024 | 26.5 | - | 26.5 |
| MTM15N40 | 18.0 | 12.2 | 30.2 |
| TOTALS | 44.5 | 12.2 | 57.0 |

Note: $t_s = 0.1 \times 10^{-6}$
 $V_{bat} = 129.6$

Transistor Base Drive Description

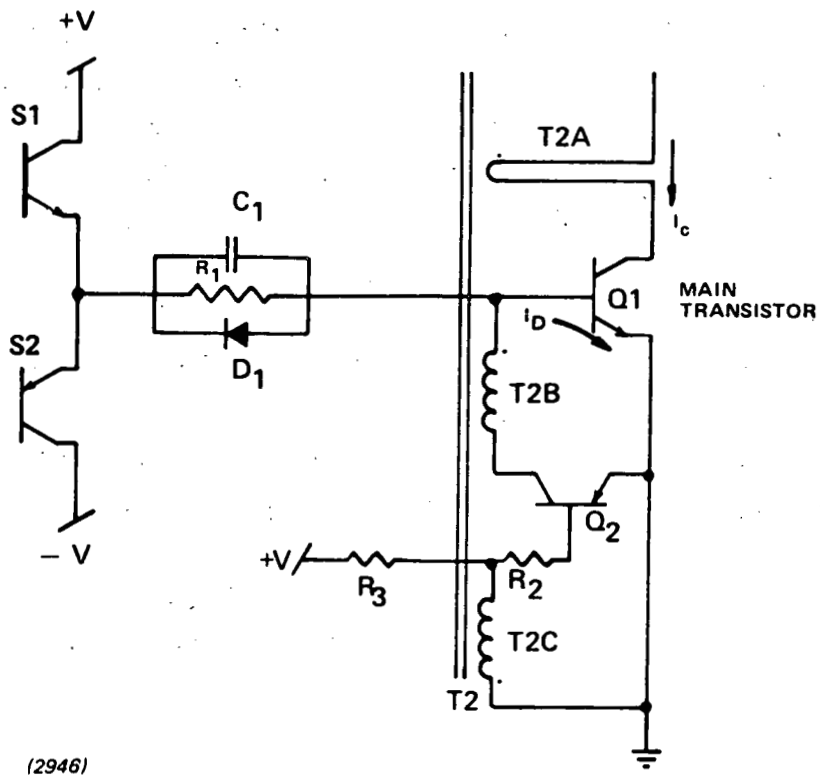
The requirements for the Darlington transistors in this application dictate that they operate over a wide range of collector currents and conduction times. These criteria and the demand for high efficiency led to the decision that a proportional base drive scheme be employed which features low saturation voltage and reduced base drive power supply requirements. To avoid ambiguity in the initial state of the proportional drive transformer core, it was desired to reset the core to the same state regardless of the length of the conduction period. An additional constraint imposed by the Darlington transistor is the requirement to supply negative base drive for at least 5 microseconds to insure forward blocking capability before the subsequent half cycle. These requirements were obtained with a proportional base drive which included an auxiliary switch in series with the feedback winding.

The base drive electrical schematic is shown in Figure 2.B.10. In the figure C_1 supplies an initial current pulse to Q_1 limited only by circuit parasitic resistance when switch S_1 closes. The base drive for Q_1 is supplied by both the feedback winding and the logic supply through R_1 .

When S_1 opens and S_2 closes, both Q_1 and Q_2 are reversed biased, disconnecting the feedback winding from the emitter of Q_1 . Core reset is obtained via R_3 .

Isolation Transformer Design

The isolation transformer requirements included transforming the battery voltage so that it exceeds the peak voltage appearing at the terminals of the input rectifier bridge, low primary-secondary leakage inductance, and high efficiency. These requirements were obtained with the use of a ferrite core and foil windings. The details of the transformer construction and electrical parameters are contained in Table 2.B.3. The measured primary-secondary leakage inductance of $0.45\mu\text{H}$, coupled with a 1.2mH magnetizing inductance, yields an inductance ratio of 2666/1. A 2:1 turns-ratio was



(2946)

Figure 2.B.10 Proportional drive scheme. The conventional proportional drive has been modified with the addition of Q2 in series with the feedback winding T2B. Independent control of the base voltage (Q1) and the core reset voltage is obtained.

selected (N_p/N_s) to allow the winding design to consist of 4 unity-turns-ratio coil sets, eight turns/coil, distributed on the U core and connected in series/parallel to form the desired turns ratio.

Table 2.B.3

Isolation Transformer Electrical Parameters

| | |
|-----------------------|--|
| Core | Ferroxcube TF4-3C8 U-I 1B4-3C8 |
| | Window Area 16cm ² Core Area 6.15cm ² |
| Conductors | Foil .015" x .500" Insulation .005" NOMEX |
| Electrical Parameters | $L_m - 1.2mH$ $L_x - 0.45\mu H$ $C_s - 200pf$ |

The core selection was based on the power rating of the transformer and the transformer efficiency. An estimate of the core area - window area product was obtained using Equation (14).

$$A_c W_c = \frac{\text{Primary Voltage (Time)}}{\text{Peak Flux}} \times \frac{\text{Wire Area}}{\text{Window Utilization}} \quad (14)$$

for $N_p/N_s = 2.0$, $V_{bat} = 120$, $f_s = 20 \times 10^3$ Hz, a current density of 1000 cir mils/amp, and a 0.4 window utilization factor,

$$A_c W_c = 164 \text{ cm}^4 .$$

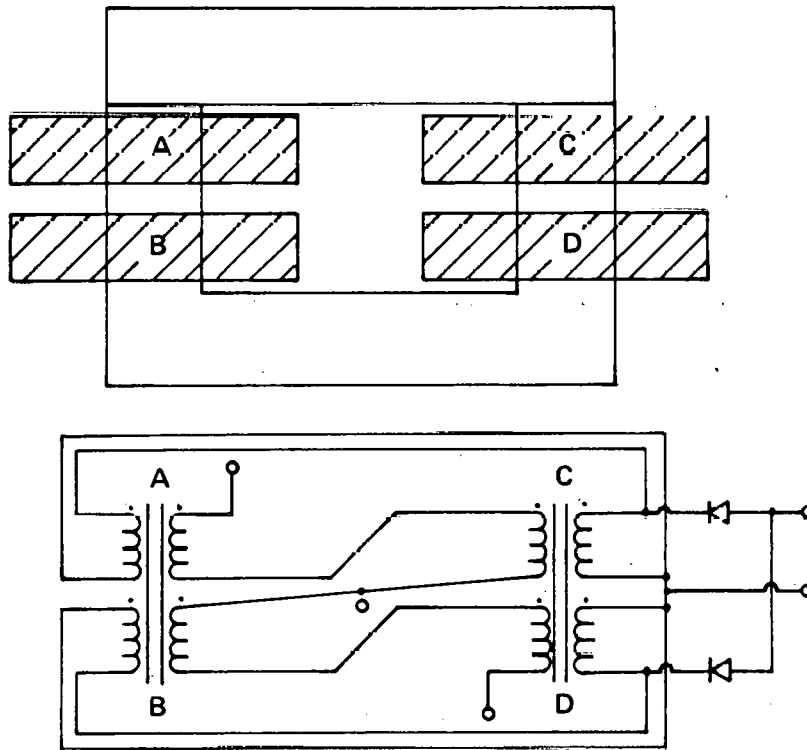
Only one ferrite core was available which met this power handling criteria, a U-I core manufactured by Ferroxcube which has a $A_c W_c$ product of 148 cm^4 .

The primary magnetizing inductance was selected to be 1mH to limit the magnetizing current to approximately 1A. The number of primary turns was selected to be 16 to limit the peak flux to 0.25 Tesla. Each secondary consists of 8 turns. Figure 2.B.11 contains a schematic of the transformer construction. A gap of 0.006 inches was included in the design to tolerate a dc current of 200mA. The projected dissipation of the transformer at full load operation is 30W.

Secondary Components

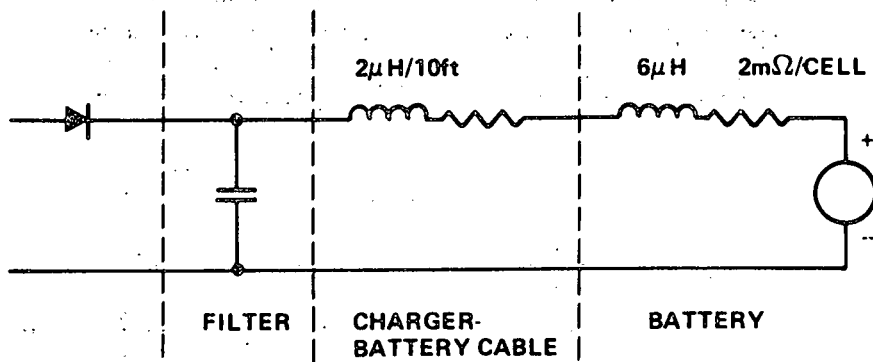
The secondary circuit components, the rectifier, filter capacitor, battery cables, and the battery can be represented by the equivalent electrical circuit shown in Figure 2.B.12. To determine design tradeoffs, the following assumption were made:

1. Charger efficiency = 1.00
2. All switching frequency harmonics are shunted by the output filter capacitor.



(2949)

Figure 2.B.11 Isolation Transformer Construction
 Each coil consists of 8 turns, being in series on the primary side and in parallel for the secondary.



(2951)

Figure 2.B.12 Secondary circuit

The total RMS current flowing out of the charger was calculated with a computer program, taking both the varying line voltage and duty cycle into account. This yields a charger output current which contains both 120 Hz and switching frequency components. The instantaneous power delivered to the battery is $P_{bat} = P_{in}$. Therefore

$$I_{bat} = \frac{P_{in}}{V_{bat}} = \frac{2V_{ac} I_{ac} \sin^2 \omega t}{V_{bat}} = I_p \sin^2 \omega t \quad (15)$$

The input power P_{in} is proportional to $\sin^2 \omega t$ since both the voltage and current are varying in phase sinusoidally.

The 120Hz component of the output current can be determined by the use of the identity,

$$\sin^2 \mu = 1/2 (1 - \cos 2\mu) \quad (16)$$

therefore

$$I_{rms-120Hz} = \frac{I_p \sqrt{2}}{4} \quad (17)$$

The 40kHz RMS requirements of the capacitor is

$$I_{RMS-40kHz}^2 = I_{RMS-charger}^2 - I_{ave-bat}^2 - I_{rms-120Hz}^2 \quad (18)$$

solving, $I_{RMS-40kHz} = 17.6A$

Therefore the filter capacitor must have an RMS current rating at 40kHz which is at least 20A, a voltage blocking capability of 150V, and a capacitance of at least 20 μ f to minimize the voltage ripple (ΔV_{C1}) appearing on the primary side switches.

It can be shown that

$$\Delta V_{C1} = \frac{I_{RMS-40kHz}}{C_{filter} \cdot 2 \cdot \pi \cdot 2f_s \cdot 2} \quad (19)$$

Figure 2.B.13 plots this relationship along with the maximum switch voltage stresses. A suitable commutation style capacitor, GE type 97F, 20 μ F was selected for the filter capacitor.

The losses in the battery are proportional to the charging RMS current. As shown previously, there is a 120Hz RMS component in the output current which has a magnitude of $\frac{I_{dc}}{\sqrt{2}}$. The additional loss in the battery, as compared to dc, can be expressed as

$$I_{dc}^2 + \frac{I_{dc}^2}{2} = I_{dc}^2 (1.5) \quad (20)$$

which is a loss penalty of 50% compared to pure dc charging. Since a typical golf cart cell has an equivalent series impedance of 2m Ω when discharged, the 108V battery will dissipate an additional 40W or approximately 1.1% of the charger input power at 3kW. This is probably a reasonable tradeoff vs. increasing the charger's size and weight by forcing the output LC filter resonant frequency to be less than 120Hz.

Motorola MR866 fast recovery rectifiers were selected to rectify the output of the isolation transformer and No.3 AWG cabling was specified to connect the charger to the battery.

Waveshape and Amplitude Controller

The control approach and block diagram is described in this section. In order to achieve near unity power factor operation, the ac line current must be a replica of the line voltage. This is achieved in the BC/SCI by

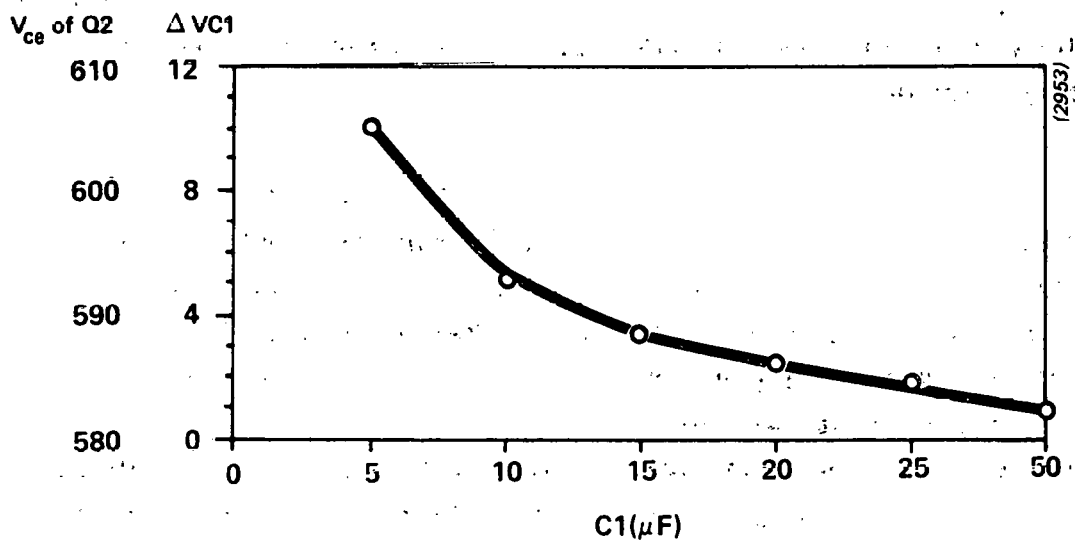


Figure 2.B.13 Increased voltage on Q2 with decreasing values of C1. ΔV_{C1} is the overshoot voltage on capacitor C1.

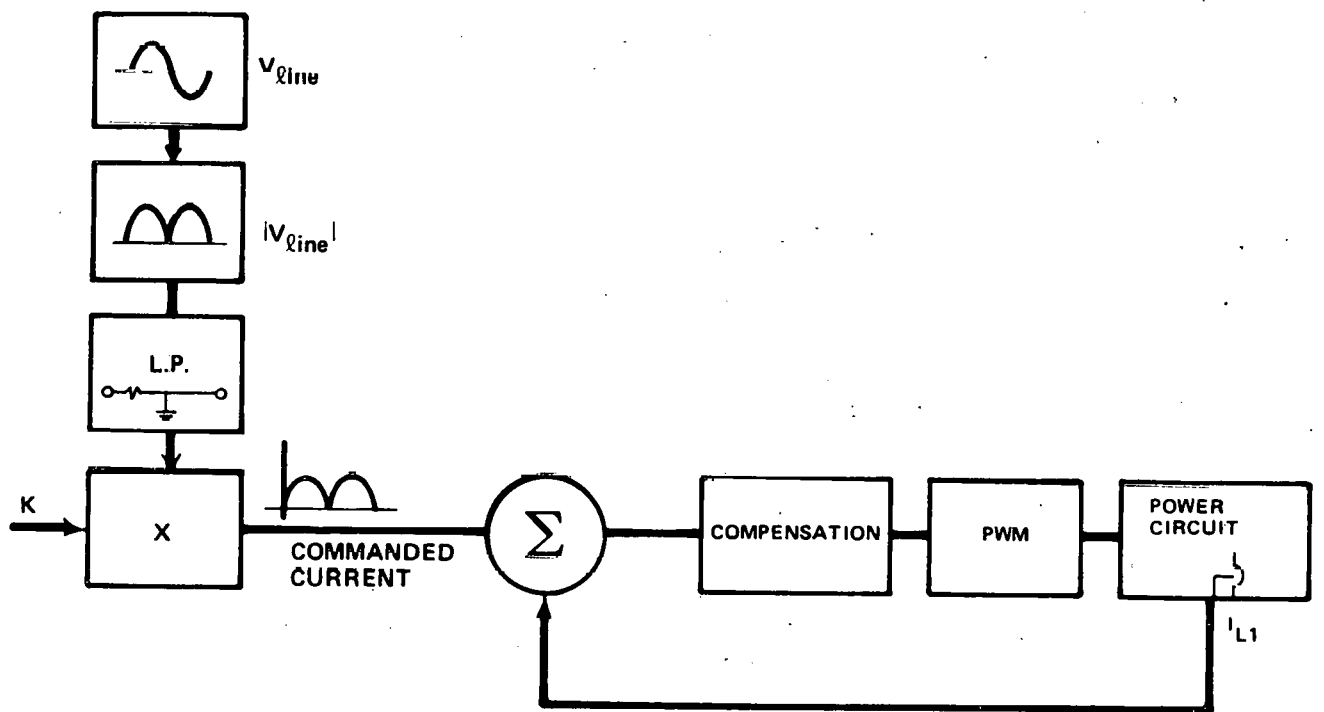
using the line voltage to obtain line current waveshape information and controlling the amplitude via a multiplier. Figure 2.B.14 contains the control system block diagram.

The ac line information is obtained via a step down transformer, rectified, and delayed with the L.P. filter to set the power factor angle. This waveform is multiplied by K , where $0 < K < 1$, to vary the amplitude of the resulting power circuit input current. K is varied in such a manner as to regulate the magnitude of the input line current or the magnitude of the battery voltage during charging.

A detailed control block diagram is presented in Figure 2.B.15. Of particular interest is the power circuit transfer function containing a pole at the origin and gain proportional to $V_b/L1$, the reflected battery voltage and the boost inductance. The high frequency input filter is represented by the double pole at 81,649 radians. The compensation consists of a pole - zero combination at 487 radians and 37037 radians respectively. The loop transmission of the complete circuit is presented in Figure 2.B.16. The function of the pole-zero pair is now evident. The first pole is located at the origin, the boost inductor "integrator," the second pole is placed at approximately 500 radians to maintain high gain to assure waveshape accuracy. The zero is introduced to improve phase margin at unity gain. Crossover is assured approximately one decade lower than the switching frequency of the converter.

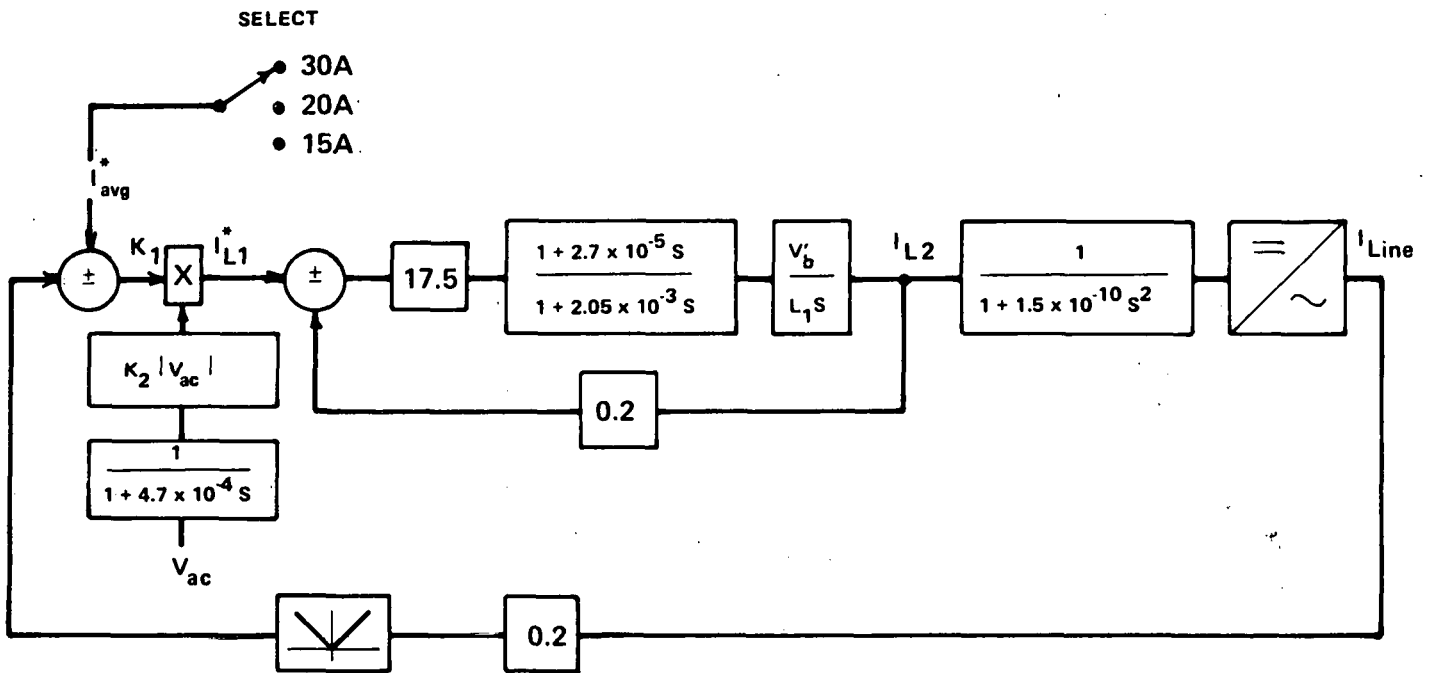
Control Power System

The power supply which is used to provide the required power circuit voltage and currents is schematically illustrated in Figure 2.B.17. This power supply is directly connected to the ac line and provides isolated $\pm 12V$ outputs which are referenced to the power circuit negative bus. This power supply is used for base drive power and provides control logic power to the system controller discussed in the previous section.



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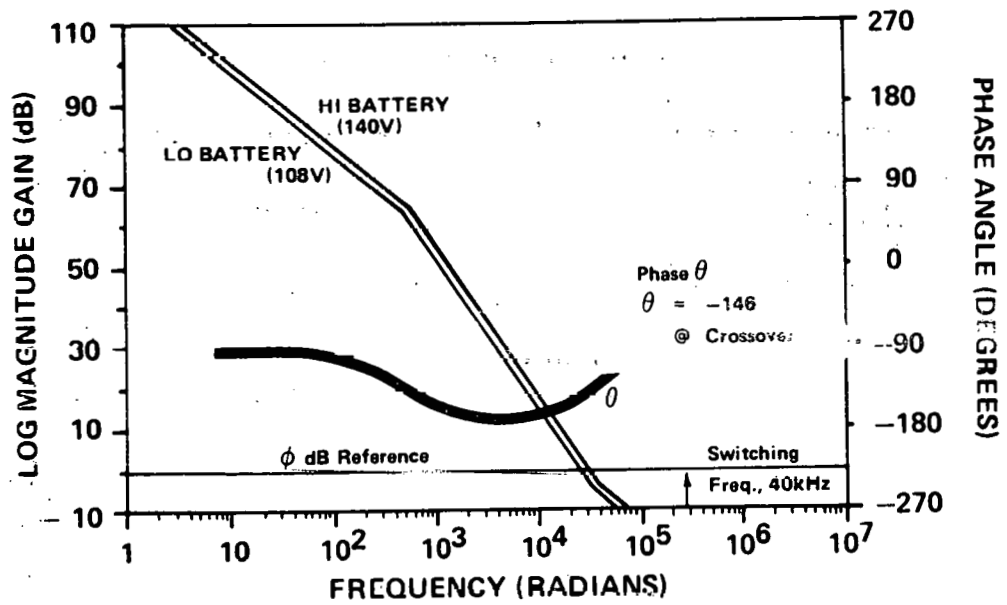
Figure 2.B.14 Power circuit control block diagram



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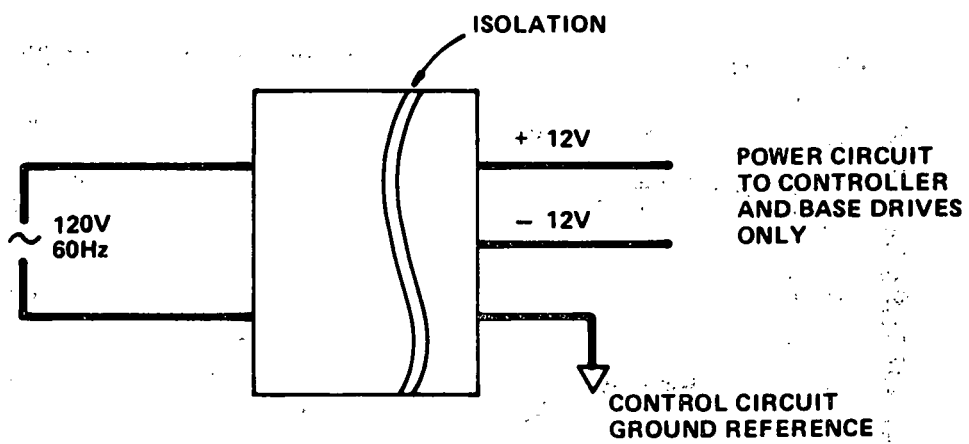
Figure 2.B.15 Power circuit controller block diagram

- i_{avg}^* = commanded avg. line current
- i_{Line} = ac line current (instantaneous)
- V_{ac} = ac line voltage (instantaneous)
- K_1 = error signal
- K_2 = scaling factor
- i_{L1}^* = commanded boost induction current
- V'_b = battery voltage as reflected through transformer



(2958)

Figure 2.B.16 Power circuit inner loop transmission characteristics



(2961)

Figure 2.B.17 Power circuit power supply concept

2.C Battery Algorithms

This section of the report addresses the models used to calculate the battery state of charge (SOC) and the recharge algorithm implemented in the BC/SCI. Two SOC models were investigated during the contract effort, a phenomenological model and a physical model, with the former implemented in the BC/SCI. The phenomenological model is discussed first. The accuracy of the SOC algorithm was tested by exercising battery modules with discharge profiles emulating driving cycles. A possible model parameter adaptor scheme is presented.

2.C.1 Phenomenological State of Charge Model

The phenomenological model may be thought of as an adaptation of both the Martin (Reference 2) model and the Shepherd (Reference 3) equation for battery voltage under dc discharge conditions. A brief review of the Martin and Shepherd models below is followed by a description of the modifications made to them in order to arrive at the new model. Finally, some of the issues involved in implementation of the phenomenological model on a microcomputer are addressed.

The Martin model summarizes the condition of a battery at any time with two state variables; $Q(t)$, the charge removed from the battery, and $C(t)$, the battery capacity. These variables change according to the equations

$$\frac{dQ}{dt} = I \quad (21)$$

$$\tau \frac{dC}{dt} + C = f(I) \quad (22)$$

where I is the battery discharge current, $f(I)$ is a function which specifies the battery capacity under conditions of dc discharge at the current, I , and τ is a characteristic time-constant of the battery. The battery is considered to be exhausted when Q reaches C (i.e., when $C - Q < 0$).

The physical interpretation of Equation 21 is obvious, the rate of change of battery charge withdrawn is the current, I . According to Equation 22, for any given instantaneous current, I , the battery capacity, C , approaches the dc battery capacity at that current, $f(I)$, with a characteristic time constant, τ .

Computation of the battery capacity for a constant-current discharge current is relatively straightforward. Given initial values for the state variables, C_0 , and Q_0 , as well as a standard discharge current, I_0 , the time to cutoff may be calculated either by numerical simulation of Equations 21 and 22, or by analytical means. State-of-Charge prediction in terms of a constant power discharge is more difficult, as the model makes no explicit prediction of battery voltage during the discharge.

Shepherd Model

The Shepherd equation is intended to predict a battery voltage profile during a dc discharge.

According to this relation,

$$v(t) = V_0 - \left(\frac{V1}{Q1}\right) \cdot Q(t) - R1 \cdot I(t) - \frac{R2 Q2}{Q2 - Q(t)} \cdot I(t) \quad (23)$$

1
2
3
4

where $v(t)$ is the predicted battery voltage, $Q(t)$ is the charge withdrawn from the battery, I is the discharge current, and V_0 , $V1$, $R1$, $R2$, and $Q2$ are parameters of the battery. The first term in Equation 23 is a constant. The second term represents the decline of equilibrium voltage due to falling electrolyte concentration as electrolyte is consumed in the battery. The third term is simply an impedance voltage drop. The fourth term is equivalent to an impedance that rises as $Q(t)$ approaches $Q2$. Shepherd proposed this impedance term to account for the shrinking active-material surface area in the battery during a discharge. According to his explanation, as the active

material was used up in the electrochemical discharge reaction, the current density necessary to maintain a constant current rose, necessitating a higher reaction overpotential.

2.C.1.a Model Modifications

It has been found experimentally that one set of coefficients (V_0 , V_1 , Q_1 , R_1 , R_2 , Q_2) is not sufficient to accurately predict battery voltage for dc discharges over a wide range of currents and temperatures. However, if R_1 , R_2 , and Q_2 are allowed to vary with both temperature, T , and current, I , then the resulting predicted voltage profiles can be fitted to actual data quite closely. In addition, a filtered battery current, obeying the differential equation,

$$\tau \frac{dI_F}{dt} + I_F = I(t) \quad (24)$$

is used in Equation 23 in place of the actual current, I , then the predicted voltage is a reasonable approximation to the measured voltage, v , even under conditions of varying current. In Equation 24, $I(t)$ is the actual battery current, while $I_F(t)$ is the filtered current. Thus, the phenomenological model predicts the battery voltage with the equation,

$$v(t) \cong V_0 - \left(\frac{V_1}{Q_1}\right)Q(t) - R_1(I_F, T)I_F(t) - \frac{R_2(I_F, T) Q_2(I_F, T)}{Q_2(I_F, T) - Q(t)} \cdot I_F(t) \quad (25)$$

Actually, due to the filtering function performed by Equation 25 the voltage predicted by Equation 25 is closer to a filtered version of the measured voltage,

$$\tau \frac{dv_F}{dt} + v_F = V_m(t) \quad (26)$$

where $v_F(t)$ is the filtered battery voltage.

In order to implement this model to predict state of charge, an array of values for R_1 , R_2 , and Q_2 at various discrete values of current and temperature are required. A microcomputer keeps track of the withdrawn charge, Q , and filtered current, I_F , during a discharge. At any time that the remaining capacity was desired, the processor would begin an imaginary discharge, varying the current so as to keep the product $v(t) * I(t)$ equal to the standard discharge power. Linear interpolation between the discrete values of temperature and current for which the battery data are stored would be used to compute estimates of R_1 , R_2 , and Q_2 , so that battery voltage predictions could be made. The remaining energy would then be the product of the standard power rate and the time (in the imaginary discharge) until the voltage fell below some cutoff level.

Any such model as the phenomenological one is founded on two basic assumptions; 1) that the battery can be described totally by its dc discharge response, and 2) that any effects of discharge at levels different from the standard rate are transient (i.e., will not significantly affect the battery capacity unless cutoff occurs within several time constants of the different-rate discharge). It is apparent from the battery tests performed during the contract that neither of the above assumptions is entirely true. However, it is believed that they are close enough, in most situations that an electric vehicle battery will encounter, to allow an accurate state-of-charge prediction.

Table 2.C.1 contains the array of Shepherd coefficients as functions of discharge current and electrolyte temperatures.

Table 2.C.1

Cell Parameters

| <u>Current (Amps)</u> | <u>Electrolyte Temperature</u> | | |
|-----------------------|--------------------------------|---------------|---------------|
| | <u>9°C</u> | <u>20°C</u> | <u>40°C</u> |
| 20 | R1 = 2.7293 | R1 = 2.9568 | R1 = 2.2395 |
| | R2 = 0.5078 | R2 = 0.3792 | R2 = 0.2180 |
| | Q2 = 125.8769 | Q2 = 164.4615 | Q2 = 188.8593 |
| 80 | R1 = 1.8282 | R1 = 1.7384 | R1 = 1.3714 |
| | R2 = 0.2137 | R2 = 0.1732 | R2 = 0.1794 |
| | Q2 = 83.0000 | Q2 = 109.4000 | Q2 = 141.3512 |
| 130 | R1 = 1.6844 | R1 = 1.5260 | R1 = 1.3090 |
| | R2 = 0.1198 | R2 = 0.1216 | R2 = 0.1331 |
| | Q2 = 69.3520 | Q2 = 91.8800 | Q2 = 121.0732 |
| 200 | R1 = 1.6320 | R1 = 1.2800 | R1 = 1.2854 |
| | R2 = 0.0940 | R2 = 0.1600 | R2 = 0.1195 |
| | Q2 = 70.7200 | Q2 = 84.8000 | Q2 = 98.2439 |

where R1 and R2 are in milliohms per cell and Q2 is in Ah.

These parameters were derived from constant current discharge experiments employing Gould PB-220 golf cart batteries. The voltage and the charge withdrawn was recorded during each discharge and the resulting voltage curve predicted by the Shepherd equation was fit to the actual voltage curve to determine the Shepherd coefficients. The battery recharge profile employed during this testing was an equilibrium recharge profile with an overcharge of 20%. This was necessary to achieve repeatable test results for the battery under test.

2.C.1.b Algorithm performance

The accuracy of the SOC algorithm was tested by exercising a 6-cell battery module with a discharge profile which emulated a SAE 227a, schedule D driving cycle. Again, the battery data consisting of voltage, current, temperature, and time was recorded during the test. Using a large minicomputer, the SOC algorithm used the recorded battery data to calculate the SOC. All actual battery tests were terminated with a constant power discharge at the 185W/cell rate (10kW for a 54 cell battery). During this interval, the calculated SOC was compared to the measured SOC and an RMS error was calculated for the predictions. A total of 32 driving cycle type tests were conducted on the batteries at ambient temperatures varying from 9°C to 45°C. Figures 2.C.1-2.C.6 illustrates the battery voltage, current, and watt-hr vs. time for two driving tests. Figures 2.C.7 and 2.C.8 show a plot of the calculated SOC and the measured SOC for these two respective tests.

Figure 2.C.9 shows the capacity variations of the batteries during the testing interval. The battery capacity (W-hr) varied from a low point of 920 Wh to a high of 1430 Wh for the six-cell module, with the lowest capacity observed at ambient temperatures of 5°C and the highest at 40°C. The RMS error in the SOC prediction was as low as 1.3 Wh/cell and as high as 37.3 Wh/cell during the testing as seen in Table 2.C.2.

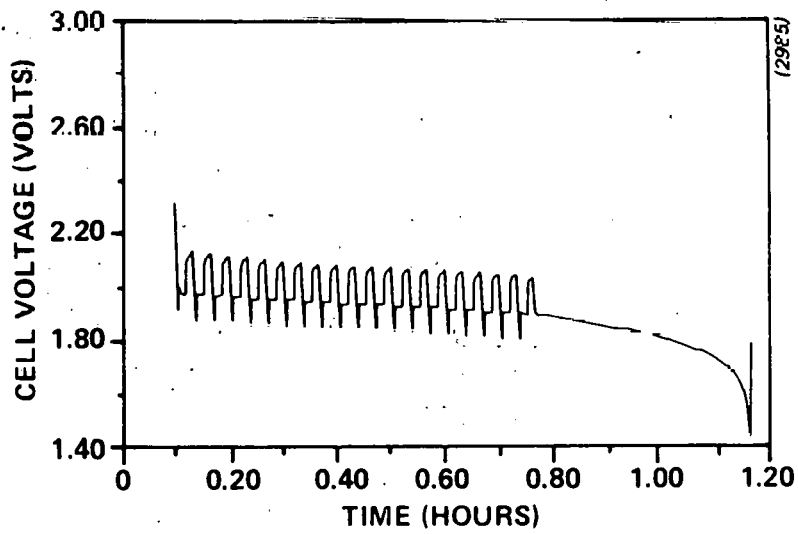


Figure 2.C.1 Cell voltage vs. time for test F49TST033.D05

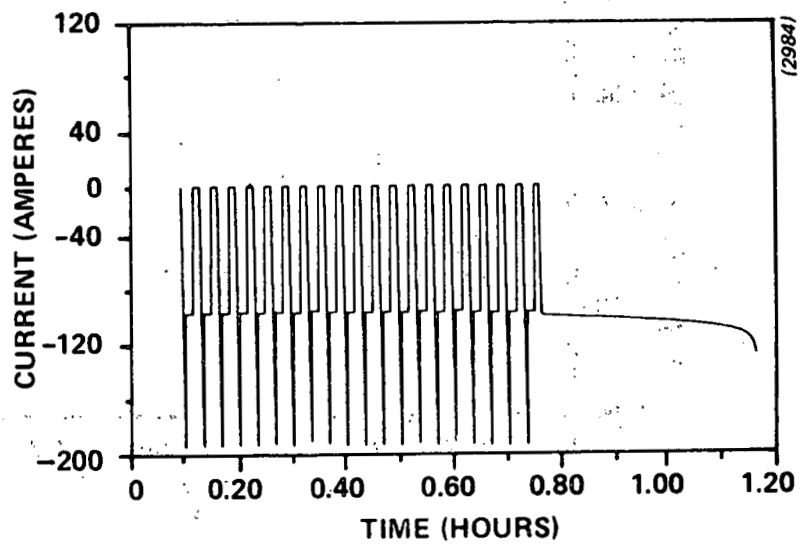


Figure 2.C.2 Battery current vs. time for test F49TST033.D05

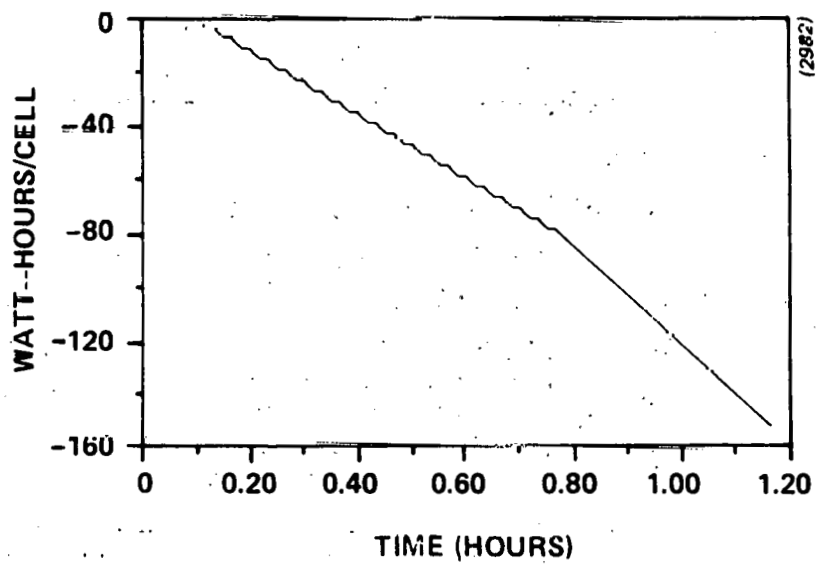


Figure 2.C.3 Battery watt-hours vs. time for test F49TST033.D05

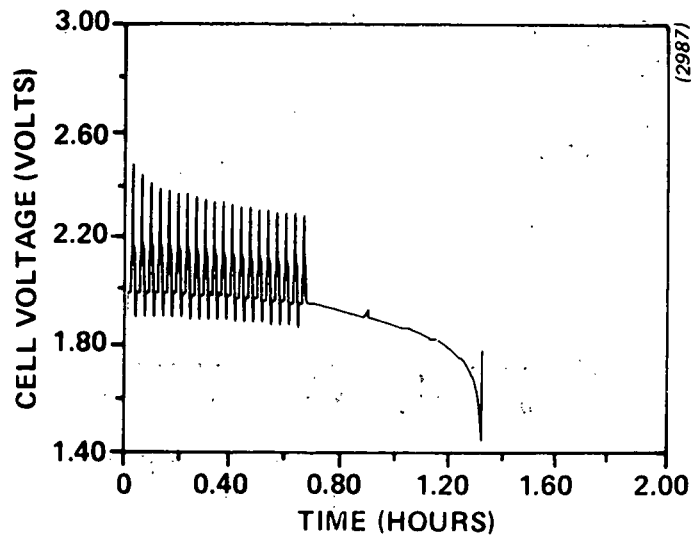


Figure 2.C.4 Cell voltage vs. time for test F43TST031.D17

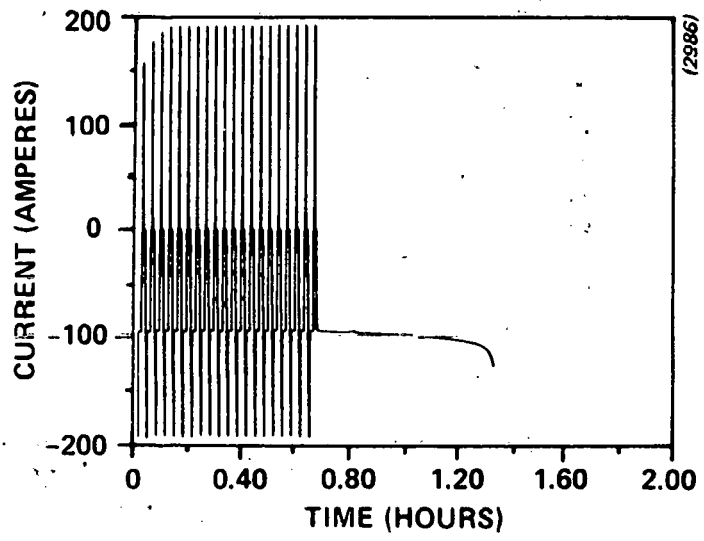


Figure 2.C.5 Battery current vs. time for test F431S1031.D17

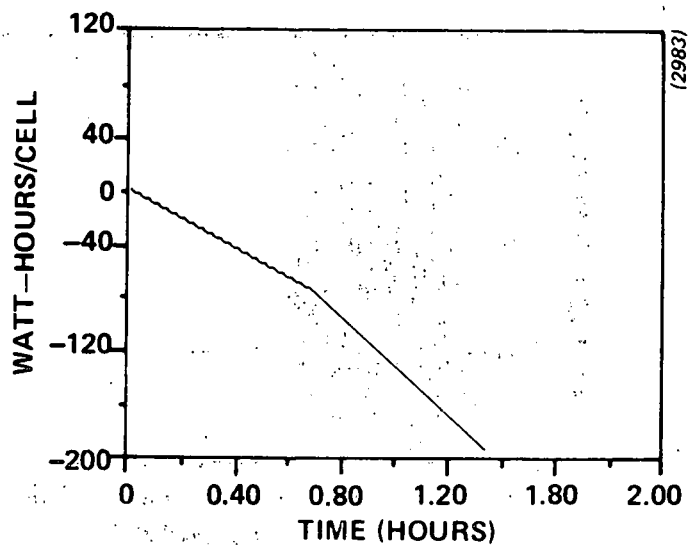


Figure 2.C.6 Battery watt-hours vs. time for test F43TST031.D17

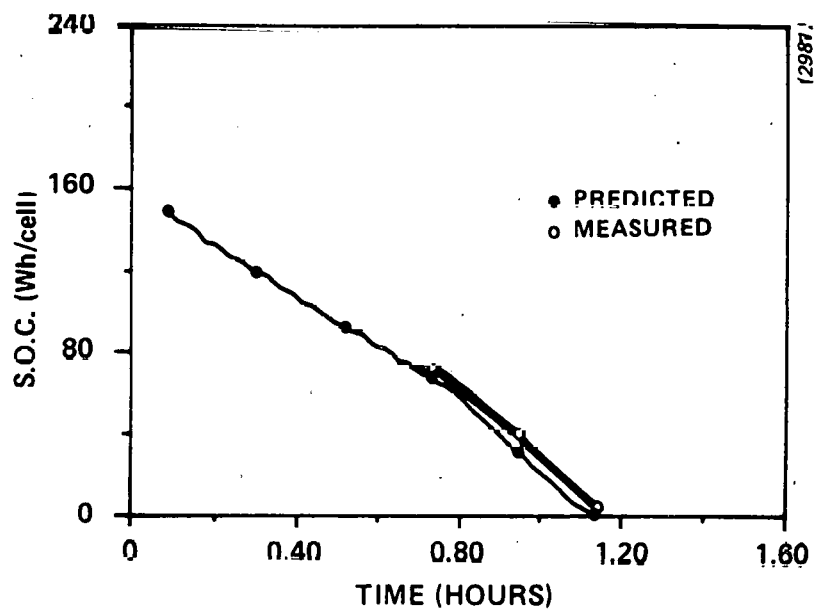


Figure 2.C.7 State-of-charge (S.O.C.) vs. time for test F49TST033.D05

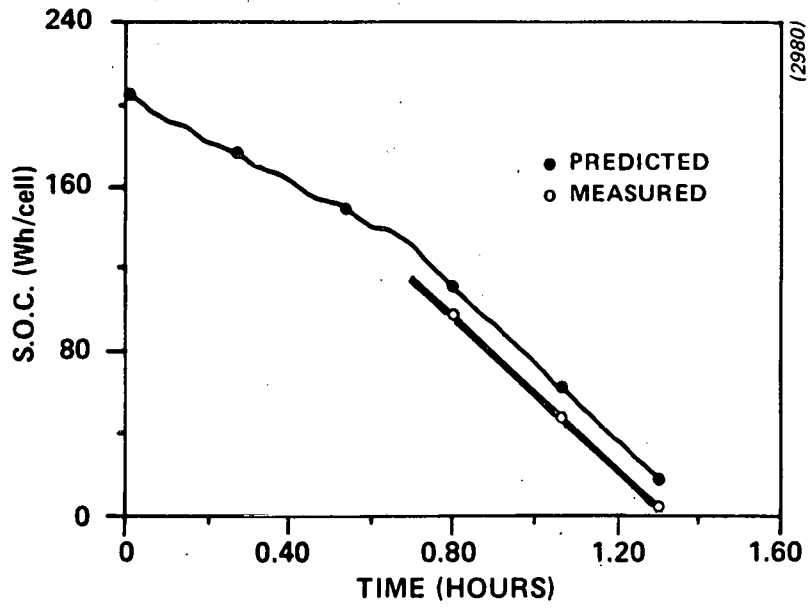
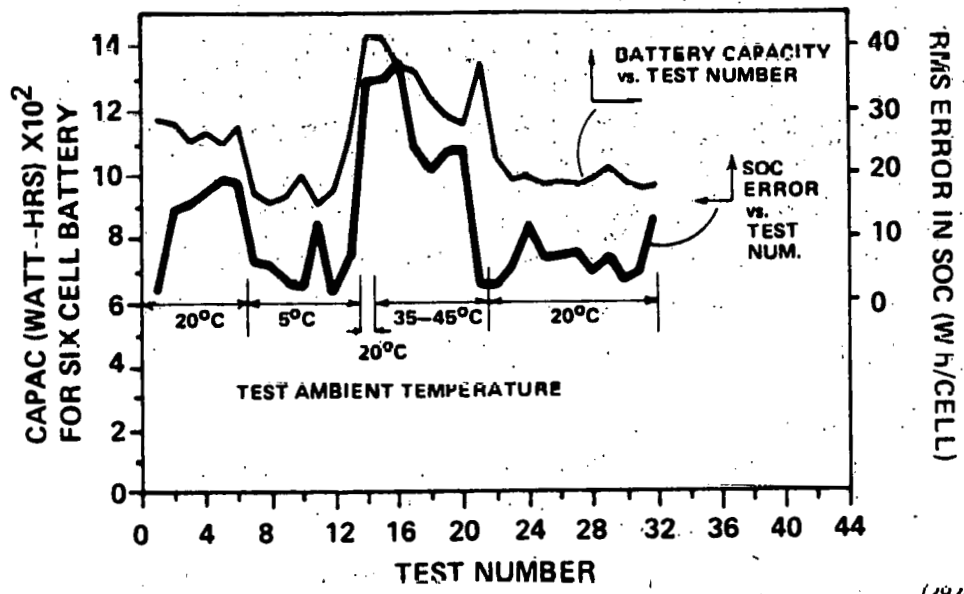


Figure 2.C.8 State-of-charge (S.O.C.) vs. time for test F43TST031.D17



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Figure 2.C.9 Battery capacity vs. test number and S.O.C. error vs. test number.

Table 2.C.2

SOC Evaluation Test and Results

| <u>TEST</u> | <u>RMS ERROR IN STATE OF CHARGE</u> |
|---------------|---|
| F43TST031.D16 | 2.05 |
| F43TST031.D17 | 14.43 |
| F43TST031.D18 | 15.40 |
| F45TST031.D19 | 17.48 |
| F45TST031.D20 | 19.03 |
| F47TST031.D21 | 18.67 |
| F47TST031.D22 | 6.63 |
| F47TST031.D23 | 7.19 |
| F47TST031.D24 | 3.26 |
| F49TST031.D25 | 2.12 |
| F49TST033.D05 | 8.50 |
| F49TST033.D06 | 1.28 |
| F49TST033.D07 | 7.33 |
| F51TST031.D26 | 34.77 |
| F51TST031.D27 | 34.99 |
| F51TST031.D28 | 37.27 |
| F51TST031.D29 | 24.56 |
| F53TST033.D08 | 20.67 |
| F53TST033.D09 | 23.67 |
| F53TST033.D10 | 24.23 |
| F53TST033.D11 | 2.58 |
| F55TST040.D23 | 2.94 |
| F55TST040.D23 | 6.34 |
| F55TST034.D01 | 12.45 |
| F55TST034.D02 | 7.07 |
| F55TST034.D03 | 7.76 |
| F55TST034.D04 | 8.30 |
| F55TST034.D05 | 5.21 |
| F57TST034.D06 | 7.69 |
| F57TST033.D13 | 3.49 |
| F57TST033.D14 | 4.96 |
| F57TST033.D15 | 12.99 |

The RMS error in the state of charge is calculated by observing the error between the measured and predicted capacity at a number of discrete points. The RMS error is calculated from these points using Equation 27.

$$\text{RMS}_{\text{error}} = \frac{1}{N} \sum_{n=1}^N (P_{\text{cac}}^{(n)} - P_{\text{act}}^{(n)})^2 \quad (27)$$

2.C.1.c Parameter Adapter

The accuracy of the phenomenological battery model is dependent on the accuracy of the Shepherd coefficients which characterize the battery performance over the range of temperature and current. Unfortunately, these parameters change as the battery ages. The parameter adaptation algorithm developed during the contract attempts to modify the Shepherd coefficients based on the recorded voltage error history of previous discharges. Conceptually, the parameter modification would occur following the completion of the discharge cycle. Although no parameter adaption algorithm was included in the developed BC/SCI hardware, this section discusses its development.

The concept of parameter adaption requires the processing of some form of record of a complete discharge rather than making decisions based upon short sub-divisions of a discharge cycle. The major disadvantage of such an approach is the amount of data compression required to fit a complete discharge record in the available microcomputer dynamic memory, on the order of 100 bytes.

The discharge summary is in the form of several separate records. Each record will describe the scheme's performance over a particular section of the discharge, during which the discharge operating point in (I,T) space, current and temperature, remained nominally within one zone. A record will be kept only if the amount of time elapsed (and/or charge removed) during the corresponding section is above some minimum value.

The accumulation of a record will be terminated (i.e., that record will be written into memory) and another started whenever,

- A) The discharge operating point leaves its "base zone" for longer than some specified time.
- B) The length of time (or amount of charge removed) during the interval becomes greater than some maximum value.

If a record is to be written, and insufficient space exists in memory to write the record, some means of evaluation of the record's "importance" will be used to determine whether or not to delete an already-written record.

Each record will consist of 6 entries, described below:

- 1) I_A - The average value of the filtered battery current during the section.
- 2) T_A - The average value of the filtered battery temperature during the section.
- 3) ΔR_A - The average value of the error in battery "impedance" prediction,

$$\Delta R \equiv \frac{V_m - V_p}{I} \quad (28)$$

where ΔR is the instantaneous error in battery impedance prediction, V_m is the measured battery voltage, V_p is the predicted battery voltage, and I is the (unfiltered) battery current.

$$\Delta R_A \equiv \frac{1}{\Delta Q} \int_{Q_i}^{Q_i + \Delta Q} \Delta R dQ \quad (29)$$

where ΔQ is the total amount of charge removed from the battery during the section, and Q_i is the charge removed from full-charged state.

- 4) ΔR_D - An "average" value of the derivative of error in battery impedance prediction with respect to charge removed.

$$\Delta R_D \equiv \frac{2}{\Delta Q} \left[\begin{array}{cc} Q_i + 1/2\Delta Q & Q_i + \Delta Q \\ - \int_{Q_i}^{Q_i + 1/2\Delta Q} \Delta R dQ & + \int_{Q_i + 1/2\Delta Q}^{Q_i + \Delta Q} \Delta R dQ \end{array} \right] \quad (30)$$

- 5) Q_i - The value of charge removed from the battery (relative to its fully-charged state) when the section began.

- 6) Q_f - The value of charge removed from the battery when the section ended where

$$Q_f = Q_i + \Delta Q \quad (31)$$

Given the values of ΔR_A and ΔR_D , along with Q_i and Q_f , a linear approximation to the error (ΔR) can be constructed as a function of Q in that section.

Suppose $\Delta R = A \cdot Q + B$

Then $\Delta R_A \equiv \frac{1}{\Delta Q} \int_{Q_i}^{Q_i + \Delta Q} \Delta R dQ$

and $\Delta R_A = A(Q_i + 1/2 \Delta Q) + B$ and from equation (30),
 $\Delta R_D = 1/2A \Delta Q$

Then, if the above equations are solved for A and B in terms of ΔR_A and ΔR_D ,

$$A = 2 \frac{\Delta R_D}{\Delta Q} \quad (32)$$

$$B = \Delta R_A - \Delta R_D - A Q_i \quad (33)$$

In order to adjust the battery parameters according to the data obtained in the records, the following procedure is used.

First, reconstruct the actual voltage profile during each section by assuming that each section can be modelled as a constant-current, constant-temperature discharge, at the current, I_A , and temperature, T_A .

Thus, the predicted battery voltage would be

$$V_p^\circ = V_0 - \left(\frac{V_1}{Q_1}\right)Q - R_1^\circ I_A - \left[\frac{R_2^\circ Q_2^\circ}{Q_2^\circ - Q} \right] I_A \quad (34)$$

where R_1° , R_2° , and Q_2° are the values of R_1 , R_2 , and Q_2 at the point (I_A , T_A), before any adjustment.

V_p° is the voltage predicted by the un-adjusted parameters.

From this information, and the linear approximation to the battery impedance as a function of charge removed, reconstruct the measured voltage during a section, since, by the definition of ΔR ,

$$\begin{aligned} V_m &= V_p^\circ + I_A \Delta R \\ &= V_p^\circ + I_A(A \cdot Q + B) \end{aligned} \quad (35)$$

where A and B are defined on the previous page.

Thus

$$\begin{aligned} V_m &= (V_0 - R_1^\circ I_A + B \cdot I_A) + \left(A \cdot I_A - \frac{V_1}{Q_1} \right) \cdot Q \\ &\quad - \frac{R_2^\circ Q_2^\circ I_A}{Q_2^\circ - Q} \end{aligned} \quad (36)$$

The predicted voltage, V_p , obtained by the use of adjusted parameters, R_1, R_2, Q_2 , is

$$V_p = V_0 - \left(\frac{V_1}{Q_1}\right) Q - R_1 I_A - \frac{R_2 Q_2 I_A}{Q_2 - Q} \quad (37)$$

The error, ΔR , with the adjusted voltage is, thus,

$$\begin{aligned} \Delta R &= (V_m - V_p)/I_A \\ &= B + \left[(R_1 - R_1^{\circ}) \right] + A \cdot Q + \frac{R_2 Q_2}{Q_2 - Q} - \frac{R_2^{\circ} Q_2^{\circ}}{Q_2^{\circ} - Q} \end{aligned} \quad (38)$$

The integral of the square of ΔR can be performed over all sections for which (I_A, T_A) is within a common zone. In this way, an increment to the parameters $\Delta R_1, \Delta R_2, \Delta Q_2$, which results in the lowest mean-squared error can be chosen (even though this increment results in different values of R_1, R_2, Q_2 for each different (I_A, T_A) in each section). Note that A and B are intermediate constants in the linearization process of curve fitting and are not minimized per se.

The change is distributed among the four operating corners which define the (I, T) zone in the following manner.

The change in the interpolated value of R_1 (obtained by use of the average operating point, (I_A, T_A)) is a fraction of the recommended change, ΔR , thus,

$$\Delta R_1^{LL} \cdot F_{LL} + \Delta R_1^{LU} \cdot F_{LU} + \Delta R_1^{UL} \cdot F_{UL} + \Delta R_1^{UU} \cdot F_{UU} = \text{FRACT} \cdot \Delta R_1 \quad (39)$$

The solution to the set of equations is

$$\Delta R_1^{LL} = \text{FRACT} \cdot F_{LL} \cdot \Delta R_1 / M \quad (40)$$

$$\Delta R_1^{LU} = \text{FRACT} \cdot F_{LU} \cdot \Delta R_1 / M \quad (41)$$

$$\Delta R_1^{UL} = \text{FRACT} \cdot F_{UL} \cdot \Delta R_1 / M \quad (42)$$

$$\Delta R_1^{UU} = \text{FRACT} \cdot F_{UU} \cdot \Delta R_1 / M \quad (43)$$

where

$$M \equiv 1 - 2 \cdot \Delta_I \cdot (1 - \Delta_I) - 2 \cdot \Delta_T \cdot (1 - \Delta_T) \quad (44)$$

$$+ 4 \cdot \Delta_I \cdot \Delta_T \cdot (1 - \Delta_I) \cdot (1 - \Delta_T)$$

and where

ΔR_1^{LL} is the change to be made in R_1 at the low-current, low-temperature corner of the zone

ΔR_1^{LU} is the change for the low-current, high-temperature corner

ΔR_1^{UL} is the change for the high-current, low-temperature corner

ΔR_1^{UU} is the change for the high-current, high-temperature corner

ΔR_1 is the optional suggested change in R_1 for the zone

Δ_I is the ratio of zone changes in current based on the geometric mean of the grid.

Δ_T is the ratio of zone changes in temperature based on the geometric mean of the grid.

FRACT is a constant such that $0.5 < \text{FRACT} < 1.0$.

and where F_{IJ} is defined as,

$$F_{LL} = (1-\Delta_I) (1-\Delta_T)$$

$$F_{LU} = (1-\Delta_I) \Delta_T$$

$$F_{UL} = \Delta_I(1-\Delta_T)$$

$$F_{UU} = \Delta_I \Delta_T$$

The concept of the parameters adapter was tested by examining a dc discharge at a constant current of 100A and 22.5°C. Two parameter grids were employed for the Shepard coefficients, a 5x3 matrix and a 4x3 matrix to determine the impact of having the operating point coincide exactly with a grid entry. Figure 2.C.10 shows the variations of R1 and Q2 using the 5x3 matrix. As shown in this Figure, Q2 seems to be stable with repeated operations on one data file; however, R1 seems headed up indefinitely.

However, when the 4x3 matrix was employed, the parameter converged on a final set in only 10 iterations. Figures 2.C.11 and 2.C.12 show the predicted and measured voltage curves for the initial iteration and the 10th iteration.

The sensitivity to the nearness of the (I,T) grid point is an area of concern in the parameter adapter strategy.

2.C.2 Physical Model

The physical model is a mathematical representation of the discharge process in a flooded, porous, lead-acid battery cell. It is a lumped-parameter approximation to the classic macrohomogeneous model (Reference 4). The battery characteristics most strongly emphasized are (1) limitations of

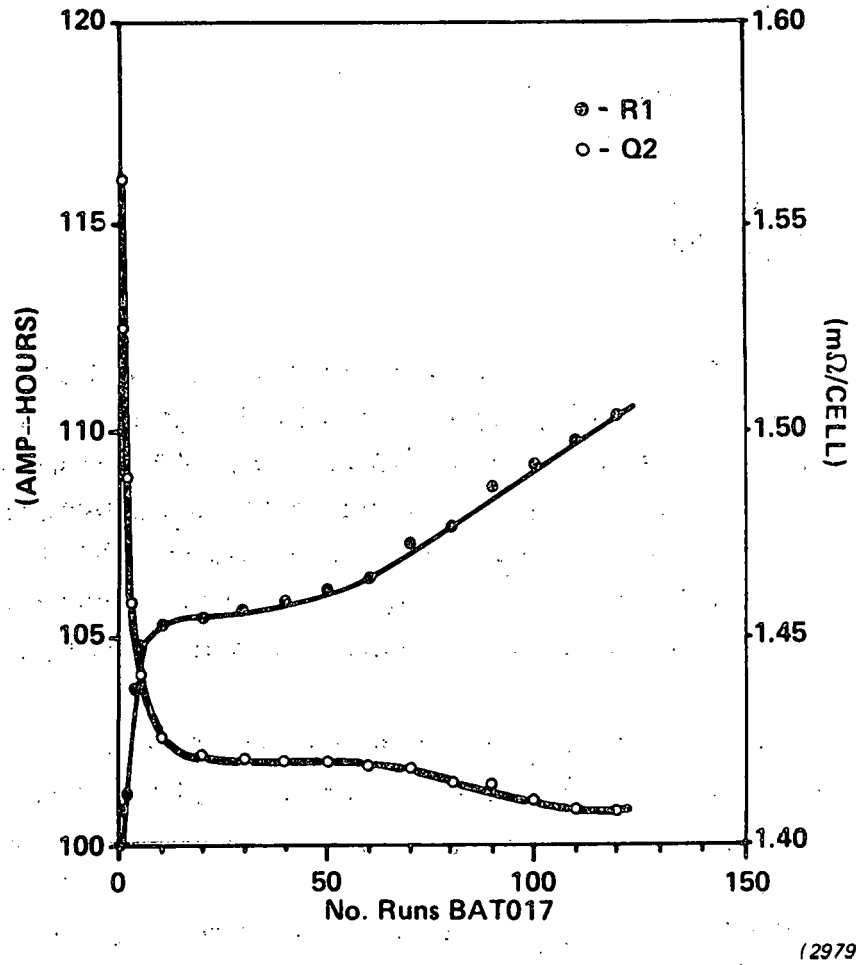


Figure 2.C.10 Variation of battery parameters, R₁, Q₂, with runs of parameter - adaptor, BAT017.

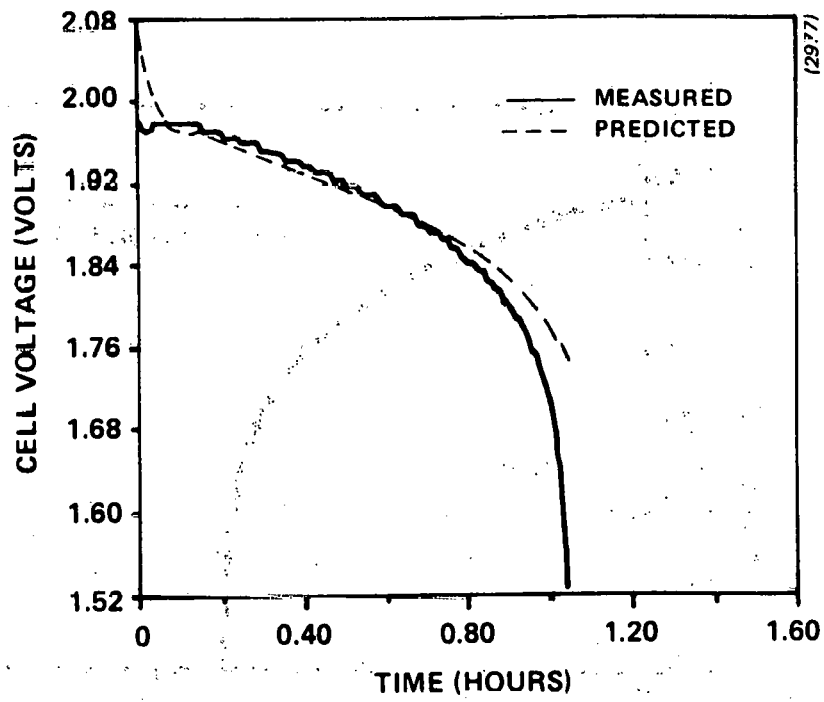


Figure 2.C.11 Predicted and measured battery voltage, test F27TST016.D01

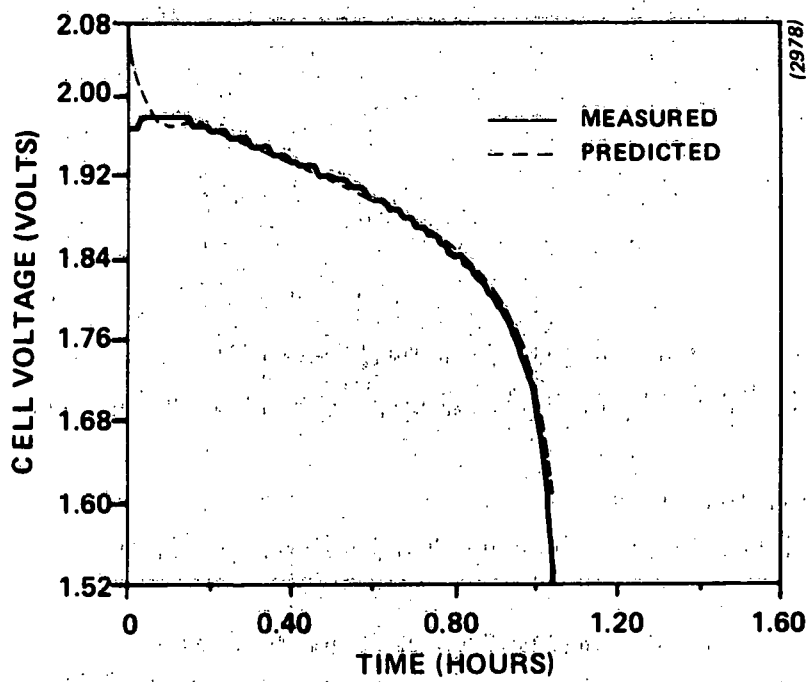


Figure 2.C.12 Predicted and measured battery voltage, test F27TST016.D01

battery charge, (2) effects of finite electrolyte diffusion rate, and (3) effects of pore-plugging on battery impedance and electrolyte diffusion.

2.C.2.a Macrohomogeneous Model for Porous Electrodes

A porous electrode is simply a rigid material with many pathways (or pores) through which a fluid may pass. The major advantage in using a porous electrode in place of a solid one for surface reactions is the much larger effective surface area afforded by the porosity. In order to obtain the same surface area to volume ratio with solid plates, one would have to use a plate thickness on the order of the pore dimensions, $\sim 1 \mu\text{m}$ for a typical lead-acid cell. Such plate thicknesses are impractical, from both economic and structural standpoints.

Unfortunately, it is this same porous nature of the lead-acid cell electrode that makes an exact analysis of the reactions and flows involved in a battery discharge very difficult, if not impossible. The approach of some researchers has been to model the pores as straight, cylindrical inclusions, perpendicular to the electrode surface (Reference 5).

A more popular approach is the macrohomogeneous model, in which the porous nature of the electrode is accounted for by treating the grid (electrode material) and fluid (electrolyte) as two separate, continuous phases that co-exist in the volume occupied by the electrode (Reference 4). The grid is modelled as a solid material whose effective conductivity and heat capacity are dependent upon the porosity (void factor), ϵ , as well as its material composition. The electrolyte is modelled as a continuous fluid media with acid concentration, temperature, and fluid velocity a function of position within the electrode. The fluid viscosity, conductivity, and diffusion coefficient are dependent upon the porosity. Since the current-producing electrochemical reaction in a lead-acid battery consumes either lead or lead-dioxide and produces lead sulfate (lower in density than either of the solid reactants), the electrode porosity can change during the course of a discharge, being itself, a function of both position and time.

For most analyses, the battery discharge is modelled as a one-dimensional process, even though this ignores some effects of the two-dimensional nature of the electrode structure (see Figure 2.C.13). Figure 2.C.14 shows a typical cell model. The cell consists of two porous electrodes (hash-marked areas in Figure 2.C.14) bounding a separator region. Contacts placed on either end of the cell supply and receive battery currents. The electrolyte fills all three regions. For a cell at rest, the electrolyte concentration in the aqueous solution is uniform. In addition, it is generally assumed that, for a fully-charged cell at rest, the distribution of active material (lead, at the negative electrode, lead-dioxide, at the positive electrode) is uniform as well.

When the cell is loaded (i.e., when current is drawn), the rate of electrochemical reaction within the cell is not uniform. Of course, no reaction occurs in the separator region, so the electrolyte concentration there goes down only due to diffusion into either electrode. At very low discharge rates, the reaction initially occurs evenly throughout both electrodes, so that the rate of usage of lead (or lead dioxide) and sulfuric acid, as well as the production of lead sulfate, is not a function of position for the early part of the discharge. At higher discharge rates, the reaction tends to be skewed towards the front face of each electrode (near the separator) due mainly to the lower voltage drop suffered by currents traveling most of the way across the electrode via the (highly conducting) grid material. This causes non-uniform usage of both active materials and electrolyte resulting in concentration gradients of these substances within the electrode. Although the unused active material cannot move through the electrode, the electrolyte is able to diffuse from regions of higher concentration to those where it is low. Thus, even if the battery is not being discharged, the concentration profile of electrolyte in the electrode may not be static.

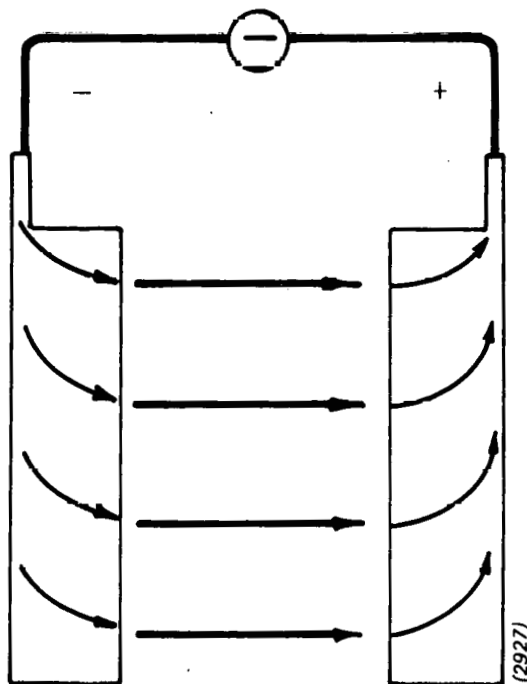
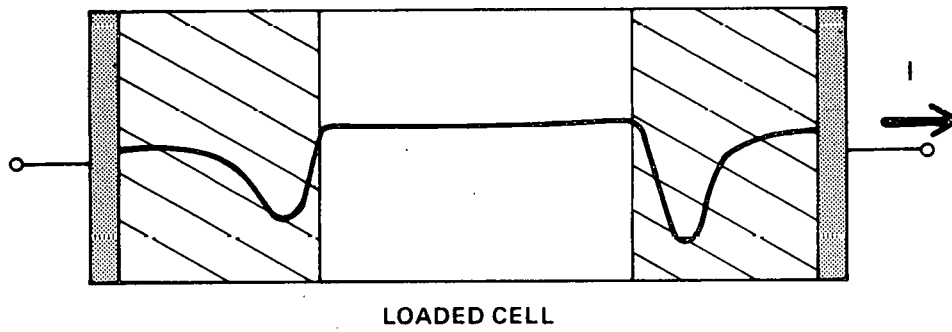
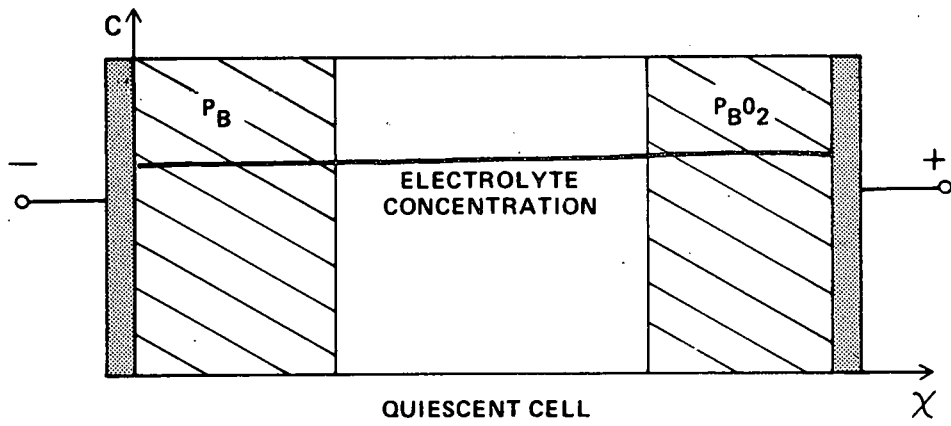


Figure 2.C.13 Lines of current flow in lead-acid battery cell. Location of tabs at top of cell results in two-dimensional dependence of current-density in electrodes.



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Figure 2.C.14 One-dimensional macrohomogeneous model for lead-acid battery cell

The electric potential and current density can be separate functions of time and position for each of the co-existing phases. The difference between grid and electrolyte potentials at any particular point in the electrode is simply the voltage drop across the Debye charge-layer at the solid-liquid interface at that point. The two current densities are constrained such that the divergence of their sum is zero (i.e., whatever current leaves one phase enters the other, except at the electrode boundaries). In all, the one-dimensional macrohomogeneous model contains at least nine space/time dependent quantities, summarized in Table 2.C.3. The list can grow even longer if all of the various possible ionic species are to be accounted for separately.

Even if the differential equations governing the changes in these quantities, with time, were known exactly, the complexity of this set would prevent its integration on any but the fastest presently available computers. In addition, not enough is yet known about the electrochemistry of lead-acid batteries to confidently specify all of the interrelationships between those nine variables. For example, the rate at which current is transferred from the solid phase to the electrolyte phase, $-v_i_2$, is a function of the solid-electrolyte potential difference, $\phi_2 - \phi_1$, the local electrolyte concentration, C , and the amount of available active material, either S^+ or S^- . Normally, the dependence of this current derivative on C and S^+ is lumped into an empirical constant in an equation as shown below,

$$v_i_2 = j_0(C, S^\pm) \cdot e^{\frac{\phi_2 - \phi_1}{V_1}} - e^{-\frac{\phi_2 - \phi_1}{V_2}} \quad (45)$$

where V_1 and V_2 are some characteristic potentials of the chemical system. Very little is written in the literature about the dependence of j_0 on either C or S^\pm , and more often than not, j_0 is made a constant for the purposes of analysis.

Table 2.C.3

List of space/time dependent variables involved
in macrohomogeneous model for battery cell.

SPACE/TIME - DEPENDENT PARAMETERS.

- C - Electrolyte ($\text{SO}_4^{=}$) Concentration
- S+ - Positive Active Material (PbO_2) Concentration
- S- - Negative Active Material (Pb) Concentration
- T - Temperature
- ϕ_1 - Electric Potential in Solid Phase (Electrode)
- ϕ_2 - Electric Potential in Liquid Phase (Electrolyte)
- ϵ - Electrode Porosity
- I_1 - Current Density in Solid Phase
- I_2 - Current Density in Liquid Phase
- j_0 - Exchange Current Density

Clearly, some approximations are necessary in order to perform a simulation of the discharge process in a lead-acid battery cell; first, in the face of unavailable information, and second, to allow processing of the equations with a reasonable amount of computer time and memory storage.

Such a set of reasonable approximations and assumptions was proposed by Simonsson in 1973 (Reference 6). Among his more important assumptions were (1) an isothermal system, (2) complete disassociation of the electrolyte into only one positive and one negative ionic species (H and HSO, respectively), and (3) the "Tafel" assumption, in which the current derivative is approximated by an exponential in the Debye-layer overpotential,

$$\frac{\partial i_2}{\partial x} = j_0 \cdot S \cdot e^{-\frac{2F}{RT} \eta} \quad (46)$$

where i is the current density in the electrolyte, j_0 is the exchange current density (assumed constant), and η is the Debye layer overpotential (Reference 7), defined by,

$$\eta \equiv (\phi_2 - \phi_1) - \phi_0 \quad (47)$$

where ϕ_0 is the equilibrium potential drop across the Debye layer (in the absence of any currents).

With these simplifications, Simonsson integrated the set of differential equations governing the discharge process to obtain some insight into how a porous lead-acid battery cell becomes exhausted before all of the reactants are used up. One of the more significant conclusions that he reached was that, for high discharge currents, the skewing of the discharge reaction density towards the front face of the electrode caused the active material there to be used up first forming a "dead-zone" in the electrode which propagated towards the back face. Any electrolyte which diffused from the separator region to the point in the electrode where the reaction was occurring would have to diffuse across this dead-zone.

In addition, Simonsson suggested that the end of discharge probably occurred when a very low electrolyte concentration, somewhere in the electrode, caused the impedance to become very large.

It is these two conclusions upon which the physical model, a lumped-parameter approximation to Simonsson's continuous model, is built. In the following section, the concepts of a dead-zone, across which battery current must flow and electrolyte must diffuse, propagating across the electrode and a battery impedance which depends strongly upon the concentration of electrolyte in the electrode are developed into a simplified model which could be implemented on a microprocessor with limited storage capabilities.

2.C.2.b Presentation of Physical Model

The physical model represents the state of a porous-electrode lead-acid battery cell with three variables. They are:

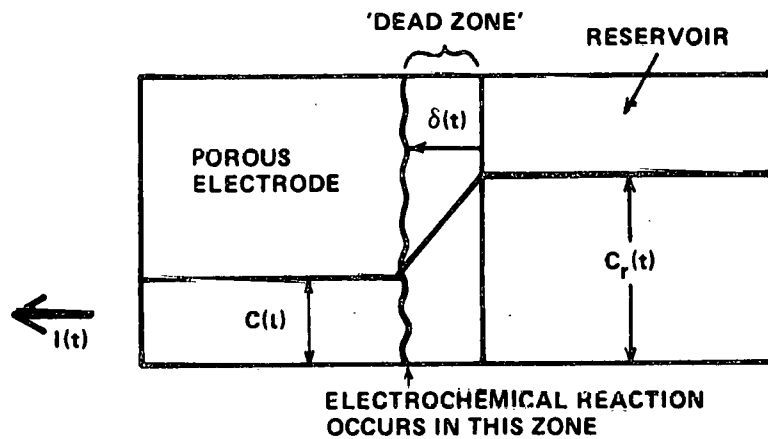
- 1) $C(t)$ The concentration of electrolyte within the electrode.
- 2) $C_r(t)$ The concentration of electrolyte outside the electrode (in either the separator region or the reservoir).
- 3) $\delta(t)$ The width of a "dead-zone" of used (or passivated) active material in the electrode.

Figure 2.C.15 gives a graphic illustration of the meaning of these variables. The differential state equations which govern changes in the variables are

$$\frac{d}{dt} \{CLA\} = -kA(C-C_r)/\delta - I/F \quad (48)$$

$$\frac{d}{dt} \{\Delta C_r V_r\} = kA(C-C_r)/\delta \quad (49)$$

$$\frac{d\delta}{dt} = \frac{L}{Q_0} \cdot I \cdot f(I) \quad (50)$$



(2930)

Figure 2.C.15 Schematic illustration of physical model for lead-acid battery cell, showing definitions of state-variables, C , C_r , δ .

where

L is the effective thickness of the electrode.

Q_0 is the total (charge equivalent of) active material content of the electrode.

A is the electrode apparent cross-sectional area.

k is the effective electrolyte diffusion coefficient through the porous electrode (k can be a function of temperature).

I is the battery current.

F is Faraday's constant.

V_r is the effective volume of the reservoir and separator regions outside the electrode.

f is an empirically-fitted function of the battery current, I, whose value approaches 1 as $I \rightarrow 0$. (For $I > 0$, $f(I) > \text{or} = 1$).

Briefly, the electrolyte content of the electrode is seen to change due to either diffusion from the reservoir or the current-producing electrochemical reaction. The reservoir electrolyte content changes only by diffusion to or from the electrode. The dead zone grows at a rate that is at least proportional to the rate of usage of active material and faster than that for large currents. As the dead zone width grows, the impedance to diffusion between the electrode and reservoir increases. The battery terminal relation is

$$V = V_{OC}(C) - R(\delta, C, C_r) \cdot I \quad (51)$$

where $V_{oc}(C)$ is the open-circuit battery voltage, and $R(\delta, C, C_r)$ is the battery impedance. It should be noted here that the open-circuit battery voltage is a function of the electrolyte concentration in the electrode only and not of δ or C_r . This is due to the fact that the potential of an unloaded battery depends only upon the voltage drop across the Debye layer at the solid-liquid interface which is determined primarily by the acid concentration there.

The battery impedance can, in general, depend on all three state variables. One possible functional dependence for $R(\delta, C, C_r)$ is

$$R = R_a + R_b \frac{\delta C_0}{L C} \quad (52)$$

where R_a , R_b , C_0 are constants. This expression ignores the effects of electrolyte concentration in the reservoir on the battery impedance and predicts that the impedance rises linearly with the dead zone width and in inverse proportion to the acid concentration in the electrode. It is likely that R_a and R_b would have to be temperature-dependent to correctly model the battery's terminal behavior over a wide range of conditions.

With initial conditions for C , C_r , and δ ; the state equations, Equations 48, 49, and 50, a fully-specified terminal relation, Equation 51, and the driving functions, $I(t)$ and $T(t)$, this model can be used to predict the battery terminal voltage as a function of time. Given values of the state variables at any time, a simulated constant-power discharge could be used to predict the time to cutoff, and thus, the remaining available energy of the battery.

2.C.2.c Discussion of Model Characteristics

As was stated in the introduction to this chapter, the physical model stresses battery capacity limitations of total battery charge, finite electrolyte diffusion rate, and electrode pore-plugging. The discussion to follow is intended to point out those characteristics of the model which demonstrate such effects.

Electrolyte can leave the entire system consisting of the electrode plus reservoir only through effects of the last term in Equation 48 due to the battery current drawn. In fact, a linear combination of Equations 48 and 49 yields a statement of conservation of charge

$$\frac{d}{dt} \frac{Q}{F} \equiv \frac{d}{dt} \{CLA + C_r V_r\} = - \frac{I}{F} \quad (53)$$

where the first equality above may be taken as a definition of Q , the relative battery charge. If Q is given a value of zero when both C and C_r are zero, then Q may be thought of as the absolute total battery content of (charge-equivalent) electrolyte. Since the electrode and reservoir start with a finite quantity of electrolyte, certainly no more than Q_i , the initial value of Q can be removed from the battery before either C or C_r becomes negative. Thus the model places a limit on the battery capacity based on the total charge-equivalent of electrolyte initially available.

If the battery is initially at rest (so that $C \equiv C_r$) and a dc discharge begun, C will fall below C_r . Assuming that $V_{OC}(C)$ is a monotonically-rising function of C , the open-circuit voltage predicted by the model will be lower than the voltage predicted for a battery at rest with the same amount of charge removed. In fact, if the discharge were stopped suddenly, C would rise (due to the diffusion term in Equation 48) towards an asymptotic value equal to the volume-average concentration in the entire cell. This could be observed from the battery terminals as a voltage transient occurring when the discharge was halted. Both of these model characteristics, depressed electrolyte concentration in the electrode under load and voltage transients

accompanying changing loads, are intended to account for effects of the finite rate of diffusion of electrolyte in a battery cell.

As a discharge proceeds, the width of the dead zone in the electrode, δ , increases. This has two effects on the model equations. First, the rate of diffusion from reservoir to electrode falls, as it is inversely proportional to δ . Second, the battery impedance rises. Both of these phenomena occur in order to account for the fact that the porosity is reduced in those regions where the current-producing electrochemical reaction has occurred. This reduction in porosity is simply due to the fact that the reaction product, lead-sulphate, is lower in density than either lead or lead-dioxide and thus takes up more space than these reactants. In most macrohomogeneous models, the electrolyte conductivity and diffusion coefficients are assumed to be proportional to the electrode void fraction. For the physical model, the only impedance to electrolyte diffusion is the (pore-plugged) dead zone. In the terminal relation proposed by Equations 51 and 52, the battery resistance has one term proportional to the dead zone width, and another that is independent of δ . This later term could account for fixed (terminal, grid) battery impedances. If desired, a third term, varying in inverse proportion to C_r , could be added to account for voltage drops across the separator region.

According to Simonsson's (Reference 6) conclusions, the discharge reaction may be thought of as always taking place at the front edge of the dead zone in a thin 'reaction layer' which propagates across the electrode. If it were assumed that the reaction completely used up all of the active material in one plane before moving on to the next, then the rate of growth of the dead zone would always be proportional to the battery current, I . The multiplier, $f(I)$, in Equation 50 causes the growth rate, $d\delta/dt$, to be proportional to I only for small currents. As the battery current grows, $d\delta/dt$ rises more quickly than I . This is intended to account for a phenomenon known as electrode passivation in which high discharge current densities can presumably cause lead-sulphate deposits to cover unused active material in the electrode so that it cannot be accessed for later discharge. Such passivated active material can be recovered only by recharging the cell.

The physical model actually goes beyond most macrohomogeneous models in that it attempts to predict the battery terminal behavior on the basis of a half-cell representation. Even though the electrochemical reactions occurring in the positive and negative battery electrodes are very different, it is the opinion of the author that they can be modelled by a single-electrode process. It is thus assumed, for the purposes of the model, that a perfect ohmic contact capable of lossless transfer of ionic to electronic current exists at the far end of the separator region. Such an assumption leaves out the possibility of separate time constants or impedances for the two electrodes. The approximation is justified by the generally accepted observation in the literature that the battery capacity is most often limited by one of the two electrodes (specifically, the positive one, PbO_2).

Analysis of Model Equations

For the purposes of mathematical analysis, it is convenient to deal with a transformed set of state variables. The dead zone width, δ , is still used, but C and C_r are replaced by Q and D , defined as

$$Q \equiv CLA + C_r V_r \quad (54)$$

$$D \equiv C_r - C \quad (55)$$

Note that Q is the same quantity that was referred to earlier as the total battery charge-equivalent content of electrolyte henceforth referred to as simply the battery charge. D is equal to the difference between electrolyte concentration in the reservoir and electrode. It may be thought of as a measure of the battery "disturbance", since $D=0$ for a battery in its equilibrium state. Transformation of Equations 48 and 49 yields

$$\frac{dQ}{dt} = - \frac{I}{F} \quad (56)$$

$$\frac{dD}{dt} = - \frac{k}{L} \left[1 + \frac{LA}{V_r} \right] \frac{D}{\delta} + \frac{I}{FAL} \quad (57)$$

Equation 56 is, as before, merely a statement of conservation of charge (actually, it is conservation of mass for the electrolyte ions). According to Equation 57, the disturbance, D , of the battery cell would always tend towards zero were it not for the driving term, $I/(FA)$, on the right hand side of the equation. It is not a constant-coefficient differential equation as δ can be a function of time.

At any time that values for C and C_r are desired (i.e., to compute the terminal voltage), Equations 54 and 55 may be inverted, yielding

$$C = \frac{Q - DV_r}{LA + Vr} \quad (58)$$

$$C_r = \frac{Q + DLA}{LA + Vr} \quad (59)$$

Before any further analysis, it is useful to introduce some normalizations.

$$Q = C_0 L A F \underline{Q} \quad (60)$$

$$D = C_0 \underline{D} \quad (61)$$

$$\delta = L \underline{\delta} \quad (62)$$

$$C = C_0 \underline{C} \quad (63)$$

$$C_r = C_0 \underline{C}_r \quad (64)$$

$$t = \tau \underline{t} \quad (65)$$

$$I = I_0 \underline{I} \quad (66)$$

where

$$I_0 = (C_0 * L * A * F / \tau) \quad (67)$$

$$\tau = L^2 / k \quad (68)$$

The constant, τ , is a battery time constant, the characteristic electrolyte diffusion time, determined by the electrode thickness and electrolyte diffusion coefficient. The current, I_0 , is the ratio of the electrolyte charge-equivalent contained in a fully charged electrode to this time constant. The concentration, C , is taken as the initial electrolyte concentration in a fully-charged battery cell. Note that the current, I_0 , may be thought of as the current necessary to fully use up all of the electrolyte contained in the electrode initially in a single battery time constant, τ . With this normalization, Equations 50, 56, and 57 become

$$\frac{dQ}{dt} = - I \quad (69)$$

$$\frac{dD}{dt} + (1 + K_2) \frac{D}{\delta} = I \quad (70)$$

$$\frac{d\delta}{dt} = \frac{1}{K_1} I f'(I) \quad (71)$$

where

$$K_1 \equiv \frac{Q_0}{C_0 L A F} \quad (72)$$

$$K_2 \equiv LA / V_r \quad (73)$$

The function $f'(I)$ is simply $f(I)$ modified to accept t as its argument. K_1 is the ratio of charge-equivalent of active material to charge-equivalent of electrolyte contained in a fully charged electrode. K_2 is the ratio of effective electrode volume to that of the reservoir.

The above equations will be solved, subject to the initial conditions,

$$\frac{\delta}{\underline{t}=0} = \delta_1 \quad (74)$$

$$\frac{Q}{\underline{t}=0} = Q_1 \quad (75)$$

$$\frac{D}{\underline{t}=0} = D_1 \quad (76)$$

and with the driving function

$$\underline{I}(\underline{t}) = I_{dc} \quad (77)$$

That is, the model equations will be solved, below, for the case of a dc discharge.

Actually, the solution of Equations 69 and 71 is simple and requires no explanation.

$$Q(\underline{t}) = Q_1 - I_{dc} \cdot \underline{t} \quad (78)$$

$$\frac{\delta(\underline{t})}{\underline{t}} = \delta_1 + \frac{1}{K_1} I_{dc} \cdot f'(I_{dc}) \cdot \underline{t} \quad (79)$$

with the solution for $\frac{\delta(\underline{t})}{\underline{t}}$, Equation 70 becomes

$$\frac{dD}{d\underline{t}} + B \frac{D}{1+\alpha\underline{t}} = I_{dc} \quad (80)$$

where

$$B = (1+K_2)/\delta_1 \quad (81)$$

$$\alpha = I_{dc} \cdot f'(I_{dc})/(\delta_1 \cdot K_1) \quad (82)$$

Since a general technique exists to solve equations of this type, the solution is simply presented.

$$\underline{D}(t) = D_1 \pm 1 + \alpha t \frac{-B/\alpha}{B+\alpha} + \frac{I_{dc}}{B+\alpha} \left[1 - (1 + \alpha t)^{-\frac{B}{\alpha} + 1} \right] \cdot (+ \alpha t) \quad (83)$$

In terms of \underline{Q} and \underline{D} ,

$$\underline{C} = \frac{K_2}{1+K_2} \underline{Q} - \frac{1}{1+K_2} \underline{D} \quad (84)$$

The normalization can be extended to the terminal relation. Using

$$\underline{V} = V_0 \underline{V} \quad (85)$$

$$V_{oc}(C) = V_0 \underline{V}_0(C) \quad (86)$$

$$R = R_0 r \quad (87)$$

$$R_a = R_0 r_a \quad (88)$$

$$R_b = R_0 r_b \quad (89)$$

where V_0 and R_0 are characteristic values for battery voltage and impedance, respectively,

$$\underline{V} = \underline{V}_C(C) - \lambda \cdot (r_a + r_b \frac{\delta}{C}) \cdot \underline{I} \quad (90)$$

where

$$\lambda \equiv R_0 I_0 / V_0 \quad (91)$$

λ is the ratio of the product of characteristic battery current and impedance to the characteristic cell voltage.

Given initial values for $\underline{\delta}$, \underline{D} , \underline{Q} , and a dc discharge current, I_{dc} (as well as all necessary battery parameters), Equations 78, 79, and 83 may be used to solve for $\underline{\delta}(t)$, $\underline{D}(t)$, and $\underline{Q}(t)$. Then, Equations 84 and 90 yield the

normalized battery voltage as a function of time. Once values for all of the constants are determined and a suitable cutoff voltage defined, the physical model solution above may be used to analytically predict the battery capacity as a function of current for dc discharges. Table 2.C.4 contains a brief summary of the battery parameter values required for such a discharge simulation.

Table 2.C.4
List of Battery Parameters and Functions Necessary for
Analytic Simulation of DC Discharge with Physical Model

| | |
|---------------------|---|
| I_{dc} | Normalized dc discharge current. |
| K_1 | Ratio of electrode active material charge-equivalent to electrolyte charge-equivalent contained in a fully-charged electrode. |
| K_2 | Ratio of effective electrode volume to reservoir volume. |
| δ_1 | Initial value for δ , dead zone width. |
| Q_1 | Initial value for Q , battery charge. |
| D_1 | Initial value for D , battery disturbance. |
| λ | Ratio of product of characteristic battery impedance and current to battery voltage. |
| V_{cut} | Normalized cutoff cell voltage. |
| $V_c(C)$ | Function specifying battery open-circuit voltage variation with C , electrolyte concentration in electrode. |
| $r(C, C_r, \delta)$ | Function specifying cell impedance variation with C , C_r and δ |

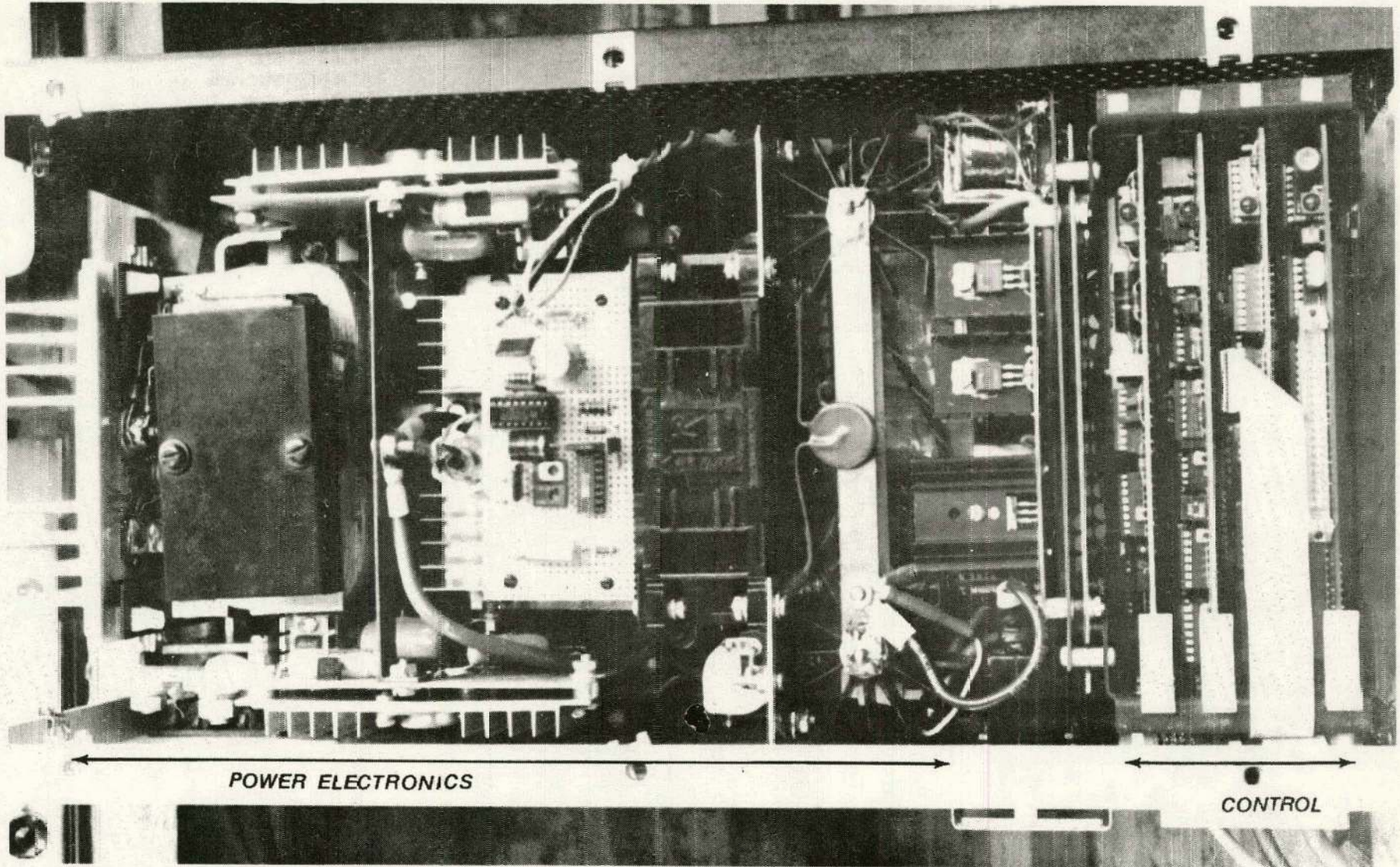
2.D Hardware Description/Operation

The operating features of the BC/SCI system are described herein. The power electronics is described with the aid of oscillographs of key operating points. The microcomputer system operation modes are discussed as well as the fault diagnostic features. Finally a mechanical summary including a weight distribution is presented.

2.D.1 Battery Charger Power Electronics

As discussed in Section 2.B, the battery charger stores energy in the boost inductor and then transforms it across the isolation transformer to the battery. Detailed electrical schematics of the power section are included in Appendix 1. Figure 2.D.1 is a photograph of the BC/SCI with the cover removed. The four control logic cards are on the right most side. The charger power circuit encompasses everything to the left of the card cage. Referring to Figure 2.D.2, an electrical schematic of the power circuit, the voltage across Q1 is illustrated in Figure 2.D.3. As seen in the oscillograph, the FET operates at a switching frequency of 40kHz. The voltage overshoot is a function of the energy stored in the leakage inductance and the snubber capacitor C2 in Figure 2.D.2. This overshoot is approximately 35V at a boost inductor currents of 15A. Figures 2.D.3 (a) and (b) are expansions of the voltage at turn off and turn on respectively. Switching speed of the device is < 100 ns.

Figure 2.D.4 is an oscillograph which shows the voltage across Q1 (V_{ds}) and Q2, Q3 (V_{ce}). The overshoot across the Darlington devices is minimal. The voltage appears as each Darlington at a 20kHz rate. Figure 2.D.5 is an oscillograph of the base voltage and the collector voltage of a Darlington transistor. As seen in the photo, base voltage is applied to the transistor when the collector voltage is held low by Q1. Similarly, the reverse voltage for turn off is applied after Q1 is re-gated. This strategy soft switches the Darlington transistors.

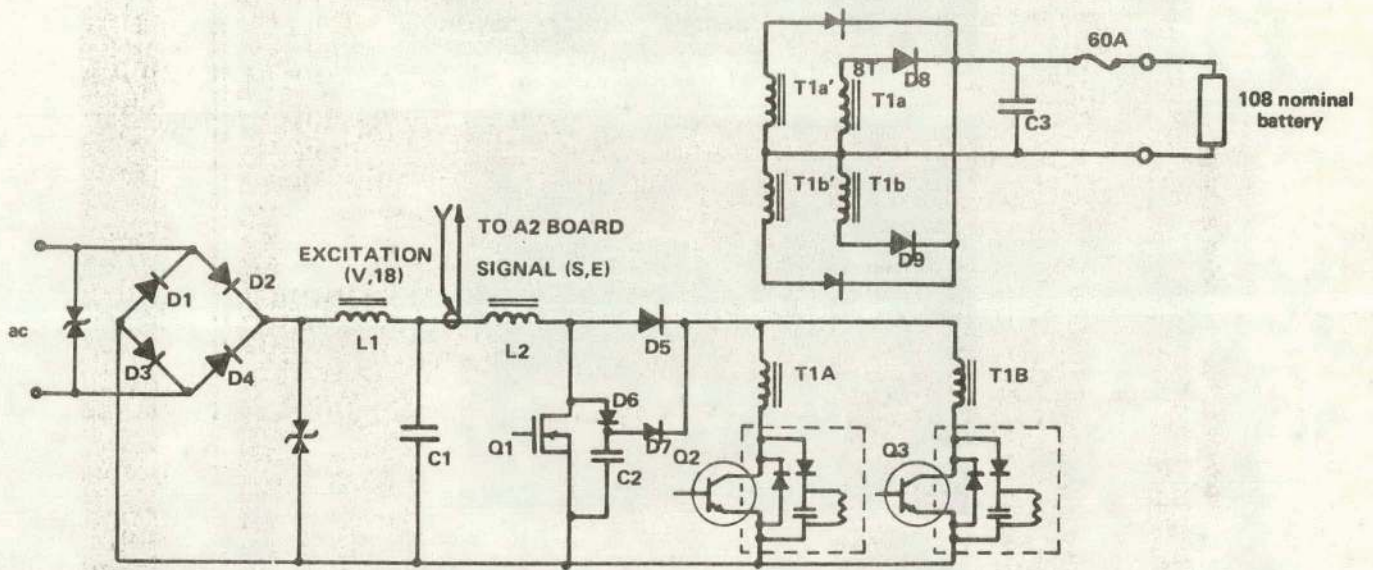


POWER ELECTRONICS

CONTROL

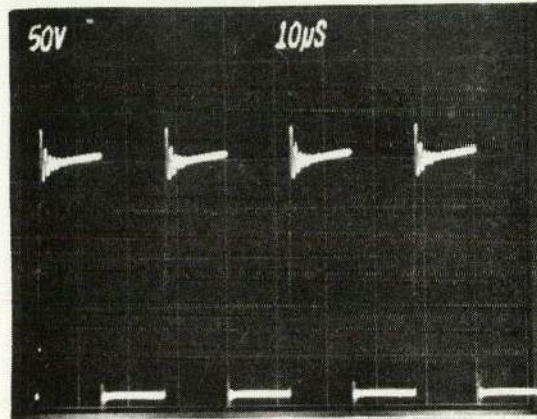
Figure 2.D.1

Top View of BC/SCI

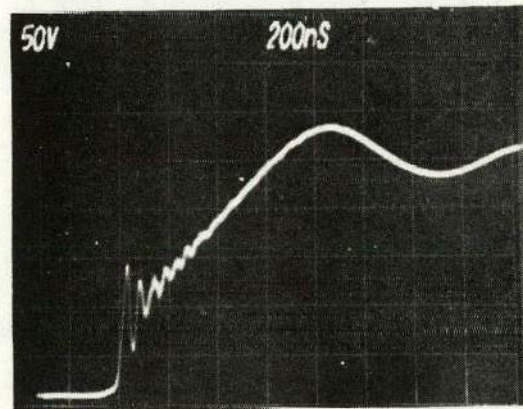


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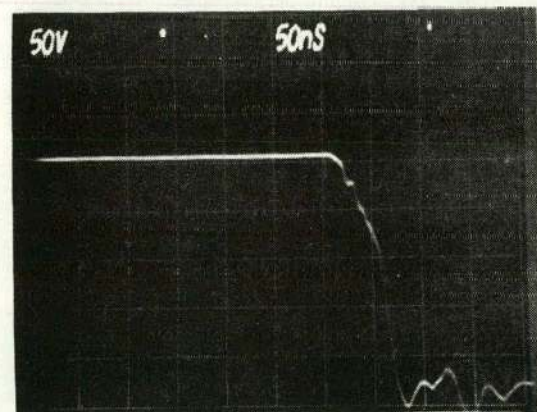
Figure 2.D.2 Simplified power circuit schematic



(a) VOLTAGE ACROSS FET
50V/div
10μs/div



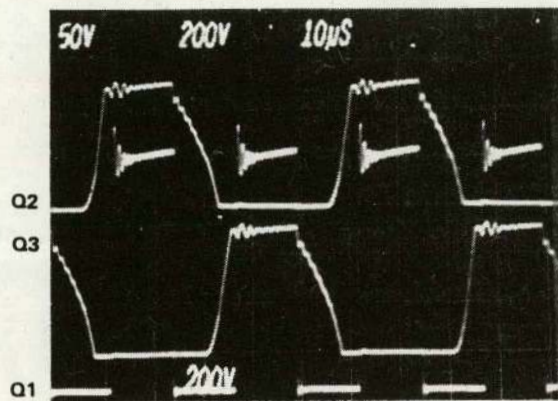
(b) VOLTAGE TURN-OFF
50V/div
200μs/div



(c) VOLTAGE TURN-ON
50V/div
50μs/div

(2963)

Figure 2.D.3 Voltage Across the FET, V_{DS} , when Charging a 108V Battery



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Figure 2.D.4 Voltages Q1, Q2, and Q3

Figure 2.D.6 shows the simultaneous voltages appearing on a Darlington transistor and the voltage clamp composed of the MR818 and RC network shown in Figure 2.D.2. The measurement point is the cathode of the MR818.

The oscillographs in Figure 2.D.3 - 2.D.6 were recorded with the converter operating at a fixed duty cycle. The remaining oscillographs illustrate the operation of the converter from the ac line with active waveshapping to emulate a resistive load.

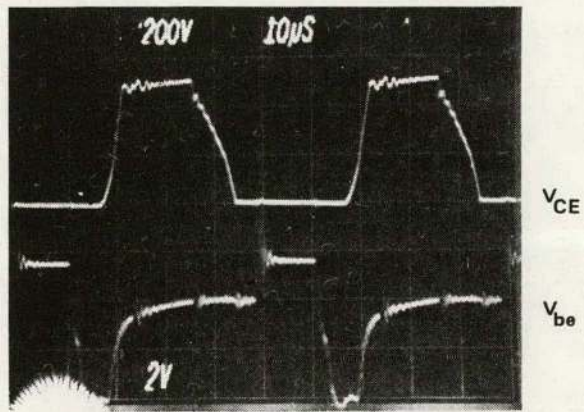
The current waveform drawn by the charger when operating at full power (1kW) is shown in Figure 2.D.7 (a). The oscillograph also records the input line voltage. The power factor is near unity. The peak current is 13A and is the larger amplitude trace in the figure. Figure 2.D.7 (b) contains the output current of the charger referenced to the ac line.

Figure 2.D.8 shows the voltage across Q1, Q2, with reference to the ac line current. As shown in the figure, both the duty cycle and the peak switch voltage is modulated with the charging current and line voltage.

It is interesting to note the effect of the switching power supply used to generate the control power for the power circuit on the ac line current waveform. The effect is shown in Figure 2.D.9, which is an oscillograph of the total input (ac line) current and its components, the switching power supply input current, and the input current to the charger power electronics. The input rectifier on the switching charger power supply contributes the current peaks to the BC/SCI ac line current. The top trace in Figure 2.D.9 should be compared to the ac line voltage shown in Figure 2.D.7 (b) to compare the waveshapping performance of the power electronics section.

2.D.2 Charger Control Electronics

The control electronics for the power section is self-contained and communicates with the microcomputer system via an optically-isolated digital bus. The power section and its power supply is referenced to the ac line



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Figure 2.D.5 V_{be} and V_{CE} of Darlington Transistor

while the microcomputer system is referenced to the vehicle battery's minus terminal.

The control electronics electrical schematic is shown in Figure 2.D.10. The main circuit functional blocks are identified in the following table with the aid of the Figure.

| Circuit Block | Function |
|---------------|--|
| 1 | Feedback Current Amplifier |
| 2 | Soft Start Circuit |
| 3 | Main System Error Amplifier |
| 4 | PWM Circuitry |
| 5 | Current Reference Circuitry |
| 6 | Line Soft Start Circuitry |
| 7 | Power Reset and Overcurrent Protection |

Fault protection in the controller is achieved by observing the feedback current and comparing it to a reference. In the event the threshold is exceeded, all switches are commanded open and a fault indication is set to the processor via U31 in Figure 2.D.10. Overcurrents in the boost inductor can be caused by the case when the peak line voltage exceeds the reflected battery voltage. For an ac input of 120 volts rms, this condition would occur should the actual battery voltage drop below 85 volts dc. There is no inherent protection for this condition since the battery voltage cannot be directly sensed (it is on the secondary side of the isolation transformer).

2.D.3 Microcomputer System Electronics

The BC/SCI low-power electronics has been designed to reside on three printed circuit boards. The first board (A1) is a low power switching power supply which generates the required microcomputer system voltages from the propulsion battery. The design employs a flyback regulator configuration

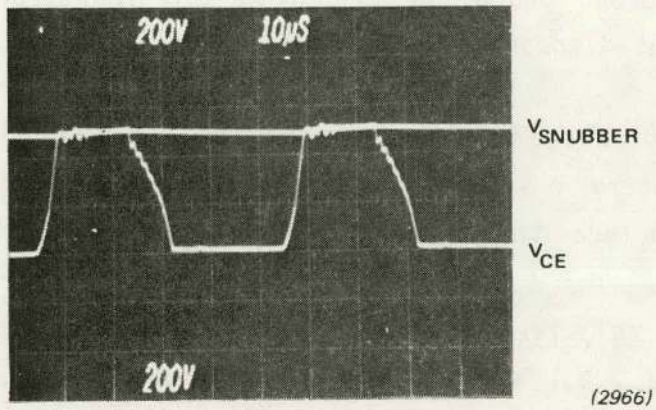


Figure 2.D.6 V_{CE} of Q1 and the Voltage Across the Snubber Clamp Connected in Parallel with the Darlington

utilizing a FET, torroidal transformer and standard PWM regulator I.C. Three outputs provide $\pm 5v$ and $+ 13.5V$.

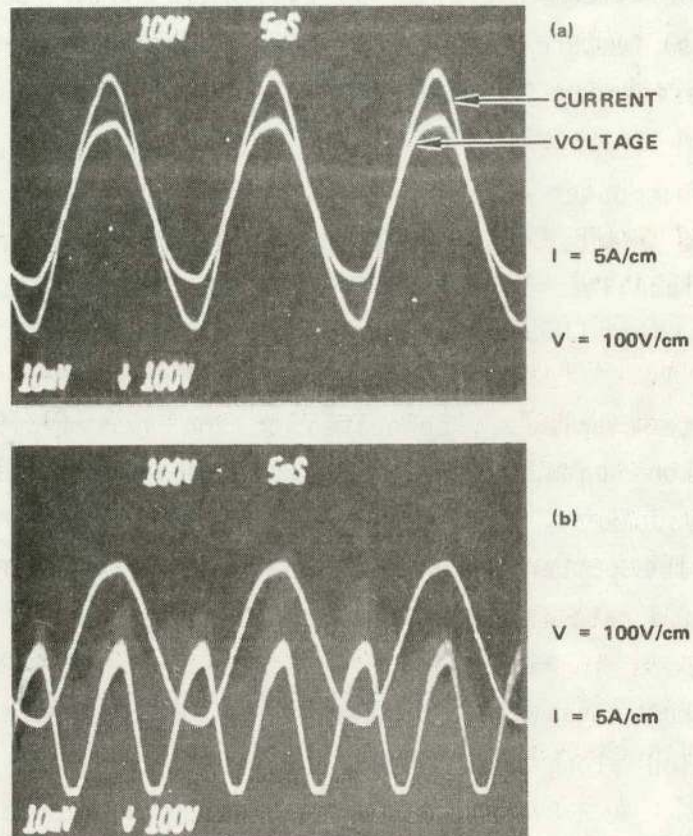
The supply can be enabled by one of three inputs. During battery discharging, an isolated set of switch contacts in the EV controller slave the SCI operation to the operation of the EV controller. During charging the supply is enabled when the power circuit switching power supply becomes energized. The last way in which the system is enabled is when the battery powered CMOS clock times out.

The second board (A2) provides the high frequency control of the BC power stage as discussed earlier.

The third board (A3) contains the signal conditioning circuitry. The critical battery parameters which are the feedback variables for the SOC algorithm include the battery voltage, current, temperature, and absolute ampere-hours. The design of the data acquisition circuitry controls both the absolute and relative error sources to achieve the confidence in the measured data. Table 2.D.1 summarizes these specifications. The absolute accuracy lists the maximum error associated with scaling, digitization and temperature variations from one SCI system to another. The relative accuracy is for measurements within the same system.

Additional inputs on the A3 board include the vehicle speed transducer interface, switch inputs, LED drivers and a digital control port to the power stage. One potentiometer is required and is used to trim the A/D's voltage reference when the board is initially constructed.

The final board in the system (A4) contains all the microcomputer circuitry. A MC6809 microprocessor with 16K of 8-bit EPROM and 2K of 8-bit CMOS RAM (TC5517AP) provide the basic nucleus of the design. A real time CMOS clock, a power-up reset circuit and a watch-dog timer complete the design. The CMOS RAM and clock are made non-volatile by a nickel-cadmium battery mounted on board A1. This battery is kept charged by a simple zener regulator off the propulsion battery. It will measure the CMOS RAM non-volatility under



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Figure 2.D.7 Charger Terminal Waveform
 (a) input voltage, input current
 (b) input voltage, output current

worst case conditions for a minimum of 58 days, more than enough for normal system servicing. A lithium primary battery may be connected into the system using jumper J7 on A4. This allows the microprocessor board to be removed from the card cage without loss of memory but is not normally used.

The watch-dog timer is constructed using a stable multivibrator configuration. The microcomputer normally retriggers the timer every .133 sec. If not, the timer will time out resetting the microcomputer and related hardware. This feature insures continued system operation in spite of occasional noise induced into the logic.

The microcomputer communicates to all peripheral subsystems via the MC6821 interface adapter. This device, software programmable, provides the necessary interface latches and buffers between the high speed microprocessor bus and the low speed CMOS logic circuits.

The remote display is connected to the system using a simple serial data communications path. The data is clocked sequentially into serial-to-parallel display drivers. After transmitting 48 bits of information, a strobe signal latches the pattern which drives individual segments on the display. The display update rate is every 0.133 sec.

All control signals are filtered and buffered using schmitt triggers. This configuration along with eight error detection bits insures valid data for the display. A 2.8V regulator supplies power to the display's filament from the 5V supply. This regulator is externally controlled to blank the display when it is not needed (charge cycle). A photoresistor controls a simple PWM circuit to vary the displays' intensity according to ambient light conditions.

Table 2.D.1
Battery Parameters

| <u>Parameter</u> | <u>Full Scale</u> | <u>Absolute Accuracy</u> | <u>Relative</u> |
|------------------|-------------------|--------------------------|-----------------|
| Voltage | 200 volts | ±1% F.S. | ±0.5% |
| Current | 400 amps | ±3% F.S. | ±0.75% |
| Ampere-Hours | 200 a-hr | ±5% F.S. | ±1.0% |
| Temperature | -25°C to 50°C | ±2°C | ±0.5°C |

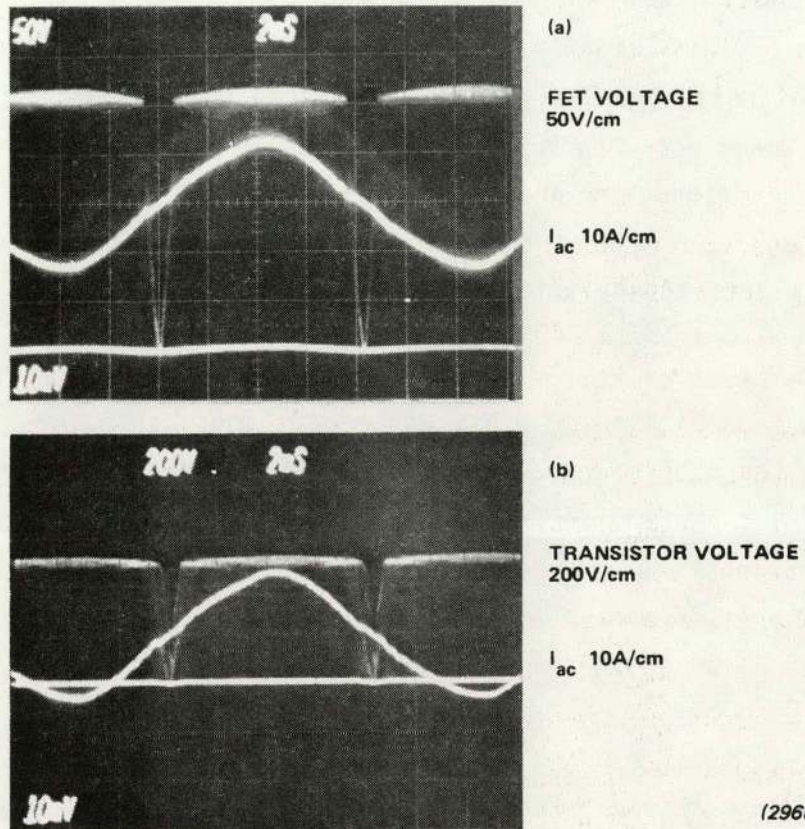


Figure 2.D.8 Switch Voltage Stress during AC Line Operation

2.D.3.a BC/SCI Software

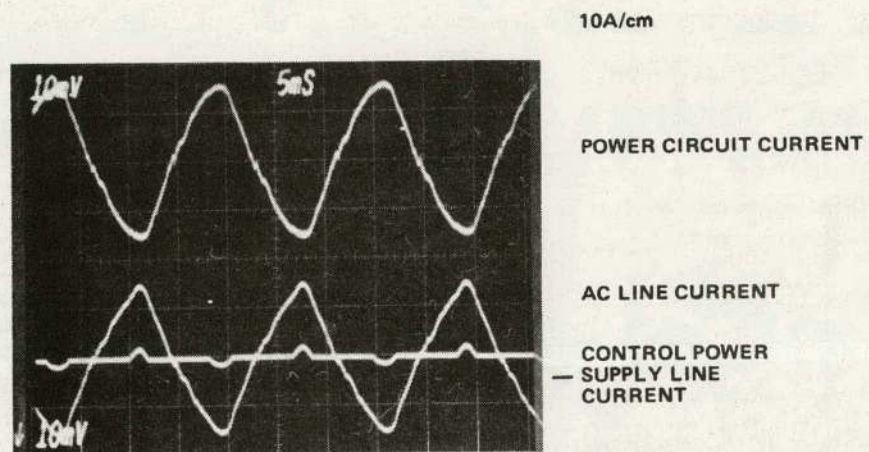
The software for the BC/SCI employs both 6809 assembly and Fortran programming languages. The software has been carefully structured to benefit from advantages provided by each language without sacrifice in overall system performance.

The real time executive provides the basic data acquisition and hardware interface functions. These tasks are characterized by being time critical in nature and are repeated at a fairly high rate (i.e., every .133 sec). Such requirements benefit greatly from the speed and bit manipulating capability provided by assembly programming.

The state-of-charge algorithm on the other hand is highly mathematical in nature. Sophisticated arithmetic operations having wide dynamic ranges are among the technical requirements. Flexibility for algorithm modifications and future enhancements also favor a high-level programming solution. Fortunately these functions are not as time critical as the data acquisition for adequate performance (i.e. every 15 sec). Fortran satisfies these requirements but does suffer the disadvantage of excessive memory requirements typical of high level languages.

The system has been structured so that the real time executive is the primary controlling module. The executive has the ability to call any one of five Fortran subroutines as is shown by the hierarchy chart in Figure 2.D.11. The chart clearly shows all BC/SCI Fortran modules and how each is called by the five main subroutines. A glossary is included in Appendix 2 which briefly describes the specific function of each module.

The flowcharts in Figures 2.D.12 - 2.D.18 illustrate the software structure. Two interrupt driven programs provide the basic data acquisition and hardware interface requirements. The first interrupt is synchronized to a one Hz clock and maintains all the software time functions. The second interrupt is generated at the end of conversion from the system's analog to digital converter. After reading and storing the converted data the A/D



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Figure 2.D.9 **Current Waveforms of**
 (a) the power circuit,
 (b) the AC line, and
 (c) the control power supply

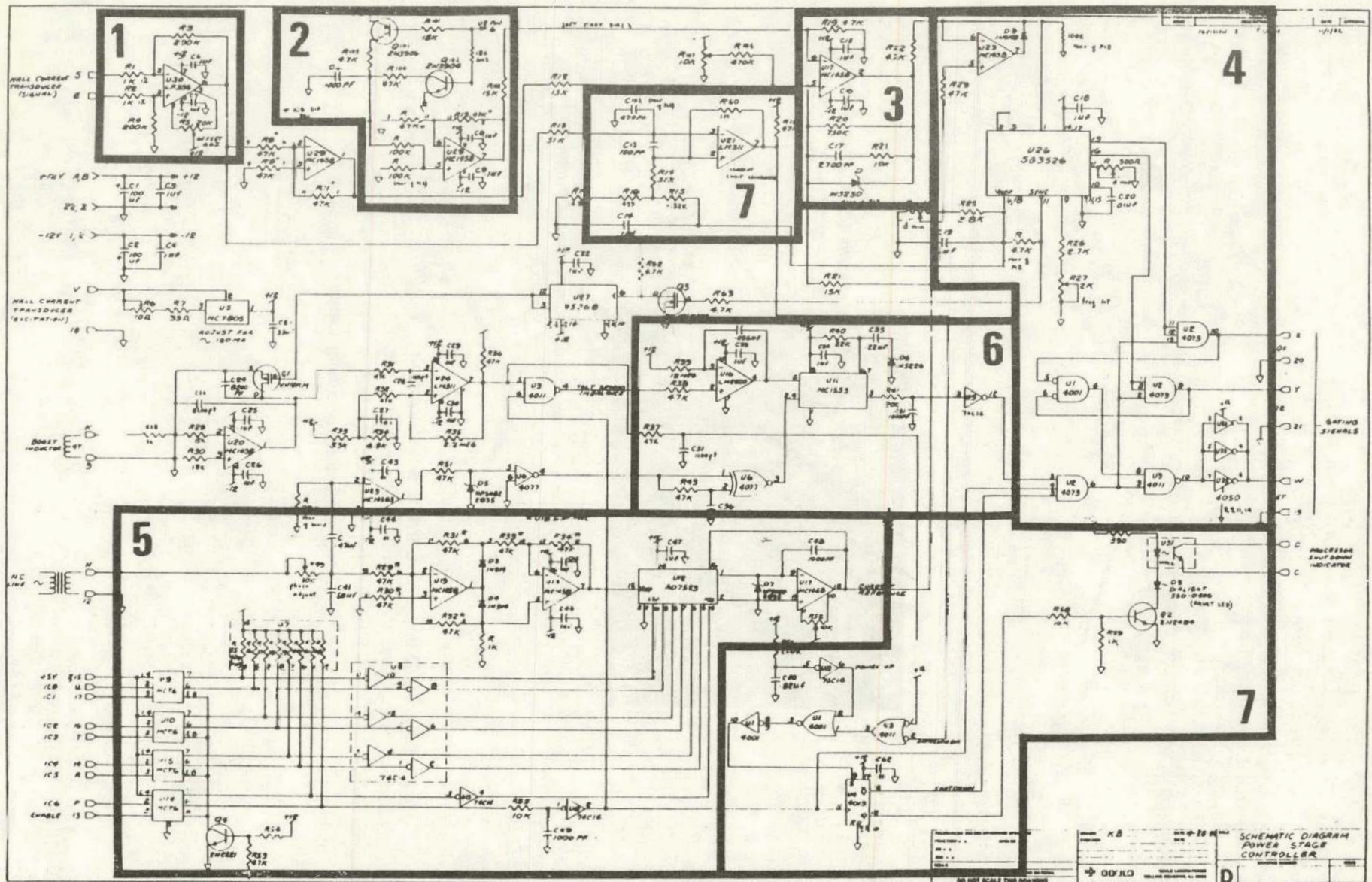
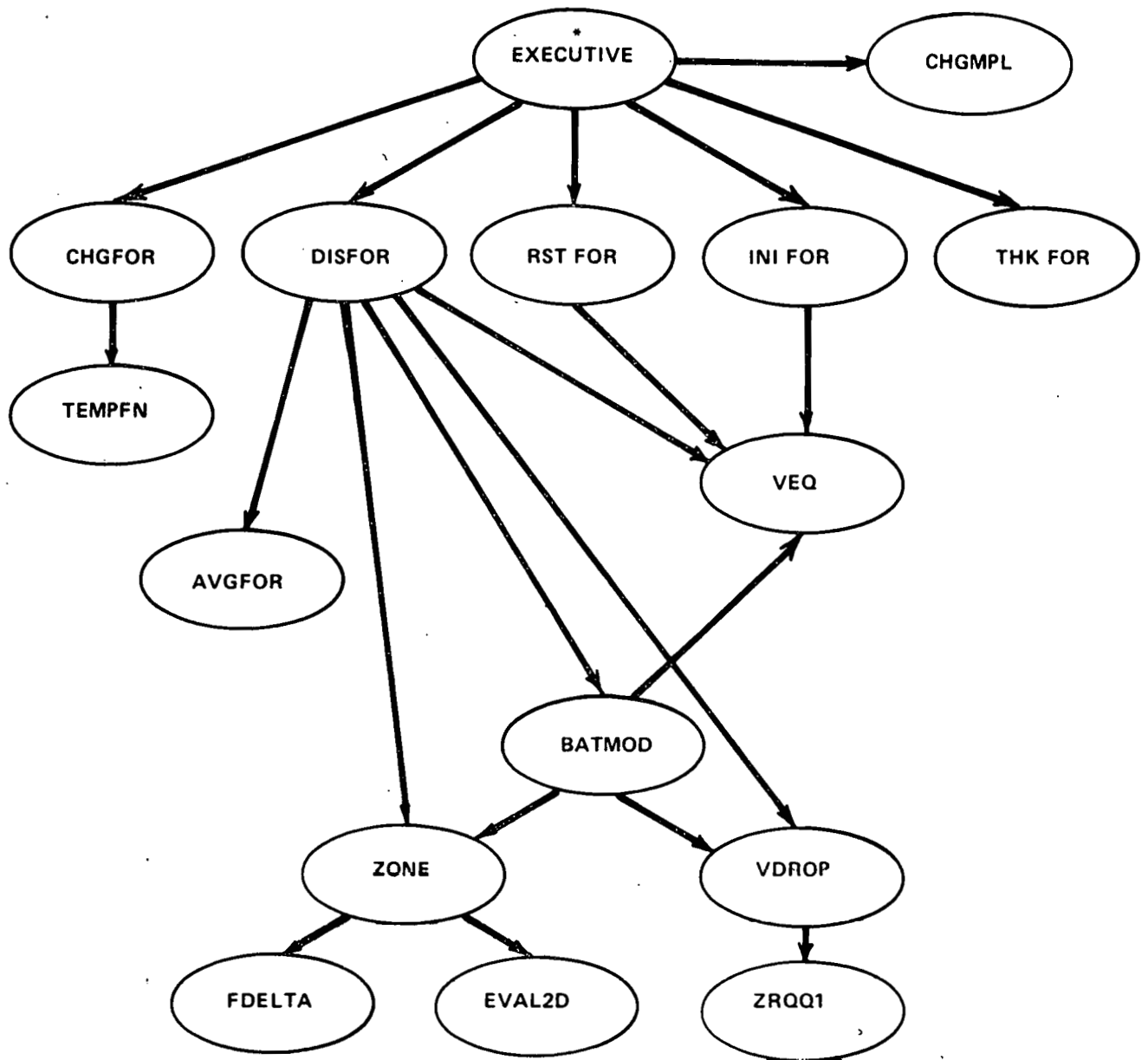


Figure 2.D.10 Power Circuit Controller

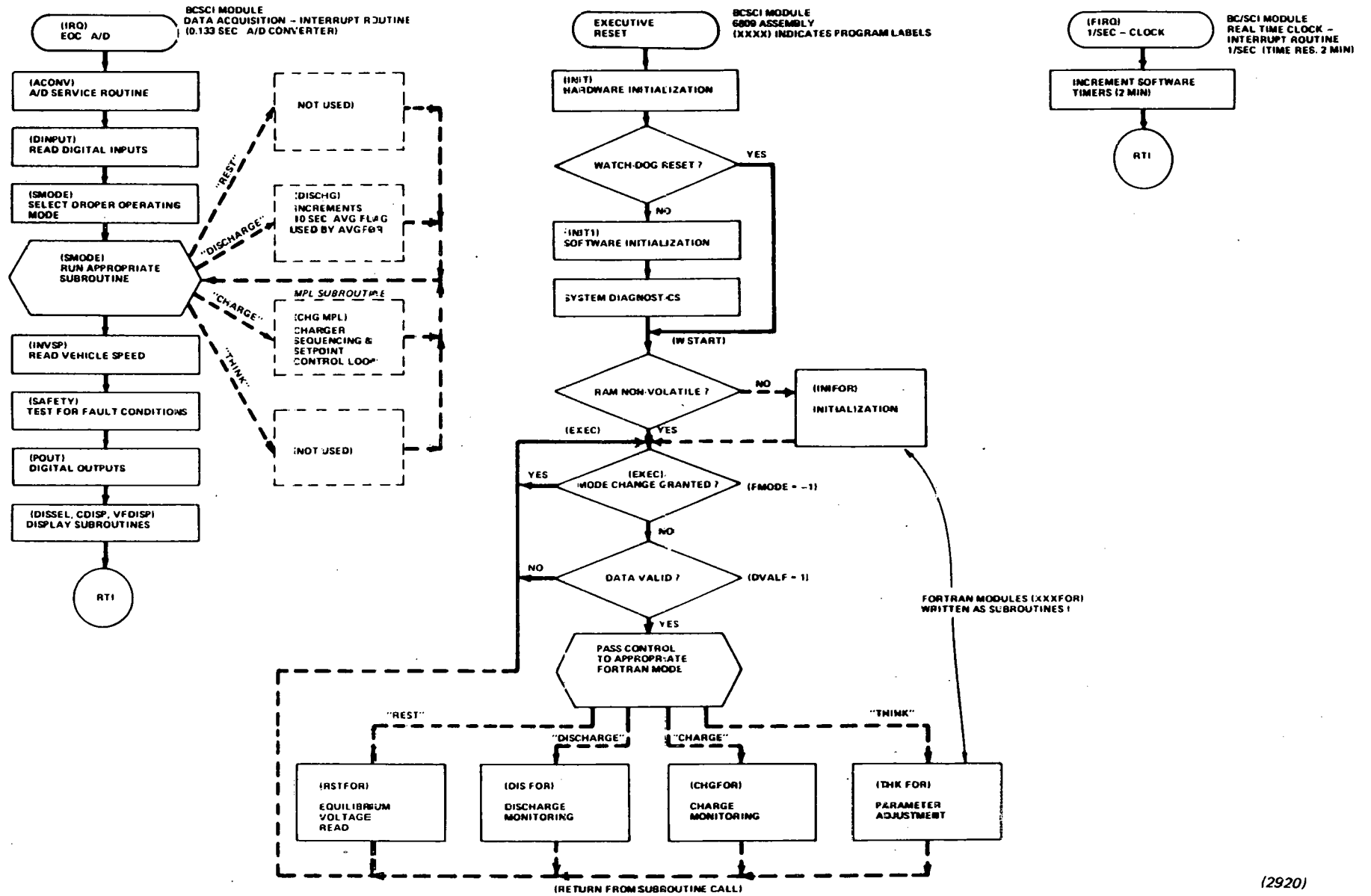
(See appendix 1 for larger version of schematic)



(2994)

*INDICATES ASSEMBLY LANGUAGE

Figure 2.D.11 Hierachy of BC/SCI subprograms



(2920)

Figure 2.D.12 Software module interaction

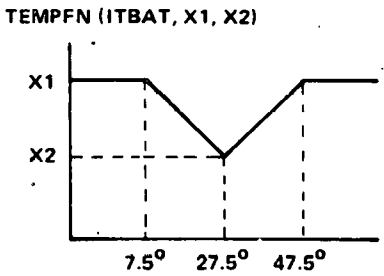
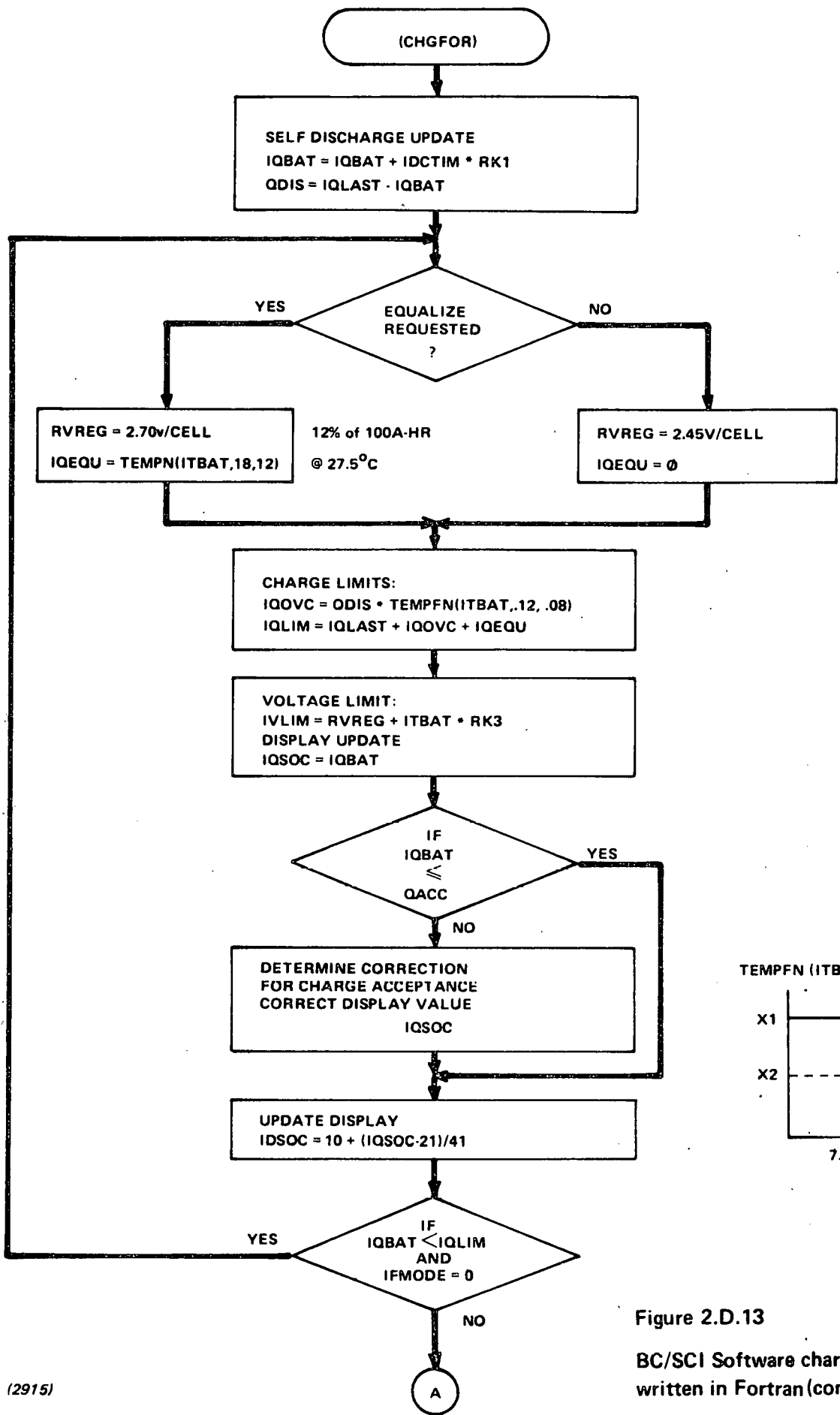
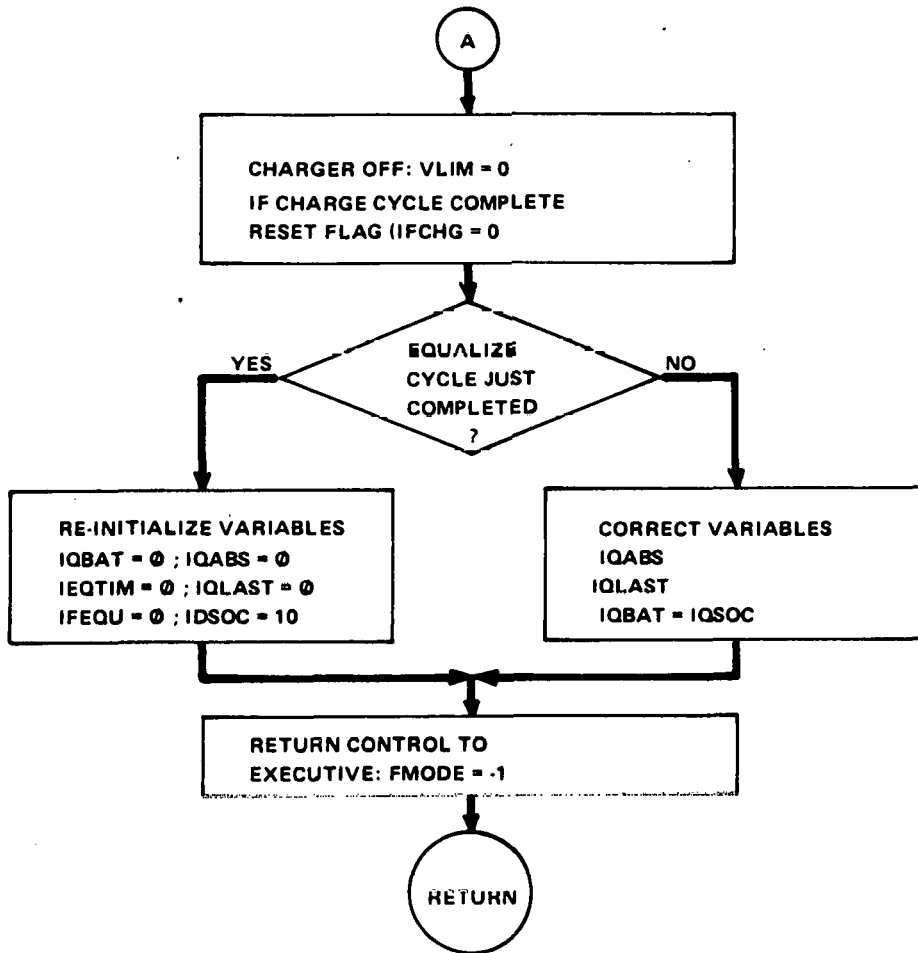


Figure 2.D.13

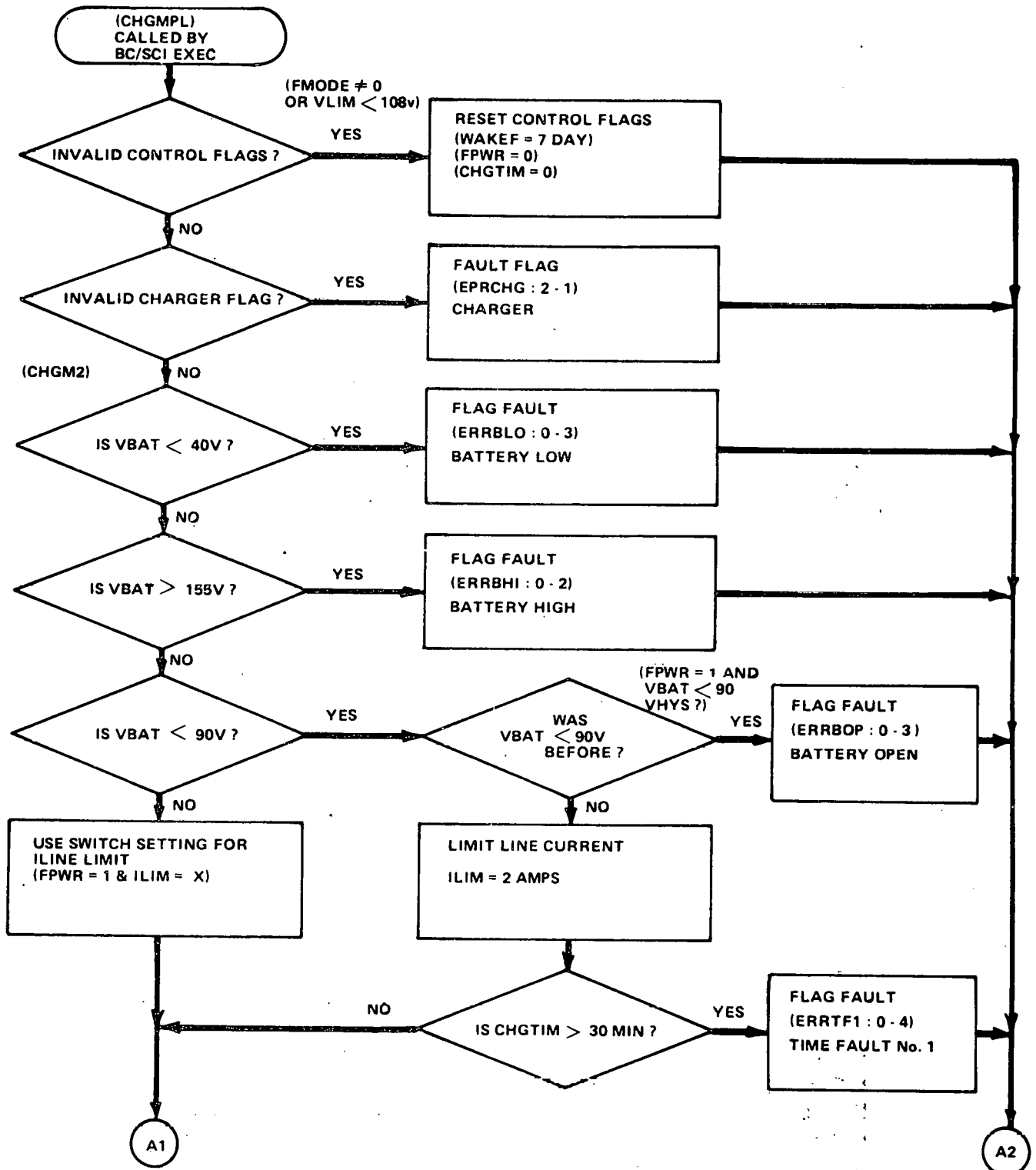
BC/SCI Software charge monitor -CHGFOR written in Fortran (cont.)



IEQTIM = 2MIN/BIT
 IDISTIM = 2MIN/BIT
 IQBAT = .2421 A-HR/BIT
 ITBAT = 1°C/BAT
 IVLIM = .050V/BIT
 IFEQU = 0 NORMAL; -1 EQUALIZE; -256 DEFER
 IFMODE = 0 NORMAL; 1 = CHARGE REQUESTED; -1 = CHARGE GRANT
 IQABS = A-HR REMOVED SINCE LAST EQUALIZE CYCLE
 RK1 = .05A/(30BIT/HR) + .2421 A-HR/BIT
 RK3
 TIME SINCE LAST EQUALIZE CYCLE
 TIME SINCE LAST DISCHARGE CYCLE
 AMP-HOUR METER "NEG OUT OF BAT"
 BATTERY TEMPERATURE
 VOLTAGE LIMIT DURING CHARGE

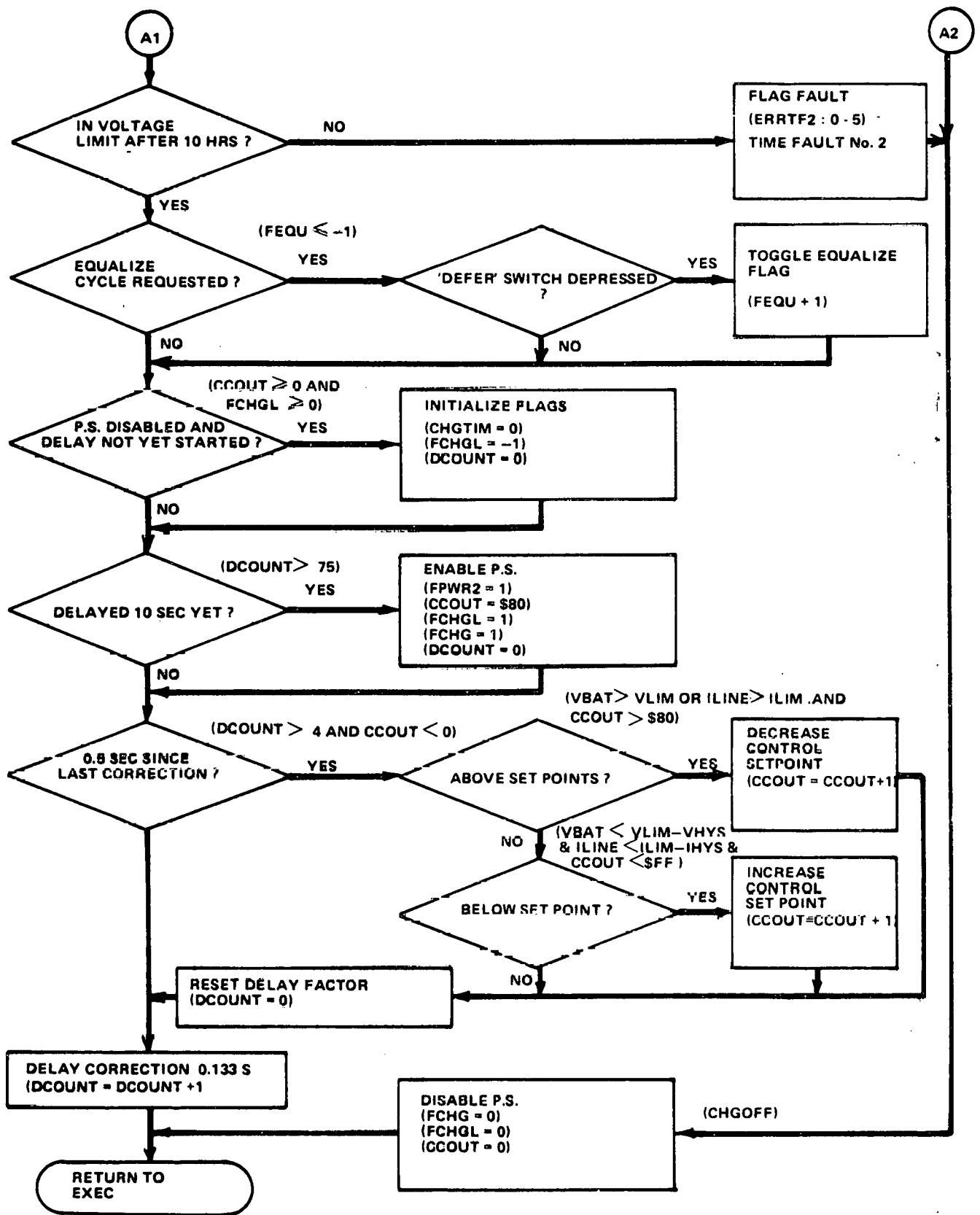
(2916)

Figure 2.D.13 (Cont.) BC/SCI Software charge monitor - CHGFOR written in Fortran



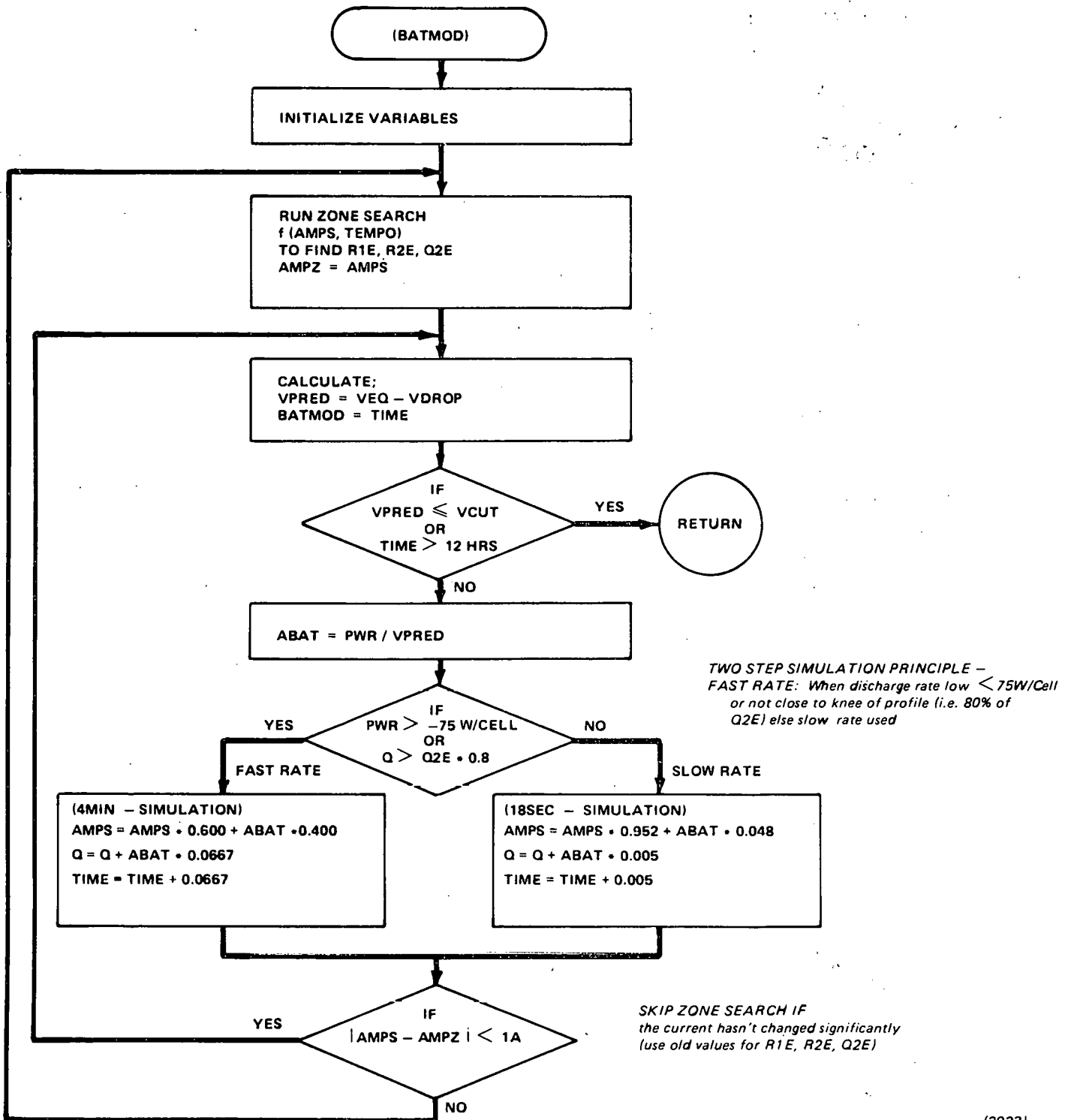
(2921)

Figure 2.D.14 BC/SCI Software
Charge control module – CHGMPL written in MPL (cont.)



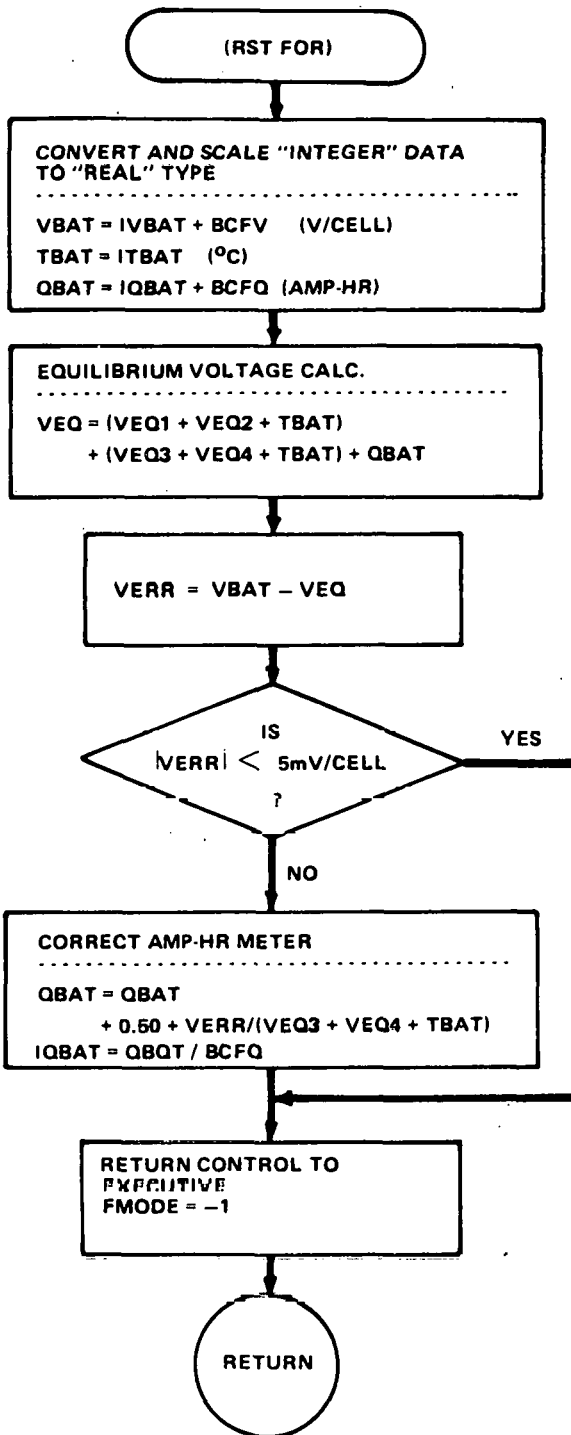
(2922)

Figure 2.D.14 (cont.) BC/SCI Software
Charge control module -- CHGMPL written in MPL



(2923)

Figure 2.D.15 BC/SCI Software Battery model – BATMOD written in Fortran as a function

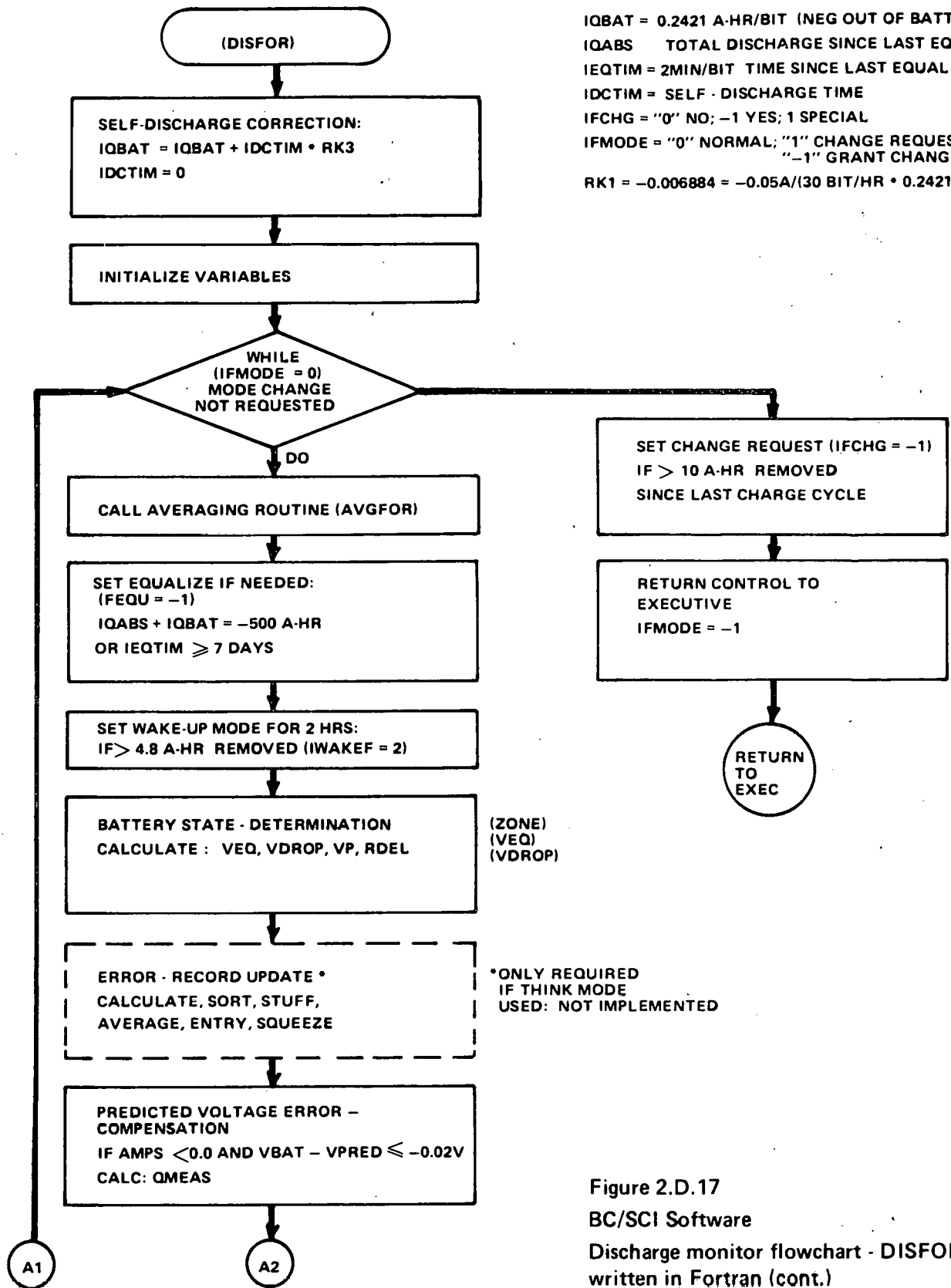


CELLS = 54
 IVBAT = 0.050V/BIT 16 BIT 2'S COMP
 ITBAT = 1°C/BIT 16 BIT 2'S COMP
 IQBAT = 0.2421 AMP-HR/BIT 16 BIT 2'S COMP
 (NEGATIVE OUT OF BATTERY)
 BCFV = 0.926 E-3 V/CELL/BIT
 BCFO = 0.2421 A-HR/BIT

 CONSTANTS:
 VEQ1 = 2.161 V/CELL
 VEQ2 = -5.16 x 10⁻⁴ (V/CELL)/°C
 VEQ3 = 1.217 x 10⁻³ (V/CELL)/A-HR
 VEQ4 = -7.42 x 10⁻⁶ [(V/CELL)/A-HR]/°C

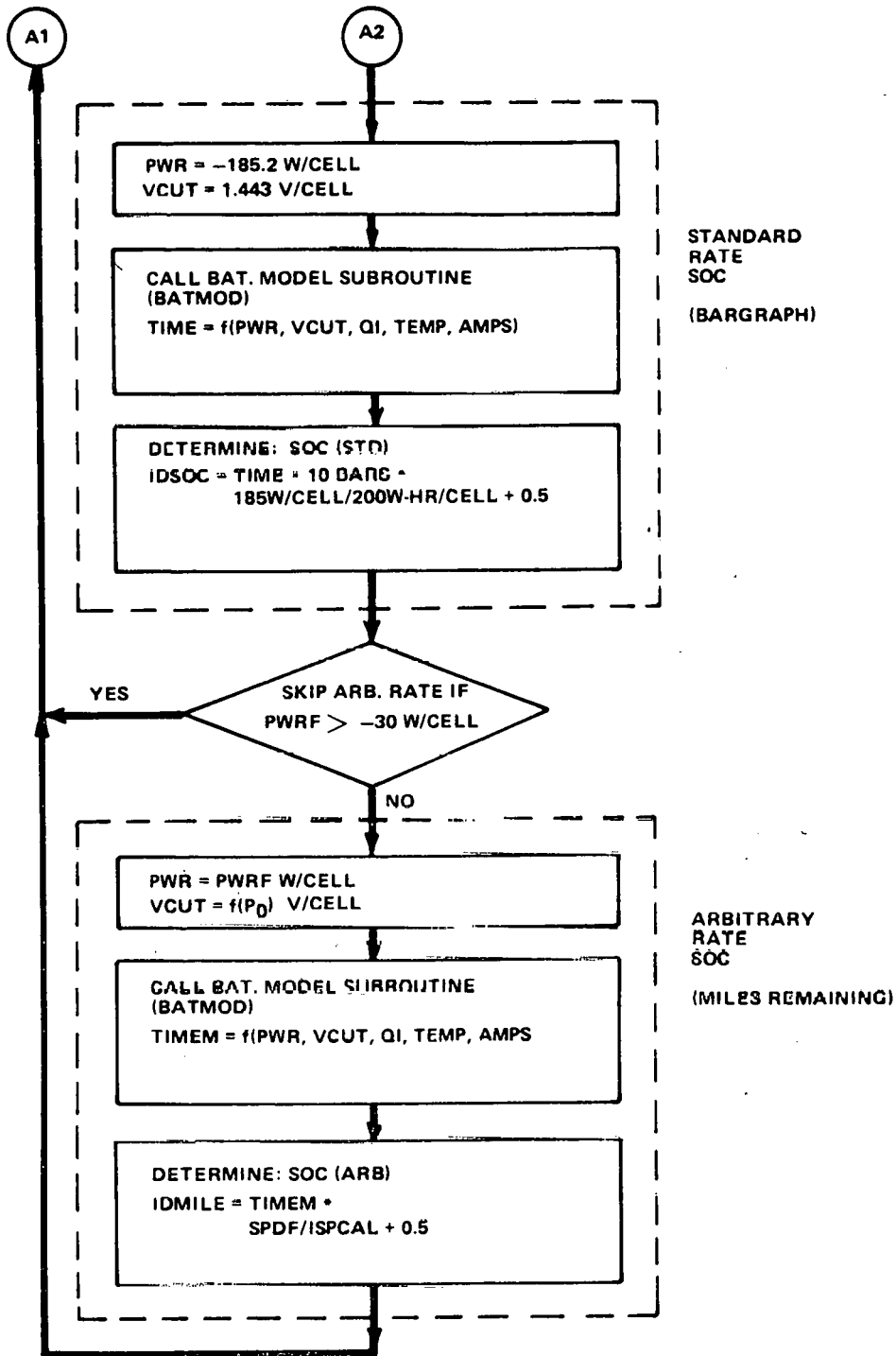
Figure 2.D.16 BC/SCI Software
 Equilibrium voltage read - rst for written in Fortran

(2924)



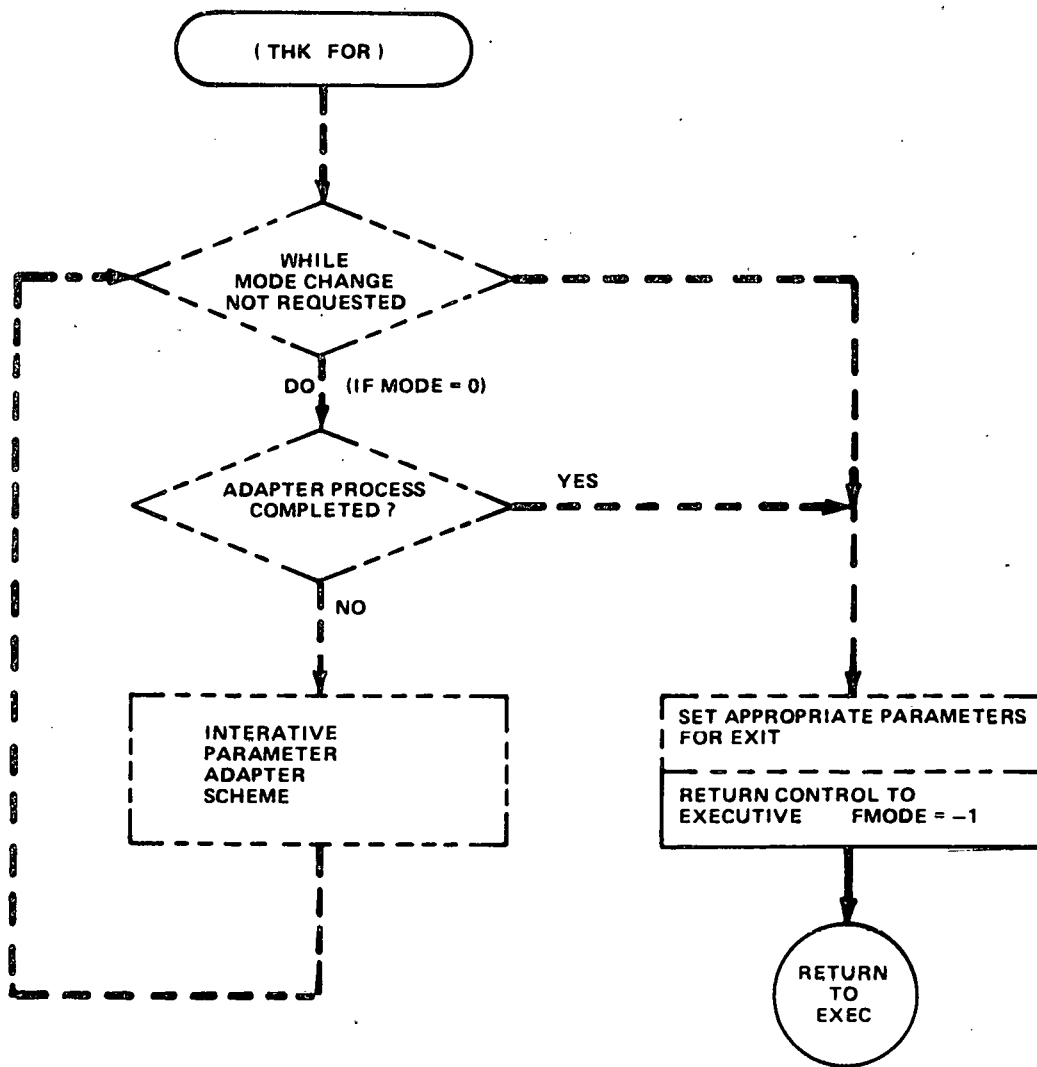
IQBAT = 0.2421 A-HR/BIT (NEG OUT OF BATTERY)
 IQABS TOTAL DISCHARGE SINCE LAST EQUALIZE
 IEQTIM = 2MIN/BIT TIME SINCE LAST EQUALIZATION
 IDCTIM = SELF - DISCHARGE TIME
 IFCHG = "0" NO; -1 YES; 1 SPECIAL
 IFMODE = "0" NORMAL; "1" CHANGE REQUEST;
 "-1" GRANT CHANGE
 RK1 = -0.006884 = -0.05A/30 BIT/HR + 0.2421 A-HR/BIT

Figure 2.D.17
 BC/SCI Software
 Discharge monitor flowchart - DISFOR
 written in Fortran (cont.)



(2918)

Figure 2.D.17 (Cont.) BC/SCI Software
Discharge monitor flowchart - DISFOR written in Fortran



(2925)

Figure 2.D.18 BC/SCI Software
 Parameter adapter flowchart THK FOR
 Possible structure not presently implemented

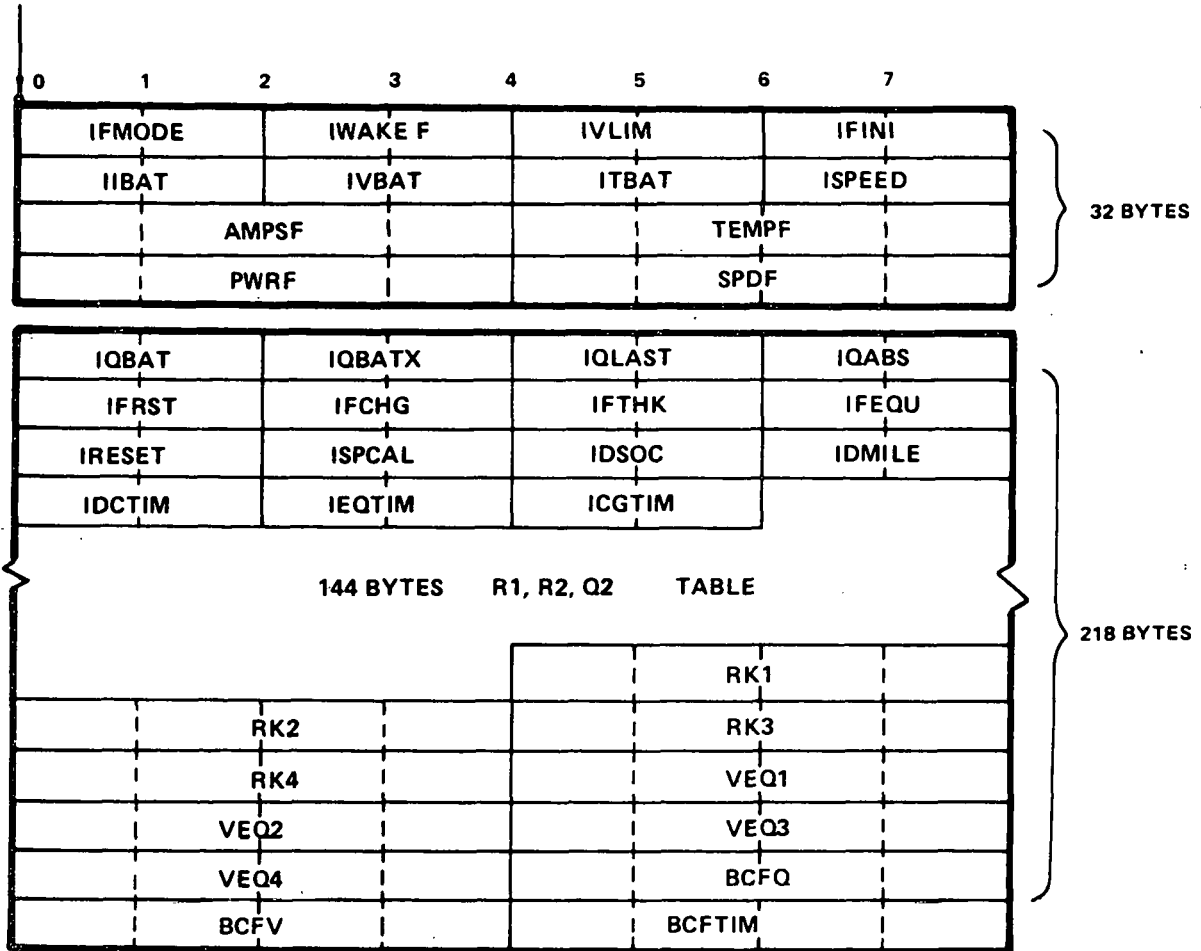
is set up for the next analog signal. Other hardware functions such as scanning inputs and controlling outputs completes the required tasks. The typical execution time for this program is approximately 10 milliseconds. It is repeated for each conversion cycle (.133 sec) and thus consumes 7.5% of the processor time.

The normal program execution starts with the executive performing the system initialization. It determines which mode has been selected and checks for valid data. Since the data acquisition is asynchronous to the main program execution, the executive must wait until the A/D conversion cycle is completed after which the data valid flag is set (DVALF=1). The executive then passes control to the appropriate Fortran subroutine Figure (2.D.12).

To guarantee controlled interaction a simple handshaking scheme was developed. If FMODE=0, the Fortran program can operate normally. When this flag is set (FMODE=1) by the interrupt program (i.e., operator requesting a mode change) the Fortran program must orderly complete whatever its doing, acknowledge the request (FMODE=-1) and return control back to the executive. The executive may then select a new mode, or the interrupt program can shut the system down depending upon requirements. This rigorous sequence guarantees predictable system operation whether the Fortran program is written with a looping (CHGFOR, DISFOR) or sequential (RSTFOR, INIFOR) program structure.

A common area in RAM has been defined to provide a means of passing arguments (data) between the assembly language executive and the Fortran subroutines and functions. This area is defined and represented in Figure 2.D.19 using a common statement for each Fortran routine and CSCT in the assembly language program. Since the entries in a common area share storage locations, their order (or memory address) is significant but not the variable name. It should be noted that integers occupy 2 bytes of storage while real numbers occupy 4 bytes of storage. A unique aspect of the BC/SCI common area is that variables which are defined by the first three statements (32 bytes) are initialized to zero during each power-up sequence; whereas the remaining eight statements (218 bytes) are non-volatile in nature. This structure,

FIRST MEMORY LOCATION



(2995)

Figure 2.D.19 Common Area -- Memory Map

while being memory efficient also simplifies the task of calling a Fortran subroutine from an assembly language program since arguments are passed in this common area rather than at time of call.

Several significant advantages should be obvious from the described structure. First the data acquisition and hardware functions are transparent to the Fortran programs. Secondly, each module may be written and modified independently of the others (except for common statements). And finally, simple handshaking and variable passing insures highly reliable and predictable system performance.

2.D.3.b System Operation and Calibration

Discharge

The system has been designed to minimize operator interface and calibration requirements. The operation of the SCI is slaved to the electric vehicle controller via a simple two wire interface. The controller must supply an isolated switch closure to the green and black wire of the interface cable. (Note: Black wire common to propulsion battery negative.) This set of contacts should be normally open and close only when the electric vehicle is enabled. As a safety feature the BC/SCI provides an isolated interlock signal (white and red wires) for use by the controller. This signal will be normally open but is closed when the ac line cord is attached to the BC/SCI. This signal should be utilized to prevent controller operation when the line cord is connected.

The discharge mode will then be selected whenever the front panel selector is in a normal position (15, 20, or 30 amps) and the electric vehicle is operated. In this mode the remote display will normally illuminate the SOC bargraph. The miles remaining display may be requested by pressing the pushbutton switch marked "miles remaining" on the display module. The display will now show, to the nearest mile, instantaneous miles remaining (averaged over the most recent 30 sec of driving). This function is only calculated for power levels exceeding 30 watts/cell. This mode will be maintained as long as

the pushbutton is depressed and for five seconds after it is released. It should be noted that after the unit is switched off the system must terminate present activity before the display disappears. This results in a variable turn-off-delay possibly as long as 17 seconds.

Charge

The charge cycle is initiated by selecting the appropriate current setting, plugging the ac line cord into the front panel receptacle and switching the front breaker from the "off" to the "on" position. This in-turn supplies power to the fan and base drive power supply and sends a one-second enable pulse to the system logic power supply.

This enable pulse provides sufficient time for the microcomputer to start operating and latch the power supply on. The power up sequence is noted by all front panel lights being illuminated for a short time. If a charge cycle has been requested (by the charge mode) the "charge" light will begin flashing at a 0.5Hz rate. This indicates that the power stage will be enabled after a 10 second delay (5 flashes). Once enabled the "charge" light is illuminated continuously. During the charge cycle the remote display is normally blanked but state of charge may be requested by depressing the "miles remaining" pushbutton. This display will be maintained as long as the pushbutton is depressed and will extinguish 5 seconds after it is released. It should be noted that the state of charge displayed during a charge cycle is not the same as that which is displayed during discharge. The charge cycle displayed is a simple percentage of ampere-hours normalized for a new battery at room temperature. The front panel current selector is marked for the original ac line requirements (15, 20, or 30 amps) for a 3kW charger. These settings have been appropriately scaled for the present 1kW rating (3, 6, or 9 amps).

If the system has requested an equalize cycle (500 A-hr removed or 7 days has elapsed since the last equalize cycle) the "EQUALIZE" light will illuminate when the charger is turned on. This indicates that the battery will be equalized during this charge cycle unless the operator defers it by

depressing the front panel switch marked "DEFER EQUALIZE". This will defer the equalize cycle until the next time a charge cycle is initiated.

When the charge cycle is completed the microcomputer will extinguish all indicators and shut itself off. It should be noted that although the charge cycle is completed the main power breaker will remain on and the internal fan will continue to operate. A discharge cycle may now be run by turning the power breaker to the "off" position and disconnecting the ac line cord. If no discharge cycle is required the breaker may be left in the "on" position. This will allow the microcomputer to run an equalize charge cycle every 7 days, an accepted standard for keeping the battery in good condition.

Wake-up

This special mode is normally transparent to the operator. The mode will be self-initiated when the battery has rested two hours after a discharge-cycle of at least 4.8 ampere-hours. The system will power itself up, read battery data and appropriately modify the system ampere-hour meter if required before turning itself off. Once this mode is completed, another discharge must take place before the mode is again requested.

Calibration

The system was designed to minimize initialization and calibration requirements. Once the SCI has been configured for a particular battery/vehicle combination, no additional operator interaction is normally required. To properly configure the SCI, the battery parameters must be initialized and the speed transducer calibrated. A new equalized battery should be attached to the system and the inductive speed pickup with magnets properly mounted to the vehicle. To perform this simple procedure, turn the front panel selector switch to the un-marked position immediately to the left of "AUX". Next, turn the unit on for a normal discharge cycle. The unit will power up and the "warning" indicator will flash with all zeros on the numeric display. The warning indicator signifies that you are in the "calibration mode." The battery parameters have already been initialized, and the system

is awaiting the transducer calibration sequence. The system has a default calibration factor which is selected for a vehicle having 13" diameter wheels, radial tires and sensing a rotating element with a 1:1 speed ratio with respect to the wheels. If this configuration is adequate the sequence can be terminated by returning the front panel selection to one of the normal positions (15, 20 or 30 amps). If not, the vehicle should be driven over a measured mile with the "miles remaining" pushbutton depressed once at the beginning and again at the end. The numeric display will flash and slowly increment during this calibration interval. Speed is not a factor during this procedure since pulses/mile are being determined. Once this is completed the sequence is terminated by returning the front panel selector to its original position. Calibration is now complete and the system will "remember" these factors as long as the system memory remains non-volatile (see logic description).

Diagnostics

The BC/SCI has a high degree of self-diagnostics to assist both the operator or repair personnel in isolating problems in the system. Tables 2.D.2 and 2.D.3 list all possible fault codes presently incorporated into the system. A fault is normally indicated three ways. First, the "FAULT" indicator on the front panel will be enabled for all faults. Second, the remote display will show an error code using the three numeric digits. Finally, if the fault corresponds to a particular board the edge mounted LED on that board will be illuminated.

A complete diagnostic sequence is executed everytime the unit is powered-up, and a sub-set thereof is performed while the system is operating. As diagnostics are performed on each board the LED on the particular board will be illuminated and then extinguished after the test is successfully completed. If a fault is detected, the test sequence will be stopped, and the display will show a particular error code. This code can then be used to determine the particular test which failed and isolate possible causes. The fault descriptions provided in the tables primarily identify the test and make no attempt to outline all possible causes for a given problem.

Table 2.0.2

Charger Run Time Fault Description

Fault Error Codes Appear on Display as: 0=X or 2-X

- 01 ERBLO - Battery Below Min Value
- 02 ERBHI - Battery Above Max Value
- 03 ERBOP - Battery Disconnected During Operation (Opened)
- 04 ERRTF1 - Time Fault =1 - Prolonged Low Battery Voltage Operation
- 05 ERRTF2 - Time Fault =2 - Prolonged Operation Without Reaching Voltage Regulation
- 06 ERRSW3 - Invalid Switch Setting for Charger Operation
- 21 ERRCHG - Power Stage Fault

Table 2.D.3

System Error Codes

4 MSB Primary - Assembly or Category
 4 LSB Secondary - Error Within Assembly or Category

Note: Ω0X Indicates Run Time Faults Check MPL Listing

ERRPWR Ω11 AUX. - Power Defective - RAM, Time Info. Lost

ERRCHG Ω21 Power Stage Fault Used INLMPL

ERRADC Ω31 A/D Conversion Invalid

ERROF Ω32 A/D Overflow Indication

ERRNEG Ω33 Analog Input Incorrect Polarity

ERRSM1 Ω34 Select Mode - Invalid Mode

ERRROM Ω41 ROM Checksum Error

ERRRAM Ω42 Bits In RAM Will Not Toggle

ERRCIO Ω43 1/Sec Interrupt

ERRCLK Ω44 Real Time Clock Doesn't Advance

ERRPIA Ω45 PIA A Input Fault

ERRPIB Ω46 PIA B Input Fault

ERRPOA Ω47 PIA A Output Fault

ERRPOB Ω48 PIA B Output Fault (Internal Check Only)

ERRTBS Ω70 Battery Thermistor Shorted

ERRTES Ω71 Enclosure Thermistor Shorted

ERRTFS Ω72 Fet Thermistor Shorted

ERRTAS Ω73 Ambient Thermistor Shorted

ERRTBO Ω75 Battery Thermistor Open or Fuse Blown

ERRTEO Ω76 Enclosure Thermistor Open

ERRTFO Ω77 FET Thermistor Open or Fuse Blown

ERRTAO Ω78 Ambient Thermistor Open or Fuse Blown

ERRTBA Ω81 Battery Overtemp.

ERRTEN Ω82 Enclosure Overtemp.

ERRTFE Ω83 FET Overtemp.

ERRTAM Ω84 Ambient Overtemp.

ERRBAT Ω91 BAT. Below Min. Value

ERRFPI Ω92 Invalid Switch Setting

ERRSOF Ω93 Speed Transducer Calibration Error

ERRSHI Ω94 Speed Counter Overflow

Since a given problem may provide multiple fault codes, all codes should be viewed before a determination is made as to the cause. This is done by depressing the "MILES REMAINING" pushbutton to direct the system to proceed with the remaining diagnostics. This sequence should be repeated until all codes are noted. Care should be exercised since the system will attempt operation after all faults are identified.

The format of the codes are two digits separated by a hyphen (i.e., x-x). The first number corresponds to a category while the second number identifies a particular problem within that category. For example all codes with a seven as the first digit correspond to a thermistor related problem. A 7-5 signifies battery thermistor open or fuse blown. This could be caused by a fuse blown on A3, a bad thermistor (opened) or possibly the battery probe not properly connected.

A fault that is detected during normal system operation stops all activities. The fault will be displayed as long as it exists or for a minimum of five seconds. If the problem disappears the system will attempt to continue where it was interrupted prior to the fault condition (e.g. 8-2 enclosure overtemperature). Additional information regarding the cause of a particular operating fault may be obtained from a complete power-up diagnostic procedure.

Test

A special mode has been included in the system to provide useful information during system troubleshooting. This mode allows you to observe selected variables during actual system operation. The mode is entered after the system is operating by switching the DIP switch No.4 on A3 to the "ON" position. During discharge this same mode can be entered by turning the front panel selector switch to the un-marked 12 o'clock setting.

The display will illuminate the warning, bargraph and numeric elements. The value displayed corresponds to the present software version number. The mode can display up to ten bytes (8 bits) in decimal form of any

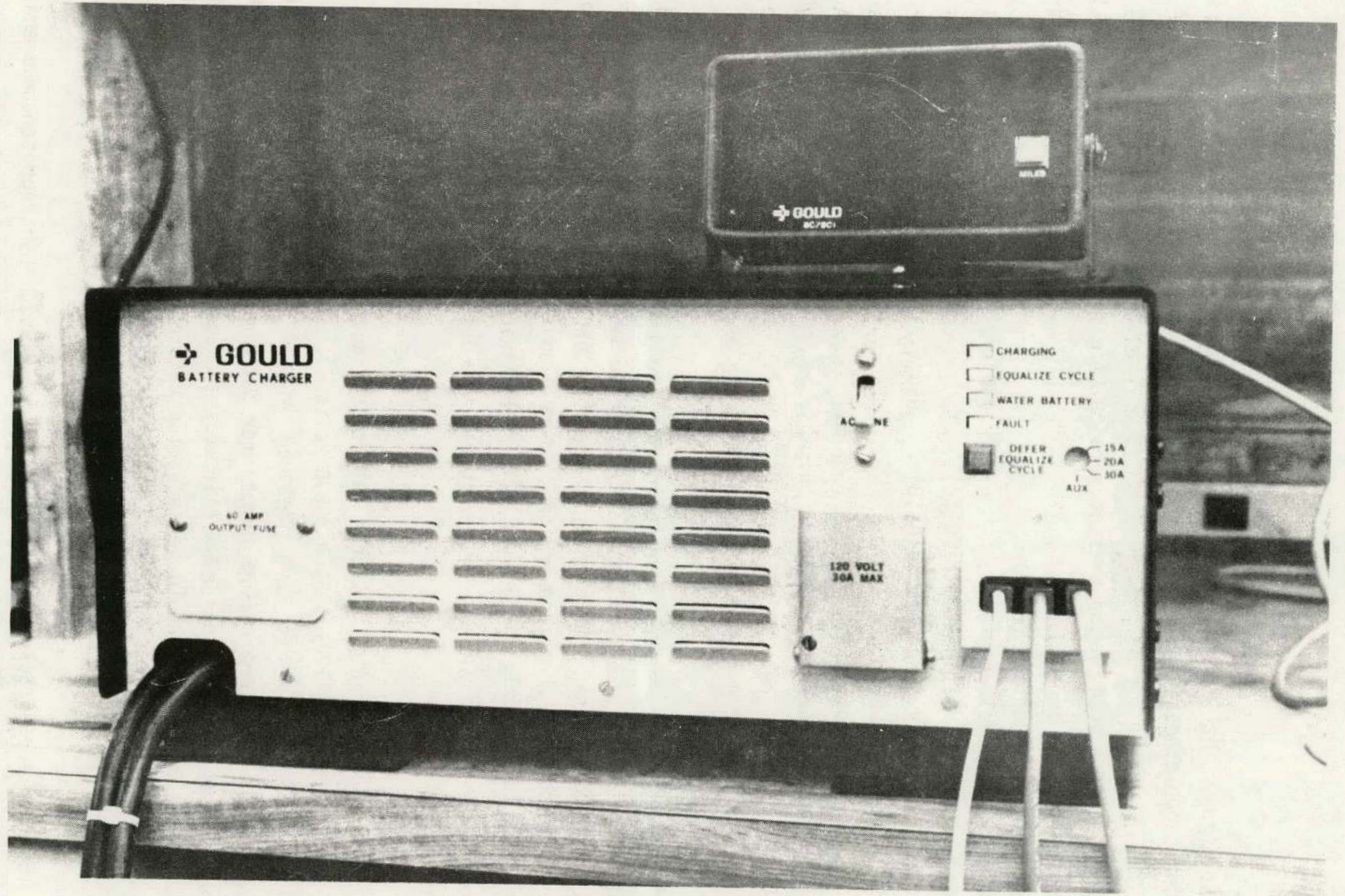


Figure 2.D.20 BC/SCI System

(2988)

memory location. The resulting display is non-standard but can be extremely useful for troubleshooting without any sophisticated test equipment.

The test sequence in the present version (i.e., 1.00) is as follows:

- 10% - Battery Voltage (8MSB)
- 20% - Battery Voltage (8LSB) .050 v/BIT
- 30% - Charging Voltage Limit (8MSB)
- 40% - Charging Voltage Limit (8LSB) .050 v/BIT
- 50% - Ampere-hour (8MSB)
- 60% - Ampere-hour (8LSB) .2421 A-HR/BIT
- 70% - Battery Current (8MSB)
- 80% - Battery Current (8LSB) .1A/BIT
- 90% - Mode Flag 0=Normal; 1=Request change; 256=Grant Change

The percentage factor corresponds to the bargraph display when the information is shown. A particular item may be selected by depressing the "MILES REMAINING" button the appropriate number of times. Scaling factors have been included to allow conversion to more familiar units, but care should be exercised to properly weigh the most significant bits. For example a voltage reading of 008 (8MSB) and 112 (8LSB) could be converted to volts by the following equation.

$$\begin{aligned} & [(8MSB)] \times 256 + (8LSB)1 .050 = \text{Battery Voltage} \\ \text{or} & [(008)] \times 256 + (112)1 .050 = 108.0 \text{ Volts} \end{aligned}$$

It should be noted that a number for battery current between 128 and 256 as the most significant byte indicates a negative quantity in two's-complement arithmetic and should be converted before using the scaling factor provided.

2.D.4 Physical Description

The complete BC/SCI is pictured in Figure 2.D.20. This photo shows the main enclosure housing the power section and the control electronics and the remote display. Figure 2.D.21 shows the comparison interface module used to

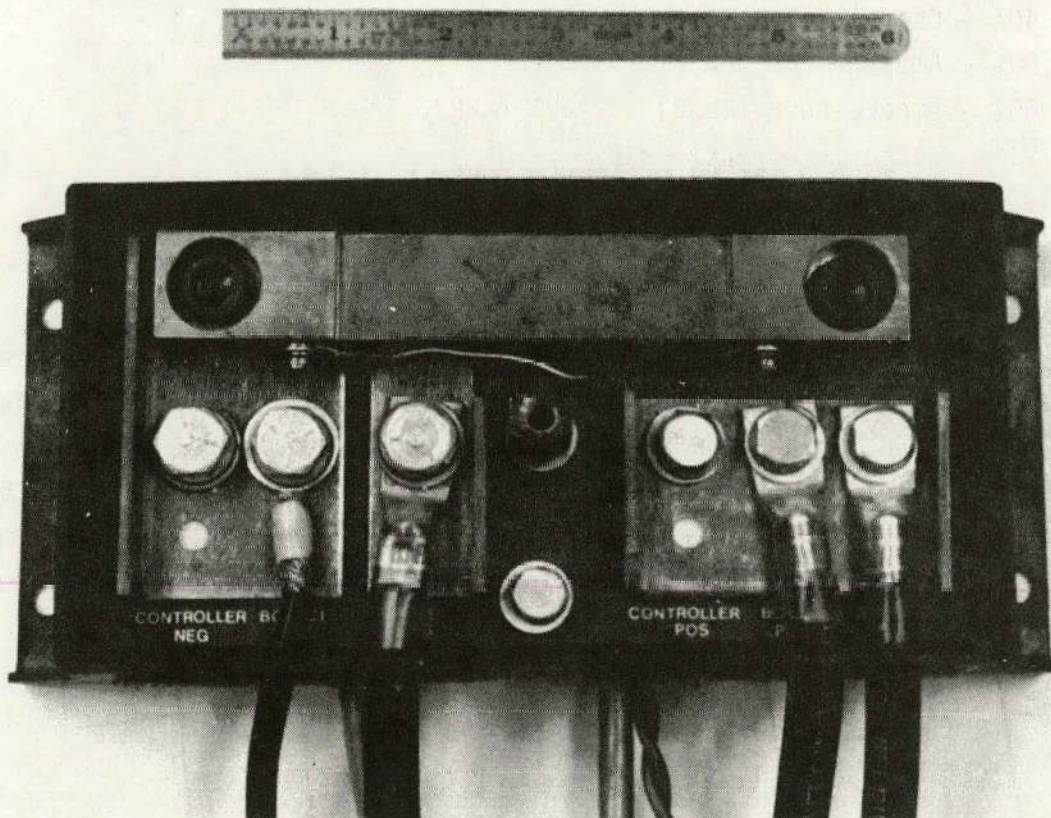


Figure 2.D.21 System Interface Module

(2990)

insert the system transducers between the battery and vehicle controller and provide the charger connection to the battery. The weights and dimensions of those three assemblies is summarized in Table 2.D.4.

Table 2.D.4
BC/SCI Assemblies Weight-Dimensions

| Assembly | Weight | Size |
|----------------|----------|-----------------------------|
| Main Enclosure | 29.5 lbs | 19.0" x 8 13/16" x 10.0" |
| Display | 1.05 lb | 6.30" x 3.2" x 2.5" |
| Interface | 3.2 lb | 8 15/16" x 4 1/4" x 2 7/16" |

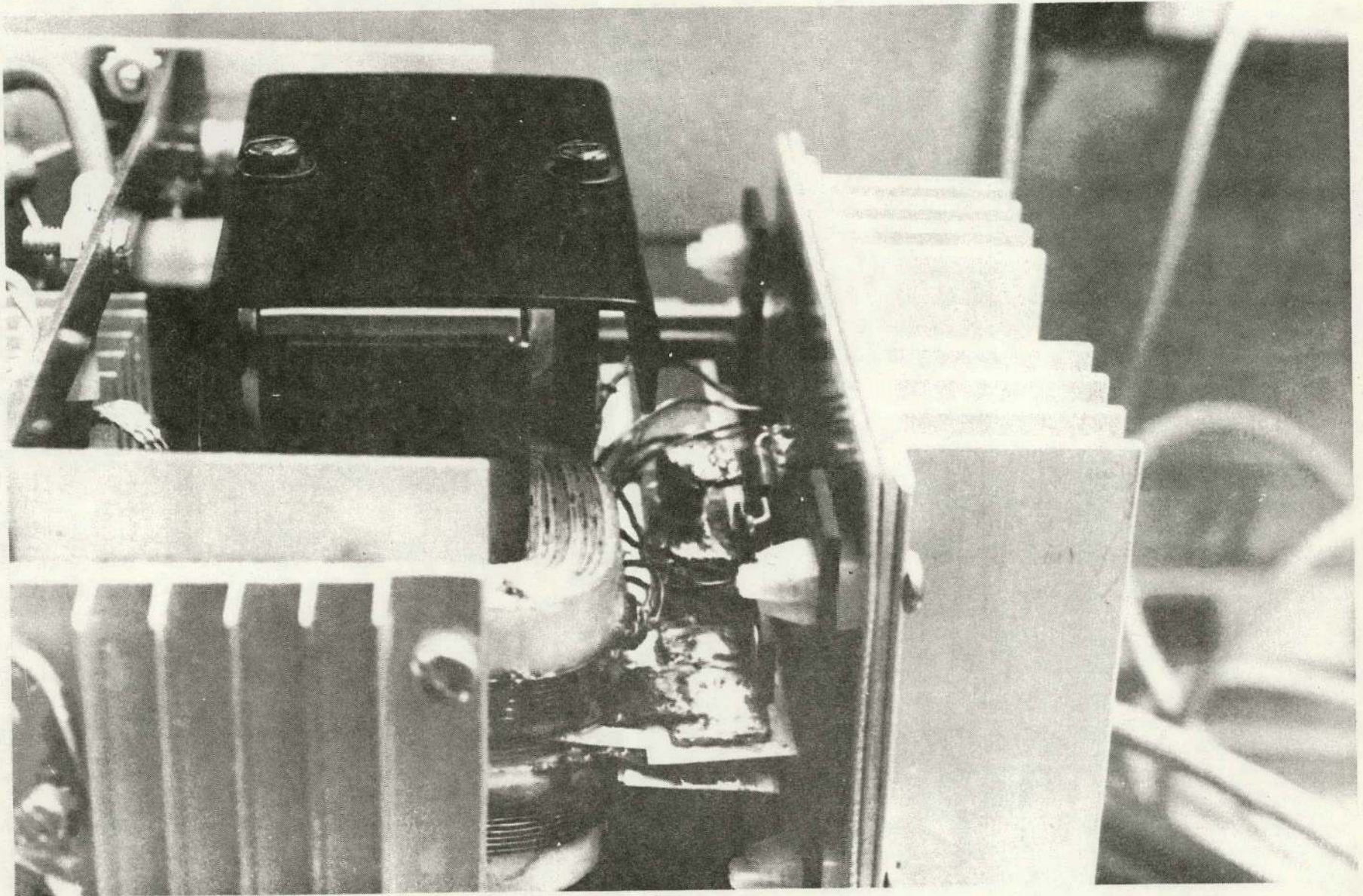


Figure 2.D.22(a) Mechanical Construction of Transformer Connection to Output Rectifiers

(2992)

The weight distribution of the Main Enclosure is summarized in Table 2.D.5.

Table 2.D.5

| Item | Weight (lb) |
|--|-------------|
| Enclosure | 7.0 |
| ac Circuit Breaker and Connector | 0.6 |
| Control Electronics/Power Supplies/Card Nest | 4.0 |
| Power Electronics | |
| Transformer | 3.40 |
| Output Filter | 1.75 |
| Output Diode and Heat Sink | 0.92 |
| Input Diode and Heat Sink | 0.22 |
| Filter Inductor, Capacitor | 0.7 |
| Boost Inductor | 5.0 |
| Darlington Xistors and Heat Sink | 0.9 |
| FET and Heat Sink | 0.8 |
| Fan | 1.0 |
| Base Drive | 0.8 |
| Bus Bars/Mounting Hardware | 2.10 |
| FET Drive | <u>0.5</u> |
| Total | 29.7 lb |

The goal of high electrical efficiency impacted the mechanical design of the charger, particularly the construction of the power circuit secondary. In order to minimize the leakage inductance inserted between the isolation transformer's secondary terminals and the filter capacitor, a strip

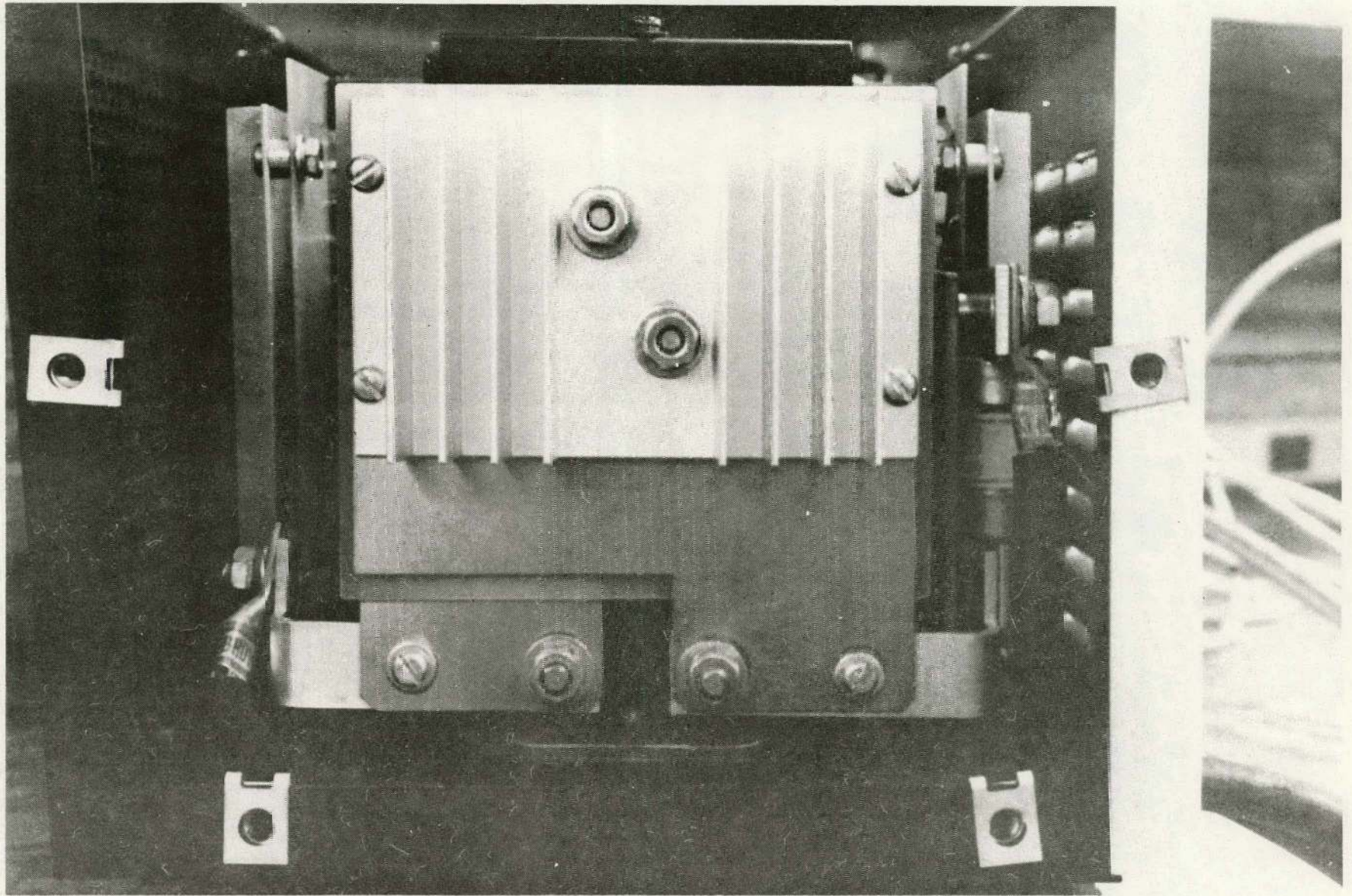


Figure 2.D.22 (b) Photo of Stripline Style Connection between Rectifiers and Output Capacitor

(2991)

line parallel-plate conductor construction was employed. This is illustrated in Figures 2.D.22 (a) and (b) respectively which show the interconnects between the transformer and the output rectifiers (a) and between the rectifiers and the output filter capacitor (b). The parallel plate conductor construction is mandatory to minimize secondary circuit leakage inductance.

For completeness, the weight of the entire BC/SCI system is tabulated including all power and interface cables.

Table 2.D.6

| <u>Item</u> | <u>Weight (lb)</u> |
|--------------------------------|--------------------|
| Main Enclosure | 29.7 |
| Display Module | 1.1 |
| Interface Module | 3.2 |
| Charger-Interface Cables | 3.5 |
| ac Line Cord | 10.0 |
| GFI Pigtail | 5.0 |
| Module Interconnection Cabling | <u>0.5</u> |
| Total | 53.0 lb |

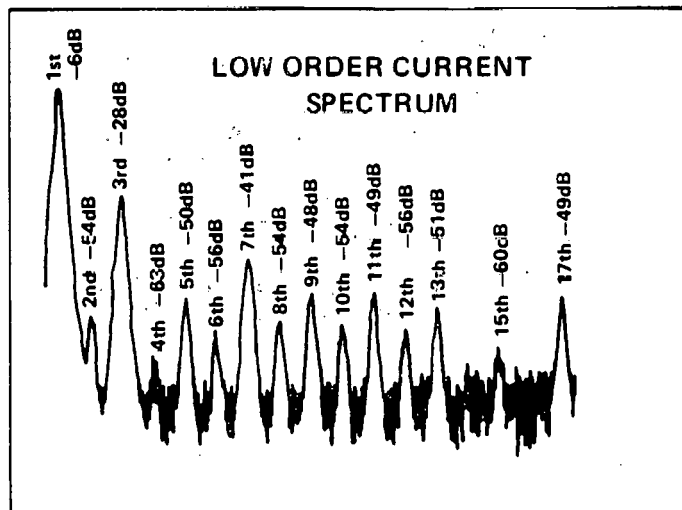
2.E Test Program

The test program consisted of a series of measurements to quantify the efficiency of the charger, the line distortion, and the accuracy of the operational SOC algorithm imbedded in the microcomputer system.

2.E.1 Power Electronics

It should be noted that downgrading the output power to 1kW did result in reduced efficiency and increased distortion compared to the original target goals. The efficiency of the charger was measured at an operating input power level of 1kW. The input power was measured with a Weston Model 432 wattmeter, and the output power was calculated using the product of the average battery voltage and the average battery current using 4 1/2 digit FLUKE meters. This approximation to determine the output power is valid since the battery ripple voltage is only 2Vp-p. The measured efficiency was 87%. This includes the loss attributable to the cooling fans, power supplies, and microcomputer system. The power circuit itself approaches the 90% efficiency level. Approximately 3% of the power is consumed by the fans and power supplies.

The line distortion of the input current waveform was measured with a HP333A Distortion Analyzer and a HP3580 Spectrum Analyzer. The measured harmonic distortion of the line current is 7.4%. This is compared to the calculated distortion employing all significant harmonics up through the 17th of 7.98%. Figure 2.E.1 shows the low order current spectrum. However, the ac line voltage used to program the current is not a pure sinusoid, as shown by its voltage spectrum in Figure 2.E.2. Its calculated Total Harmonic Distortion (THD), also through the 17th harmonic, is 2.5% and implies that the charger, if perfect, would also exhibit a current THD of 2.5%. Therefore the charger introduces a THD of approximately 5% (7.4-2.5) on the utility grid at the 1kW operating point. Figure 2.E.3 shows the high order current spectrum, specifically the 40kHz and 20kHz switching noise. The THD introduced by these spectral lines is only 0.64%.



(2971)

Figure 2.E.1 Harmonic Spectra of the BC/SCI line current
 1st harmonic = 60 Hz; 2nd harmonic = 120 Hz; etc.

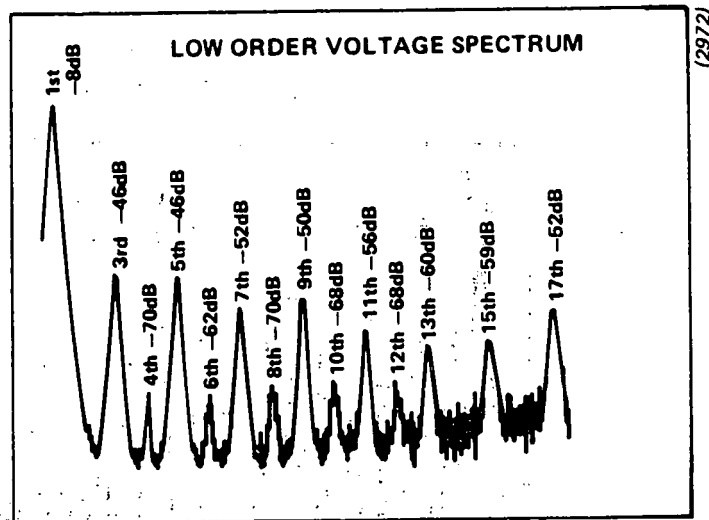


Figure 2.E.2 Harmonic Spectra of the applied ac line voltage
 1st harmonic = 60 Hz; 3rd harmonic = 180 Hz; etc.

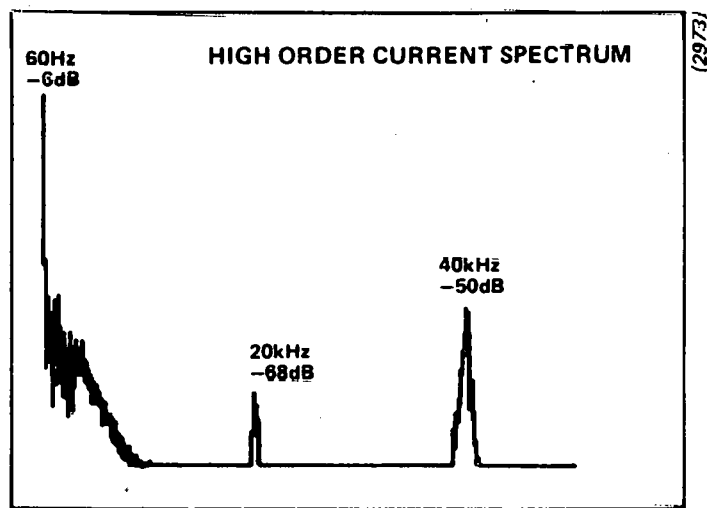


Figure 2.E.3 Harmonic Spectra of the BC/SCI line current due to switching noise

2.E.2 SOC Algorithm

The complete BC/SCI system was attached to a 54-cell battery composed of Gould PB-220 6V golf-cart batteries. Two complete discharge-charge cycles were performed and the results presented graphically in Figures 2.E.4 and 2.E.5.

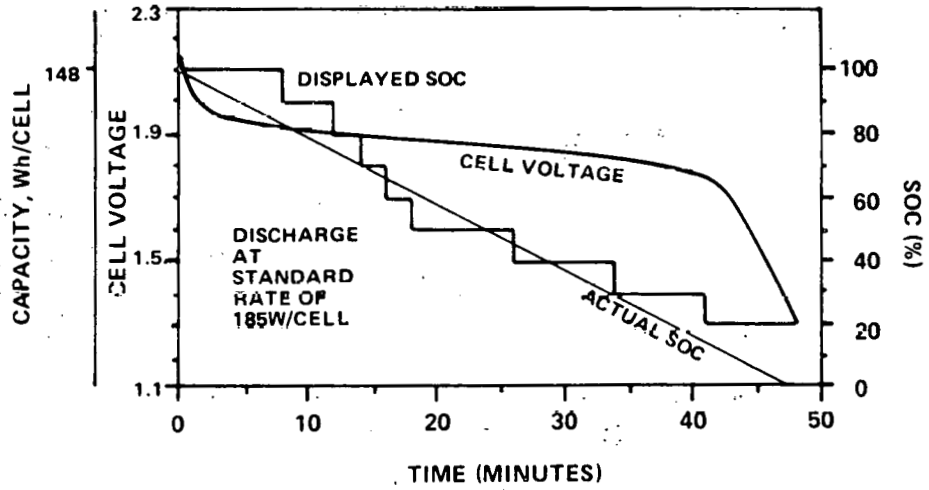
In Figure 2.E.4, the actual battery state-of-charge, the average cell voltage, and the displayed SOC is plotted as a function of time during a constant-power discharge of 10kW (185W/cell). The predicted SOC is optimistic near this end of the discharge. This is due in part to the poor performance of this particular battery pack (only 148Wh/cell compared with 200Wh/cell nominally) and the unavailability of a parameter adaptor in the implemented BC/SCI.

In Figure 2.E.5, a constant-power discharge was also performed, but two six-minute rest periods were included in the test to demonstrate the ability of the SOC to track battery recuperation. Again, the SOC is optimistic. The battery parameter adaptor was not included in the SOC hardware and software due to the time limitation of the contract. The adaptor would allow for more accurate SOC indications, especially with sub-standard battery packs.

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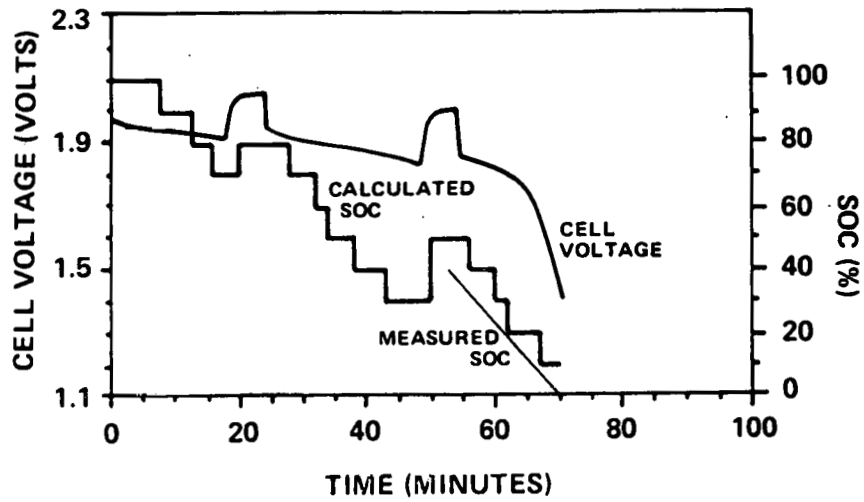
3. Conclusions and Recommendations

The BC/SCI system designed and constructed during this contract successfully fulfilled most of the original performance target goals. Some of the targets were revised during the program due to state-of-the-art limitations and the short duration of the program. Overall efficiency of the charger is 87% at an output power level of 1kVA which is consistent with the original goal of 90 percent or better at 3kVA. The weight of the entire BC/SCI system is under 531b including the pigtailed and interconnecting cables. The charger introduces a T.H.D. of 5% on the utility grid at the 1kW operating point. Although this is more than the original target, it is extremely low considering the present state-of-the-art. The power factor of the charger is at the targeted goal of 0.94.



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Figure 2 E 4 SOC test on a constant-power discharge (185W/cell)



(2975)

Figure 2.E.5 SOC test on a constant-power discharge (185W/cell) with rest intervals

The battery SOC algorithm implemented in the BC/SCI is capable of +0, -10% accuracy only when equipped with accurate battery parameters. The feasibility of tracking these battery parameters as the battery ages was demonstrated under laboratory conditions; however it is not included in the BC/SCI software set. The contract program was too short to complete the development required to implement the adaptor algorithm.

The battery recharge algorithm incorporates depth-of-charge information obtained while calculating the SOC. This charging information should prolong the life of the propulsion battery since the amount of overcharge is carefully controlled.

The impact of transformer isolation on circuit efficiencies and protection circuitry is significant. The inclusion of the transformer in the charger eliminates the only stiff voltage bus in the system (the battery) and makes measurements of the battery terminal voltage for circuit protection difficult. As a result, the transformer must be of extremely high quality, particularly in minimizing its leakage inductance, since no voltage source is available for snubbing.

The microcomputer system which exercises the algorithms is also complex. The self-diagnostics imbedded within the system are also mandatory in a computer of this size.

Some recommendations are suggested for future high performance EV battery chargers:

1. Elimination of the transformer in the charger circuit topology could increase the energy conversion efficiency by 3% or more. In addition, a more foolproof scheme of circuit protection could be instituted. There is, however, a safety requirement to isolate the input power line from the battery charging cables. Alternate means of accomplishing this isolation could be investigated.

2. The goal of limiting the RMS harmonic currents injected into the utility to 100mA or less is, in Gould's opinion, too strict. The 100mA limit is equivalent to 0.4% T.H.D. Utilities can be satisfied with significantly higher distortion. If the injected RMS current was 1A, the T.H.D. in the line current would only be 4%. This assumes full current operation of 25A_{RMS}. Gould recommends that 5% T.H.D. be the limit.

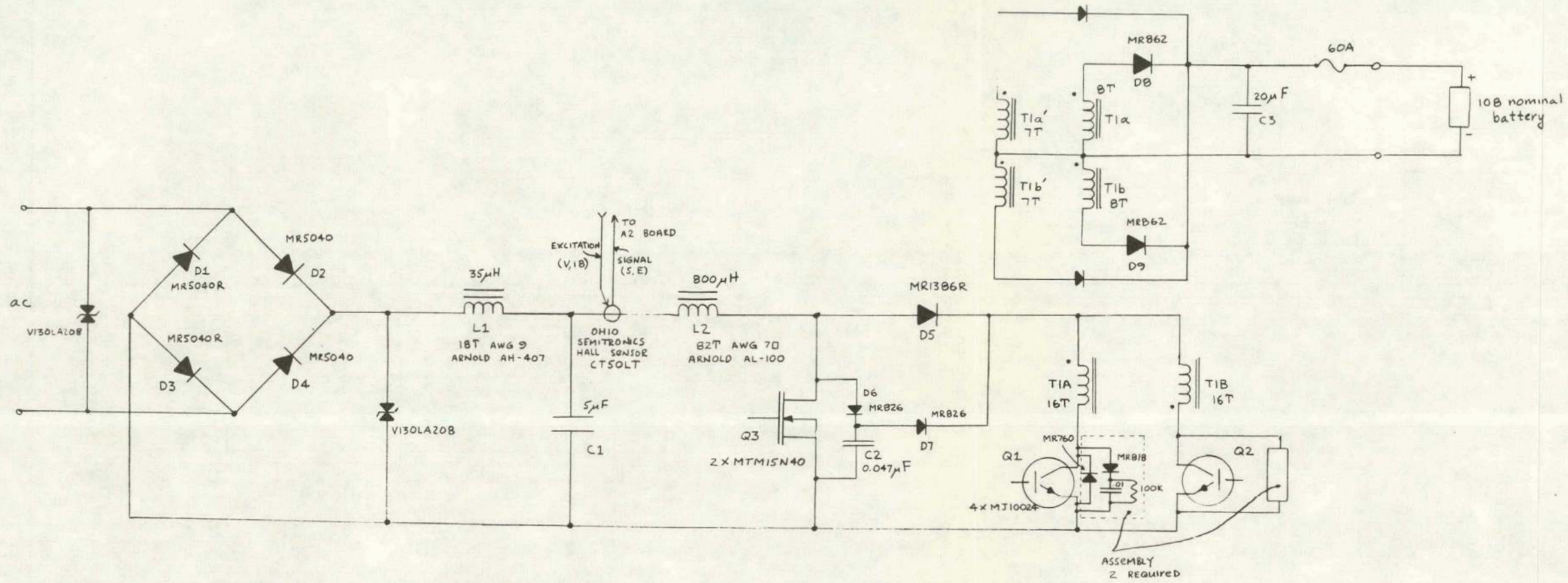
3. An adaptive algorithm is required to insure accurate (+0, -10%) SOC indication over the useful life of the battery. A significant development effort would be required to implement an algorithm with the existing hardware package. Gould recommends that this developmental effort be initiated.

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4. References

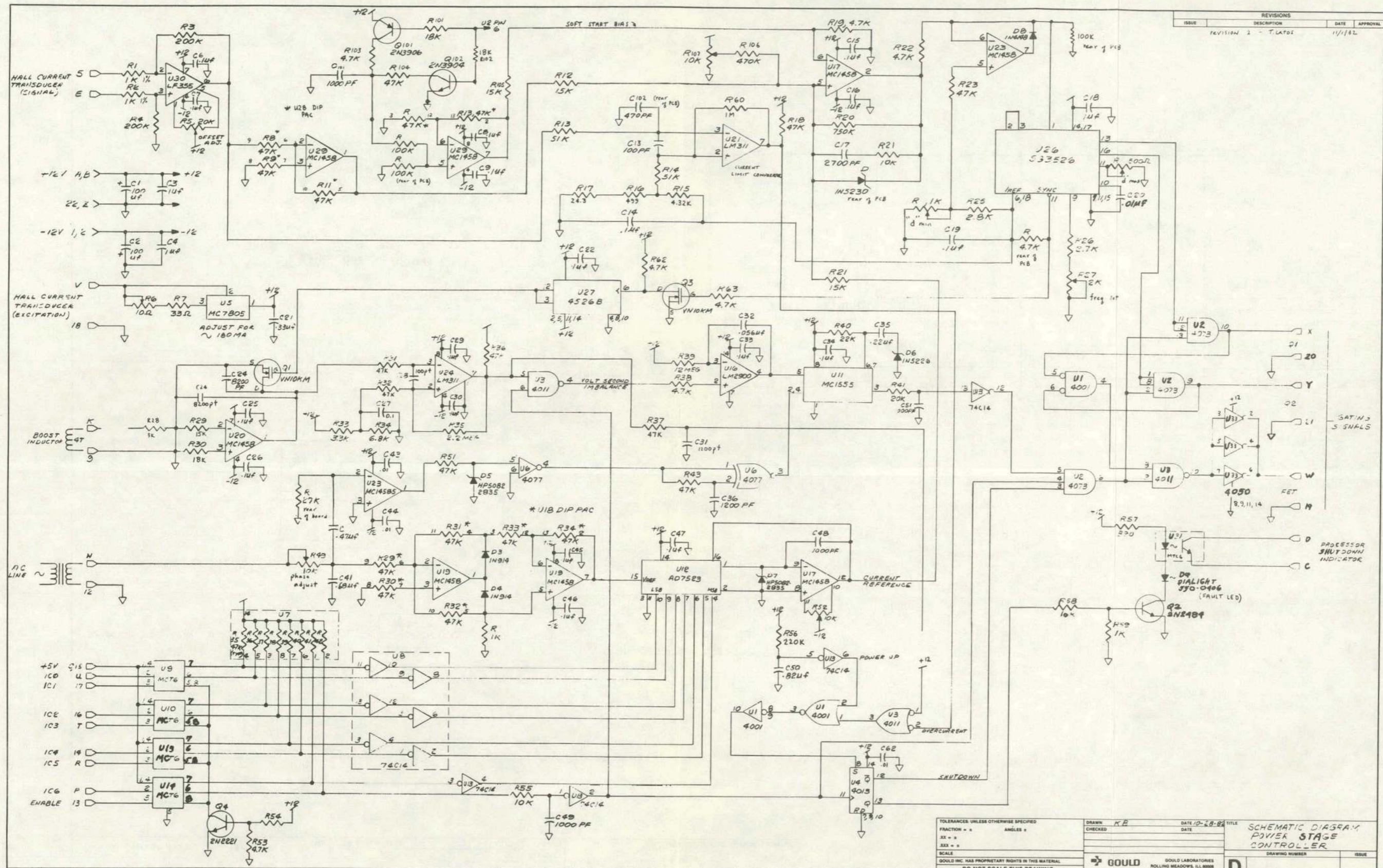
1. P.W. Clark, "Converter Regulation by Controlled Conduction Overlap," U.S. Patent 3,938,024, Feb. 10, 1976, assigned to Bell Laboratories, Inc., Murray Hill, NJ, 07974, USA.
2. H. L. Martin, "External Model for Performance Prediction of Lead-Acid Batteries in Electric Vehicle Usage--A Dynamic System Approach," Electric and Hybrid Vehicle Systems Development Laboratory 79-1, Purdue University, April 1979.
3. C. M. Shepherd, "An Equation Characterising the Discharge of a Battery," J. Electrochem. Soc. 112 (1965), 657-664.
4. Newman, John, and William Tiedmann, "Porous Electrode Theory with Battery Applications, AIChE, Vol. 21, No. 1, January, 1975, pp. 25-41.
5. deLevie, Robers, "Electrochemical Response of Porous and Rough Electrodes," Paul Delahy (ed.), Advan. Electrochem. Electrochem. Eng., 6, 329 (1967).
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T1 : FERROXCUBE U-I
 1F4-3CB
 184-3CB
 WINDINGS FOIL - 0.015" x 0.500"
 INSULATION 0.010" NUMEX

| | | | | | | | |
|--|------------|-----------------------------|--|--------------------|--|--------------------------------|-------|
| TOLERANCES: UNLESS OTHERWISE SPECIFIED | | DRAWN T. Latoj | | DATE 10 Nov 82 | | TITLE JPL BC/SCI POWER CIRCUIT | |
| FRACTION = ± | ANGLES = ± | CHECKED | | DATE | | | |
| .XX = ± | | | | | | | |
| .XXX = ± | | | | | | | |
| SCALE | | GOULD | | GOULD LABORATORIES | | DRAWING NUMBER | ISSUE |
| GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL | | ROLLING MEADOWS, ILL. 60008 | | | | | |
| DO NOT SCALE THIS DRAWING | | | | C | | | |



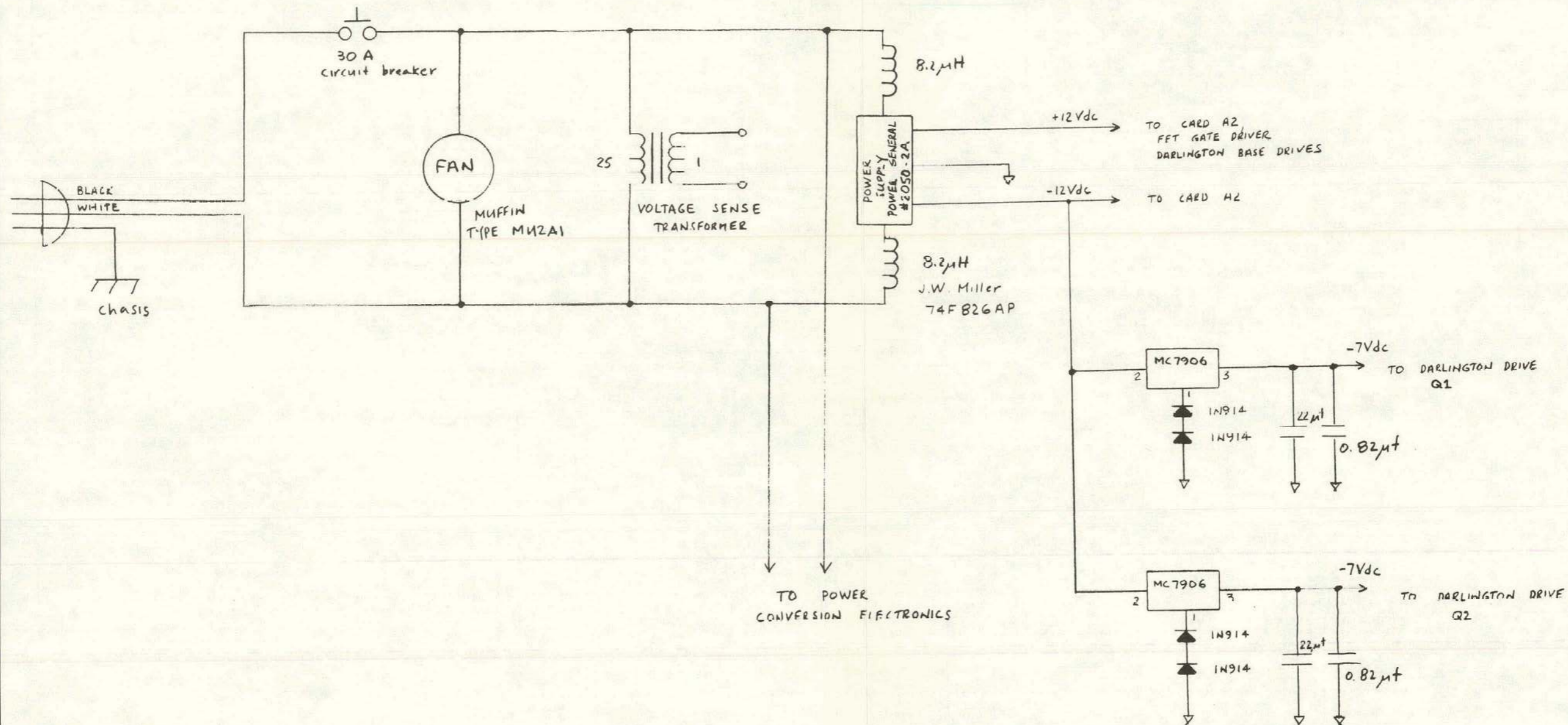
| REVISIONS | | | |
|------------|-------------|---------|----------|
| ISSUE | DESCRIPTION | DATE | APPROVAL |
| REVISION 2 | T. LATO | 11/1/82 | |

| | | | |
|---|--------------------|---|---|
| TOLERANCES UNLESS OTHERWISE SPECIFIED | DRAWN: <i>KE</i> | DATE: 10-28-82 | TITLE: SCHEMATIC DIAGRAM POWER STAGE CONTROLLER |
| FRACTION: $\frac{\quad}{\quad}$ | CHECKED: <i>KE</i> | DATE: | DRAWING NUMBER: |
| ANGLE: \angle | | | ISSUE: |
| SCALE: $\frac{\quad}{\quad}$ | | | |
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| GOULD | | <small>GOULD LABORATORIES ROLLING MEADOWS, ILL. 60068</small> | |

Figure 2.D.10 Power Circuit Controller

(Enlarged from page 104)

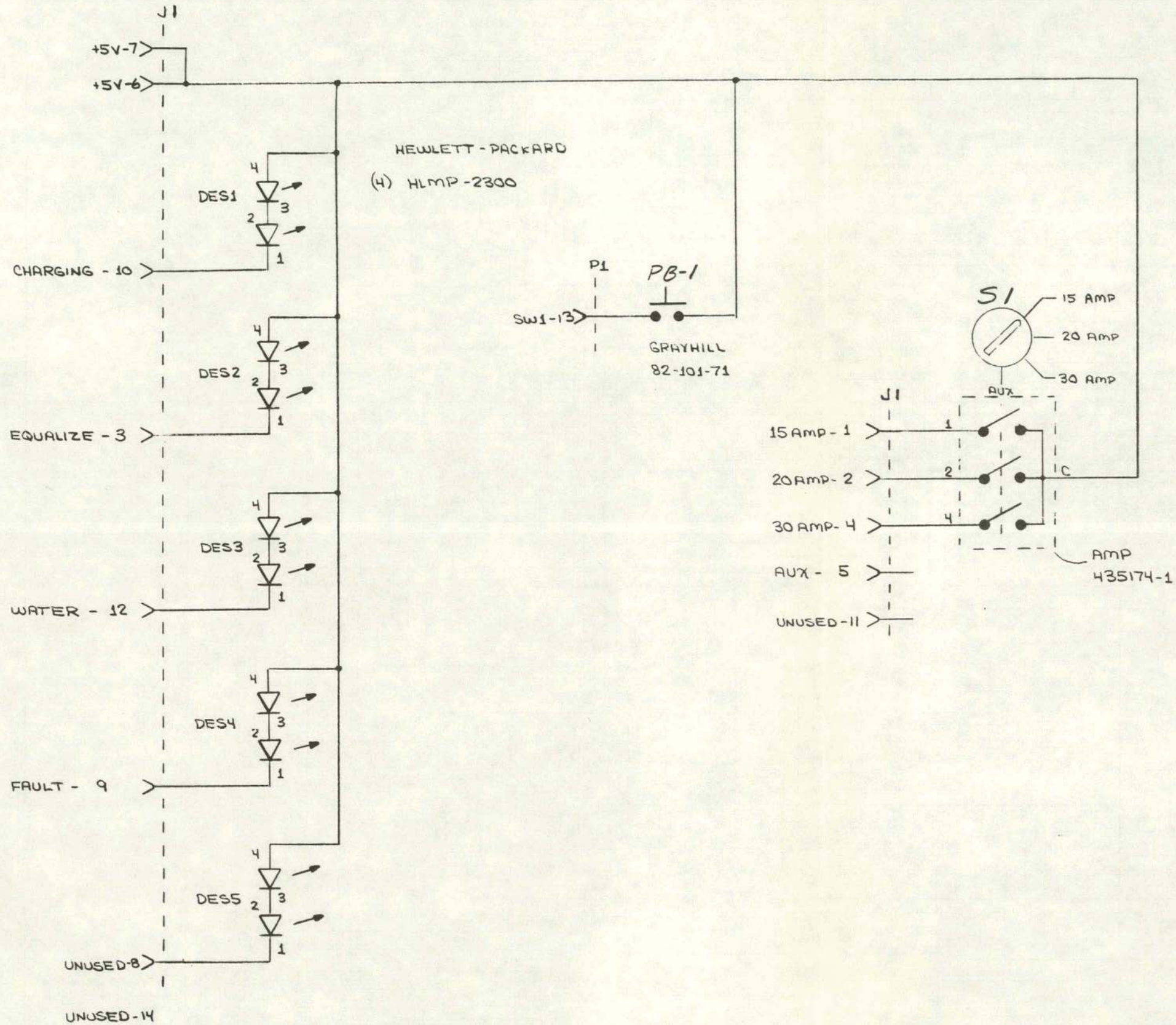
| REVISIONS | | | |
|-----------|-------------|------|----------|
| ISSUE | DESCRIPTION | DATE | APPROVAL |
| | | | |



TOLERANCES: UNLESS OTHERWISE SPECIFIED
 FRACTION = ± ANGLES ±
 .XX = ±
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DRAWN T. Latos DATE 9 Nov 82
 CHECKED DATE
 GOULD GOULD LABORATORIES
 ROLLING MEADOWS, ILL. 60008

TITLE ac Power Distribution
 AND
 dc Power Supply Schematic
 DRAWING NUMBER ISSUE

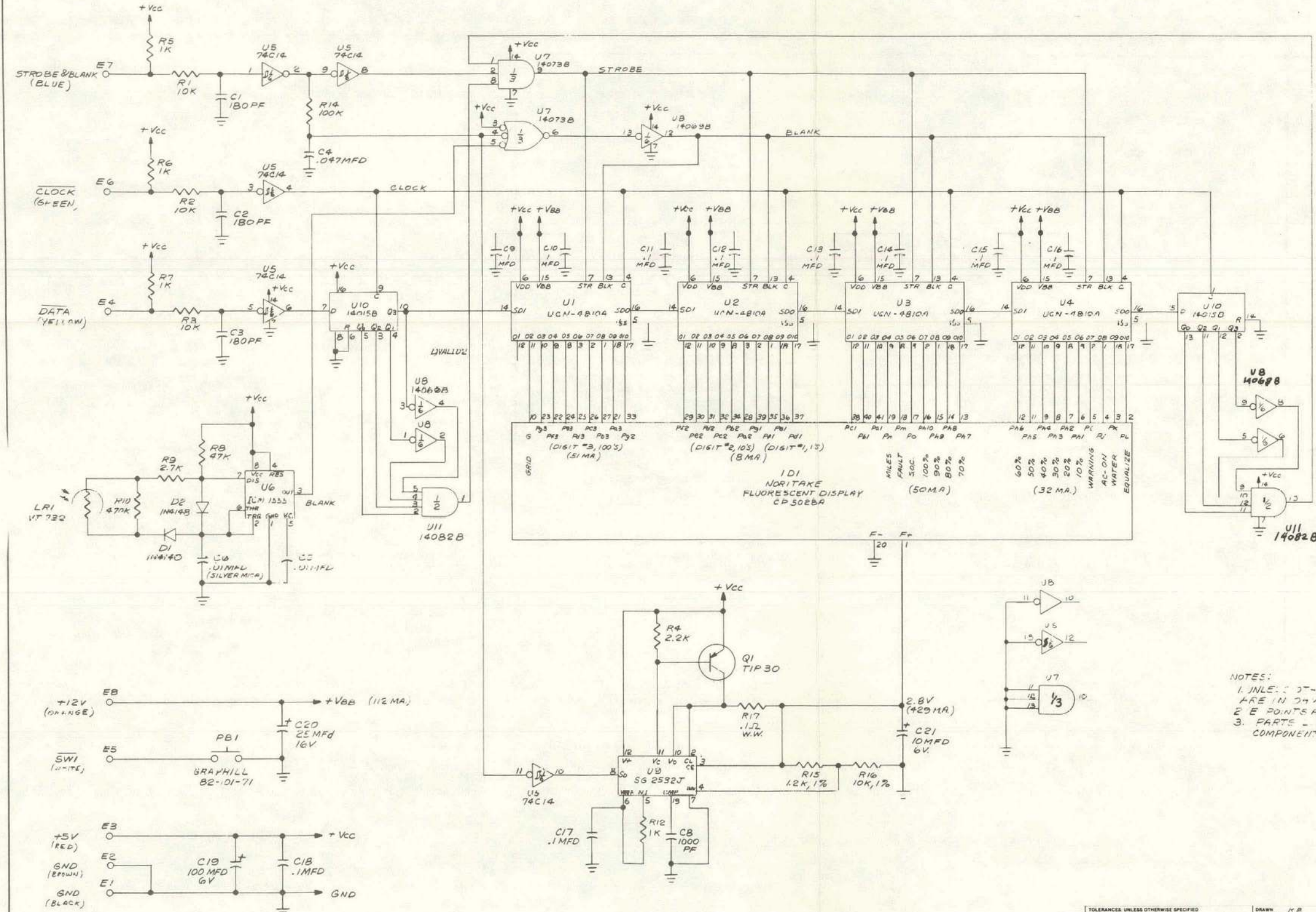


P1 - 14 PIN DIP SOCKET

FRONT PANEL - BC/SCI

SK-1101481

| REVISIONS | | | |
|-----------|-------------|------|----------|
| ISSUE | DESCRIPTION | DATE | APPROVAL |
| | | | |

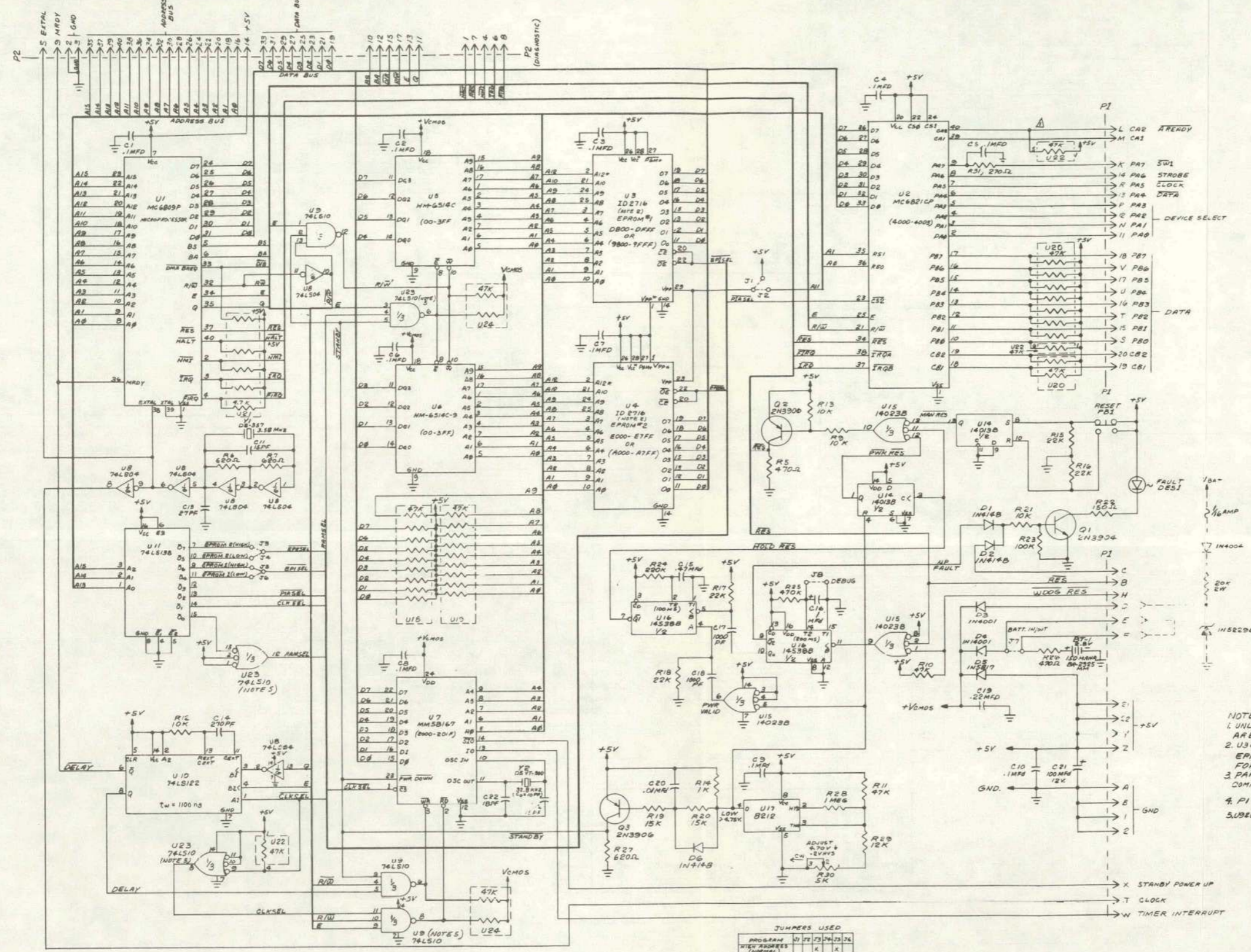


NOTES:
 1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4 WATT, 5%.
 2. SOLDER POINTS ARE SOLDER TERMINATION.
 3. PARTS LIST - PL-SK-422B.
 COMPONENT LAYOUT - SK

| | | | |
|--|--|-----------------------------|---|
| TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTION - 1/100 ANGLES - 1/16 | DRAWN BY CHECKED | DATE 11-29-69 | TITLE SCHEMATIC DIAGRAM, DISPLAY BOARD A1 |
| SCALE GOULD INC. HAS PROPRIETARY RIGHTS IN THIS MATERIAL DO NOT SCALE THIS DRAWING | GOULD GOULD LABORATORIES ROLLING MEADOWS, ILL. 60068 | DRAWING NUMBER SK-1422B1 | ISSUE |

| REV | DESCRIPTION | DATE | APPROVAL |
|-----|-------------|------|----------|
| | | | |

ARTWORK SK-1513B1, NOT CHANGED
FB 3-11-82



- NOTES:
- UNLESS OTHERWISE SPECIFIED RESISTORS ARE 1/4 WATT, 5%.
 - U3 & U4 MAY USE EITHER 16K, 32K, OR 64K EPROM CHIPS. * INDICATES PIN NOS FOR 64K CHIP.
 - PARTS LIST: PL-SK-1513B1. COMPONENT LAYOUT: SK-9513B1.
 - P1 SPARE PINS: 3, 5, 6, 7, 9, 10. SUBSTITUTION MANUFACTURER CANNOT BE SUBSTITUTED.

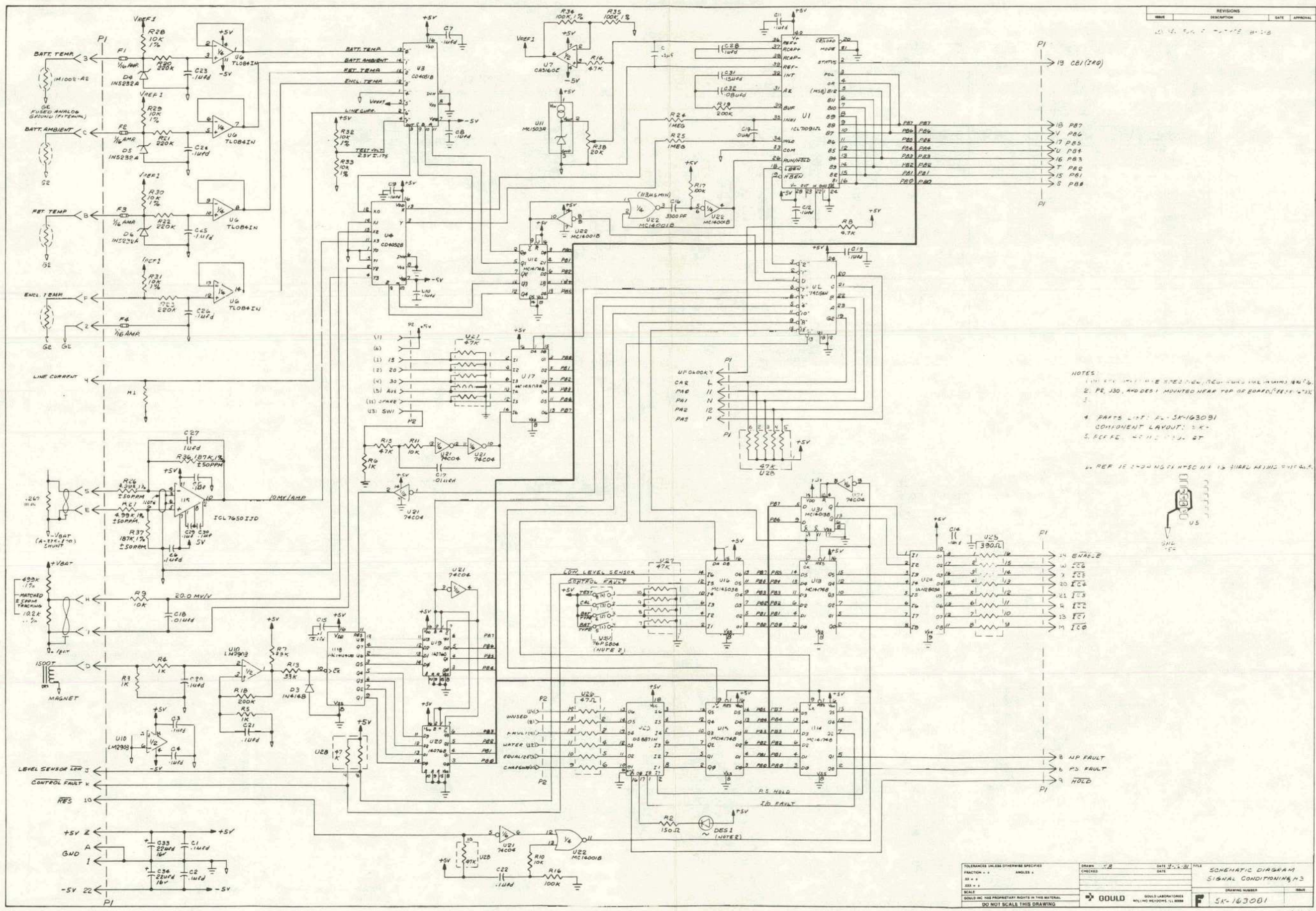
JUMPERS USED

| PROGRAM | J1 | J2 | J3 | J4 | J5 | J6 |
|----------------------------|----|----|----|----|----|----|
| WEEK ADDRESS (NORMAL) | X | X | X | X | X | X |
| LOW ADDRESS (RAMISE DEBUS) | X | X | X | X | X | X |
| 16K EPROM USED | X | | | | | |
| 32K EPROM USED | X | | | | | |
| 64K EPROM USED | X | | | | | |

X DENOTES USED

| | | | |
|---|---------------------|---------------|---------------------------------------|
| TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTION = X ANGLE = ° DIM = . | DRAWN BY CHECKED | DATE SCALE | SCHEMATIC DIAGRAM MICROCOMPUTER A2 |
| BOULL | DATE | SCALE | SK-1513B1 |

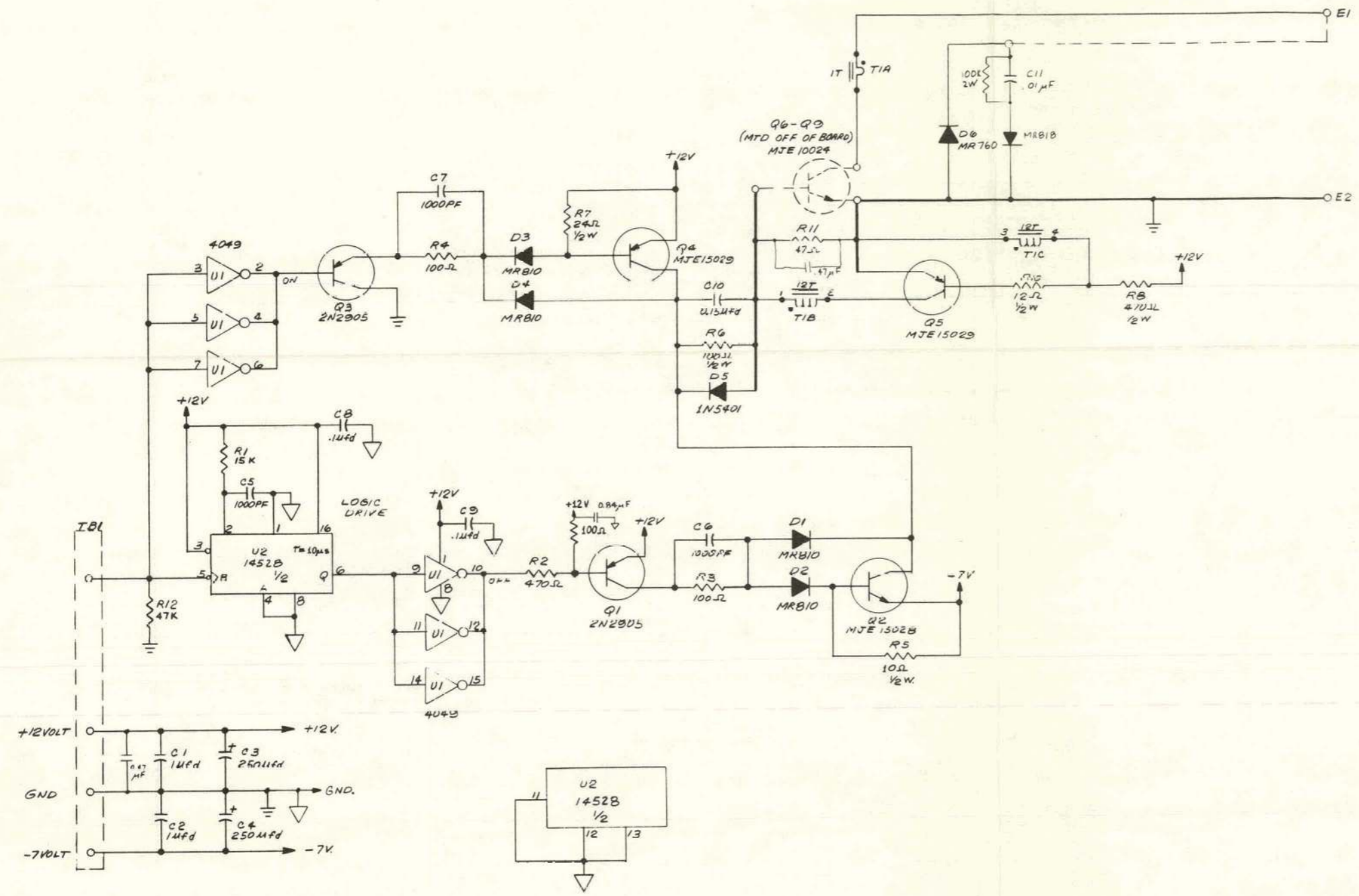
| REV | DESCRIPTION | DATE | APPROVAL |
|-----|-------------|------|----------|
| 1 | | | |



NOTES:
 1. THE BOARD IS TO BE MOUNTED ON A PCB WITH THE DIMENSIONS SHOWN.
 2. P1, P2, P3, AND P4 ARE MOUNTED NEAR THE TOP OF BOARD, P5 TO P10 ARE MOUNTED NEAR THE BOTTOM.
 3. THE BOARD IS TO BE MOUNTED ON A PCB WITH THE DIMENSIONS SHOWN.
 4. PARTS LIST: PL-5K-163091
 COMPONENT LAYOUT: 2X-
 5. SEE FIG. 40-111-101-01
 6. REF. TO FIG. 40-111-101-01 IS SHOWN AS THE PART NUMBER.

| | | | | | |
|---------------------------------------|--|----------|---------------|--------------|--------------------------|
| TOLERANCES UNLESS OTHERWISE SPECIFIED | FRAC. ± .1 | ANGLES ± | DRAWN: J.B. | DATE: 3-5-82 | TITLE: SCHEMATIC DIAGRAM |
| | ± .01 | | CHECKED: J.B. | | SIGNAL CONDITIONING PCB |
| | ± .005 | | | | |
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| | ± .001 | | | | |
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| REVISIONS | | | |
|-----------|-------------|---------|----------|
| ISSUE | DESCRIPTION | DATE | APPROVAL |
| ① | REVISION | 1/25/82 | K.C.D. |
| ② | REVISION | 1/11/82 | T.L. |



NOTES:
 1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE IN OHMS, 1/4 WATT, 5% TOL.
 2. REF. PARTS LIST: RL-SK-1921B1.

| | | | |
|--|---------------------------|---|---------------------------------------|
| TOLERANCES UNLESS OTHERWISE SPECIFIED | DRAWN <i>K.B.</i> | DATE 3-21-81 | TITLE SCHEMATIC DIAGRAM BASE DRIVE |
| FRACTION = 1/2 | CHECKED | DATE | |
| XXX = 1/2 | | | |
| SCALE | GOULD | GOULD LABORATORIES ROLLING MEADOWS, ILL. 60068 | DRAWING NUMBER D SK-1921B1 |
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Appendix 2

Alphabetical Glossary of BC/SCI FORTRAN Modules

Alphabetical Glossary of BC/SCI FORTRAN Modules

AVGFOR - This subroutine performs the required averaging of data for time constants greater than thirty seconds in duration. Battery current and temperature are averaged over one battery time constant (6 min), while vehicle speed and power are averaged over thirty seconds. Proper scaling to common engineering units is also performed by this routine.

BATMOD - This function models the battery in increments of time using the input parameters as a starting point and iteratively removes energy at constant power until the cutoff voltage is reached. The module is called with arguments for the present current, temperature, and state (amp-hours) of the battery, in addition to the desired values for the discharge power level and final cutoff voltage. The simulation iterates until the predicted voltage is less than the desired cutoff voltage. The function returns to the calling program with a value for the time (in hours) to cutoff.

CHGFOR - The charge monitor subroutine controls the BC/SCI operation during the charge cycle. The routine calculates the charge required to recharge a battery for a given temperature and depth of discharge. It also determines the appropriate voltage limit based upon electrolyte temperature and whether equalization is required. Charge acceptance and state of charge functions are also performed by this program.

DISFOR - The discharge monitor tracks parameters during a discharge and determines the battery state-of-charge for both the standard and arbitrary rates. Amp-hour meter compensation is also provided by comparing the known voltage with the predicted values. This error signal is appropriately "weighted" with a confidence factor.

EVALZD - This function calculates the battery parameter values from a two dimensional table. Using the indexes and fractions for each of the two dimensions of the battery parameter table, a linear interpolation is made to determine the actual value for a given temperature and current. This general approach allows the function to be used for all three battery parameters (R1, R2, Q2) using appropriate arguments.

FDELTA - The function calculates the fractional distance that a given value is between the two most adjacent elements in a list.

INIFOR - The initialization subroutine initializes all parameters normally stored in Fortran common area (RAM). These parameters include the I-T table of R1, R2 and Q2 determined for a set of 54-Gould PB220 lead-acid cells. Fortran scaling factors normally stored in random access memory are also initialized by this routine. If requested this program will also initialize the amp-hour meter using the equilibrium voltage and temperature as a direct determination for the battery's state of charge.

RSTFOR - The rest monitor subroutine, uses the battery voltage and temperature to determine a correction factor for the system amp-hour meter.

TEMPFN - This fixed shaped function is evaluated for a specific plateau and valley over a 40°C temperature range. The "V" shaped function is centered at 27.5°C and spans ±20°C.

VDROP - This function calculates the internal voltage term for the battery model's impedance. This factor is based upon the battery parameters (R1, R2, Q2) and present conditions (Q, I). The answer is scaled to a volts/cell basis.

VEQ - This function calculates the equilibrium voltage based upon battery state of charge and temperature. The calculated answer is scaled in volts per cell.

ZONE - This subroutine controls the table search and interpolation of the battery parameters as a function of current and temperature. The boundary values for the I-T matrix are defined by the subroutine.

ZRQQ1 - This function calculates the portion of the battery impedance term which is dependent upon state of charge. An upper limit is imposed for the maximum value for this term.

SPECIAL NOTES:

THKFOR - This subroutine is where the parameter adaptation scheme would normally be implemented. A dummy subroutine is included to satisfy all the symbol requirements of the linking loader.

NO UNDEFINED SYMBOLS

MEMORY MAP

| S | SIZE | STR | END | COMMENT |
|---|------|------|------|---------|
| A | 000E | FFF2 | FFFF | |
| B | 0041 | 0020 | 0060 | 0000 |
| C | 00FA | 0200 | 02F9 | 00FA |
| D | 03D9 | 0300 | 06D8 | 0033 |
| P | 2FBE | C000 | EF8D | 003E |

| MODULE NAME | BSCT | DSCT | PSCT |
|-------------|------|------|------|
| BCSCI | 0020 | 0300 | C000 |
| CHGMPL | 005B | 0314 | CA90 |
| INIFOR | 0061 | 0316 | CC60 |
| RSTFOR | 0061 | 032E | CFB0 |
| CHGFOR | 0061 | 0346 | D090 |
| TEMPFN | 0061 | 036E | D420 |
| DISFOR | 0061 | 03B2 | D4D0 |
| THKFOR | 0061 | 043E | D990 |
| BATMOD | 0061 | 043E | D7D0 |
| AVGFOR | 0061 | 04EA | DBE0 |
| VDROP | 0061 | 04EA | DCD0 |
| ZONE | 0061 | 0534 | DD60 |
| VEQ | 0061 | 05AA | DF60 |
| FDELTA | 0061 | 05C8 | DFE0 |
| EVAL2D | 0061 | 05F0 | E050 |
| ZRQ01 | 0061 | 062A | E140 |
| SQRT | 0061 | 065E | E1D0 |
| ABS | 0061 | 0672 | E270 |
| ET#R12 | 0061 | 0676 | E290 |
| ET#R03 | 0061 | 0676 | E2A0 |
| ET#R04 | 0061 | 0678 | E2E0 |
| ET#R14 | 0061 | 0686 | E3B0 |
| ET#R00 | 0061 | 0688 | E3F0 |
| ET#R01 | 0061 | 0688 | E6D0 |
| RTDUM | 0061 | 0688 | EBC0 |
| ET#R16 | 0061 | 0690 | EBD0 |
| ET#R26 | 0061 | 0694 | EC50 |
| F#V | 0061 | 069A | ECD0 |
| ERROR# | 0061 | 069A | ECF0 |
| ET#R08 | 0061 | 06A6 | ED80 |
| LPOUT | 0061 | 06A6 | EDB0 |
| CNOUT | 0061 | 06A6 | EE10 |
| IOPKG | 0061 | 06A6 | EE40 |
| EXIT | 0061 | 06A6 | EF40 |
| VECTOR | 0061 | 06A6 | EF50 |

COMMON SECTIONS

| NAME | S | SIZE | STR |
|--------|---|------|------|
| T# | D | 000F | 06A6 |
| .SCR## | D | 000C | 06B5 |
| .ADDM | P | 0004 | EF50 |
| .MPCOM | D | 0017 | 06C1 |
| .ERSTR | P | 0001 | EF54 |
| .LCRLF | P | 0003 | EF55 |
| .LFMFD | P | 0004 | EF58 |
| .LNRDY | P | 0017 | EF5C |
| .XBRKV | P | 0003 | EF73 |

. XCBRK P 0003 EF76
. CFMFD P 0004 EF79
. CNNUL P 0002 EF7D
. CIC D 0001 0&D8
. INIT P 0002 EF7F
. IOADR P 000E EF81
. M12CA P 0002 EF8C

DEFINED SYMBOLS

MODULE NAME: BCSCI

CCOUT B 0051 FCHGL B 0056 FFLT B 0033 FIRQ P C14C
FPIN B 004C ILINE D 0304 INTT P C003 IRQ P C129
SYIN B 004E

MODULE NAME: CHGMPL

CHGMPL P CA90

MODULE NAME: INIFOR

INIFOR P CC60

MODULE NAME: RSTFOR

RSTFOR P CFB0

MODULE NAME: CHGFOR

CHGFOR P D090

MODULE NAME: TEMPFN

TEMPFN P D420

MODULE NAME: DISFOR

DISFOR P D4D0

MODULE NAME: THKFOR

THKFOR P D990

MODULE NAME: BATMOD

BATMOD P D9D0

MODULE NAME: AVGFOR

AVGFOR P DBE0

MODULE NAME: VDROP

VDROP P DCD0

MODULE NAME: ZONE

ZONE P DD60

MODULE NAME: VEQ

VEQ P DF60

MODULE NAME: FDELTA

FDELTA P DFE0

MODULE NAME: EVAL2D

EVAL2D P E050

MODULE NAME: ZRQQ1

ZRQQ1 P E140

MODULE NAME: SQRT
SQRT P E1D0

MODULE NAME: ABS
ABS P E270

MODULE NAME: ET#R12
ET#R12 P E290

MODULE NAME: ET#R03
ET#R03 P E2A0

MODULE NAME: ET#R04
ET#R04 P E2E0

MODULE NAME: ET#R14
ET#R14 P E3E0 ET#R24 P E3E2

MODULE NAME: ET#R00
ET#R00 P E3F0 IM#R A 0000 NEG# P E40D SLOG# P E690
STADT# P E50C

MODULE NAME: ET#R01
ET#R01 P E6D0 RM#R A 0001

MODULE NAME: RTDUM
ERNUM# D 068E IM#RI# P EBC0 .PRI# P EBC0 SPND# P EBC0
WAIT P EBC1 WAITZ P EBC7

MODULE NAME: ET#R16
ET#R16 P EBD0

MODULE NAME: ET#R26
ET#R26 P EC50

MODULE NAME: F#V
F#V P ECD0

MODULE NAME: ERROR#
ERROR# P ECF0 STACK# A 00FF

MODULE NAME: ET#R0B
CLALL# P ED9C ET#R0B P ED80

MODULE NAME: L#OUT
L#ORLF P EDF# L#DAT1 P EDDE L#DATA P EDC8 L#OUT P EDB0

MODULE NAME: C#OUT
C#OUT P EE10 P#DATA# P EE29

MODULE NAME: I#PKG
I#NE P EED8 I#NP P EE91 I#NPE P EF35 INITLZ P EE40
L#OUT# P EEF8 L#CH# P EE94 L#ORLF# P EE85 P#DAT1# P EEC

MODULE NAME: EXIT
EXIT P EF40

PAGE 001 BCSCI . SA:1

```
0010      NAM      BCSCI
0012      OPT      REL, CRE, P=58, G, LLE=120
0014      TTL      -***- ENGINEERING PROTOTYPE -- VERSION 1.0 EXECUTIVE
0016 *
0018 *      9/29/82 ASSEMBLY DATE : J. R. M.
0020 *
0022 *      DISK #200 ( BACKUP : #210)
0024 *      BCSCI7 . SA  SOURCE FILE
0026 *      BCSCI7 . RO  OBJECT FILE
0028 *      BCSCI7 . LO  MEMORY IMAGE FILE
0030 *
0032 FROM   EQU      100      PROGRAM VERSION 1.00 IN FROM
0034 *
0036 *      SSTACK=#00-FF
0038 *      USTACK=#100-11F
0040 *      BSCT= $120-1BF      (SET TO $20)
0042 *      CSCT= $200-2FF
0044 *      DSCT= $300-7FF
0046 *      PSCT= $C000-DFFF & E000-EFFF
0048 *
0050      SFC      3
0052 *
0054 *      CMOS -- RANDOM ACCESS MEMORY TC-5517AP $0000-07FF
0056 *      NON-VOLATILE
0058 *
0060 SSTACK EQU      $FF      SYSTEM STACK AREA
0062 USTACK EQU      $11F     USER STACK AREA
0064 BSCT  EQU      $01      PAGE #1 DIRECT MODE ADDRESSING
0066 SPAD  EQU      $120     SCRATCH PAD AREA - AND FLAG STORAGE
0068 CELK  EQU      $200     COMMON BLOCK VARIABLE STORAGE
0070 CELKZ EQU      $220     COMMON BLOCK ZERO PRESET
0072 GLOBAL EQU      $300     GLOBAL DATA AREA
0074 RAMS  EQU      $000     FIRST RAM MEMORY LOCATION
0076 RAME  EQU      $7FF     LAST RAM MEMORY LOCATION
0078      SFC      3
0080      ASCT
0082      ORG      $2000
0084 *
0086 *      HARDWARE EQUATES
0088 *
0090 *      REAL TIME CLOCK - NATIONAL MM58167N $2000-$201F
0092 *
0094 *      COUNTERS - BCD CODED
0096 *
0098 RTCCTS EQU      *      90      THOUSANDTHS OF SECONDS
0100 RTCCHS EQU      *+1    99      HUNDREDTHS & TENTHS OF SECONDS
0102 RTCCS  EQU      *+2    59      SECONDS
0104 RTCCM  EQU      *+3    59      MINUTES
0106 RTCCH  EQU      *+4    29      HOURS
0108 RTCCDW EQU      *+5    07      DAY OF WEEK
0110 RTCCDM EQU      *+6    39      DAY OF MONTH
0112 RTCCMO EQU      *+7    19      MONTH
0114 *
0116 *      LATCHES - BCD CODED
0118 *
0120 RTCLTS EQU      *+8      THOUSANDTHS OF SECONDS  90
0122 RTCLHS EQU      *+9      HUNDREDTHS & TENTHS OF SECONDS  99
0124 RTCLS  EQU      *+10     SECONDS  59
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0126 RTCLM EQU *+11 MINUTES 59
0128 RTCLH EQU *+12 HOURS 29
0130 RTCLDW EQU *+13 DAY OF WEEK 07
0132 RTCLDM EQU *+14 DAY OF MONTH 39
0134 RTCLMO EQU *+15 MONTH 19
0136 *
0138 * INTERRUPT CONTROL & STATUS , ONCE EVERY :
0140 * MONTH, WEEK, DAY, HOUR, MIN. , SEC. , .1SEC. , COMP
0142 * D7 D6 D5 D4 D3 D2 D1 D0
0144 *
0146 RTCISR EQU *+16 INTERRUPT STATUS REGISTER ( READ )
0148 RTCICR EQU *+17 INTERRUPT CONTROL REGISTER ( WRITE ) 1 ENABLE
0150 *
0152 * RESET LATCHES & COUNTERS
0154 * MONTH, DAY OF MONTH, DAY OF WEEK, HOURS, MIN. , SEC. , .01&.1SEC. , .001SEC
0156 * D7 D6 D5 D4 D3 D2 D1 D0
0158 *
0160 RTCCRE EQU *+18 COUNTER RESET
0162 RTCLRE EQU *+19 LATCH RESET
0164 *
0166 * STATUS -- D0=1 COUNTER ROLLOVER
0168 *
0170 RTCSR EQU *+20 STATUS REGISTER
0172 *
0174 * SYNCHRONIZE -- RESET THOUSANDTHS OF SEC. , HUNDREDTHS & TENTHS OF SEC.
0176 * & SEC. COUNTER
0178 *
0180 RTCGO EQU *+21 RESET COUNTER "GO" COMMAND
0182 *
0184 * STANDBY INTERRUPT OUTPUT ENABLE D0=1
0186 *
0188 RTCSEY EQU *+22 STANDBY INTERRUPT
0190 RTCTST EQU *+23 TEST MODE
0192 *
0194 SPC 3
0196 ORG $4000
0198 *
0200 * PARALLEL INTERFACE ADAPTER -- MC 6821 $4000-$4003
0202 *
0204 PIA1AD EQU * DATA DIR. REGISTER -- DISPLAY CONTROL; DEV. SEL.
0206 PIA1AC EQU *+1 CONTROL REGISTER -- SYNC ; IRQ
0208 PIA1BD EQU *+2 DATA DIRECTION REGISTER -- CMOS DATA BUS
0210 PIA1BC EQU *+3 CONTROL REGISTER -- FIRO
0212 PAGE
0214 *
0216 * MULTIPLEXER ADDRESSES
0218 * (LABEL). -- INDICATES LABEL'S MUX ADDRESS
0220 *
0222 AI SET 0
0224 *
0226 * SINGLE ENDED ANALOG INPUTS
0228 *
0230 BIPO EQU $80 BIPOLAR INPUT FLAG
0232 *
0234 TBAT. SET AI BATTERY TEMPERATURE
0236 TAMB. SET AI+1 AMBIENT TEMPERATURE
0238 TFET. SET AI+2 FET TEMPERATURE
0240 TENC. SET AI+3 ENCLOSURE TEMPERATURE

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0242 ASI4.  SET    AI+4    UNUSED
0244 TREF.  SET    AI+5    REFERENCE TEMPERATURE
0246 ILINE. SET    AI+6    AC LINE CURRENT
0248 TEST.  SET    AI+7    TEST VOLTAGE
0250 *
0252 *      DIFFERENTIAL ANALOG INPUTS
0254 *
0256 ADI16. SET    AI+16   UNUSED
0258 VBAT.  SET    AI+32   BATTERY VOLTAGE
0260 IBAT.  SET    AI+48+BIPO BATTERY CURRENT
0262 *
0264 END.   SET    $FFFF   END OF SEQUENCE CHARACTER
0266       SPC    3
0268       DSCT
0270 **
0272 **      ABSOLUTE ADDRESS LABELS FOR FORTRAN/MPL ROUTINES
0274 **      OFFSET (XXX$) OF ANALOG IDENTIFER INTO GLOBAL AREA
0276 **
0278 IBAT   RMB    2        .1 AMP / BIT
0280 IBAT$  EQU    0
0282 VBAT   RMB    2        .050 V / BIT -> .926MVPC/BIT
0284 VBAT$  EQU    2
0286 ILINE  RMB    2
0288 ILINE$ EQU    4
0290 TREF   RMB    2
0292 TREF$  EQU    6
0294 TBAT   RMB    2
0296 TBAT$  EQU    8
0298 TAMB   RMB    2
0300 TAMB$  EQU    10
0302 TENC   RMB    2
0304 TENC$  EQU    12
0306 TFET   RMB    2
0308 TFET$  EQU    14
0310 TEST   RMB    2
0312 TEST$  EQU    16
0314       SPC    3
0316 **
0318 **      BLANK COMMON SECTION FOR FORTRAN & MPL MODULES
0320 **
0322       CSCT
0324 *      GLOBAL FLAGS : VOLATILE
0326 FMODE   RMB    2        MODE CONT. 0-NORM. ,1-REQ. CHNG. ,NEG. CHNG. GRANT
0328 WAKEF   RMB    2        BCD CODED (DAYS 0-30 ; HOURS 0-24)
0330 VLM     RMB    2        VOLTAGE LIMIT SETPOINT
0332 FINTF   RMB    2        FORTRAN INITIALIZATION FLAG
0334 *      GLOBAL DATA INSTANTANEOUS : VOLATILE
0336 XIBAT   RMB    2        DUPLICATION OF IBAT IN DSCT
0338 XVBAT   RMB    2        DUPLICATION OF VBAT IN DSCT
0340 TBATL   RMB    2        1C / BIT
0342 SPEED   RMB    2        PULSES / 6 SEC.
0344 *      GLOBAL DATA FILTER : VOLATILE (REAL DATA TYPE)
0346 AMP$F   RMB    4        BATTERY CURRENT - AMPS
0348 TEMPF   RMB    4        BATTERY TEMPERATURE - DEGREES C
0350 PWR$F   RMB    4        POWER OUT OF BATTERY - WATTS / CELL
0352 SPDF    RMB    4        VEHICLE SPEED - PULSES / HOUR
0354 *      GLOBAL DATA : NON-VOLATILE
0356 AMPH    RMB    4        3.694XE-6 AMR / BIT -> .2421 A-HR/BIT (2BYTE)

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0358 QLAST RMB 2 AMP-HOUR METER AFTER LAST CHARGE CYCLE
0360 QABS RMB 2 ABSOLUTE DISCHARGED AMP-HOURS SINCE EQUALIZE
0362 * GLOBAL VARIABLES : NON-VOLATILE
0364 FRST RMB 2 REST MODE FLAG
0366 FCHG RMB 2 CHARGE MODE FLAG "0"--NO "NEG"--YES "POS"--SPECIAL
0368 FTHK RMB 2 THINK MODE FLAG
0370 FEQU RMB 2 EQUALIZE STATUS FLAGS
0372 RESET RMB 2 NON-VOLATILE MEMORY RESET FLAG
0374 SPDCAL RMB 2 SPEED TRANSDUCER CALIBRATION FACTOR
0376 DSOC RMB 2 ALGORITHM S. O. C. INFORMATION
0378 DMILE RMB 2 ALGORITHM MILEAGE INFORMATION
0380 DISTIM RMB 2 TIME SINCE LAST SELF-DISCHARGE
0382 EQUTIM RMB 2 TIME SINCE LAST EQUALIZE
0384 CHGTIM RMB 2 TIME SINCE START OF CHARGE CYCLE
0386 SPC 3
0388 **
0390 ** GLOBAL VARIABLES NOT IN COMMON SECTION ( USED BY MPL )
0392 **
0394 XDEF ILINE
0396 XDEF FCHGL,FFLT
0398 XDEF CCOUT,FPIN,SYIN
0400 SPC 3
0402 **
0404 ** STARTING ADDRESSES FOR INTERRUPT VECTORS
0406 **
0408 XDEF INIT,FIRQ,IRQ
0410 SPC 3
0412 **
0414 ** EXTERNAL LABELS
0416 **
0418 XREF CHGMPL
0420 XREF CHGFOR,DISFOR,RSTFOR,THRFOR
0422 XREF INIFOR
0424 SPC 3
0426 **
0428 ** INSERT VARIABLE OFFSET FOR STORAGE LOCATION INTO 1ST BYTE
0430 ** OF ANALOG IDENTIFIER
0432 **
0434 IBAT. SET IBAT**$100+IBAT.
0436 VBAT. SET VBAT**$100+VBAT.
0438 ILINE. SET ILINE**$100+ILINE.
0440 TREF. SET TREF**$100+TREF.
0442 TBAT. SET TBAT**$100+TBAT.
0444 TAMB. SET TAMB**$100+TAMB.
0446 TENC. SET TENC**$100+TENC.
0448 TFET. SET TFET**$100+TFET.
0450 TEST. SET TEST**$100+TEST.
0452 PAGE
0454 **
0456 ** SYSTEM EQUATES
0458 **
0460 WARM EQU $AA55 VALID WARM-START FLAG
0462 ROMS EQU $C000 START ADDRESS - ROM CHECK SUM TEST
0464 ROME EQU $FFFF END ADDRESS
0466 *
0468 * PIA CONFIGURATION DDR:DATA DIRECTION REG. ; PR:PERIPHERAL REG.
0470 *
0472 PIAADR EQU %00110001 CB1(IN) NEG. - IRQ ENABLED; CB2(OUT)="0"; DDR

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0474 FIAAFR EQU      Z00110101                      ;PR
0476 FIAADR EQU      Z00111011 CA1(IN) POS. - FIRQ ENABLED; CA2(OUT)="1"; DDR
0478 FIAAFR EQU      Z00111111                      ;PR
0480 DSON EQU        FIAAFR! $F7 CA2 "0" DEVICE SELECT ACTIVE
0482 DSOFF EQU       FIAAFR CA2 "1" DEVICE SELECT DISABLED
0484 SPC             3
0486 **
0488 ** LOCAL VARIABLE STORAGE AREA -- DIRECT MODE ADDRESSING
0490 **
0492 BSCT
0494 FIAHAD RMB       1 DUMMY COPY OF FIAHAD (FIA REGISTER)
0496 WARMF RMB        2 WARM-START FLAG INDICATES WATCH-DOG RESET
0498 FINT RMB         1 INITIALIZATION FLAG
0500 ISECC RMB        1 INTERRUPT SECONDS COUNTER
0502 MUXPTR RMB       2 MULTIPLEXIER TABLE POINTER
0504 LVALUE RMB       2 TEMPORARY STORAGE OF LAST A/D VALUE
0506 DVALF RMB        1 DATA VALID FLAG
0508 CADC RMB         1 A/D CYCLE COUNTER
0510 FAVG RMB         1 DATA AVERAGE FLAG
0512 FCAL RMB         2 CALIBRATE MODE FLAG
0514 SFDC RMB         1 SPEED LOOP COUNTER
0516 FSHUTD RMB       1 SHUTDOWN DELAY FLAG
0518 FMODE2 RMB       1 ADC CHANGE FLAG
0520 FMODE RMB        2 POINTER FOR PRESENT OPERATING MODE
0522 FFLT RMB         1 FAULT DISPLAY FLAG "1" ACTIVE
0524 FTST RMB         2 TEST DISPLAY FLAG "1" ACTIVE; RUNNING
0526 DDELAY RMB       1 FLAG USED TO HOLD SW1 REMOTE DISPLAY BUTTON
0528 DEFLT RMB        1 DEFAULT FLAG; FORCES DEFALUT SETTINGS
0530 TSTPTR RMB       2 TEST ROUTINE TABLE POINTER
0532 DFLTC RMB        1 FAULT DELAY COUNTER
0534 VFDATA RMB       6 TRANSMITTED PATTERN SEQUENCE
0536 DSTAT RMB        1 WARN, AC-ON, WATER, EQUALIZE; FAULT, BAR, NUM, GRID
0538 DSTATM RMB       1 DISPLAY STATUS MASK
0540 DBAR RMB         1 BINARY CODED BAR POSITION
0542 DNUM RMB         3 100'S 10'S 1'S
0544 DIVW RMB         2 DIVIDER WORKSPACE
0546 LOOPC RMB        1 TRANSMIT LOOP COUNTER
0548 BITC RMB         1 TRANSMIT BYTE COUNTER
0550 DISAF RMB        1 POWER STAGE DISABLE FLAG
0552 FFIN RMB         2 FRONT PANEL INPUTS
0554 SYIN RMB         1 SYSTEM INPUTS
0556 AXIN RMB         2 AUX. INPUTS
0558 CCOUT RMB        1 CHARGER CONTROL OUTPUTS
0560 FFOUT RMB        2 FRONT PANEL OUTPUTS; MASK
0562 AXOUT RMB        1 AUXILIARY OUTPUTS
0564 CHGF RMB         1 CHARGE FLAG & DELAY COUNTER
0566 FCHGL RMB        1 CHARGE INDICATOR
0568 FWARN RMB        1 WARNING INDICATOR
0570 FFLASH RMB       1 FLASH COUNT
0572 FLASHV RMB       1 VFD FLASH
0574 FLASHL RMB       1 LED FLASH
0576 SPC             3
0578 **
0580 ** LOCAL VARIABLE STORAGE AREA -- NON-VOLATILE
0582 **
0584 DSCT
0586 EDELAY RMB       2 ELECTROLYTE DELAY COUNT
0588 *

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0590 *   PROM IDENTIFIER BYTES
0592 *
0594       PSCT
0596 ID    FCB    PROM    PROM I. D. BYTES VERSION #
0598       FCB    $12    PROM SEQUENCE # (i. e. 1/ST OF 2 PROMS )
0600 CKSUM FCB    $FF    CHECK SUM TEST BYTE
0602       PAGE
0604 **
0606 **
0608 **   HARDWARE INITIALIZATION SEQUENCE - RESET
0610 **
0612 **
0614 INIT  ORCC   $450    MASK INTERRUPTS (SWI RE-ENTRY)
0616       LDS   $SSTACK INITIALIZE SYSTEM STACK POINTER
0618       LDU   $CLOCAL  INITIALIZE GLOBAL POINTER
0620       LDA   $BSCT    .
0622       TFR   A,DF    INITIALIZE DIRECT PAGE REGISTER
0624 *
0626       LBSR  PIAINT  INITIALIZE PIA
0628 *
0630 *   POWER-UP OR WATCH-DOG RESET
0632 *
0634       LDA   .AXOUT   NORMAL POWER-UP RESET? HOLD OFF
0636       BPL   INIT1   YES
0638       LDD   WARMF   WARM-START FLAG
0640       CMPD  $WARM   VALID
0642       LBEQ  WSTART  YES, JUMP TO WARM START ENTRY POINT
0644 *
0646 *   NORMAL START-UP : RUN COMPLETE DIAGNOSTICS & INITIALIZE SYSTEM
0648 *
0650 *   INITIALIZE SYSTEM FLAGS & SCRATCH PAD AREA
0652 *
0654 INIT1  LDX   $SPAD+1 LOWER ADDRESS LIMIT +1 (NOT PIAXAD)
0656 INIT1A CLR   0,X+   CLEAR BYTE
0658       CMPX  $CBLKZ  UPPER ADDRESS LIMIT
0660       BLO  INIT1A
0662       LDA  $82
0664       STA  .AXOUT   SET: HOLD, OC FAULT; RESET: I/O FAULT, LPS FAULT
0666       CLR  CCOUT   DISABLE POWER STAGE
0668       LDD  $0F0F
0670       STD  .FFOUT  SET: FAULT, CHG, ECU, WATER (LED'S)
0672       LBSR DOUT
0674       LBSR DINPUT  INITIALIZE INPUT SWITCH POSITIONS
0676 *
0678 *   RUN SYSTEM DIAGNOSTIC - UC
0680 *
0682       LBSR  PIATST  RUN DIAGNOSTICS ON PIA
0684       LBSR  ROMTST  TEST PROGRAM MEMORY - BYTE CHECKSUM
0686       LBSR  WDOG    RESET WATCH-DOG TIMER
0688       LBSR  RAMTST  TEST VARIABLE MEMORY - BIT TOGGLE
0690       LBSR  CLKTST  TEST REALTIME CLOCK
0692 *
0694       LDA  RTCISR
0696       BITA $01     TIMER COMPARE - WAKE-UP MODE
0698       BEQ  INIT1B
0700       LDA  RTCLDM
0702       CMFA $02     1 DAY OR LONGER WAKE-UP PERIOD
0704       BHS  INIT1B  YES: DON'T RUN FORRST SUBROUTINE

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0706      LDX      #-1
0708      STX      FRST      SET FLAG FOR REST MODE
0710 INIT1B CLR      RTCSEY   DISABLE STANDBY INTERRUPT
0712 *
0714      LBSR     TIMEA      CORRECT TIME COUNTERS FOR SHUTDOWN PERIOD
0716      LDD      EQUIM
0718      CMFD     #5040      TEST FOR 7 DAYS
0720      BLO     INIT1C      NO: DON'T EQUALIZE
0722      LDD      #-1
0724      STD     FEQU       SET EQUALIZE FLAG
0726      STD     FCHG       SET CHARGE REQUEST FLAG
0728 *
0730 *      INITIALIZE CONTROL FLAGS
0732 *
0734 INIT1C LDD      #-1
0736      STA     FINT       SET INITIALIZATION FLAG
0738      STD     FMODE      SET MODE CHANGE
0740      LBSR     DINFUT     INPUT SWITCH POSITIONS-CHANGE FLAG INITIZATION
0742 *
0744      LDA     FFIN       CHECK FOR SPECIAL CHARGE CYCLE REQUEST
0746      BITA     #480       EQUALIZE BUTTON DEPRESSED?
0748      BEQ     INIT2      NO
0750      LDD     #1         SET SPECIAL CYCLE REQUEST FLAG
0752      STD     FCHG
0754 *
0756 INIT2  LBSR     SMODE     DETERMINE REQUESTED OPERATING MODE
0758 *
0760      LBSR     PWRST      TEST NON-VOLATILITY OF RAM
0762 *
0764      TST     DEFLT      RAM DATA VALID
0766      BEQ     INIT2B     YES
0768 *
0770      LDX     #CELKZ     1ST DATA LOCATION IN COMMON AREA
0772 INIT2A CLR      0,X+     ZERO DATA STORAGE AREA
0774      CMFX     #RAME      LAST MEMORY LOCATION-1
0776      BLO     INIT2A     NOT YET
0778 *
0780 *      RUN DIAGNOSTICS - SIGNAL CONDITIONING (I/O)
0782 *
0784 INIT2B LDA     #484
0786      STA     AXOUT      SET: HOLD, I/O FAULT, ; RESET: OC FAULT, LPS FAULT
0788      LBSR     DOUT2      UPDATE AUX OUTPUTS
0790 *
0792 *      INITIALIZE ADC FOR PROPER DIAGNOSTICS
0794 *
0796      CLR     RTCICK      INHIBIT TIMER INTERRUPTS
0798      LDA     PIA1AD      CLEAR FIRQ FLAG
0800      LDA     PIA1BD      CLEAR IRQ FLAG
0802      LDX     PMODE
0804      PSHS    X           SAVE NORMAL MODE POINTER
0806      LDX     #TBLDIA
0808      STX     PMODE      SET DIAGNOSTIC MODE
0810      LDA     #01
0812      STA     FMODE2     FLAG MODE CHANGE TO ADC ROUTINE
0814 INIT3  CHAI     #4EF     ENABLE IRQ
0816      TST     FAVG       ALL DIAGNOSTIC INPUTS READ?
0818      BEQ     INIT3      NO
0820      ORCC     #450       MASK ALL INTERRUPTS

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0822      LDB      FFLT      CHECK FOR ADC FAULTS
0824      BEQ      INIT4     NONE
0826      LBSR     ERROR     DISPLAY FAULT
0828 INIT4  FULS      X
0830      STX      FMODE     RETRIEVE NORMAL MODE POINTER
0832      INC      FMODE2    SET MODE CHANGE FLAG
0834      CLR      DVALF     DATA NOT VALID
0836 *
0838      LBSR     ADCTST    TEST A/D CONVERTER ON KNOWN INPUT
0840 *
0842      LBSR     TMPTST    TEST THERMISTORS FOR OPENS OR SHORTS
0844 *
0846      LDA      #B80
0848      STA      AXOUT     SET: HOLD ; RESET: BOARD FAULT LED'S
0850      LBSR     DOUT2
0852 *
0854 INIT5  LDD      #F0
0856      STD      FPOUT     RESET ALL FRONT PANEL LED'S
0858      LBSR     DOUT1
0860 *
0862      CLR      FINT      INITIALIZATION COMPLETE
0864 *
0866 *      WARM-START ENTRY POINT
0868 *
0870 WSTART LDA      PIA1BD   CLEAR IRQ FLAG
0872      LDA      RTCISR   CLEAR PRIOR INTERRUPTS
0874      LDA      PIA1AD   CLEAR FIRO - FLAG
0876      LDA      #F04
0878      STA      RTCICR   SET TIMER INTERRUPT - 1 SEC.
0880      LDD      #WARM
0882      STD      WARMF     SET SYSTEM RUNNING CODE
0884      ANDCC   #BAF     ENABLE FIRO & IRQ
0886      LDU      #USTACK   SET USER STACK FOR FORTRAN USE
0888      SPC      3
0890 **
0892 **      INITIALIZE FORTRAN PROGRAMS
0894 **      AFTER A POWER LOSS OR SPECIAL REQUEST
0896 **
0898      LDD      FCHG
0900      CNPD     #0
0902      BGT      EXECI     REQUEST SPECIAL CHARGE CYCLE
0904      TST      DEFLT
0906      BEQ      EXEC
0908 EXECI  JSR      INIFOR   RUN INITIALIZATION
0910      CLR      DEFLT
0912      SPC      3
0914 **
0916 **      FORTRAN ENTRY AND RETURN EXECUTIVE
0918 **
0920 EXEC   LDD      FMODE     MODE CHANGE GRANTED?
0922      BMI      EXEC      YES - WAIT FOR EXECUTIVE TO RECONIZE
0924      TST      DVALF     DATA VALID FOR FORTRAN ROUTINE ?
0926      BEQ      EXEC      NO - WAIT FOR MODE CHANGE TO BE COMPLETED
0928      LDY      FMODE     DETERMINE SELECTED MODE
0930      JSR      [FOR.Y]   ENTER APPROPRIATE FORTRAN MODE ROUTINE
0932      BRA      EXEC      SELECT NEW MODE
0934      PAGE
0936 **
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0938 **      INTERRUPT SERVICE ROUTINE : IRQ
0940 **
0942 **      TRIGGERED BY END OF CONVERSION SIGNAL FROM A/D CONVERTER
0944 **
0946 **
0948 IRQ     LBSR   ACONV   SERVICE ADC , AVERAGE VALUES , CAL. AMP-HOURS
0950       TST    FINT    INITIALIZATION?
0952       BNE    IRQ1    YES, RETURN
0954 *
0956       LBSR   DINPOT   READ DIGITAL INPUTS
0958 *
0960       LBSR   SMODE   SELECT PROPER OPERATING MODE
0962 *
0964       LBSR   INVSP   READ VEHICLE SPEED
0966 *
0968       LBSR   SAFETY   CHECK MISC. FAULT CONDITIONS
0970 *
0972       LBSR   DISSEL   SELECT PROPER DISPLAY
0974 *
0976       LBSR   DOUT    OUTPUT DIGITAL INFORMATION
0978 *
0980       LBSR   CDISP   CONFIGURE VACUUM FLUORESCENT ELEMENTS
0982 *
0984       LBSR   VFDISP  TRANSMIT INFORMATION TO DISPLAY
0986 *
0988 IRQ1    LDA     RTCISR  ACKNOWLEDGE MISSED CLOCK INTERRUPT
0990       RTI
0992       SFC     6
0994 **
0996 **      INTERRUPT SERVICE ROUTINE : FIRQ
0998 **
1000 **      1/SEC. TIMER - REAL TIME CLOCK
1002 **
1004 **
1006 **
1008 FIRQ    PSHS   A,B,X,Y  SAVE PRESENT STATE
1010       LDA    PIA1AD  CLEAR FIRQ FLAG
1012       LDA    RTCISR  ACKNOWLEDGE INTERRUPT
1014       CMPA  #404    TEST 1/ SEC
1016       BEQ   FIRQ1   OK
1018       LDB   #ERRCLO
1020       STB   FFLT    SET FAULT CODE
1022 FIRQ1  COM    FFLASH  TOGGLE FLASH BIT
1024       LDA   ISECC   ADVANCE SECONDS COUNTER
1026       INCA
1028       CMPA  #120    WAIT 2 MINUTES
1030       BLO   FIRQ2
1032       LDD   #401    SET FOR 10COUNT ADVANCE (2 MIN.)
1034       LBSR  TIME    ADVANCE TIME LOCATIONS
1036       CLRA  RESET COUNTER
1038 FIRQ2  STA    ISECC
1040       PULS  A,B,X,Y
1042       RTI
1044       PAGE
1046 **
1048 **      A/D CONVERTER SERVICE ROUTINE - INTERSIL 7109 ADC
1050 **
1052 **      2 BYTE READS   12 BIT MAGNITUDE VALUE , POLARITY , OVERRANGE

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| | | B11 - B0 | B15 | B14 |
|-------------|------|----------|--|-----|
| 1054 ** | | | | |
| 1056 ** | | | | |
| 1058 ** | | | | |
| 1060 ** | | | | |
| 1062 ** | | | | |
| 1064 ** | | | | |
| 1066 ** | | | | |
| 1068 ** | | | | |
| 1070 ** | | | | |
| 1072 ** | | | | |
| 1074 ** | | | | |
| 1076 ** | | | | |
| 1078 ** | | | | |
| 1080 ** | | | | |
| 1082 ** | | | | |
| 1084 ** | | | | |
| 1086 ** | | | | |
| 1088 ** | | | | |
| 1090 ** | | | | |
| 1092 ** | | | | |
| 1094 ** | | | | |
| 1096 ** | | | | |
| 1098 ** | | | | |
| 1100 ** | | | | |
| 1102 ACONV | LDA | PIA1BD | CLEAR IRQ FLAG | |
| 1104 | LDU | #GLOBAL | SET U-REG AS GLOBAL POINTER | |
| 1106 | TST | FMODE2 | CHANGE MODES ? | |
| 1108 | BEQ | ACON1 | NO | |
| 1110 | CLR | FAVG | NO AVERAGING FOR ONE COMPLETE CYCLE | |
| 1112 | CLR | CADC | RESET CYCLE COUNTER | |
| 1114 | LEBR | ACONV7 | | |
| 1116 ACON1 | TST | FAVG | AVERAGING STARTED? | |
| 1118 | BEQ | ACON1A | NO | |
| 1120 | LDA | #01 | | |
| 1122 | STA | DVALF | SET DATA VALID INDICATION | |
| 1124 ACON1A | LDA | #01 | LOW BYTE SELECT CODE | |
| 1126 | LBSR | INPUT | | |
| 1128 | STB | LVALUE+1 | SAVE 8 LSB | |
| 1130 | LDA | #02 | HIGH BYTE SELECT CODE | |
| 1132 | LBSR | INPUT | | |
| 1134 | STB | LVALUE | SAVE 4 MSB + POLARITY + OVERFLOW | |
| 1136 * | | | | |
| 1138 | LDX | MUXPTR | | |
| 1140 | PSHS | X | POSITION POINTER ON STACK FOR FUTURE REFERENCE | |
| 1142 * | | | | |
| 1144 * | | | | |
| 1146 * | | | | |
| 1148 | LDA | LVALUE | RECALL LAST VALUE | |
| 1150 | TFR | A, B | | |
| 1152 | ANDB | #0F | | |
| 1154 | STB | LVALUE | STRIP OFF POLARITY & OVERFLOW INFORMATION | |
| 1156 | BITA | #40 | TEST OVERFLOW BIT | |
| 1158 | BEQ | ACONV2 | O. K. | |
| 1160 | LDY | #0FFF | | |
| 1162 | STY | LVALUE | SET MAX. VALUE | |
| 1164 | LDB | #ERROF | | |
| 1166 | STB | FFLT | SET OVERFLOW ERROR CODE | |
| 1168 * | | | | |

```

1170 *      VERIFY PROPER POLARITY
1172 *
1174 ACONV2 BITA    #080    TEST POLARITY
1176      BNE      ACONV3    POSITIVE , O. K.
1178      LDD      LVALUE
1180      COMA
1182      COMB
1184      ADDD     #01      FORM 2'S COMPLEMENT
1186      STD      LVALUE
1188      CMPD     #-50     MORE THAN 50MV NEGATIVE
1190      BGT      ACONV3    NO
1192      LDB      1,X
1194      BITB     #080     BIPOLAR DESIGNATED INPUT
1196      BNE      ACONV3    YES , CONTINUE
1198      LDB      #ERRNEG
1200      STB      FFLT     SET POLARITY ERROR CODE
1202 *
1204 ACONV3 LDY      LVALUE
1206      TST      FAVG
1208      BEQ      ACONV4    NO AVERAGING
1210 *
1212 *      AVERAGE DATA (LVALUE + 7(OVALUE))/8
1214 *
1216      LDD      #0703
1218      STB      DIVW      PRE-SAVE DIVISOR 2^DIVW
1220      PSHS     A          SET MULTIPLIER FOR QMUL ROUTINE
1222      LDA      [1,S]     RETRIEVE OFFSET TO VARIABLE STORAGE LOCATION
1224      LDD      A,U       FETCH PRIOR AVERAGE
1226      LBSR     QMUL
1228      LEAS     1,S       CLEAN UP STACK AFTER MULTIPLY
1230      ADDD     LVALUE    ADD NEW CONTRIBUTION TO AVERAGE
1232      LBSR     QDIV      QUICK DIVIDE BY 8
1234 *
1236      CMPD     LVALUE    CORRECT FOR AVERAGING OFFSETS
1238      BEQ      ACON3B
1240      BGT      ACON3A
1242      ADDD     #01
1244      BRA      ACON3B
1246 ACON3A SUBD     #01
1248 *
1250 ACON3B TFR      D,Y     TEMPORARY HOLD AVERAGE VALUE
1252 ACONV4 LDA      [0,S]   FETCH VARIABLE OFFSET
1254      STY      A,U       SAVE NEW AVERAGE
1256 *
1258 *      CALCULATE AMP-HOURS IF NECESSARY
1260 *
1262      LDX      [0,S++]    RETRIEVE MUX POINTER
1264      CMPX     #IBAT     CHECK FOR BATTERY CURRENT INPUT
1266      BNE      ACONV5    NO
1268      LDA      CADC
1270      PSHS     A
1272      LDD      LVALUE
1274      LBSR     QMUL
1276      LEAS     1,S       CLEAN UP STACK
1278      DMI      ACON4A
1280      LDX      #0        SET 8MSB FOR POS. NUMBER
1282      BRA      x+5
1284 ACON4A LDX      #FFFF    SET 8MSB FOR NEG. NUMBER

```

```

1286      ADDD   AMPH+2   ACCUMULATE RAW VALUE OF AMP--HOURS
1288      STD    AMPH+2
1290      TFR    X, D
1292      ADCB   AMPH+1
1294      ADCA   AMPH
1296      STD    AMPH
1298      CLR    CADC     RESET CYCLE COUNTER
1300      BRA    ACONV6
1302 *
1304 * LINEARIZE BATTERY THERMISTOR READING
1306 *
1308 ACONV5 CMPX   #TBAT.   BATTERY THERMISTOR INPUT
1310      BNE    ACONV6   NO
1312      LDX   #TELTHE   SET TABLE POINTER
1314      LDD   TBAT#.U   GET AVERAGED RAW VALUE
1316      LBSK  LTBL      LINEARIZE SUBROUTINE
1318      SUBD  #40        CORRECT FOR TABLE OFFSET
1320      STD   TBATL     SAVE RESULTS
1322 *
1324 ACONV6 LDX    MUXPTR
1326      LEAX  2, X      ADVANCE POINTER
1328      INC   CADC      ADVANCE CYCLE COUNTER
1330      LDD   0, X
1332      CMPD  #END.     END OF TABLE
1334      BNE   ACONV8   NO , CONTINUE
1336 *
1338      LDA   #01
1340      STA   FAVG      SET AVERAGE FLAG
1342      STA   DVALF     SET DATA VALID FLAG
1344 ACONV7 LDY    FMODE
1346      LDX   ADC, Y    POINT TO 1'ST TABLE ENTRY
1348 *
1350 ACONV8 STX    MUXPTR  SAVE NEW POINTER VALUE
1352      LDA   #0        MUX DEVICE SELECT CODE
1354      LDB   1, X      READ NEW MUX ADDRESS
1356      LBSR  OUTPUT    CONFIGURE A/D CONVERTER
1358      CLR   FMODE2    MODE CHANGE COMPLETE
1360 *
1362 * DUPLICATE ITEMS TO COMMON BLOCK FOR EXTERNAL ACCESS
1364 *
1366      LDD   IBAT      COPY BATTERY CURRENT
1368      STD   XIBAT
1370      LDD   VBAT      COPY BATTERY VOLTAGE
1372      STD   XVBAT
1374      RTS
1376      PAGE
1378 **
1380 ** SELECT OPERATING MODE - SUBROUTINE
1382 **
1384 ** DETERMINES APPROPRIATE OPERATING MODE BASED UPON
1386 ** DIGITAL INPUTS AT FFIN AND FREST AND TRANSFERS
1388 ** CONTROL TO SPECIFIC ROUTINE.
1390 ** IF NO VALID MODE DETERMINED FOR 3 CYCLES : SHUTDOWN
1392 SMODE CLR    FCAL     RESET CALIBRATE FLAG
1394      CLR   FTST      RESET TEST FLAG
1396      LDB   #01
1398      LDA   SYIN
1400      BITA  #08        TEST MODE?

```

| | | | |
|------|-------------|----------|--------------------------------------|
| 1402 | BNE | SMODE2 | YES |
| 1404 | BITA | ##04 | CALIBRATE MODE? |
| 1406 | BNE | SMODE1 | YES |
| 1408 | LDA | FPIN | |
| 1410 | ANDA | ##07 | |
| 1412 | CMFA | ##00 | TEST MODE? |
| 1414 | BEQ | SMODE2 | YES |
| 1416 | CMFA | ##05 | CALIBRATE MODE? |
| 1418 | BNE | SMODE3 | NO, CONTINUE |
| 1420 | SMODE1 STB | FCAL | SET CALIBRATE FLAG |
| 1422 | BRA | SMODE3 | |
| 1424 | SMODE2 STB | FTST | SET TEST MODE FLAG |
| 1426 | SMODE3 LDY | ##0 | SET INVALID MODE FLAG |
| 1428 | LDD | FRST | REST FLAG ACTIVE |
| 1430 | BEQ | *+6 | NO |
| 1432 | LDY | ##TLRST | SET REST MODE |
| 1434 | LDD | FTHK | THINK FLAG ACTIVE |
| 1436 | BEQ | *+6 | NO |
| 1438 | LDY | ##TLTHK | SET THINK MODE |
| 1440 | LDA | FPIN | |
| 1442 | BITA | ##08 | AC-LINE ON |
| 1444 | BNE | SMODE4 | NO |
| 1446 | LDX | FCHG | CHARGE CYCLE REQUESTED |
| 1448 | BEQ | *+6 | NO |
| 1450 | LDY | ##TLCHG | SET CHARGE MODE |
| 1452 | SMODE4 BITA | ##40 | E. V. CONTROLLER ON |
| 1454 | BNE | *+6 | NO |
| 1456 | LDY | ##BLDIS | SET DISCHARGE MODE |
| 1458 | CLRA | | RESET SHUTDOWN FLAG |
| 1460 | LDB | ##ERRSM1 | SET ERROR CODE FOR POSSIBLE SHUTDOWN |
| 1462 | TST | FINT | INITIALIZE SEQUENCE ? |
| 1464 | BEQ | SMODE5 | NO |
| 1466 | CMFY | ##0 | CHECK FOR VALID MODE |
| 1468 | LBED | SHUTD | INITIALIZATION AND NO VALID MODE |
| 1470 | STY | FMODE | SAVE SELECTED MODE |
| 1472 | RTS | | RETURN |
| 1474 | * | | |
| 1476 | SMODE5 CMFY | ##0 | CHECK FOR VALID MODE |
| 1478 | BNE | SMODE6 | U. R. |
| 1480 | LDX | FMODE | |
| 1482 | LBMI | SHUTD | MODE CHANGE COMPLETE AND NO NEW MODE |
| 1484 | LDA | FSHUTD | |
| 1486 | INCA | | |
| 1488 | CMFA | ##225 | DELAY SHUTDOWN FOR (30 SEC / .133) |
| 1490 | LBHI | SHUTD | DELAY COMPLETED |
| 1492 | SMODE6 STA | FSHUTD | |
| 1494 | CMFY | FMODE | CHECK LAST MODE |
| 1496 | BEQ | SMODE8 | SAME CONTINUE |
| 1498 | LDX | FMODE | |
| 1500 | BNE | SMODE7 | CHANGE ALREADY REQUESTED |
| 1502 | LDX | ##1 | |
| 1504 | STX | FMODE | SET CHANGE REQUEST FLAG |
| 1506 | SMODE7 BPL | SMODE9 | REQUEST NOT YET ACKNOWLEDGED |
| 1508 | LDA | ##01 | |
| 1510 | STA | FMODE2 | SET ADC CHANGE FLAG |
| 1512 | CLR | DVALF | RESET DATA VALID FLAG |
| 1514 | STY | FMODE | SET NEW MODE POINTER |
| 1516 | SMODE8 LDX | ##0 | |

```

1518          STX      FMODE      RESET MODE CONTROL FLAG
1520 SMODE9 LDY      FMODE      RETAIN PRIOR MODE
1522          JMP      [0,Y]      RUN APPROPRIATE MODE SUBROUTINE AND RETURN
1524          PAGE
1526 *
1528 *
1530 *          CHARGE MODE - SUBROUTINE WRITTEN IN MPL : CHGMPL
1532 *
1534 *
1536 CHARGE RTS
1538 *
1540 *
1542 *          DISCHARGE MODE - SUBROUTINE CALLS FORTRAN AVGFOR TO FILTER
1544 *          BATTERY AND VEHICLE DATA DURING DISCHARGE
1546 *
1548 *
1550 DISCHG TST      DVALF      DATA VALID
1552          BNE      DISCH1     YES
1554          LDD      #-1       SET INITIALIZATION FLAG FOR FORTRAN
1556          BRA      DISCH2
1558 DISCH1 LDD      FINTF
1560          BMI      DISCH3     WAIT FOR INITIALIZATION TO ACKNOWLEDGE
1562          ADD      #01       INCREMENT DELAY COUNT
1564 DISCH2 STD      FINTF
1566 DISCH3 RTS
1568 *
1570 *
1572 *          REST MODE - SUBROUTINE
1574 *
1576 *
1578 REST  RTS
1580 *
1582 *
1584 *          THINK MODE - SUBROUTINE
1586 *
1588 *
1590 THINK RTS
1592          PAGE
1594 **
1596 **          VEHICLE SPEED INPUT & CALIBRATION SUBROUTINE
1598 **          FCAL=1 FLAGS CALIBRATION REQUEST
1600 **          FCAL+1=1 FLAGS CALIBRATION IN PROGRESS
1602 **          CALIBRATION FACTOR = SPDCAL
1604 **          SW1 STARTS AND ENDS CALIBRATION PROCEEDURE
1606 **          OVER CALIBRATED MILE COURSE
1608 **
1610 INVSP TST      FCAL      CALIBRATE SPEED TRANSDUCER?
1612          BEQ      INV2      NO
1614          TST      FCAL+1    ALREADY STARTED?
1616          BNE      INV1      YES
1618          LDA      .AXIN+1    SW1 DEPRESSED?
1620          BEQ      INV4A     NO
1622          STA      FCAL+1    SET START FLAG
1624          LDD      #0
1626          STD      SPDCAL
1628          BRA      INV4A
1630 INV1  LDA      #04      COUNTER SELECT CODE
1632          LBSR     INPUT     READ COUNTER

```

| | | | |
|------|-------|---------|---|
| 1634 | CLRA | | CLEAR 4 MSB |
| 1636 | TST | .AXIN+1 | SW1 DEPRESSED? |
| 1638 | BEQ | INV1A | NO |
| 1640 | CLR | FCAL+1 | FINISH CALIBRATION |
| 1642 | BRA | INV1B | |
| 1644 | INV1A | CMFB | #225 |
| 1646 | | BLO | INV5 |
| 1648 | INV1B | ADD | SPDCAL |
| 1650 | | BPL | INV1C |
| 1652 | | LDB | #ERRSOF |
| 1654 | | STB | FFLT |
| 1656 | | LDD | #1 |
| 1658 | | CLR | FCAL+1 |
| 1660 | INV1C | STD | SPDCAL |
| 1662 | | BRA | INV4A |
| 1664 | INV2 | LDD | SPDCAL |
| 1666 | | BNE | INV3 |
| 1668 | | LDD | #1754 |
| 1670 | | STD | SPDCAL |
| 1672 | INV3 | LDA | SPDC |
| 1674 | | INCA | |
| 1676 | | CMFA | #45 |
| 1678 | | BLO | INV5A |
| 1680 | | LDA | #404 |
| 1682 | | LBSR | INPUT |
| 1684 | | CMFB | #200 |
| 1686 | | BLO | INV4 |
| 1688 | | LDA | #ERRSHI |
| 1690 | | STA | FFLT |
| 1692 | | CLRB | |
| 1694 | INV4 | CLRA | |
| 1696 | | STD | SPEED |
| 1698 | INV4A | LDA | #405 |
| 1700 | | LBSR | DEVSEL |
| 1702 | INV5 | CLRA | |
| 1704 | INV5A | STA | SPDC |
| 1706 | | RTS | |
| 1708 | | PAGE | |
| 1710 | ** | | |
| 1712 | ** | | DISPLAY SELECT - SUBROUTINE |
| 1714 | ** | | |
| 1716 | ** | | SELECTS APPROPRIATE DISPLAY FOR V.F. & LED INDICATORS |
| 1718 | ** | | DEPENDING UPON CURRENT OPERATING MODE - NORMAL DISPLAY |
| 1720 | ** | | & IF SW1 (REMOTE DISPLAY) DEPRESSED - REQUESTED DISPLAY |
| 1722 | ** | | |
| 1724 | ** | | ANNUNCIATORS ARE SET BASED UPON FLAGS |
| 1726 | ** | | OR ASSOCIATED INPUTS |
| 1728 | ** | | |
| 1730 | ** | | FLASHING OF DESIGNATED ANNUNCIATORS WHEN ACTIVATED |
| 1732 | ** | | |
| 1734 | ** | | |
| 1736 | ** | | SPECIAL FUNCTIONS INCLUDE : |
| 1738 | ** | | TEST AND FAULT MODES |
| 1740 | ** | | TRIGGER BY FTST & FFLT |
| 1742 | ** | | TRANSFERRING CONTROL TO DISTST & DISFLT ROUTINES |
| 1744 | ** | | |
| 1746 | ** | | |
| 1748 | | PSCT | |

```

1750 *
1752 DISSEL TST FTST CHECK FOR TEST MODE
1754 BNE DISTST
1756 CLR FTST+1
1758 TST FFLT CHECK FOR FAULT MODE
1760 LENE DISFLT
1762 TST FCAL CHECK FOR CALIBRATE MODE
1764 LENE DISCAL
1766 CLR FCAL+1
1768 CLR FLASHL
1770 CLR FLASHV
1772 LDY PMODE SET MODE POINTER
1774 TST .AXIN
1776 BMI DIS1 REMOTE DISPLAY PUSHBUTTON (SW1) - DEPRESSED
1778 LDA DDELAY
1780 BNE DIS2 HOLD REQUESTED DISPLAY
1782 LDD DISPLAY SELECT NORMAL DISPLAY FORMAT
1784 BRA DIS3
1786 DIS1 LDA #38 (38 x 133)-1=5 SEC.
1788 DIS2 DECA
1790 STA DDELAY
1792 LDD DISP2.Y SELECT REQUESTED DISPLAY FORMAT
1794 *
1796 DIS3 STA DSTAT SET VFD STATUS
1798 STB .FPOUT+1 SET FRONT PANEL LED'S MASK
1800 CLR .FPOUT RESET ALL LED'S
1802 LDA #FFF
1804 STA DSTATM ENABLE ALL FUNCTIONS
1806 *
1808 LBSR ACPWR AC-ON INDICATOR
1810 LBSR EL0W WATER INDICATOR
1812 LBSR CH0LED CHARGING INDICATOR
1814 LBSR EQU0L EQUALIZE INDICATOR
1816 LBSR WARN WARNING INDICATOR
1818 LBSR SOC SOC INDICATOR
1820 LBSR FLASH FLASH INDICATORS
1822 *
1824 LDA DMILE+1 MILES REMAINING - 0LSE
1826 LBSR ECD CONVERT TO DISPLAYABLE FORM
1828 LDB #000
1830 ORB DNUM SET MILES INDICATOR
1832 STB DNUM
1834 RTS
1836 PAGE
1838 * SPECIAL TEST DISPLAY ROUTINE
1840 * INHIBITS NORMAL DISPLAY ; USES 3 DIGIT NUMERIC TO
1842 * DISPLAY BCD VALUE OF ANY SYSTEM VARIABLES.
1844 * TABLE : TBLTST DEFINES VARIABLES & THEIR DISPLAYED ORDER
1846 *
1848 * SW1 REMOTE DISPLAY PUSHBUTTON STEPS THROUGH TABLE
1850 *
1852 * BAR-GRAPH USED TO INDICATE DISPLAYED VARIABLE
1854 * ( i. e. 3 BARS FOR 3'RD ELEMENT IN TABLE )
1856 *
1858 * WARNING INDICATOR FLASHES TO INDICATE NON-NORMAL DISPLAY
1860 *
1862 *
1864 DISTST TST FTST+1 TEST ALREADY RUNNING ?

```



```

1866      BEQ      DIST0      NO, INITIALIZE
1868      LDX      TSTPTR     RETAIN LAST POINTER LOCATION
1870      LDB      .AXIN+1    REMOTE PUSHBUTTON DEPRESSED?
1872      BEQ      DIST1      NO
1874      INC      DBAR
1876      LEAX     2,X        ADVANCE POINTER TO NEXT ENTRY
1878      CMPX     #TELTSE+2  END OF TABLE
1880      BNE      DIST1      NO
1882 DIST0  CLR      DBAR
1884      LDA      #001
1886      STA      FTST+1     SET RUN FLAG
1888      LDX      #TBLTST
1890 DIST1  STX      TSTPTR     RESET POINTER
1892      LDA      [0,X]      FETCH TABLE VALUE
1894      LBSR     BCD        CONVERT BINARY TO BCD VALUE
1896      LDA      #487      SET WARNING, BAR, NUMERIC GRID "ON"
1898      STA      DSTAT
1900      STA      DSTATM
1902      LDB      #480      SET WARNING TO FLASH
1904      STB      FLASHV
1906      LDD      #0
1908      STD      .FPOUT     BLANK LED'S
1910      LBR      FLASH     FLASH DISPLAYS & RETURN
1912      PAGE
1914 *
1916 *      SPECIAL FAULT DISPLAY - ROUTINE
1918 *
1920 *      DISPLAYS NUMERIC FAULT CODE FROM FFLT
1922 *      4 MSB PRIMARY (P) & LSB SECONDARY CODE (S)
1924 *      IN P - S FORMAT
1926 *      WARNING AND FAULT INDICATORS FLASH
1928 *
1930 DISFLT LDA      #48B      WARNING, FAULT, NUMERIC, GRID ACTIVATED
1932      STA      DSTAT
1934      STA      DSTATM
1936      LDB      #48B      WARNING FAULT FLASH
1938      STB      FLASHV
1940      LDB      FFLT      FAULT CODE & FLAG
1942      TFR      B,A
1944      ANDA     #30F
1946      STA      DNUM+2     SAVE SECONDARY CODE
1948      LDA      #16
1950      MUL
1952      STA      DNUM      SEPARATE PRIMARY & SECONDARY CODES
1954      LDB      #40A      SAVE PRIMARY CODE
1956      STB      DNUM+1     NEGATIVE SIGN CODE
1958      LDD      #0808     INSERT BETWEEN CODES
1960      STD      .FPOUT     ACTIVATE FRONT PANEL FAULT INDICATION
1962      STA      FLASHL     FLASH LED FAULT
1964      LBSR     FLASH     FLASH DISPLAYS
1966      LDA      DFLTC
1968      INCA
1970      CMPA     #22        ADVANCE FAULT DELAY COUNT
1972      BLS      DISFL1     DISPLAY 3 SEC. (22 x .133) YET?
1974      CLR      FFLT      NO
1976      CLRA
1978 DISFL1 STA      DFLTC     RESET FAULT CODE
1980      RTS      RESET DELAY COUNT
          SAVE DELAY COUNT

```

```

1982          SPC      3
1984 *
1986 *      SPECIAL CALIBRATE DISPLAY
1988 *      DISPLAYS M.S. BYTE OF CALIBRATION FACTOR
1990 *      FLASHING FACTOR INDICATES CALIBRATION IN PROGRESS
1992 *
1994 DISCAL LDA      #483      SELECT WARNING & NUMERIC
1996          STA      DSTAT
1998          STA      DSTATM
2000          LDB      #480      FLASH WARNING
2002          TST      FCAL+1    CALIBRATION IN PROGRESS?
2004          BEQ      DISC1     NO
2006          LDB      #402      FLASH NUMERIC
2008 DISC1  STE      FLASHV
2010          LDD      #40
2012          STD      FFOUT     BLANK LED DISPLAY
2014          LDA      SPDCAL    DISPLAY M.S. BYTE OF FACTOR
2016          LBSR     BCD
2018          L      A      FLASH  FLASH DISPLAY & RETURN
2020          PAGE
2022 **
2024 **      CONFIGURE BIT PATTERN FOR V.F. DISPLAY
2026 **
2028 **      FORMS PROPER BIT SEQUENCE FOR LATER USE BY
2030 **      VFDIS SUBROUTINE
2032 **
2034 **      INPUTS: DSTAT , DSTATM , DEAR , DNUM(3) , FDNEW
2036 **      USES: X , Y , A , B , S ; IDISP ; TELNUM ; TELBAR
2038 **      OUTPUTS: VFDATA - VFDATA+5
2040 **      RETURNS
2042 **
2044 CDISP  LBSR     IDISP
2046          LDA      DSTAT
2048          ANDA     DSTATM     MASK DISPLAY STATUS
2050          PSHS     A
2052          TFR     A,B
2054          ANDB    #4F0      RETAIN ANNUNCIATOR STATUS ONLY
2056          ORB     S,Y
2058          STB     S,Y      SAVE AT VFDATA6
2060 *
2062          BITA     #401      TEST "GRID" BIT
2064          BEQ     CDISP1     "OFF"
2066          LDB     #404
2068          ORB     0,Y
2070          STB     0,Y
2072 *
2074 CDISP1 BITA     #408      TEST "FAULT" BIT
2076          BEQ     CDISP2     "OFF"
2078          LDB     #408
2080          ORB     3,Y
2082          STB     3,Y      ACTIVATE FAULT INDICATOR
2084 *
2086 CDISP2 BITA     #404      TEST BAR-GRAPH REQUEST BIT
2088          BEQ     CDISP3     DO NOT DISPLAY BAR-GRAPH
2090          LDX     #TELBAR    SET POINT TO 1ST TABLE ENTRY
2092          LDB     DEAR      BAR-GRAPH DATA
2094          CMPB    #((TELBAE-TELBAR)/2) CHECK FOR MAX. TABLE SIZE
2096          BLS     *+4      OK

```

```

2098     LDB     #((TBLBAE-TBLBAR)/2 SET MAX. SIZE
2100     LSLB    DOUBLE BYTE TABLE X 2
2102     ABX     OFFSET POINTER
2104     LDA     0,X
2106     LDB     1,X
2108     ORA     3,Y
2110     STA     3,Y      SAVE AT VFDATA+3
2112     STB     4,Y      SAVE AT VFDATA+4
2114 *
2116 CDISP3 PULS  A
2118     BITA    #02
2120     BEQ    CDISP4
2122     LDX    #TELNUM  CONVERT BCD TO SEVEN SEGMENTS
2124     LDB    DNUM     100'S
2126     BSR    TEL
2128     LDA    #8
2130     MUL    SHIFT LEFT FOUR TIMES
2132     ORA    0,Y
2134     STA    0,Y
2136     STB    1,Y
2138 *
2140     LDB    DNUM+1   10'S
2142     BSR    TEL
2144     LDA    #16
2146     MUL
2148     ORA    1,Y
2150     STA    1,Y
2152     STB    2,Y
2154 *
2156     LDB    DNUM+2   1'S
2158     BSR    TEL
2160     LDA    #32
2162     MUL
2164     ORA    2,Y
2166     STA    2,Y
2168     ORB    3,Y
2170     PSHS   B
2172     LDA    DNUM
2174     ANDA   #0C0     ISOLATE MILES & FAULT ANNUNCIATORS
2176     LSRA
2178     LSRA
2180     LSRA
2182     ORA    0,S+
2184     STA    3,Y
2186 CDISP4 RTS
2188 *
2190 *     TABLE LOOK-UP SUBROUTINE FOR 16 ENTRY TABLE
2192 *
2194 *     INPUT: 'X' REG POINTING TO 1'ST TABLE ADDRESS
2196 *           'B' REG ARGUMENT
2198 *     OUTPUT: 'B' REG - VALUE FROM TABLE
2200 *
2202 TEL  ANDB   #0F
2204     LDB    B,X
2206     RTS
2208     SPC    3
2210     PAGE
2212 **

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2214 **          VACUUM FLUORESCENT DISPLAY SUBROUTINE
2216 **
2218 **          TRANSMITS TO DISPLAY SERIAL BIT PATTERN PREVIOUSLY
2220 **          STORED AT      VFDATA-VFDATA+5
2222 **
2224 **          SEQUENCE IS REPEATED THREE CONSECUTIVE TIMES
2226 **
2228 **          FDISP FLAG DETERMINES WHETHER DISPLAY IS ACTIVE OR BLANKED
2230 **
2232 VFDISP LDA      DSTAT      CHECK FOR GRID ACTIVE COMMAND
2234          LSRA
2236          LECC      BLANK      NO, BLANK DISPLAY & RETURN
2238          LDA      #403      TRANSMIT 3 TIMES
2240          STA      LOOPC      PRESET LOOP COUNTER
2242 VFDIS1 LDX      #VFDATA+5  SET POINTER FOR FIRST BYTE TO BE TRANSMITTED
2244          LDB      PIA1AD     SET CLOCK'="1" (PA5)
2246          ORB      #420
2248 VFDIS2 LDA      #408
2250          STA      BITC      PRESET BIT COUNTER
2252          LDA      0,X
2254 VFDIS3 LSRA      USE CARRY TO TEST BITS
2256          ORB      #410      SEGMENT OFF DATA'="1" (PA4)
2258          EOC      *+4
2260          ANDB     #4EF      SEGMENT ON DATA'="0" (PA4)
2262          STB      PIA1AD
2264          NOP      WAIT 90S BEFORE CLOCKING
2266          ANDB     #4DF
2268          STB      PIA1AD     SET LLOCK'="0" (PA5)
2270          ORB      #420
2272          STB      PIA1AD     SET CLOCK'="1"
2274          DEC      BITC
2276          BNE      VFDIS0     FULL BYTE NOT TRANSMITTED
2278          LEAX     -1,X
2280          CMPX     #VFDATA-1
2282          BNE      VFDIS2     ALL BYTES NOT TRANSMITTED
2284          ORB      #440      LATCH DATA INTO DRIVERS
2286          STAB     PIA1AD     SET STROBE="1"
2288          NOP
2290          ANDB     #4BF      WAIT 90S
2292          STB      PIA1AD     SET STROBE="0"
2294          STB      PIA1AD     DUPLICATE IN RAM
2296          DEC      LOOPC
2298          BNE      VFDIS1     REPEAT TRANSMIT SEQUENCE
2300          RTS
2302          SPC      3
2304 *
2306 *          BLANK VACUUM FLLORESCENT DISPLAY
2308 *
2310 *          BLANKS DISPLAY BY TURNING OFF FILAMENT
2312 *          "LOW POWER MODE"
2314 *
2316 BLANK LDA      #47F      FORCE STROBE "HIGH" (PA6)
2318          STA      PIA1AD
2320          STA      PIA1AD     DUPLICATE IN RAM
2322          RTS
2324          PAGE
2326 **
2328 **          SAFETY - SUBROUTINE

```

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2330 **      RUNS SPECIFIC FAULT DIAGNOSTICS DURING
2332 **      PROGRAM EXECUTION AND CAN TRIGGER SPECIAL
2334 **      FAULT DISPLAY OR EMERGENCY SHUTDOWN (POWER STAGE DISABLED)
2336 **
2338 SAFETY CLR      DISAF      RESET DISABLE FLAG
2340          LDY      # (TBLTEE-TBLTEM+1)/6 SET COUNTER
2342          LDX      #TBLTEM POINT TO 1'ST TABLE ENTRY
2344          LDU      #GLOBAL SET GLOBAL POINTER
2346 SAFE1 LDA      0,X      READ OFFSET
2348          LDD      A,U      READ VALUE
2350          CMPD     1,X      ABOVE LOWER LIMIT
2352          BGT      SAFES3 NO
2354          CMPD     3,X      ABOVE UPPER LIMIT
2356          BGE      SAFEZ2 NO
2358          LDB      5,X
2360          STB      DISAF      SET DISABLE FLAG
2362 SAFE2 LDB      5,X
2364          STB      FFLT      SET APPROPRIATE ERROR CODE
2366 SAFE3 LEAX     6,X
2368          LEAY     -1,Y
2370          BNE      SAFE1
2372 *
2374          LDA      FFIN
2376          ANDA     #407
2378          CMPA     #06      TEST FOR VALID INPUT CODES
2380          BLT      SAFE4     O.K.
2382          LDB      #ERRFPI
2384          STB      FFLT      SET APPROPRIATE ERROR CODE
2386 SAFE4 RTS
2388          SFC      6
2390 **
2392 **      SYSTEM SHUTDOWN SUBROUTINE
2394 **      SETS WAKE-UP MODE
2396 **      AND REMOVES LOGIC POWER
2398 **
2400 SHUTD ORCC     #50      SET FIRQ & IRQ MASK
2402          LDA      #47F
2404          STA      FIA1AD BLANK VFD
2406          STA      FIA2AD DUPLICATE IN RAM
2408          LDA      #BFF
2410          STA      RTCLRE RESET ALL LATCHES
2412          STA      RTCORE RESET ALL COUNTERS
2414          LDD      WAKEF BCD CODED WAKE-UP TIME
2416          BNE      SHUTD1
2418          LDD      #50100 1 DAY - 0 HR DEFAULT SETTING
2420 SHUTD1 ADDD     #50100 ADJUST DAYS FOR INITIALIZATION POINT
2422          STA      RTCLDM DAYS (0-30)
2424          STB      RTCLH  HOURS(0-23)
2426          LDA      #501
2428          STA      RTCLDW INITIALIZE LATCHES TO AGREE WITH COUNTERS
2430          STA      RTCLMO
2432          STA      RTCSBY ENABLE STANDBY INTERRUPT
2434          STA      RTCICR ENABLE COMPARATOR FLAG
2436          LDX      #50
2438          STX      WARMF RESET RUNNING FLAG
2440          CLR      CCOUT
2442          STX      FFOUT BLANK LED'S
2444          CLR      AXOUT CLEAR HOLD BIT

```

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2446          LBSR   DOUT   KILL POWER
2448 SHUTD2  BRA     SHUTD2  WAIT TO DIE
2450          SFC     3
2452 **
2454 **      ADJUST TIME FOR SHUTDOWN INTERVAL
2456 **
2458 TIMEA   LDX     #RTCCM
2460 TIMA1   LDY     0,X      READ MIN. AND HOUR COUNTER
2462          LDA     3,X      READ DAY OF MONTH COUNTER
2464          TST    RTCSR   COUNTER ROLLOVER?
2466          BNE    TIMA1   YES
2468          PSHS   A,Y
2470          LDB   #02
2472 TIMA2   LDA     B,S
2474          LBSR   BINARY  CONVERT BCD TO RTNARY
2476          STA   B,S
2478          DECB
2480          BPL   TIMA2
2482          LDA   0,S+
2484          SUBA  #1        CORRECT FOR CLOCK INITIALIZATION
2486          LDB   #24      CONVERT TO DAYS
2488          MUL
2490          ADDB  1,S      INCLUDE HOUR COUNTER VALUE
2492          ADCA  #0
2494          TFR   D,Y
2496          LDB   #60
2498          PSHS  B
2500          TFR   Y,D
2502          LBSR  QMUL     CONVERT TO HOURS
2504          ADDB  1,S      INCLUDE COUNTER VALUE
2506          ADCA  #0
2508          LSRB
2510          RORB
2512          BCC   TIMA3   WEIGHT TIME FOR 2MIN/COUNT
2514          ADDD  #001    ROUND ANSWER
2516 TIMA3   LEAS   3,S      CLEAN STACK & FALL INTO TIME
2518          SFC     3
2520 **
2522 **      SUBROUTINE TO ADVANCE TIME COUNTERS
2524 **      BASED UPON VALUE STORED IN D' REG UPON ENTRY
2526 **
2528 TIME    TFR     D,Y
2530          LDX   #TELTIM  1ST TIME LOCATION
2532 TIM1    ADDD   [0,X]    ADVANCE COUNT
2534          BCC   TIM2
2536          LDD   #FFFFF   SET MAX VALUE
2538 TIM2    STD    [0,X]    SAVE NEW COUNT
2540          LEAX  2,X      NEXT TIME LOCATION
2542          TFR   Y,D      RE-COPY ORIGINAL VALUE
2544          CMPX  #TELTIE  END OF TABLE
2546          BLS   TIM1     NO
2548          RTS
2550          SFC     6
2552 **
2554 **      LINEARIZING TABLE LOOK-UP
2556 **
2558 **      V=V0+(V0-V1)(A-A0)/256
2560 **

```

2562 ** "X" - REG = POINTER TO 1ST TABLE LOCATION
 2564 ** "A,B" 12BIT POSITIVE VALUE
 2566 **
 2568 ** TABLE VALUES: 8BIT UNSIGNED NUMBERS
 2570 ** RESULT: V<256 IN "A,B" - REG
 2572 **
 2574 LTBL TSTA NUMBER POSITIVE?
 2576 BPL LTBL1 YES; LINEARIZE FROM TABLE
 2578 CLRB
 2580 BRA LTBL2 DEFAULT TO LOWEST TABLE ENTRY
 2582 LTBL1 EXG A,B
 2584 ABX ADJUST POINTER BY CORRECT OFFSET
 2586 LDB 0,X READ LOWER VALUE (V0)
 2588 SUBB 1,X -(V1)
 2590 BHS *+3
 2592 NEGB FORM ABSOLUTE
 2594 MUL (V0-V1)(A-A1)
 2596 TSTB CHECK 8LSB
 2598 BPL *+3
 2600 INCA ROUND 8 MSB
 2602 LDB 0,X DIFFERENCE NEGATIVE
 2604 SUBB 1,X
 2606 BLS *+3 POSITIVE SLOPE
 2608 NEGA NO CORRECT FOR UNSIGNED MULTIPLY
 2610 TFR A,B
 2612 LTBL2 ADDB 0,X
 2614 CLRA
 2616 RTS
 2618 PAGE

2620 **

2622 ** DIGITAL INPUTS

2624 **

2626 ** FRONT PANEL SWITCHES : FPIN STORAGE LOCATION

2628 ** : FPIN+1 FLAG BIT CHANGES

2630 ** SELECT CODE 07

2632 ** SW3 B0-B2 0-TEST; 1-15 AMP; 2-20 AMP; 3-30 AMP; 4-AUX CHARGER

2634 ** 5-CALIBRATE; 6-UNUSED; 7-UNUSED

2636 ** AC ON B3 "0" AC-LINE ACTIVE

2638 ** EVC-ON B6 "0" EV CONTROLLER ACTIVE

2640 ** SW2 B7 "1" DEFER EQUALIZE CYCLE-DEBOUNCED

2642 **

2644 ** DIP & MISC. INPUTS : SYIN STORAGE LOCATION

2646 ** SELECT CODE 08

2648 **

2650 ** BATTERY TYPE B0-B1 0-GOULD ; 1-UNUSED ; 2-UNUSED ; 3-UNUSED

2652 ** (DIP SWITCH #1&2)

2654 ** CALIBRATE MODE B2 "1" ACTIVE (DIP SWITCH #3)

2656 **

2658 ** TEST MODE B3 "1" ACTIVE (DIP SWITCH #4)

2660 **

2662 ** POWER STAGE FAULT B6 "0" FAULT

2664 **

2666 ** ELECTROLYTE LOW B7 "1" LOW

2668 **

2670 ** REMOTE DISPLAY & AUX. INPUTS : AXIN

2672 ** : AXIN+1 FLAGS A "1"-"0" CHANGE

2674 **

2676 ** SW1 B7 "0" DEPRESSED --FILTERED

2678 **
 2680 DINPUT LDA #07 FRONT PANEL SELECT CODE
 2682 BSR INPUT READ CURRENT VALUE
 2684 ANDB #0CF MASK OFF USED INPUTS
 2686 TFR B, A
 2688 EORB FFIN FORM CHANGE INDICATION
 2690 STD FFIN SAVE NEW VALUE & CHANGE INFORMATION
 2692 *
 2694 DIN1 LDA #08 SYSTEM INPUT SELECT CODE
 2696 BSR INPUT READ VALUE
 2698 ANDB #0CF SELECT USED INPUTS
 2700 STB SYIN SAVE VALUE & CHANGES
 2702 *
 2704 DIN2 CLRB
 2706 LDA PLA1AD AUXILIARY INPUTS***CAUTION***MAY CLEAR FIRE FLAG
 2708 COMA REVERSE LOGIC SENSE; "1"=DEPRESSED
 2710 ANDA #80 SELECT USED INPUTS - B7
 2712 BPL DINF NOT DEPRESSED
 2714 CMFA .AXIN FLAG - CHANGES
 2716 BEQ DINF
 2718 LDB #80 SW1 JUST DEPRESSED
 2720 DINF STD .AXIN SAVE VALUE & CHANGE
 2722 RTS
 2724 PAGE

2726 **

2728 **

2730 ** DIGITAL OUTPUTS

2732 **

2734 ** POWER STAGE CONTROL : CCOUT (D SELECT CODE)

2736 ** DATA B0-B6 BINARY

2738 ** ENABLE B7 "1" ACTIVE

2740 **

2742 **

2744 ** FRONT PANEL INDICATORS : .FFOUT , .FFOUT +1 (A SELECT CODE)

2746 ** CHARGING PB0 "1" ON

2748 ** EQUALIZE PB1 "1" ON

2750 ** WATER BAT PB2 "1" ON

2752 ** FAULT PB3 "1" ON

2754 ** PB4-PB5 UNUSED

2756 **

2758 ** MISC OUTPUTS : .AXOUT (B SELECT CODE)

2760 ** L. P. S. FAULT PB0 "1" ON BOARD LED'S

2762 ** LC FAULT PB1 "1" ON BOARD LED'S

2764 ** I/O FAULT PB2 "1" ON BOARD LED'S

2766 ** PB3-PB4 UNUSED

2768 ** L. P. S. HOLD PB7 "1" ACTIVE

2770 **

2772 **

2774 DOUT LDA #0D DEVICE SELECT CODE

2776 LDB CCOUT

2778 BSR OUTPUT

2780 *

2782 DOUT1 LDA #0A DEVICE SELECT CODE

2784 LDB .FFOUT FRONT PANEL DATA

2786 ANDB .FFOUT+1 ENABLE MASK

2788 BSR OUTPUT

2790 *

2792 DOUT2 LDA #0B DEVICE SELECT CODE


```

2794     LDB     . AXOUT   AUX. OUTPUT
2796     BSR     OUTPUT
2798     RTS
2800     PAGE
2802 *
2804 *     FIA OUTPUT
2806 *     ENTRY - "A" DEVICE CODE ; "B" DATA TO BE OUTPUTED
2808 *     NON-INTERRUPTIBLE ( 64 CYCLES )
2810 *     0,X PIA1AD     2,X PIA1ED
2812 *     1,X PIA1AC     3,X PIA1EC
2814 *
2816 OUTPUT LDX     #PIA1AD   SET PIA REFERENCE PTR.
2818     PSHS    A           TEMP. SAVE DEVICE CODE
2820     LDA     #F0
2822     ANDA    PIA1AD     RETAIN PB7-PB4
2824     ORA     0,S+      MERGE NEW DEVICE CODE
2826     STA     0,X       OUTPUT DEVICE CODE
2828     LDA     #PIABDR
2830     STA     3,X       SELECT "B" DATA DIRECTION REG.
2832     LDA     #FF
2834     STA     2,X       CONFIGURE AS OUTPUTS
2836     LDA     #PIABPR
2838     STA     3,X       SELECT "B" PERIPHERAL REG.
2840     STB     2,X       OUTPUT DATA
2842     LDA     #DSON
2844     STA     1,X       LATCH DATA OUTPUTED
2846     LDA     #DSOFF
2848     STA     1,X       DEVICE DESELECTED
2850     RTS
2852     SPC     3
2854 *
2856 *     FIA INPUT "B" SIDE ( NON INTERRUPTIBLE ) ( 64 CYCLES )
2858 *     ENTER : A-REG DEVICE CODE ( NON-USED BITS B7-B4 MUST BE 0 )
2860 *     RETURN : B-REG DATA READ
2862 *
2864 *     PIA1AD     0,X
2866 *     PIA1AC     1,X
2868 *     PIA1ED     2,X
2870 *     PIA1EC     3,X
2872 *
2874 INPUT  LDX     #PIA1AD   SET PIA REFERENCE PTR.
2876     PSHS    A           TEMP. SAVE DEVICE CODE
2878     LDA     #F0
2880     ANDA    PIA1AD     RETAIN PA7-PA4 STATUS
2882     ORA     0,S+      MERGE NEW DEVICE SELECT CODE
2884     STA     0,X       OUTPUT DEVICE SELECT CODE
2886     LDA     #PIABDR
2888     STA     3,X       SELECT "B" DATA DIRECTION REG.
2890     CLR     2,X       CONFIGURE "B" AS INPUTS
2892     LDA     #PIABPR
2894     STA     3,X       SELECT "B" PERIPHERAL REG.
2896     LDA     #DSON
2898     STA     1,X       DEVICE SELECT ACTIVE
2900     LDA     #DSOFF
2902     LDB     2,X       READ DATA
2904     STA     1,X       DEVICE SELECT "DISABLED"
2906     RTS
2908     SPC     3

```

```

2910 *
2912 *          WATCH-DOG RESET - SETS "A" REG. WITH DUMMY SELECT CODE
2914 *          FALLS INTO DEUSEL TO TOGGLE DEVICE SELECT LINE
2916 *
2918 WDOG   LDA    #00F          SELECT UNUSED DEVICE CODE
2920       SFC    3
2922 *
2924 *          PIA-SELECT CODE OUTPUT (DEVICE SELECT) ( 43 CYCLES )
2926 *          ENTRY : REG "A" DEVICE CODE "B" REG UNALTERED
2928 *          NON-INTERRUPTIBLE
2930 *
2932 DEUSEL FSHS   A            SAVE DEVICE CODE
2934       LDA    #0F0
2936       ANDA   PTAXAD        RETAIN PA7-PA4 STATUS
2938       ORA    0,51          MERGE DEVICE SELECT CODE
2940       STA    PIA1AD        OUTPUT DEVICE SELECT CODE
2942       LDA    #050N
2944       STA    PIA1AC        DEVICE SELECT "ACTIVE"
2946       LDA    #0SOFF
2948       STA    PIA1AC
2950       RTS
2952       SFC    3
2954       PAGE
2956 *
2958 *          ELECTROLYTE LEVEL SENSING - ROUTINE
2960 *
2962 *          FILTERS LEVEL SENSING INPUT ( .5 HR. )
2964 *          SETS OR RESETS APPROPRIATE DISPLAY INDICATORS ACCORDINGLY
2966 *          ( LED & VFD )
2968 *          INPUT: SYIN
2970 *          USES: EDELAY(2) X,A,B, REG.
2972 *          OUTPUTS: DSTAT , FPOUT
2974 *
2976 FILTE1 EQU    6767          FILTER CONSTANT (6767XX .133 SEC)=15 MIN
2978 *
2980 ELOW   LDX    EDELAY
2982       BNE    *+5            VALID DELAY COUNT
2984       LDX    #FILTE1-1    USE DEFAULT SETTING
2986       CMPX   #FILTE1      15 MIN(TIME CONSTANT)
2988       BLT    ELOW1
2990       LDA    #020          SET WATER INDICATOR "ON" - VFD
2992       ORA    DSTAT
2994       LDE    #004          SET WATER INDICATOR "ON" - LED
2996       ORA    .FPOUT1
2998       BRA    ELOW2
3000 ELOW1 LDA    #00F          RESET VFD INDICATOR
3002       ANDA   DSTAT
3004       LDE    #0FE          RESET LED INDICATOR
3006       ANDB  .FPOUT
3008 ELOW2 STA    DSTAT          SAVE VFD STATUS
3010       STE    .FPOUT        SAVE LED STATUS
3012       LEAX  1,X            ADVANCE DELAY 1 COUNT
3014       LDA    SYIN
3016       EMI    *+4            ELECTROLYTE LOW INDICATION
3018       LEAX  -2,X           DECREMENT DELAY 1 COUNT
3020       CMPX   #001          TEST MIN. COUNT
3022       BLT    ELOW3        YES
3024       CMPX   #FILTE1*2    TEST MAX. COUNT

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3026      BGT      ELOW3      YES
3028      STX      EDELAY      SAVE NEW COUNT
3030 ELOW3      RTS
3032      SFC      3
3034 *
3036 *      EQUALIZE STATUS INDICATORS
3038 *
3040 *      SETS OR RESETS VF AND LED INDICATORS
3042 *      DEPENDING UPON STATUS OF FEQU+1 ; 0 - RESETS ,ELSE- SETS
3044 *      INPUTS : FEQU+1, DSTAT, FFOUT
3046 *      USES : A, B, REG.
3048 *      OUTPUTS : DSTAT, FFOUT
3050 *
3052 EQUAL      TST      FEQU+1      TEST EQUALIZE REQUEST FLAG
3054      BEQ      EQUAL1      INDICATORS "OFF" & RETURN
3056      LDA      #10      "EQUALIZE" ON - VFD
3058      ORA      DSTAT
3060      LDE      #02      "EQUALIZE" ON - LED
3062      ORE      FFOUT
3064      BRA      EQUAL3
3066 EQUAL1     LDA      #EF      "EQUALIZE" OFF - VFD
3068      ANDA     DSTAT
3070      LDE      #FD      "EQUALIZE" OFF - LED
3072      ANDB     FFOUT
3074 EQUAL3     STA      DSTAT      SAVE VFD STATUS
3076      STE      FFOUT      SAVE LED STATUS
3078      RTS
3080      SFC      3
3082 *
3084 *      AC POWER STATUS INDICATOR
3086 *      FLAG: FFIN (B3)
3088 *      "0": AC-ON
3090 *      "1": OFF
3092 *
3094 ACPWR      LDA      FFIN
3096      BITA     #00
3098      BNE     ACPWR1      AC POWER OFF
3100      LDA      #40      "AC-ON" ON -VFD
3102      ORA      DSTAT
3104      BRA     ACPWR2
3106 ACPWR1     LDA      #EF
3108      ANDA     DSTAT
3110 ACPWR2     STA      DSTAT
3112      RTS
3114      SFC      3
3116 *
3118 *      CHARGING STATUS INDICATOR
3120 *      FLAG : FCHG
3122 *      =0 : LED OFF
3124 *      >0 : LED ON
3126 *      <0 : LED FLASHING
3128 *
3130 CHGLED     TST      FCHGL
3132      BEQ      CHGL1
3134      LDA      FFOUT
3136      ORA      #01
3138      STA      FFOUT      SET LED ON
3140      TST      FCHGL      POSITIVE ?

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3142          BFL      CHGL2      YES
3144          LDA      FLASHL
3146          ORA      #$01
3148          STA      FLASHL      SET LED TO FLASH
3150          BRA      CHGL2
3152 CHGL1     LDA      FFOUT
3154          ANDA     #$FE
3156          STA      FFOUT      TURN LED OFF
3158 CHGL2     RTS
3160          SFC      3
3162 *
3164 *          WARNING INDICATOR
3166 *          FLAG : FWARN
3168 *          =0 : OFF
3170 *          >0 : ON
3172 *          <0 : FLASHING
3174 *
3176 WARN      TST      FWARN
3178          BEQ      WARN1
3180          LDA      DSTAT
3182          ORA      #$80
3184          STA      DSTAT      SET WARNING ON
3186          TST      FWARN
3188          BFL      WARN2
3190          LDA      FLASHV
3192          ORA      #$80
3194          STA      FLASHV      SET FLASH ON
3196          BRA      WARN2
3198 WARN1     LDA      DSTAT
3200          ANDA     #$7F
3202          STA      DSTAT      TURN WARNING OFF
3204 WARN2     RTS
3206          SFC      3
3208 *
3210 *          SOC - SUBROUTINE
3212 *          DISPLAYS BARGRAPH 0-100%
3214 *          FLASHES IF DSOC =0 TO 20%
3216 *          DSOC 16 BIT FORTRAN INTERGER
3218 *          DEAR 8 BIT DISPLAY
3220 *
3222 SOC       LDD      DSOC      DISPLAY STATE OF CHARGE
3224          BFL      *+3      DON'T DISPLAY NEGATIVE VALUE
3226          CLR     CLRB
3228          STB     DEAR      ON BAR-GRAPH - 8LSB
3230          CMP     #2      0, 10%, OR 20%
3232          BHI     SOC1      NO
3234          LDA      FLASHV
3236          ORA     #$04      SET FLASH CODE
3238          STA     FLASHV
3240 SOC1     RTS
3242          SFC      3
3244 *
3246 *          FLASH - SUBROUTINE
3248 *
3250 *          FLASHES APPROPRIATE INDICATOR ON VFD OR LED
3252 *          BASED UPON FFLASH+1, FFLASH+2, "1" FLASHES
3254 *          FLASH RATE DEPENDENT ON SETTING AND RESETTING OF FFLASH
3256 *
```

```

3258 *      INPUT : FFLASH, FFLASH+1, FFLASH+2, DSTATM, FFOUT+1
3260 *      USES : A, B REG.
3262 *      OUTPUT : DSTATM, FFOUT+1
3264 *
3266 FLASH TST      FFLASH      FLASH REQUEST?
3268      BFL      FLASH1      NO
3270      LDA      DSTATM
3272      LDB      FFOUT+1
3274      EORA     FLASHV      VFD - BLANK NORMALLY ON ELEMENTS
3276      EORB     FLASHL      LED - BLANK NORMALLY ON INDICATORS
3278      STA      DSTATM
3280      STB      FFOUT+1
3282 FLASH1 RTS
3284      PAGE
3286 *
3288 *      SUBROUTINE : QUICK MULTIPLIER ( RE-ENTRANT ) 16x7 BIT
3290 *      (A,B) * STACK(S)          115 CYCLES - POS.
3292 *      A,B 16 BIT SIGNED NUMBER 170 CYCLES - NEG.
3294 *      MULTIPLIER PRESAVED ON STACK(S) POSITIVE NUMBER <= 128
3296 *      RESULT : STACK, A, B 24 BIT SIGNED NUMBER
3298 *
3300 QMUL  LEAS  -4,S      RESERVE WORKSPACE ON STACK
3302      CLR   0,S      RESET NEGATIVE # FLAG
3304      TSTA  CHECK FOR NEGATIVE #
3306      BFL   QMUL1     NO
3308      INC   0,S      SET NEGATIVE FLAG
3310      COMA  1'S COMPLEMENT
3312      COMB  1'S COMPLEMENT
3314      ADDD  #1       2'S COMPLEMENT
3316 QMUL1 STB   1,S      TEMP. SAVE 2'ND BYTE
3318      LDB   6,S      MULTIPLIER
3320      MUL
3322      TFR   D,X
3324      LDA   1,S      2'ND BYTE
3326      LDB   6,S
3328      MUL
3330      LEAX  A,X      ADD RESULTS TOGETHER
3332      STX   1,S      SAVE 24 BIT ANSWER
3334      STB   3,S
3336      TST   0,S      CHECK FOR NEGATIVE #
3338      BEQ   QMUL2     NO
3340      COM   1,S      COMPLEMENT 24 BITS
3342      COM   2,S
3344      COM   3,S
3346      LDD   2,S
3348      ADDD  #1       FORM 2'S COMPLEMENT
3350      STD   2,S      SAVE COMPLEMENT
3352      ECC   QMUL2
3354      INC   1,S
3356 QMUL2 LDA   1,S
3358      STA   6,S      SAVE 4 MSB IN STACK ON RETURN
3360      LDD   2,S      SAVE 16 LSB IN A,B REG
3362      LEAS  4,S      CLEAN STACK
3364      RTS
3366      SPC   3
3368 *
3370 *      SUBROUTINE : QUICK DIVIDER
3372 *      TRUE ROUND OFF OF (A,B)/2^DIVW

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3374 *          ENTERS WITH DIVISOR PRESAVED AT DIVW
3376 *          DIVW+1 WORKSPACE
3378 *          (A,B) 16 BIT SIGNED NUMBER
3380 *
3382 QDIV CLR DIVW+1 CLEAR WORKSPACE
3384 TSTA NEG NUMBER?
3386 BPL QDIV1 NO
3388 INC DIVW+1 SET NEGATIVE FLAG
3390 BSR COM16 2'S COMPLEMENT
3392 QDIV1 ASRA
3394 RORB /2
3396 DEC DIVW
3398 BGT QDIV1
3400 BCC QDIV2
3402 ADDD #01
3404 QDIV2 TST DIVW+1
3406 BEQ QDIV3
3408 BSR COM16
3410 QDIV3 RTS
3412 SPC 3
3414 *
3416 * 16 BIT 2'S COMPLEMENT OF (A,B)
3418 *
3420 COM16 COMA 1'S COMPLEMENT OF 8 MSB
3422 COMB 1'S COMPLEMENT OF 8 LSB
3424 ADDD #01 2'S COMPLEMENT OF 16 BITS
3426 RTS
3428 PAGE
3430 *
3432 * ROUTINE TO INITIALIZE DISPLAY'S BIT PATTERNS
3434 *
3436 * FOR BLANK DISPLAY--
3438 * & SETS PROPER SEQUENCE CODE TO BRACKET
3440 * SERIAL DATA ( START & FINISH )
3442 *
3444 * INPUT: NONE
3446 * USES: Y, A
3448 * OUTPUTS: VFDATA(6)
3450 * RETURNS: "Y" REG POINTING TO VFDAT1
3452 *
3454 IDISP LDY #VFDATA SET POINTER TO 1'ST DATA
3456 LDA #0A0
3458 STA 0,Y SET FINISH CODE
3460 CLRA BLANK ALL ACTIVE ELEMENTS
3462 STA 1,Y
3464 STA 2,Y
3466 STA 3,Y
3468 STA 4,Y
3470 LDA #0A SET START CODE
3472 STA 5,Y
3474 RTS
3476 SPC 3
3478 *
3480 * CONVERT 8 BIT BINARY VALUE A-REG.
3482 * TO 3 BCD VALUES AT
3484 * DNUM, DUM+1, DUM+2
3486 *
3488 BCD CLR DNUM CLEAR RESULT LOCATIONS

```

```

3490      CLR      DNUM+1
3492 BCD1    SUBA    #100
3494      BCS     BCD2      LESS THAN 100
3496      INC     DNUM      INCREMENT HUNDREDS DIGIT
3498      BRA     BCD1
3500 BCD2    ADDA    #100      RESTORE #
3502 BCD3    SUBA    #10
3504      BCS     BCD4      LESS THAN 10
3506      INC     DNUM+1    INCREMENT TENS DIGIT
3508      BRA     BCD3
3510 BCD4    ADDA    #10      RESTORE #
3512      STA     DNUM+2    SET ONE'S DIGIT
3514      RTS
3516      SPC     3
3518 *
3520 *      BCD TO BINARY CONVERSION
3522 *      ENTERS A-REG WITH BCD NUMBER
3524 *      EXITS A-REG WITH BINARY CONVERSION
3526 *      AFFECTS NO OTHER REGISTERS
3528 *
3530 BINARY  PSHS    B
3532      TFR     A,B        DUPLICATE A-REG
3534      ANDB   #0F        SEPERATE BCD DIGITS
3536      ANDA   #F0
3538      PSHS    B        TEMPORARY SAVE
3540      LDB     #160      X10 & SHIFT 4 POSITIONS
3542      MUL
3544      ADDA   S+        SUM LOWER DIGIT
3546      PULS   B        RETRIEVE ORGINAL CONTENTS
3548      RTS
3550      PAGE
3552 **
3554 **      ERROR SUBROUTINE - SPECIAL FAULT DISPLAY
3556 **
3558 **      ENTER : 'B' REG. CONTAINING ERROR CODES
3560 **      OUTPUTS : DISPLAYS FAULT CODE ON VFD
3562 **      HALTS PROGRAM EXECUTION UNTIL FAULT IS ACKNOWLEDGED BY
3564 **      DEPRESSING REMOTE DISPLAY PUSHBUTTON WHEREUPON EXECUTION
3566 **      RETURNS & TRIES TO CONTINUE
3568 **
3570 ERROR   STE     FFLT      PRE-SET FAULT FLAG
3572      LBSR   DISFLT
3574      LBSR   CDISP
3576 ERR1    LBSR   VFDISP
3578      LBSR   DIN1
3580      LDB     AXIN+1    REMOTE PUSHBUTTON DEPRESSED
3582      BEQ    ERR1      NO
3584      CLR     FFLT      RESET FAULT FLAG
3586      CLR     DFLTC
3588 ERR2    RTS
3590      SPC     3
3592 *
3594 *      PIA INITIALIZATION SEQUENCE
3596 *
3598 *      PA0-PA3  DEVICE SELECT (OUT)
3600 *
3602 *      PA4-PA6  DATA, CLOCK, STROBE & BLANK (OUT)  REMOTE DISPLAY
3604 *      PA7      SW1 (IN)  REMOTE DISPLAY

```

```

3606 *
3608 *      CA1      TIMER INTERRUPT (IN) FIRO
3610 *      CA2      AREADY (OUT)
3612 *
3614 *      PB0-PB7   CMOS DATA BUS (IN OR OUT)
3616 *
3618 *      CB1      ADC EOC (STATUS) - (IN) IRQ
3620 *      CB2      UNUSED
3622 PIAINT LDE      #PIABDR
3624      STB      PIA1BC   SELECT DATA DIRECTION REGISTER
3626      LDA      #FF      PB0-PB7, CONFIGURE AS OUTPUTS
3628      STA      PIA1BD
3630      LDB      #PIABPR   CB1-INPUT - IRQ ENABLED - CB2 (OUT) ="0"
3632      STB      PIA1BC
3634      LDA      PIA1BD   CLEAR IRQ FLAG
3636      LDB      #PIAAPR   CA1 (IN) - FIRO ENABLED - CA2 (OUT) = "1"
3638      STB      PIA1AC   SELECT PERIPHERAL REGISTER
3640      LDA      #FF      PA0-PA6="1" (BLANK DISPLAY)
3642      STA      PIA1AD   FRE-SET OUTPUTS
3644      STA      PIA1AD   DUPLICATE IN RAM
3646      LDB      #PIAADR
3648      STB      PIA1AC   SELECT DATA DIRECTION REGISTER
3650      STA      PIA1AD   PA0-PA6 OUTPUTS ; PA7 INPUT
3652      LDB      #PIAAPR
3654      STB      PIA1AC   SELECT PERIPHERAL REG.
3656      LDA      PIA1AD   CLEAR IRQ FLAG
3658      RTS
3660      PAGE
3662 *
3664 *      SYSTEM DIAGNOSTICS - SUBROUTINES
3666 *
3668 *
3670 *      ROM TEST : CHECKSUM 13 CYCLES/BYTE
3672 *
3674 ROMTST LDX      #ROMS+3  1'ST ROM ADDRESS AFTER ID & CHECKSUM BYTES
3676      CLRA
3678 ROM1   EDRA     0,X+
3680      CMPX     #ROME+1  LAST ROM ADDRESS COMPLETED
3682      BNE      ROM1     NO
3684      CMPA     CKSUM    CHECKSUM VALID
3686      BRA      ROM2     YES ***** TEMP. DEFEATED (BEQ NORMAL BRANCH)*****
3688      LDB      #ERRORM  SET ERROR CODE
3690      LBSR     ERROR
3692 ROM2   RTS
3694      SPC      3
3696 *
3698 *      TEST RAM BY TOGGLING ALL BITS & CHECKING FOR CHANGES 2048 BYTES
3700 *
3702 RAMTST LDX      #0
3704 RAM2   LDA      0,X
3706      COM      0,X      COMPLEMENT RAM LOCATION
3708      ADDA     0,X
3710      CMPA     #FF      CHECK FOR VALID RESULT
3712      BEQ      RAM3     BYTE TEST O.K., NEXT LOCATION
3714      LDB      #ERRRAM  SET ERROR CODE
3716      LBSR     ERROR
3718 RAM3   COM      0,X+   RETURN RAM TO ORIGINAL VALUE
3720      CMPX     #4800    CHECK 2048 BYTES

```



```

3722      BNE      RAM2      NO
3724      RTS
3726      SPC      3
3728 *
3730 *      TEST REAL TIME CLOCK BY SEEING IF MILLISECOND COUNTER ADVANCES
3732 *
3734 CLKTST LDX      #40      RESET SOFTWARE COUNTER
3736 CLK1   LDA      RTCCTS   READ CLOCK COUNTER
3738      LDB      RTCSCR   CHECK FOR VALID READ
3740      BNE      CLK1     READ AGAIN
3742      PSHS     A
3744 CLK2   LEAX     1,X
3746      CMPX     #90      11 CYCLES @ 3.58 MHZ
3748      BNE      CLK2     WAIT 1.1mS
3750 CLK2A  LDB      RTCCTS   READ COUNTER AGAIN
3752      LDA      RTCSCR   CHECK FOR VALID READ
3754      BNE      CLK2A   NO READ AGAIN
3756      CMPB     0,S+     DID CLOCK ADVANCE?
3758      BNE      CLK3     YES
3760      LDB      #ERRCLK  SET ERROR CODE
3762      LBSR     ERROR
3764 CLK3   RTS
3766      SPC      3
3768 *
3770 *      TEST RAM & CLOCK NON-VOLATILITY AUX. POWER
3772 *
3774 PWR1ST LDA      #55      TEST VALUE
3776      TST      FCAL     CALIBRATE REQUESTED
3778      BNE      PWR2     YES
3780      CMPA     RAMS     TEST BOTTOM OF MEMORY
3782      BNE      PWR1     FAILED
3784      CMPA     RAME     TEST TOP OF MEMORY
3786      BEQ      PWR3
3788 PWR1   LDB      #ERRPWR  ERROR
3790      LBSR     ERROR     DISPLAY FAULT
3792      BRA      PWR2A   CONTINUE BUT DON'T RESET
3794 PWR2   STA      RAMS     SET KNOWN TEST VALUE
3796      STA      RAME
3798 PWR2A  LDA      #FF
3800      STA      DEFLT   SET DEFAULT FLAG
3802      STA      RTCORE  RESET CLOCK
3804 PWR3   RTS
3806      SPC      3
3808 *
3810 *      PIA TEST SEQUENCE - AS CONFIGURED IN ECSCI
3812 *      NOTE: B SIDE MUST BE PRESET TO BC OUTPUTS UPON ENTRY
3814 *
3816 PIATST LDA      PIA1AD
3818      BITA     #40      TEST A SIDE INPUTS
3820      BNE      PIA1     OK
3822      LDB      #ERRPIA  ERROR
3824      LBSR     ERROR     DISPLAY ERROR CODE
3826      LDA      PIA1AD
3828 PIA1   COM      PIA1AD  TOGGLE A OUTPUTS
3830      ADDA     PIA1AD
3832      COM      PIA1AD  RETURN OUTPUTS TO ORIGINAL STATES
3834      ANDA     #7F      TEST OUTPUTS B0-B6
3836      CMPA     #7F      OUTPUTS TOGGLED

```

```

3838      BEQ      PIA2      0. K.
3840      LDB      #ERRPOA
3842      LBSR     ERROR
3844 PIA2  LDA      #PIABDR
3846      STA      PIA1EC
3848      LDB      #BFF
3850      STB      PIA1BD    CONFIGURE B SIDE AS OUTPUTS
3852      LDA      #PIABPR
3854      STA      PIA1EC
3856      LDA      PIA1ED
3858      COM      PIA1BD    TOGGLE B DATA REG.
3860      ADDA     PIA1ED
3862      CMPA     #BFF      REGISTER TOGGLES
3864      BEQ      PIA3      YES
3866      LDB      #ERRPOD
3868      LBSR     ERROR
3870 PIA3  LDA      #PIABDR    CONFIGURE B SIDE AS INPUTS
3872      STA      PIA1EC
3874      CLR      PIA1BD
3876      LDA      #PIABPR
3878      STA      PIA1EC
3880      LDA      PIA1BD
3882      CMPA     #BFF      B INPUTS PULLED HIGH
3884      BEQ      PIA4      YES
3886      LDB      #ERRPIB
3888      LBSR     ERROR
3890 PIA4  RTS
3892      SPC      3
3894 *
3896 * TEST ANALOG TO DIGITAL CONVERTER
3898 *
3900 ADCTST LDD      TEST#.U    2.5 V TEST REFERENCE
3902      CMPD     #2675    UPPER LIMIT
3904      BGT      ADC1      OUT OF RANGE
3906      CMPD     #2325    LOWER LIMIT
3908      BGT      ADC2      OK
3910 ADC1  LDB      #ERRADC    SET ERROR CODE
3912      LBSR     ERROR
3914 ADC2  RTS
3916      SPC      3
3918 *
3920 * TEST THERMISTOR INPUTS - FOR OPENS OR SHORTS
3922 *
3924 TMPTST LDX      #TBLTUS    SET POINTER TO 1ST TABLE LOCATION
3926 TMPL1  LDA      0. X      READ VARIABLE OFFSET
3928      LDD      A. U      READ VARIABLE
3930      CMPD     #50       TEST FOR SHORTS
3932      BGT      TMP2      0. K.
3934      LDB      1. X      FETCH ERROR CODE FROM TABLE
3936      PSHS     X         SAVE TABLE POINTER
3938      LBSR     ERROR     DISPLAY SHORTED ERROR CODE
3940      BRA      TMP3      TEST NEXT INPUT
3942 TMP2  SUBD     TREF#.U
3944      CMPD     #-50      TEST FOR OPENS
3946      BLT      TMP4      0. K.
3948      LDB      2. X      FETCH ERROR CODE FROM TABLE
3950      PSHS     X
3952      LBSR     ERROR     DISPLAY OPEN ERROR CODE

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3954 TMP3    FULS    X          RETRIEVE LAST POINTER LOCATION
3956 TMP4    LEAX    3,X        NEXT TABLE ENTRY
3958        CMPX    #TELTDE    TEST FOR LAST ENTRY
3960        ELS     TMP1
3962        RTS
3964        SPC     3
3966 *
3968 *    SOFTWARE TRAP - MACRO
3970 *
3972 *
3974 TRAP    MACR
3976        SWI
3978        SWI
3980        SWI
3982        ENDM
3984        PAGE
3986 **
3988 **    TABLE
3990 **    MULTIPLEXER SEQUENCING FOR EACH OPERATING MODE
3992 **
3994 **    1ST BYTE - OFFSET TO STORAGE LOCATION FOR EACH
3996 **                ANALOG INPUT
3998 **
4000 **    2ND BYTE - MULTIPLEXER ADDRESS FOR EACH ANALOG INFUT
4002 **
4004 *
4006 *    CHARGE MODE
4008 *
4010 MUXCHG  FDB     IBAT.
4012        FDB     VBAT.
4014        FDB     ILINE.
4016        FDB     TBAT.
4018        FDB     IBAT.
4020        FDB     VBAT.
4022        FDB     ILINE.
4024        FDB     TENC.
4026        FDB     IBAT.
4028        FDB     VBAT.
4030        FDB     ILINE.
4032        FDB     TFET.
4034        FDB     END.
4036 *
4038 *    DISCHARGE MODE
4040 *
4042 MUXDIS  FDB     IBAT.
4044        FDB     VBAT.
4046        FDB     IBAT.
4048        FDB     TBAT.
4050        FDB     IBAT.
4052        FDB     TENC.
4054        FDB     END.
4056 *
4058 *    REST MODE
4060 *
4062 MUXRST  FDB     VBAT.
4064        FDB     TBAT.
4066        FDB     TENC.
4068        FDB     END.

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4070 *
4072 *   THINK MODE
4074 *
4076 MUXTHK FDB   TENC.
4078       FDB   END.
4080 *
4082 *   DIAGNOSTIC MODE
4084 *
4086 MUXDIA FDB   TREF.
4088       FDB   TFET.
4090       FDB   TENC.
4092       FDB   TAMB.
4094       FDB   TBAT.
4096       FDB   TEST.
4098       FDB   END.
4100       PAGE
4102 **
4104 **   TABLES : SELECT MODE LOOK-UP
4106 **
4108 **   0 PTR TO EXECUTIVE/MPL MODE ROUTINE
4110 **   FOR PTR TO FORTRAN ROUTINE
4112 **   ADC PTR TO MULTIPLEXER TABLE
4114 **   DISP1 NORMAL DISPLAY
4116 **   DISP2 OPTIONAL DISPLAY ( SW1 DEPRESSED )
4118 **
4120 FOR     EQU     2           ADDRESS OF FORTRAN ROUTINE
4122 ADC     EQU     4           ADDRESS OF MULTIPLEXER TABLE
4124 DISP1   EQU     6
4126 DISP2   EQU     8
4128 *
4130 *   CHARGE MODE
4132 *
4134 TELCHG FDB   CHGMPL
4136       FDB   CHGFOR
4138       FDB   MUXCHG
4140       FDB   $000F   BLANK - VFD ; ENABLE - LED'S
4142       FDB   $C50F   AC-ON, WARNING, BAR, GRID - VFD; ENABLE LED'S
4144 *
4146 *   DISCHARGE MODE
4148 *
4150 TELDTS FDB   DTSCHG
4152       FDB   DISFOR
4154       FDB   MUXDIS
4156       FDB   $0500   BARGRAPH - VFD ; BLANK LED
4158       FDB   $0300   NUMERIC - VFD ; BLANK LED
4160 *
4162 *   REST MODE
4164 *
4166 TELRST FDB   REST
4168       FDB   RSTFOR
4170       FDB   MUXRST
4172       FDB   $0008   BLANK - VFD ; BLANK - LED ; ALLOW FAULT
4174       FDB   $0508   BARGRAPH - VFD ; BLANK - LED ; ALLOW FAULT
4176 *
4178 *   THINK MODE
4180 *
4182 TELTHK FDB   THINK
4184       FDB   THKFOR

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```

4186      FDB      MUXTHK
4188      FDB      $0008      BLANK - VFD ; BLANK - LED ; ALLOW FAULT
4190      FDB      $0508      BARGRAPH - VFD ; BLANK - LED ; ALLOW FAULT
4192 *
4194 *      DIAGNOSTIC MODE - USED DURING INITIALIZATION ONLY
4196 *
4198 TELDIA FDB      0
4200      FDB      0
4202      FDB      MUXDIA
4204      FDB      0
4206      FDB      0
4208      PAGE
4210 **
4212 **      TABLE: BINARY TO SEVEN SEGMENT DECODER      f      b
4214 **      BIT7-0      0sfedcba      SEGMENT DESIGNATION      s
4216 **
4218 **
4220 **
4222 TELNUM FCB      %00111111 (0) 0
4224      FCB      %00000110 (1) 1
4226      FCB      %01011011 (2) 2
4228      FCB      %01001111 (3) 3
4230      FCB      %01100110 (4) 4
4232      FCB      %01101101 (5) 5
4234      FCB      %01111101 (6) 6
4236      FCB      %00000111 (7) 7
4238      FCB      %01111111 (8) 8
4240      FCB      %01100111 (9) 9
4242      FCB      %01000000 (A) -
4244      FCB      %00000000 (B)
4246      FCB      %00000000 (C)
4248      FCB      %00000000 (D)
4250      FCB      %00000000 (E)
4252      FCB      %00000000 (F) BLANK
4254      SFC      3
4256 **
4258 **      TABLE : BAR-GRAPH PERCENT STATE OF CHARGE
4260 **
4262 **
4264 TELBAR FDB      $0400      0%
4266      FDB      $0401      10%
4268      FDB      $0403      20%
4270      FDB      $0407      30%
4272      FDB      $040F      40%
4274      FDB      $041F      50%
4276      FDB      $043F      60%
4278      FDB      $047F      70%
4280      FDB      $04FF      80%
4282      FDB      $05FF      90%
4284 TELBAE FDB      $07FF      100%
4286      SFC      3
4288 **
4290 **      TABLE : TEST DISPLAY SEQUENCE
4292 **
4294 **      Z-BYTE ADDRESS OF VARIABLE LOCATION
4296 **
4298 **      MAXIMUM LENGTH, TEN CHARACTERS
4300 **

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```

4302 **
4304 TELTST FDB ID
4306 FDB VBAT
4308 FDB VBAT+1
4310 FDB V LIM
4312 FDB V LIM+1
4314 FDB AMFH
4316 FDB AMFH+1
4318 FDB IBAT
4320 FDB IBAT+1
4322 TELTSE FDB FMODE+1
4324 SFC 3
4326 **
4328 ** TIME TABLE: USED BY TIME ROUTINE TO ADVANCE COUNTERS
4330 ** ENTRIES ARE ADDRESSES OF COUNTERS
4332 ** TO BE ADVANCED
4334 **
4336 TELTIM FDB EQU TIM
4338 FDB DISTIM
4340 TELTIE FDB CHG TIM
4342 PAGE
4344 **
4346 ** TABLE OF THERMISTOR LIMITS
4348 ** 1ST BYTE - OFFSET TO VARIABLE ADDRESS STORAGE LOCATION
4350 ** 2ND BYTE - FIRST LIMIT CAUSES FAULT INDICATION
4352 ** 3RD BYTE - SECOND LIMIT CAUSES POWER STAGE TO BE DISABLED
4354 **
4356 TELTEM FCB TBAT$ THERMISTOR - BATTERY ELECTROLYTE
4358 FDB 1060 50 C
4360 FDB 0
4362 FCB ERR TBA
4364 FCB TENC$ THERMISTOR - MAIN ENCLOSURE
4366 FDB 696 65 C
4368 FDB 596 70 C
4370 FCB ERR TEN
4372 FCB TFET$ THERMISTOR - FET HEATSINK
4374 FDB 521 75 C
4376 FDB 446 80 C
4378 FCB ERR TFE
4380 FCB TAMB$ THERMISTOR - BATTERY AMBIENT
4382 FDB 596 70 C
4384 FDB 0
4386 TELTEE FCB ERR TAM
4388 SFC 3
4390 **
4392 ** THERMISTOR ERROR CODE TABLE
4394 ** 1ST BYTE OFFSET TO VARIABLE STORAGE LOCATION
4396 ** 2ND BYTE SHORTED ERROR CODE
4398 ** 3RD BYTE OPEN ERROR CODE
4400 **
4402 TELTOS FCB TBAT$, ERR TBS, ERR TBO
4404 FCB TENC$, ERR TES, ERR TEO
4406 FCB TFET$, ERR TFS, ERR TFO
4408 TELTOE FCB TAMB$, ERR TAS, ERR TAO
4410 SFC 3
4412 **
4414 ** TABLE LOOK-UP:
4416 ** THERMISTOR LINEARIZATION

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```

4418 **      SIERRAN-WESTERN #1M1002-A2
4420 **      VREF=4.000 V ; R=10K BIASING
4422 **      OFFSET BY 40 C
4424 **
4426 TELTHE FCB      185      145 C (0.00V) ACTUAL TEMPERATURE
4428 FCB      140      100 C (.256V)
4430 FCB      115      75 C (.512V)
4432 FCB      101      61 C (.768V)
4434 FCB      91       51 C (1.024V)
4436 FCB      83       43 C (1.280V)
4438 FCB      76       36 C (1.536V)
4440 FCB      70       30 C (1.792V)
4442 FCB      64       24 C (2.048V)
4444 FCB      58       18 C (2.304V)
4446 FCB      52       12 C (2.560V)
4448 FCB      46       6 C (2.816V)
4450 FCB      40       0 C (3.072V)
4452 FCB      32      -8 C (3.328V)
4454 FCB      22     -18 C (3.584V)
4456 FCB      5      -35 C (3.840V)
4458 FCB      0     -40 C (4.096V) "OFF SCALE"
4460 PAGE
4462 **
4464 **      EQUATE TABLE OF SYSTEM ERROR CODES
4466 **
4468 **      4 MSB PRIMARY - ASSEMBLY NUMBER
4470 **      4 LSB SECONDARY - ERROR WITHIN ASSEMBLY
4472 **
4474 * NOTE:      $0X      INDICATES RUN TIME FAULTS CHECK MPL LISTING
4476 *
4478 ERRPWR EQU      $11      AUX. - POWER DEFECTIVE - RAM, TIME INFO. LOST
4480 *
4482 ERRCHG EQU      $21      POWER STAGE FAULT USED INLMPL
4484 *
4486 ERRADC EQU      $31      A/D CONVERSION INVALID
4488 ERROF EQU      $32      A/D OVERFLOW INDICATION
4490 ERRNEG EQU      $33      ANALOG INPUT INCORRECT POLARITY
4492 ERRSM1 EQU      $34      SELECT MODE - INVALID MODE
4494 *
4496 ERRROM EQU      $41      ROM CHECKSUM ERROR
4498 ERRRAM EQU      $42      BITS IN RAM WILL NOT TOGGLE
4500 ERRCIO EQU      $43      1/SEC INTERRUPT
4502 ERRCLK EQU      $44      REAL TIME CLOCK DOESN'T ADVANCE
4504 ERRPIA EQU      $45      PIA A INPUT FAULT
4506 ERRPIB EQU      $46      PIA B INPUT FAULT
4508 ERRPOA EQU      $47      PIA A OUTPUT FAULT
4510 ERRPOB EQU      $48      PIA B OUTPUT FAULT (INTERNAL)CHECK ONLY)
4512 *
4514 ERRTES EQU      $70      BATTERY THERMISTOR SHORTED
4516 ERRTEB EQU      $71      ENCLOSURE THERMISTOR SHORTED
4518 ERRTFS EQU      $72      FET THERMISTOR SHORTED
4520 ERRTAS EQU      $73      AMBIENT THERMISTOR SHORTED
4522 ERRTEO EQU      $75      BATTERY THERMISTOR OPEN OR FUSE BLOWN
4524 ERRTEB EQU      $76      ENCLOSURE THERMISTOR OPEN
4526 ERRTFO EQU      $77      FET THERMISTOR OPEN OR FUSE BLOWN
4528 ERRTAO EQU      $78      AMBIENT THERMISTOR OPEN OR FUSE BLOWN
4530 *
4532 ERRTEA EQU      $81      BATTERY OVERTEMP.

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PAGE 040 BCSCI . SA: 1

| | | | | |
|------|--------|-----|------|------------------------------------|
| 4534 | ERRTEN | EQU | \$82 | ENCLOSURE OVERTEMP. |
| 4536 | ERRTFE | EQU | \$83 | FET OVERTEMP. |
| 4538 | ERRTAM | EQU | \$84 | AMBIENT OVERTEMP. |
| 4540 | * | | | |
| 4542 | ERRBAT | EQU | \$91 | BAT. BELOW MIN. VALUE |
| 4544 | ERRFPI | EQU | \$92 | INVALID SWITCH SETTING |
| 4546 | ERRSOF | EQU | \$93 | SPEED TRANSDUCER CALIBRATION ERROR |
| 4548 | ERRSHI | EQU | \$94 | SPEED COUNTER OVERFLOW |
| 4550 | ERR | EQU | \$99 | |
| 4552 | | END | | |

PAGE 001 VECTOR SA:1

```
0010      NAM      VECTOR
0020      OPT      REL, CRE, P=58, G, LLE=120
0030      TTL      -***-      VECTOR TABLE BCSCI
0040 *
0050 *      11/5/82 ASSEMBLY DATE : J. R. M
0060 *
0070 *      DISK #200 (BACKUP : #210)
0080 *      VECTOR SA SOURCE FILE
0090 *      VECTOR PO OBJECT FILE
0100 *
0110      XREF      INIT, FIRQ, IRQ
0120 **
0130 **      INTERRUPT VECTOR STORAGE
0140 **
0150      ASCT
0160      ORG      $FFF2
0170 *
0180      FDB      INIT      SWI3 VECTOR (UNUSED)
0190      FDB      INIT      SWI2 VECTOR (UNUSED)
0200      FDB      FIRQ      FAST INTERRUPT VECTOR (TIMER 1/SEC)
0210      FDB      IRQ      NORMAL INTERRUPT VECTOR (EOC -ADC)
0220      FDB      INIT      SWI VECTOR (TRAP RESTART)
0230      FDB      INIT      NMI VECTOR (UNUSED)
0240      FDB      INIT      RESTART VECTOR (POWER-UP & WATCH-DOG)
0250      END
```

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0010 /*      CHGMPL :
0020      CHARGER CONTROL SUBROUTINE CALLED BY BC/SCI EXECUTIVE
0030      THIS PROGRAM CONTROLS THE POWER STAGE BY INCREMENTING
0040      OR DECREMENTING THE CONTROL SET POINT CCOU AS REQUIRED.
0050      CCOU : BIT7=ENABLE ; BIT0-6=MAGNITUDE
0060
0070      THE REGULATING ALGORITHM FOLLOWS A CONSTANT POWER PROFILE
0080      REGULATING TO ILIM (ILINE MAX) DEPENDENT UPON FRONT PANEL SWITCH
0090      CHARGING UP TO THE V LIM SET BY THE CHARGE MONITOR ALGORITHM.
0100      THE CONTROL ALGORITHM WILL THEN REGULATE AT THIS VOLTAGE
0110      SETPOINT UNTIL THE CHARGE MONITOR ALGORITHM DETERMINES
0120\     THAT THE CHARGE CYCLE IS FINISHED. (BY SETTING V LIM=0)
0130
0140      POWER STAGE STATUS MAYBE VERIFIED BY CHECKING FCHG (1=ON ; 0=OFF)
0150
0160      STATUS INDICATORS ( "CHARGE" & "EQUALIZE" ) ARE CONTROLLED AS
0170      APPROPRIATE DURING THE CHARGE CYCLE.
0180      "CHARGE" - WILL FLASH DURING POWER ON DELAY
0190                - STEADY WHEN POWER STAGE ENABLED
0200      "EQUALIZE" - REQUESTED ONLY BY ALGORITHM BUT MAYBE DEFERED
0210                  (OR TOGGLED) BY DEPRESSING SW2
0220
0230      THIS ROUTINE ALSO PROVIDES POWER STAGE PROTECTION FOR THE FOLLOWING
0240      ABNORMAL CONDITIONS:
0250                LOW BATTERY VOLTAGE - LIMIT MAX CURRENT
0260                HIGH BATTERY VOLTAGE - INHIBIT CHARGER OPERATION
0270                TIME LIMIT - FOR OPERATION AT BELOW NORMAL VOLTAGE LEVELS
0280                TIME LIMIT - TO VOLTAGE REGULATION POINT
0290
0300      VERSION 1.0 28-JUNE-82 JOHN R MEZERA
0310      FILE: CHGMPL4 11/6/82
0320 */
0330
0340 $      NAM      CHGMPL
0350
0360 CHGMPL:  PROCEDURE
0370          GO TO CHGM1      ! SKIP AROUND CONSTANT TABLE
0380
0390
0400
0410 /*
0420      SCALING FACTORS:
0430                BATTERY VOLTAGE - 50 MV / BIT
0440                AC LINE CURRENT - .01 AMP / BIT
0450                FAULT TIMER      - 2 MIN / BIT
0460
0470      CONSTANTS:
0480
0490          UNLESS OTHERWISE SPECIFIED ALL VOLTAGES REFER TO BATTERY VOLTAGES
0500          AND ALL CURRENTS REFER TO AC LINE CURRENTS
0510
0520          VHYS - VOLTAGE HYSTERSIS FOR REGULATION SETPOINT
0530          VHYS2 - VOLTAGE HYSTERSIS FOR FAULT TIMER
0540          IHYS - CURRENT HYSTERSIS FOR REGULATION SETPOINT
0550          ILOW - REDUCED LINE CURRENT SETPOINT FOR LOW BATTERIES
0560          VMIN - MINIMUM VOLTAGE POWER STAGE WILL CHARGE
0570          VMAX - MAXIMUM VOLTAGE BEFORE FAULT DISABLE
0580          VLOW - ABNORMALLY LOW VOLTAGE WHERE CHARGE CURRENT IS LIMITE

```

```

0590
0600          FTIM1 -   FAULT TIME FOR LOW VOLTAGE OPERATION
0610          FTIM2 -   FAULT TIME BEFORE VOLTAGE REGULATION POINT
0620 */
0630
0640          DCL PSCT VHYS   SIGNED BIN(2) INIT(5)      ! .25 V / .050V/BIT
0650          DCL PSCT VHYS2 SIGNED BIN(2) INIT(100)     ! 5 V / .050V/BIT
0660          DCL PSCT IHYS   SIGNED BIN(2) INIT(5)      ! .05 AMPS / .01A/BIT
0670          DCL PSCT ILOW   SIGNED BIN(2) INIT(200)    ! 2 AMPS / .01A/BIT
0680          DCL PSCT VMIN   SIGNED BIN(2) INIT(1800)   ! 90 VOLTS / .050V/BIT
0685 */      Temp. changed from normal          (300)   ! 40 VOLTS / .050V/BIT */
0690          DCL PSCT VMAX   SIGNED BIN(2) INIT(3100)   ! 155 VOLTS / .050V/BIT
0700          DCL PSCT VLOW   SIGNED BIN(2) INIT(1800)   ! 90 VOLTS / .050V/BIT
0710          DCL PSCT FTIM1   BIN(2) INIT(15)         ! 30 MIN / 2MIN/BIT
0720          DCL PSCT FTIM2   BIN(2) INIT(600)         ! 20 HOURS / 2MIN/BIT
0730
0740
0750
0760 */      COMPILER TIME CONSTANTS:
0770
0780          ERRELO -   BATTERY BELOW MIN VALUE
0790          ERREHI -   BATTERY ABOVE MAX VALUE
0800          ERREOP -   BATTERY DISCONNECTED DURING OPERATION (OPENED)
0810          ERRTF1 -   TIME FAULT #1 - FOR LOW VOLTAGE OPERATION
0820          ERRTF2 -   TIME FAULT #2 - BEFORE VOLTAGE REGULATION
0830          ERRSW3 -   INVALID SWITCH SETTING FOR CHARGER OPERATION
0840          ERRCHG -   POWER STAGE FAULT
0850 */
0860
0870 */      FAULT ERROR CODES APPEAR ON DISPLAY AS : 0-X OR 2-X      */
0880
0890          DCL   ERRELO   CONST($01)
0900          DCL   ERREHI   CONST($02)
0910          DCL   ERREOP   CONST($03)
0920          DCL   ERRTF1   CONST($04)
0930          DCL   ERRTF2   CONST($05)
0940          DCL   ERRSW3   CONST($06)
0950
0960          DCL   ERRCHG   CONST($21)
0970
0980
0990
1000 */
1010          VARIABLES :
1020          ILINE -   AC LINE CURRENT
1030          CCOUT -   CHARGER CONTROL OUTPUT SETPOINT NORMAL CONTROL RANGE
1040          $80 -> $FF ; E7=ENABLE E6-E0 - MAGNITUDE
1050          DDCOUNT - INTERNAL DELAY COUNTER FOR SETPOINT UPDATE
1060          ILIM -   CURRENT REGULATION LIMIT
1070          FFIN -   FRONT PANEL SWITCH INPUTS (1ST BYTE DATA INFORMATION)
1080          SYIN -   SYSTEM INPUTS (BIT6 = POWER STAGE FAULT)
1090          PTR -   TABLE LOOK-UP POINTER
1100 */
1110
1120
1130          DCL DSCT ILINE SIGNED BIN(2) EXTERNAL ! FORTRAN & EXECUTIVE
1140          DCL BSCT CCOUT SIGNED BIN(1) EXTERNAL
1150          DCL BSCT DDCOUNT BIN(1)

```

1160 DCL DSCT ILIM SIGNED BIN(2)
 1170 DCL BSCT FPIN BIN(1) EXTERNAL ! EXEC. ONLY UPPER BYTE
 1180 DCL BSCT SYIN BIN(1) EXTERNAL ! EXECUTIVE
 1190 DCL BSCT PTR BIN(2)

1200
 1210
 1220
 1230 /*

1240 FLAGS: MODE FLAG.
 1250 FCHGL - CHARGE LIGHT (INDICATOR FLAG)
 1260 0 ="OFF"; 1="ON" ; -1=FLASH
 1270 FPWR - FULL POWER FLAG SET IF POWER STAGE HAS
 1280 BEEN FULLY ENABLED DURING PRESENT CHARGE CYCLE
 1290 FPWR? - POWER STAGE IS OR WAS ENABLED
 1300 FCHGS - CHARGER STATUS FLAG 1="ON"; 0="OFF"
 1310 FFLT - FAULT FLAG ERROR CODES

1320 */
 1330

1340 DCL BSCT FCHGL SIGNED BIN(1) EXTERNAL
 1350 DCL BSCT FPWR BIN(1)
 1360 DCL BSCT FPWR2 BIN(1) ! EXECUTIVE
 1370 DCL BSCT FCHGS SIGNED BIN(1)
 1380 DCL BSCT FFLT BIN(1) EXTERNAL

1390
 1400
 1410
 1420 /*

1430 COMMON SECTION WITH FORTRAN AND EXECUTIVE MODULES
 1440 BLANK COMMON VARIABLES:
 1450 FMODE - MODE FLAG 0 = NORMAL, 1 - EXECUTIVE REQUEST CHANGE;
 1460 -1 = FORTRAN GRANTS CHANGE
 1470 WAKEF - WAKE UP FLAG BCD (DAYS; HOURS)
 1480 VLIM - VOLTAGE REGULATION LIMIT

1490
 1500

XXXX - 4 BYTES NOT USED BY CHGMPL

1510
 1520

VBAT - BATTERY VOLTAGE

1530
 1540

XXXX - 34 BYTES NOT USED BY CHGMPL

1550
 1560

FEQU - EQUALIZE FLAG 0=NO; -1=YES; SET INITIALLY
 BY CHARGE MONITOR ALGORITHM

1570
 1580

FRMULL - LOWER BYTE OF PTR01 SET (FF) OR RESET (0) DEPENDING
 UPON FRONT PANEL DEFER SWITCH (SW2)

1590
 1600

XXXX - 12 BYTES NOT USED BY CHGMPL

1610
 1620

CHGTIM - CHARGE CYCLE TIMER

1630
 1640 */
 1650

1660
 1670 DCL CSCT FMODE SIGNED BIN(2) ! FORTRAN & EXECUTIVE
 1680 DCL CSCT WAKEF BIN(2)
 1690 DCL CSCT VLIM SIGNED BIN(2) ! FORTRAN & EXECUTIVE
 1700 \$ CSCT
 1710 \$ FMB 4
 1720 DCL CSCT VBAT SIGNED BIN(2) ! FORTRAN & EXECUTIVE
 1730 \$ CSCT

```

1740 $           RMB      34
1750           DCL CSCT   FEQU   SIGNED BIN(2)           ! EXECUTIVE
1760 $           CSCT
1770 $           RMB      12
1780           DCL CSCT   CHGTIM       BIN(2)
1790
1800
1810
1820 /*          TABLE LOOK-UP MAX LINE CURRENT XX.XX AMPS RMS */
1830
1840           DCL PSCT   TELAMP(1,4) SIGNED BIN(2) INIT(300,600,900,0)
1850           DCL           DATA       SIGNED BIN(2) BASED
1860
1870
1880
1890 CHGM1:
1900 /*          TEST FOR PROPER STATUS BEFORE ENABLING OPERATION
1910           DISABLE IF MODE CHANGING OR SETPOINT NOT YET VALID */
1920
1930           IF (FMODE # 0) OR (VLIM < 2160) THEN !CHANGING OR INVALID?
1940           DO                                     ! YES
1950           WAKEF = $0700                         ! SET 7 DAY WAKE-UP TIME
1960           FPWR = 0                               ! INITIALIZE FLAGS
1970           CHGTIM= 0                              ! INITIALIZE / RESET TIMER
1980           GO TO CHGOFF                           ! DISABLE POWER STAGE AND RETURN
1990           END
2000
2010
2020
2030 /*          TEST FOR POWER STAGE FAULT NOTE: FAULT BIT (SYIN BIT6)
2040           1=FAULT - IF POWER STAGE NEVER ENABLED
2050           0=FAULT - ONCE POWER STAGE ENABLED           */
2060
2070 $ LDA SYIN
2080 $ ANDA #$40 MASK OFF ALL BUT FAULT BIT
2090 $ LDB FPWR2
2100 $ CMPD #$0
2110 $ BEQ CHGM2 OK; FOR DISABLED STATE
2120 $ CMPD #$4000
2130 $ BGT CHGM2 OK; FOR ENALED STATE
2140
2150           FFLT=ERRCHG                            ! SET "CHARGER" ERROR CODE
2160           GO TO CHGOFF                           ! DISABLE CHARGER AND RETURN
2170
2180
2190 CHGM2:
2200
2210 /*          TEST FOR ABNORMAL CONDITIONS AND FLAG FAULTS */
2220
2230           IF VBAT < VMIN THEN                    ! IS BATTERY BELOW MIN VALUE?
2240           DO
2250           FFLT = ERRELO                            ! YES, SET "BATTERY LOW" ERROR CODE
2260           GO TO CHGOFF
2270           END
2280
2290           IF VBAT > VMAX THEN                    ! IS BATTERY ABOVE MAX VALUE
2300           DO
2310           FFLT = ERREHI                            ! YES, SET "BATTERY HIGH" ERROR CODE

```

```

2320             GO TO CHGOFF
2330             END
2340
2350
2360
2370 /* TEST FOR LOW VOLTAGE CHARGER OPERATION & LIMIT PERFORMANCE */
2380
2390             IF VBAT < VLOW THEN ! LOW VOLTAGE MODE?
2400             DO ! YES
2410                 IF (FPWR=1) AND (VBAT < VLOW - VHYS2) THEN ! WAS IT IN NORMAL MODE?
2420                 DO ! YES
2430                     FFLT=ERRBOP ! SET "BATTERY OPEN" ERROR CODE
2440                     GO TO CHGOFF
2450                 END
2460
2470             ELSE ! NO
2480             DO
2490                 ILIM=ILOW ! CONTROL TO LOW CURRENT LIMIT
2500
2510                 IF CHGTIM > FTIM1 THEN ! LOW VOLTAGE OPERATION TOO LONG?
2520                 DO ! YES
2530                     FFLT=ERRTF1 ! SET "TIME FAULT #1" ERROR CODE
2540                     GO TO CHGOFF
2550                 END
2560
2570                 ELSE GO TO CHGM3
2580             END
2590             ELSE
2600             DO
2610                 FPWR=1 ! SET NORMAL OPERATION
2620
2630
2640
2650
2660 /* TABLE LOOK-UP FOR NORMAL CURRENT LIMIT */
2670
2680             IF (FPIN & #07=0) OR (FPIN & #07>4) THEN
2690             DO
2700                 FFLT=ERRSW3 ! INVALID SWITCH SETTING
2710                 GO TO CHGOFF ! DISABLE CHARGER
2720             END
2730             PTR= ADDR(TBLAMP) + ((FPIN & #07 - 1) % 1) ! INDEX TO PROPER ENTRY
2740             ILIM=PTR->DATA ! SET CURRENT LIMIT
2750             END
2760
2770
2780 CHGM3:
2790
2800 /* TEST FOR CHARGE TIME FAULT */
2810
2820             IF (VBAT < V LIM - VHYS2) AND (CHGTIM > FTIM2) THEN
2830             DO
2840                 FFLT=ERRTF2 ! SET FAULT TIME #2 ERROR CODE
2850                 GO TO CHGOFF ! DISABLE POWER STAGE AND RETURN
2860             END
2870
2880
2890

```

```

2900 /* DEFER EQUALIZE CYCLE BY OPERATOR REQUEST */
2910
2920     IF FEQU <= -1 THEN           ! ALGORITHM REQUESTS EQUALIZE CYCLE
2930     DO                               ! CHECK FOR OPERATOR DEFERAL
2940 $   LDD FFIN                       IS SW2 DEPRESSED?
2950 $   BPL CHGCTL                     NO
2960 $   BITE #480                      JUST DEPRESSED?
2970 $   BEQ CHGCTL                     NO
2980 $   COM FEQU+1                     TOGGLE EQUALIZE STATUS
2990     END
3000     ELSE   FEQU=0                   ! INSURE VALID EQUALIZE FLAG
3010
3020
3030
3040 /* DELAY INITIAL CHARGER TURN-ON
3050     IF POWER STAGE OFF AND DELAY SEQUENCE NOT ALREADY STARTED */
3060
3070 CHGCTL:
3080     IF (CCOUT>=0) AND (FCHGL>=0) THEN ! START DELAY?
3090     DO                               ! YES
3100         CHGTIM=0                   ! INITIALIZE CHARGE TIMER
3110         FCHGL=-1                  ! FLASH CHARGE INDICATOR
3120         DCOUNT=0                  ! INITIALIZE DELAY COUNTER
3130     END
3140
3150     IF DCOUNT > 75 THEN ! DELAY COMPLETE?
3160     DO                               ! YES
3170         CCOUT=480                  ! ENABLE POWER STAGE
3180         FCHGL=1                    ! TURN CHARGE LIGHT ON
3190         FCHGS=1                    ! SET CHARGER STATUS
3200         FPR2=1                     ! FLAG ENABLED CONDITION
3210         DCOUNT=0                  ! RESET DELAY COUNTER
3220     END
3230
3240
3250
3260 /* CONTROL SETPOINT UPDATE ONCE EVERY 4TH CYCLE */
3270
3280     IF (DCOUNT>4) AND (CCOUT<0) THEN ! 4TH CYCLE?
3290     DO                               ! YES
3300
3310         IF ((VBAT>V LIM) OR (ILINE>I LIM)) AND (CCOUT>480)
3320         THEN CCOUT=CCOUT-1 ! DECREMENT CONTROL SETPOINT
3330     ELSE
3340     DO
3350         IF (VBAT<V LIM-V HYS) AND (ILINE<I LIM-I HYS) AND
3360         (CCOUT<4FF) THEN CCOUT=CCOUT+1 ! INCREMENT SETPOINT
3370     END
3380
3390         DCOUNT=0                    ! RESET CYCLE COUNT
3400     END
3410
3420     DCOUNT=DCOUNT+1                ! ADVANCE DELAY COUNTER
3430     GO TO CHGEND                    ! RETURN
3440
3450
3460 CHGOFF:   FCHGS=0                  ! SET CHARGER STATUS
3470         FCHCL=0                    ! TURN OFF CHARGE INDICATOR

```

PAGE 007 CHGMPL . SA: 1

3480 CCOUT=0 ! DISABLE POWER STAGE
3490
3500
3510 CHGEND: RETURN
3520 END

C INIFOR Motorola-6809 ndh:29-Sep-82
 C
 C Written by - Neil D. Herbert 29-Sep-82
 C Computer & Software Systems
 C Gould Electronics Laboratory
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472
 C

C Modifications:

C *****
 C Initialize Variables Ver 0.0
 C *****

C Description:

C If necessary, the battery voltage and temperature
 C are used to determine the state of charge.

C Inputs: Battery voltage & temperature.

C Outputs: Corrected Amp-hour meter value.

C Subprograms called: VEQ

SUBROUTINE INIFOR

*H INIFOR

C Arguments: (none)

C Standard Formats:

C Declarations:

```

COMMON IFMODE, IWAKEF, IVLIM, IFINI
COMMON IIBAT, IVBAT, ITBAT, ISPEED
COMMON AMPSF, TEMPF, PWERF, SPDF
COMMON IQBAT, ICEATX, IQLAST, IQABS
COMMON IFRST, IFCHG, IFTHK
COMMON IFEQU, IRESET, ISPCAL
COMMON IDSOC, IDMLE, IDCTIM, IEQTIM, ICGTIM
COMMON R1(4,3), R2(4,3), Q2(4,3)
COMMON RK1, RK2, RK3, RK4
COMMON VEQ1, VEQ2, VEQ3, VEQ4
COMMON BCFQ, BCFV, BCFTIM
    
```

C Function Definitions:

C Main Body:

C Assign initial values to COMMON variables

```

ISPCAL=1745
R1(1,1)=2.7293E-3
R1(2,1)=1.8282E-3
R1(3,1)=1.6844E-3
R1(4,1)=1.6320E-3
R1(1,2)=2.9568E-3
    
```

```

R1(2,2)=1.7384E-3
R1(3,2)=1.5260E-3
R1(4,2)=1.2800E-3
R1(1,3)=2.2395E-3
R1(2,3)=1.3714E-3
R1(3,3)=1.3090E-3
R1(4,3)=1.2854E-3
R2(1,1)=0.5078E-3
R2(2,1)=0.2137E-3
R2(3,1)=0.1198E-3
R2(4,1)=0.0940E-3
R2(1,2)=0.3792E-3
R2(2,2)=0.1732E-3
R2(3,2)=0.1216E-3
R2(4,2)=0.1600E-3
R2(1,3)=0.2180E-3
R2(2,3)=0.1794E-3
R2(3,3)=0.1331E-3
R2(4,3)=0.1195E-3
Q2(1,1)=-125.88
Q2(2,1)=-83.00
Q2(3,1)=-69.35
Q2(4,1)=-70.77
Q2(1,2)=-164.46
Q2(2,2)=-109.40
Q2(3,2)=-91.88
Q2(4,2)=-84.80
Q2(1,3)=-188.86
Q2(2,3)=-141.35
Q2(3,3)=-121.07
Q2(4,3)=-98.74
RK1=-.006884 ;-.050/(30bit/hr*0.2421A.hr/bit)
RK3=-2.16 ;-2mv/cell/des.C*(54cells/.050v/bit)
RK4=-10.33 ;2.5% of nominal 100A.Hr capacity
VEQ1=2.161 ;volts/cell
VEQ2=-5.16E-4 ;volts/cell/des.C
VEQ3=1.217E-3 ;volts/cell/A.hr
VEQ4=-7.42E-6 ;volts/cell/A.hr/des.C
BCFQ=0.2421 ;A.Hr/bit
BCFV=0.924E-3 ;volts/cell/bit
BCFTIM=2 ;minutes/bit

C
C
C If adjustment not specified, skip it
IF(IFCHG.LE.0) GOTO 900

C
C Convert and Scale "Inteser" data to "Real"
VBAT=IVBAT*BCFV
TBAT=ITBAT ;ides.C/bit
QBAT=IQBAT*BCFQ

C
C Calculate Equilibrium Voltage & Voltage Error
VERR=VBAT-VEQ(QBAT,TBAT)

C
C If Voltage Error <= 5mv/cell then skip correction
IF(ABS(VERR).LE.0.005) GOTO 900

C
C Correct A. hr meter

```

PAGE 003 INIFOR .SA:1

QBAT=QBAT+1.0*VERR/(VEQ3+VEQ4*TBAT)
IQBAT=QBAT/BCFQ

C

900 CONTINUE

C Return Control To Executive

RETURN

END

C RSTFOR Motorola-6809 ndh: 27-Sep-82
 C
 C Written by - Neil D. Herbert 26-Aug-82
 C Computer & Software Systems
 C Gould Electronics Laboratory
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472

C Modifications:
 C Added more COMMON as needed for DISFOR.
 C Neil D. Herbert 03-Sep-82 ndh-001
 C Made calculation of VEQ an external function.
 C Neil D. Herbert 08-Sep-82 ndh-002
 C Replaced some integer variables with real in COMMON.
 C Corrections from J. Mezera:
 C Added some constants to the COMMON.
 C Neil D. Herbert 13-Sep-82 ndh-010
 C Edited for Motorola-6809.
 C Neil D. Herbert 27-Sep-82 ndh-020

 Rest Monitor Ver 2.0

C Description:
 C After a 2-hour rest, the battery voltage and temperature
 C are used to determine the state of charge.
 C 1/2 the difference is then added to the Amp-hour meter.
 C
 C Inputs: Battery voltage & temperature.
 C
 C Outputs: Corrected Amp-hour meter value.
 C
 C Subprograms called: VEQ

SUBROUTINE RSTFOR

#H RSTFOR

C Arguments: (none)

C Standard Formats:

C Declarations:

ndh-010 begin

COMMON IFMODE, IMAKEF, IVLIN, IFINI
 COMMON IIBAT, IVBAT, ITBAT, ISPEED
 COMMON AMPSF, TEMPF, PWRP, SPDF
 COMMON IQBAT, IQBATX, IQLAST, IQABS
 COMMON IFRST, IFCHG, IFTHK
 COMMON IFEQU, IRESET, ISPCAL
 COMMON IDSOC, IDMILE, IDCTIM, IEQTIM, ICGTIM
 COMMON R1(4,3), R2(4,3), Q2(4,3)
 COMMON RK1, RK2, RK3, RK4

ndh-020

PAGE 002 RSTFOR SA:1

```
COMMON VEQ1, VEQ2, VEQ3, VEQ4
COMMON BCFQ, BCFV, BCFTIM
C
C ;ndh-010 end
C
C ;ndh-020
C
C Function Definitions:
C
C Main Body:
C
C Convert and Scale "Inteser" data to "Real"
  VBAT=IVBAT*BCFV ;ndh-010, 020
  TBAT=ITBAT ;ndh-010, 020
  QBAT=IQBAT*BCFQ ;ndh-010, 020
C
C Calculate Equilibrium Voltase & Voltase Error
  VERR=VBAT-VEQ(QBAT, TBAT) ;ndh-002
C
C If Voltase Error <= 5mv/cell then skip correction
  IF(ABS(VERR).LE.0.005) GOTO 900
C
C Correct A. hr meter
  QBAT=QBAT+0.5*VERR/(VEQ3+VEQ4*TBAT)
  IQBAT=QBAT/BCFQ ;ndh-010
C
900 CONTINUE
C Return Control To Executive
  IFRST=0 ; REST cycle completed ;ndh-010
  IFMODE=-1
  RETURN
  END
```

C CHGFOR Motorola-6809 ndh: 27-Sep-82
 C
 C Written by - Neil D. Herbert 26-Aug-82
 C Computer & Software Systems
 C Gould Electronics Laboratory
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472
 C

C Modifications:

C Changed sign of IQEAT to --out of battery.
 C Neil D. Herbert 27-Aug-82 ndh-001
 C

C Modified Charge Acceptance algorithm.
 C Neil D. Herbert 30-Aug-82 ndh-002
 C

C Added adjustment of IQLAST for temperature.
 C Assume none of the "over-charge" goes into the battery.
 C Neil D. Herbert 31-Aug-82 ndh-003
 C

C New Charge Correction.
 C Neil D. Herbert 31-Aug-82 ndh-004
 C

C Moved all correction code into charging loop
 C to keep State-Of-Charge indicator up to date.
 C Neil D. Herbert 02-Sep-82 ndh-005
 C

C Added more COMMON as needed for DISFOR.
 C Moved update of IQABS from DISFOR.
 C Neil D. Herbert 03-Sep-82 ndh-006
 C

C Changed function TEMPF to TEMPFN.
 C Replaced some interer variables with real in COMMON.
 C Corrections from J. Mezera.
 C Added some constants to the COMMON.
 C Neil D. Herbert 13-Sep-82 ndh-010
 C

C Edited for Motorola-6809.
 C Neil D. Herbert 27-Sep-82 ndh-020
 C

C *****
 C Charge Monitor Ver 2.0
 C *****

C Description:

C Sets charging parameters.
 C When charging done, sets battery Amp-hour meter value.
 C

C Inputs: Battery Amp-hour meter value.
 C Battery temperature.
 C

C Outputs: Battery voltage limit during charge.
 C New battery Amp-hour meter value.
 C

C Subprograms called: TEMPFN ndh-010
 C
 C

\$H CHGFOR

C

C Arguments: (none)

C

C Standard Formats:

C

C Declarations:

C

C

```

;ndh-010 begin
COMMON      IFMODE, IWAKEF, IVLIM, IFINI
COMMON      IIBAT, IVBAT, ITBAT, ISPEED
COMMON      AMPSE, TEMPF, PWRP, SPDF
COMMON      IQBAT, IQBATX, IQLAST, IQABS
COMMON      IFRST, IFCHG, IFTHK          ;ndh-020
COMMON      IFEQU, IRESET, ISPCAL
COMMON      IDSOC, IDMILE, IDCTIM, IEQTIM, ICCTIM
COMMON      R1(4,3), R2(4,3), Q2(4,3)
COMMON      RK1, RK2, RK3, RK4
COMMON      VEQ1, VEQ2, VEQ3, VEQ4
COMMON      BCFQ, BCFV, BCFTIM

```

C

```

;ndh-010 end

```

C

```

;ndh-020

```

C

C Function Definitions:

C

C Main Body:

C

```

IQBAT=IQBAT+IDCTIM*RK1 ;Adjust for self-discharge ;ndh-020
QDIS=IQLAST-IQBAT ;Total discharge ;ndh-001
IDCTIM=0 ;Reset Self-Discharge timer ;ndh-005

```

C

C

C Besin Charging loop *****

200

```

CONTINUE
IF(IFEQU.EQ.-1) GOTO 220 ;Equalize Requested?
IQEQU=0 ; NO.
RVREG=2646.0 ;2.45v/cell*54cells/.050v/bit ;ndh-010
GOTO 300

```

220

```

CONTINUE ; YES.
IQEQU=TEMPFN(ITBAT,74.3,49.6) ;12 to 18% ;ndh-005,010
RVREG=2916.0 ;2.70v/cell*54cells/.050v/bit ;ndh-010

```

C

300 CONTINUE

C Calculate Charge-IN Limits

```

IQQVC=QDIS*TEMPFN(ITBAT,0.12,0.08) ;ndh-010
IQNLIM=IQLAST+IQQVC ;ndh-005
IQLIM=IQNLIM+IQEQU ;ndh-005

```

C Calculate & SET Voltage Limit

```

IVLIM=RVREG+ITBAT*RK3 ;ndh-020

```

C

C (Possible location for THKFOR)

C

```

;ndh-005 begin

```

C

```

IQSOC=IQBAT ;Update State-Of-Charge

```

C

C Calculate Charge Acceptance Point at current Temperature

```

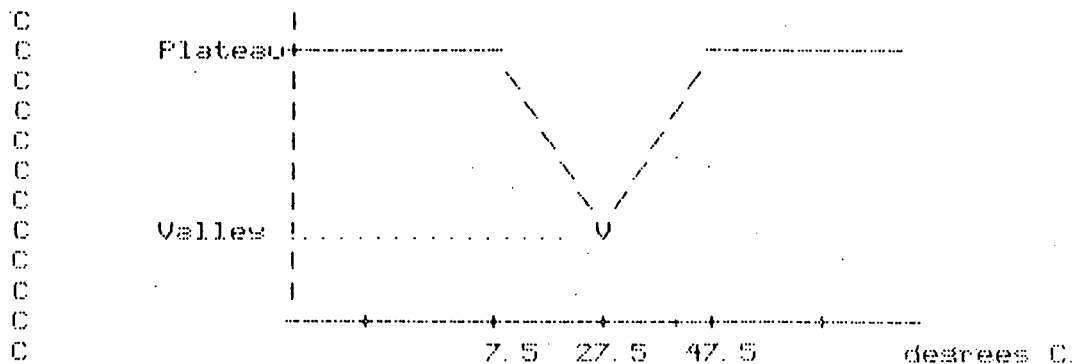
QACC=-TEMPFN(ITBAT,72.3,62.0) ;17.5-15.0% ;ndh-002,004,010,020

```

```

IQBAT=IQLAST*QACC/-62.0 ; Adjust for temperature ;ndh-003,020
C
IF(IQBAT.LE.QACC) GOTO 400 ; If no adj. needed ;ndh-001,002,004
C Calculate Amp-Hour Corrections ;ndh-004 begin
C
QCOR=(IQBAT-QACC)/(IQLIM-QACC)
IQB4=IQB4+QCOR*RK4 ;ndh-020
IF(IQB4.LT.QACC) IQB4=QACC ; Limit of IQLAST
C
C Correct Battery State-Of-Charge
IF(IQLIM.GT.IQNLIM .AND. IQBAT.GT.IQNLIM)
& IQB4=IQB4*(1.-(1.0*(IQBAT-IQNLIM)/(IQLIM-IQNLIM)) ;ndh-020
C ;ndh-005
IQSOC=IQB4-(IQB4-QACC)*(1.-QCOR)
C ;ndh-004 end
400 CONTINUE
IDSOC=10+(IQSOC-21)/41 ; Update State-Of-Charge Display
C ;ndh-005 end
IF(IQBAT.LT.IQLIM .AND. IFMODE.EQ.0) GOTO 200
C If not done charging and no mode change request,
C then repeat charging loop ^
C End charging loop =====
C
C
C IQLIM=0 ; Charger OFF
IF(IQBAT.GE.IQLIM) IFCHG=0 ; CHARGE completed ;ndh-010,020
C
IF(IFEQU.NE.-1 .OR. IQBAT.LT.IQLIM) GOTO 600 ; Equ. complete?
IQBAT=0 ; YES.
IQABS=0 ; Reset Absolute Amp-Hours
IEQTIM=0 ; Reset Equilibize Timer
IFEQU=0 ; Reset Equilibize Flag
IQLAST=0 ;ndh-004
IDSOC=10 ; Reset S-O-C Display ;ndh-005
GOTO 900 ;ndh-004
C
600 CONTINUE ; NO.
C Update total charge taken from battery since last equilization
IQABS=IQABS-QDIS+IQB4-IQSOC ;ndh-006
C Save battery state-of-charge normalized for temperature
IQLAST=IQB4*-62.0/QACC ;ndh-003,004,005,020
IQBAT=IQSOC
C
900 CONTINUE
C Grant Mode Change Request
IFMODE=-1
C
RETURN
END
C
C
C *****
C
C TEMPFN
C
C Description:
C Returns the value of a temperature dependant variable of the form:
C

```

Inputs: Temperature, Plateau, Valley of the function
 Outputs: Evaluated function of temperature between Plateau and Valley
 Subprograms called: (none)

FUNCTION TEMPFN(ITBAT, PLATOH, VALLEY) ;ndh-010

#H TEMPFN

Arguments: ITBAT = Temperature of battery (C.)
 PLATOH = Max value of function below 7.5 or above 47.5 degrees
 VALLEY = Minimum value of function at 27.5 degrees C.

Declarations:

Main Body:

FARG=ITBAT-27.5 ;ndh-020
 A2=VALLEY+(PLATOH-VALLEY)/20.*ABS(FARG) ;ndh-020
 AMIN1=PLATOH
 IF(A2.LT.AMIN1) AMIN1=A2
 TEMPFN=AMIN1 ;ndh-010
 RETURN
 END

C DISFOR Motorola-6809 ndh:27-Sep-82
 C
 C Written by - Neil D. Herbert 03-Sep-82
 C Computer & Software Systems
 C Gould Electronics Laboratory
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472
 C

C Modifications:

- C Replaced some interger variables with real in COMMON.
- C Corrections from J. Mezera.
- C Added some constants to the COMMON.
- C Neil D. Herbert 13-Sep-82 ndh-010
- C
- C Corrections from J. Mezera.
- C Neil D. Herbert 16-Sep-82 ndh-011
- C
- C Correction for VMIN from J. Mezera.
- C Neil D. Herbert 17-Sep-82 ndh-012
- C
- C J. Mezera changed IRESET flag and added IFCHG flag settings.
- C Neil D. Herbert 20-Sep-82 ndh-013
- C
- C Removed update of IQABS and test for IQBAT limit.
- C Added check for SQRT(neg. arg).
- C Neil D. Herbert 22-Sep-82 ndh-014
- C
- C Allowed pos. or neg. current by operator.
- C Removed unused argument Instantaneous Battery Current
- C from BATMOD.
- C Skip BATMOD for update of IDMILE
- C if filtered power > -30 watts.
- C Neil D. Herbert 23-Sep-82 ndh-015
- C
- C Edited for Motorola-6809.
- C Neil D. Herbert 27-Sep-82 ndh-020
- C
- C Added Calls to AVGFDR routine to filter variables
- C John R. Mezera 7-Oct-82 Jrm-022
- C
- C Modified Qmeas algorithm to speed up execution
- C by using a larger iteration step size and updating
- C from last calculated value.
- C John R. Mezera 28-Oct-82 Jrm-023
- C
- C Changed Qmeas algorithm to save best correction
- C last calculated. Also added settings of wake-up mode.
- C John R. Mezera 3-Nov-82 Jrm-024

C
 C *****
 C Discharge Monitor Ver 2.0
 C *****

C Description:

C Monitors discharging parameters & provides state of charge
 C and miles for display.

C Inputs: Battery Amp-hour meter value.
 C (Battery temperature, current, voltage, power.
 C Vehicle speed.

C Outputs: % State-Of-Charge and Miles left.

C Subprograms called: ZONE, VEQ, VDROF, BATMOD

SUBROUTINE DISFOR

\$H DISFOR

C Arguments: (none)

C Standard Formats:

C Declarations:

```

COMMON                                                           ;ndh-010 begin
COMMON                    IFMODE, IWAKEF, IVLIM, IFINI
COMMON                    IIBAT, IVEAT, ITBAT, ISPEED
COMMON                    AMPGF, TEMPF, PWRP, SPDF
COMMON                    IQBAT, IQBATX, IQLAST, IQABS
COMMON                    IFRST, IFCHG, IFTHK                   ;ndh-020
COMMON                    IFEQU, IRESET, ISPCAL
COMMON                    IDSOC, IDMILE, IDCTIM, IEQTIM, ICGTIM
COMMON                    R1(4,3), R2(4,3), Q2(4,3)
COMMON                    RK1, RK2, RK3, RK4
COMMON                    VEQ1, VEQ2, VEQ3, VEQ4
COMMON                    BCFQ, BCFV, BCFTIM

```

;ndh-010 end

;ndh-020

C Function Definitions:

C Main Body:

```

;nhd-010 begin
;ndh-010 end

```

C Adjust for Self-discharge

```

  IQBAT=IQBAT+IDCTIM*RK1                                           ;ndh-020
  IDCTIM=0

```

C Initialize variables

```

  THETA=0.0
  QMEAS=IQDAT*BCFQ
  QCOR=0.0

```

C Begin Discharging loop

```

200        CONTINUE
C Run Average Routine if needed
  CALL AVGFOR                                                       ;Jrm-022

```

C If charge removed >= 500 A. Hr or its been >= 7 days,

```

C then set equalize flag.
  IF((IQABS+IQBAT).LT. -2065 .OR. IEQTIM.GE. 5040)

```

```

&         IFEQU=-1 ;Time to Equalize?           ;ndh-010,014,020
C
C Set Wake-up mode for 2 hours if at least 4.8 A-hr have
C been removed since last charge cycle
         IF((IQLAST-IQBAT).GT.20) IWAKEF=2       ;Jrm-024
C
C Determine Battery State                       ;ndh-010 begin
CALL ZONE(AMPSF,TEMPF,R1E,R2E,Q2E)
TEMP=TEMPF
AMPS=AMPSF
TBAT=ITBAT
QBAT=IQBAT*BCFQ
ABAT=IIBAT*0.1
VBAT=IVBAT*BCFV
VPRED=VEQ(QBAT,TBAT)-VDROP(AMPS,R1E,R2E,Q2E,QBAT,ABAT) ;ndh-020
VDEL=VBAT-VPRED
C
C Error record update for use by "think" mode   ;ndh-010 end
C         RDEL=VDEL/AMPS                         ;ndh-010
C
C Predict Voltage Error & Compensate A. Hr value for battery model
         IF(AMPS.GE.-5.0) GOTO 600               ;ndh-015
         IF(VDEL.GT.-20.0E-3) GOTO 570          ;ndh-012,020,023
C Only correct QBAT if VDEL is more negative than -20mv ;ndh-012
         FARG=AMPS-ABAT
         GAMMA=2.0/ZRQQ1(1.0,Q2E,QBAT)+ABS(FARG)/5.0
         THELTA=0.7/(1.0+GAMMA)                 ;Jrm-024 begin
         IF(THELTA.LT.THELTA-.05) GO TO 560
         THELTA=THELTA                           ;Jrm-024 end
         VPRIME=VEQ(QMEAS,TBAT)-VDROP(AMPS,R1E,R2E,Q2E,QMEAS,ABAT)
         STEP=1.0                                ;ndh-011
         IF(VPRIME.GT.VBAT) STEP=-1.0
550      CONTINUE
         QMEAS=QMEAS+STEP*2.0                    ;ndh-020,023
         VPRIME=VEQ(QMEAS,TBAT)-VDROP(AMPS,R1E,R2E,Q2E,QMEAS,ABAT)
         IF((VPRIME-VBAT)*STEP.LE.0.0) GOTO 550
         QMEAS=QMEAS-STEP*2.0                    ;Jrm-023
         FARG=THELTA*(QMEAS-QBAT)
         IF(QCOR.LT.FARG) GO TO 555
         QCOR=FARG                               ;Jrm-024
555      CONTINUE
560      CONTINUE                               ;Jrm-024
570      CONTINUE
600      CONTINUE                               ;ndh-015
         QI=QBAT+QCOR                            ;Jrm-024
C
C Calculate State-Of-Charge at "Standard" Rate for Bar Display
         PWR=-185.2                              ;ndh-020
         VCUT=1.443                              ;ndh-020
C
C
         TIME=BATMOD(AMPS,TEMP,QI,PWR,VCUT)      ;ndh-010 begin
         TIME=TIME*9.25                          ;ndh-015
         TIME=TIME*9.25                          ;10*185w/cell/(200w.Hr/cell)
         IF(TIME.GT.10.0) TIME=10.0 ;max display range
         IDSOC=TIME+0.5                          ;round up integer
C
C Calculate State-Of-Charge at "Driving" Rate for Miles Display
         IF(PWR.GT.-30.0) GOTO 220               ;ndh-015
C If filtered power out of battery is less than 30 watts,

```

PAGE 004 DISFOR SA:1

```
C skip BATMOD ;ndh-015
  PWR=PWRF
C
  ;ndh-014 begin
  FARG=1.0+2.77E-3*PWR
  IF(FARG.LT.0.0) FARG=0
  VCUT=0.85*(1.0+SQRT(FARG))
C
  ;ndh-014 end
C
  5*1.70v/cell*(1+SQRT(1-4*.002v/cell/AMP/PWR/1.7**2))
C Run Average Routine if needed
  CALL AVGFOR ;jrm-022
C
  TIMEM=BATMOD(AMPS,TEMP,QI,PWR,VCUT) ;ndh-015
220 CONTINUE
  IDMILE=SPDF*TIMEM/ISPCAL+0.5 ;(pulses/hour)/(pulses/mile)
C
  ;ndh-010 end
C
  IF(IFMODE.EQ.0) GOTO 200
C If not done discharging, then repeat discharging loop ^
C End discharging loop
C
C
C Set Charge Flag if 10A-hr or more removed
  IF(QIQLAST-IQEAT.LT.-41)-IFCHG=-1 ;ndh-013
C
C Grant Mode Charge Request
  IFMODE=-1
C
  RETURN
  END
```

PAGE 001 THKFOR .SA:1

C THKFOR Motorola-6809
C
C Written by - John R Mezera 5-Nov-82
C Gould Electronics Laboratory
C Gould, Inc., Rollins Meadows, Ill.

C Modifications:

C *****
C Think Monitor Ver 1.0
C *****

C Description:

C Inputs:

C Outputs:

C Subprograms called:

C SUBROUTINE THKFOR

\$H THKFOR

C Arguments. (none)

C Standard Formats:

C Declarations:

COMMON IFMODE, IWAKEF, IVLIM, IFINI
COMMON IIBAT, IUBAT, ITBAT, ISPEED
COMMON AMPSE, TEMPF, PWRP, SPDF
COMMON IQBAT, IQBATX, IQLAST, IQABS
COMMON IFRST, IFCNG, IFTHK
COMMON TTTQU, IRESET, ISPCAL
COMMON IDSOC, IDMLE, IDCTIM, IERTIM, ICGTIM
COMMON R1(4,3), R2(4,3), Q2(4,3)
COMMON RK1, RK2, RK3, RK4
COMMON VEQ1, VEQ2, VEQ3, VEQ4
COMMON BCFO, BCFV, BCFTTM

C Function Definitions:

C Main Body:

C Return Control To Executive

IFTHK=0 ;THINK cycle completed
IFMODE=-1
RETURN
END

C BATMOD Motorola-6809 ndh:27-sep-82
C
C Written by - Neil D. Herbert 09-Sep-82
C GLEER Computer & Software Systems
C Gould, Inc., Rollins Meadows, Ill.
C 312/640-4472

C Modifications:

C Changed inteser arguments to real.
C Changed from Subroutine to Function.
C Corrections from J. Mezera.
C Neil D. Herbert 13-Sep-82 ndh-010

C Corrections from J. Mezera.
C Neil D. Herbert 16-Sep-82 ndh-011

C Change from J. Mezera which by-passes ZONE to speed up
C algrithm if current hasn't changed by more than 1AMP.
C Neil D. Herbert 17-Sep-82 ndh-012

C Changed test for skip ZONE to avoid divide-by-zero error.
C Neil D. Herbert 22-Sep-82 ndh-013

C Removed argument Instantaneous Battery Current ABAT0.
C Added Return if time to Cutoff Volatse exceeds 12 hours.
C Neil D. Herbert 23-Sep-82 ndh-014

C Edited for Motorola-6809.
C Neil D. Herbert 27-Sep-82 ndh-020

C Added two step simulation rate depending upon discharge rate
C or when simulation nears knee of voltage profile. This decreased
C exection time with minimal desrasation in simulation accuracy.
C John R. Mezera 7-Oct-82 Jrm-021

C *****
C Battery Model Ver 2.0
C *****

C Description:

C Models the battery in increments of time
C using the input parameters as a starting point,
C and iteratively removes energy at constant power
C until the cutoff voltage is reached.

C Inputs: Battery current, temperature, state, power,
C & cutoff voltage ; ndh-010 begin

C Outputs: Hours to cutoff voltage

C Subprograms called: ZONE, VEQ, VDROF

C FUNCTION BATMOD(AMPS0, TEMP0, QI, PWR, VCUT)

4H BATMOD

C Arguments: ; ndh-014

```

C          AMPS0          = Battery Current filtered over 6 min.
C          TEMP0          = Battery Temperature filtered over 6 min.
C          QI             = Modified State of charge
C          FWR            = Power Rate filtered over 30 sec.
C          VCUT           = Cutoff Voltage
C
C Standard Formats:
C
C Declarations:
C
C                                     ;ndh-020
C
C Main Body:
C
C          AMPS=AMPS0
C          ABAT=AMPS0          ;ndh-014
C          Q=QI
C          TIME=0. 0
C
C Beginning of Iteration Loop  ++++++
200  CONTINUE
C Predict Battery Voltage
C          CALL ZONE(AMPS,TEMP0,R1E,R2E,Q2E)          ;ndh-011
C          AMPZ=AMPS          ;last current used in ZONE ;ndh-012
C
C Inner loop to skip ZONE  ++++++
300  CONTINUE          ;ndh-012
C          VPRED=VEQ(Q,TEMP0)-VDROP(AMPS,R1E,R2E,Q2E,Q,ABAT) ;ndh-011
C
C          BATMOD=TIME
C          IF(VPRED.LE.VCUT) RETURN          ;ndh-014, jrm-021
C          IF(TIME.GT.12.0) RETURN          ;jrm-021
C
C Re-Compute Battery Current
C          ABAT=PWR/VPRED
C
C Two step simulation
C          Fast rate if discharge rate low (<75watts/cell)
C          Slow rate at knee of characteristic (within 80% of Q2E)
C
C          IF(PWR.GT.-75.0) GO TO 400          ;jrm-021
C          IF(Q.GT.Q2E*0.80) GO TO 400          ;jrm-021
C          Slow Rate: 18 sec simulation
C          AMPS=AMPS*0.952+ABAT*0.048 ;A/(1+t/T)+a/(1+T/t) ;ndh 020
C          Increment Time
C          Q=Q+ABAT*.005 ;model hours "t"          ;ndh-020
C          TIME=TIME+.005 ;t          ;ndh-020
C          GO TO 500
C          Fast Rate: 4 min simulation
400  CONTINUE
C          AMPS=AMPS*0.600+ABAT*0.400 ;A/(1+t/T)+a/(1+T/t) ;jrm-021
C          Increment Time
C          Q=Q+ABAT*.0667 ;model hours "t"          ;jrm-021
C          TIME=TIME+.0667 ;t          ;jrm-021
500  CONTINUE
C
C          FARG=AMPS-AMPZ          ;ndh-020

```


PAGE 003 BATMOD .SA:1

```
      IF(ABS(FARG).LT.1.0) GOTO 300      ;ndh-012,013,014,020
C If current hasn't changed by more than 1Ame,
C then skip ZONE ;ndh-012,013
C
      GOTO 200
C End of Iteration Loop *****
C
C
      END
```

```

SUBROUTINE AVGFOR
*
*H      AVGFOR
COMMON IFMODE, IWAKEF, IULIM, IFINT
COMMON IIBAT, IVBAT, ITBAT, ISPEED
COMMON AMPSF, TEMPF, PWRF, SPDF      ; REAL DATA TYPE
COMMON IQBAT, IQBATX, IQLAST, IQABS
COMMON IFRST, IFCHG, ITHK
COMMON IFEQU, IRESET, ISPCAL
COMMON IDSOC, IDMILE, IDCTIM, IEQTIM, ICHTIM
*
* TEST FOR INITIALIZATION
*
      IF (IFINT.GE.0) GO TO 100
      TEMPF=ITBAT      ; INITIALIZE TO REAL VALUE
      IFINT=0         ; RESET REQUEST FLAG
100    CONTINUE
*
* CHECK FOR FILTER DELAY
*
      IF (IFINT.LT.75) GO TO 200      ; DELAY 10 SEC
      IFINT=0
*
* AVERAGE CURRENT AND TEMPERATURE OVER A BATTERY TIME CONSTANT (6 MIN.)
*
      AMPSF=(0.973*AMPSF)+(0.0027*IIBAT) ; SCALE & AVERAGE TO AMPS (0.1A/BIT)
      TEMPF=(0.973*TEMPF)+(0.027*ITBAT) ; AVERAGE TO DEGREES (1 C/BIT)
*
* AVERAGE POWER AND SPEED OVER 30 SEC. TIME INTERVAL
*
      PWRF=(.750*PWRF)+(2.315E-5*IIBAT*IVBAT); SCALE & AVERAGE TO WATTS/CELL
      ; (0.1A/BIT*926E-3V/CELL/BIT)
*
      SPDF=(.750*SPDF)+(50.0*ISPEED)      ; SCALE & AVERAGE TO PULSES/HOUR
      ; (PULSES / 6 SEC.)
*
200    CONTINUE
      RETURN

```

C VDROF Motorola-6809 ndh:27-Sep-82
C
C Written by - Neil D. Herbert 08-Sep-82
C GLEER Computer & Software Systems
C Gould, Inc., Rollins Meadows, Ill.
C 312/640-4472
C

C Modifications:
C Corrections from J. Mezera.
C Neil D. Herbert 13-Sep-82 ndh-010
C Correction in value of R0 from J. Mezera
C Neil D. Herbert 16-Sep-82 ndh-011
C
C Edited for Motorola-6809.
C Neil D. Herbert 27-Sep-82 ndh-020
C

C Voltage Drop Ver 2.0
C *****

C Description:
C Calculates voltage drop for given internal resistance,
C state of charge, and current values.
C
C Inputs: Internal battery resistance, charge, and current.
C
C Outputs: Calculated Voltage drop.
C
C Subprograms called: ZRQQ1
C
C

FUNCTION VDROF(AMPS, R1, R2, Q2, Q, ABAT)

\$H VDROF
C
C Arguments: AMPS = Filtered Current
C R1 = Internal resistance "R1"
C R2 = Internal resistance "R2"
C Q2 = Battery capacity
C Q = Battery state of charge
C ABAT = Instantaneous Current
C

C Declarations:
C
C ; ndh-020
C

C Main Body:
C
C VDROF=(0.75E-3-R1-ZRQQ1(R2, Q2, Q))*AMPS-0.75E-3*ABAT ; ndh-010, 020
C RETURN
C END

C ZONE Motorola-6809 ndh:27-Sep-82

C Written by -- Neil D. Herbert 08-Sep-82

C GLEER Computer & Software Systems
C Gould, Inc., Rollins Meadows, Ill.
C 312/640-4472

C Modifications:

C Replaced some integer variables with real in COMMON.
C Corrections from J. Mezera.
C Added some constants to the COMMON.

C Neil D. Herbert 13-Sep-82 ndh-010

C Edited for Motorola-6809.

C Neil D. Herbert 27-Sep-82 ndh-020

C *****
C Zone Interpolation in 2-D Ver 2.0

C *****

C Description:

C Controls the table search and interpolation for R1, R2, & Q2
C as functions of current and temperature.

C Inputs: Battery current and temperature.

C Outputs: Interpolated values for R1, R2, & Q2.

C Subprograms called: FDELTA, EVAL2D

C SUBROUTINE ZONE(AMPS, TEM, R1E, R2E, Q2E)

\$\$\$ ZONE

C Arguments: AMPS = Battery current ; ndh-010

C TEMP = Battery temperature ; ndh-010

C R1E = Interpolated value of R1

C R2E = Interpolated value of R2

C Q2E = Interpolated value of Q2

C Standard Formats:

C Declarations:

C ; ndh-010 begin

COMMON IFMODE, IWAREF, IULIM, IFINI

COMMON IIBAT, IVEAT, ITEAT, ISPEED

COMMON AMPSF, TEMPF, FWRP, SPDF

COMMON IQBAT, IQBATX, IQLAST, IQABS

COMMON IFRST, IFCHG, IFTHK ; ndh-020

COMMON IFEQU, IRESET, ISPCAL

COMMON IDSOC, IDMILE, IDCTIM, IEQTIM, ICGTIM

COMMON R1(4,3), R2(4,3), Q2(4,3)

COMMON RK1, RK2, RK3, RK4

COMMON VEQ1, VEQ2, VEQ3, VEQ4

COMMON BCFQ, BCFV, BCFTIM

PAGE 002 ZONE SA: 1

```
C
C
C          DIMENSION          LISTA(4),LISTT(3)
C          DIMENSION          FRACT(2,2)
C
C
C          ;ndh-010 end
C
C          ;ndh-020 basin
C          ;ndh-010 basin
C
C          LISTA(1)=-20
C          LISTA(2)=-80
C          LISTA(3)=-130
C          LISTA(4)=-200
C
C          ;ndh-010 end
C
C          LISTT(1)=9
C          LISTT(2)=20
C          LISTT(3)=40
C
C          ;ndh-020 end
C
C Main Body:
C          IAMPS=AMPS          ;ndh-010
C          ITEMP=TEMP         ;ndh-010
C
C Determine where we are in the table
C          J=1
C          DO 120 I=2,3
C              IF(IAMPS.LE.LISTA(I)) J=I
120          CONTINUE          ;ndh-020
C          K=1
C          DO 140 I=2,2
C              IF(ITEMP.GE.LISTT(I)) K=I
140          CONTINUE
C
C Interpolate Values within table
C          ADEL=FDELTA(IAMPS,LISTA(J),LISTA(J+1))
C          TDEL=FDELTA(ITEMP,LISTT(K),LISTT(K+1))
C          FRACT(1,1)=(1-ADEL)*(1-TDEL)
C          FRACT(1,2)=(1-ADEL)*TDEL
C          FRACT(2,1)=ADEL*(1-TDEL)
C          FRACT(2,2)=ADEL*TDEL
C          R1E=EVAL2D(FRACT,R1,J,K)
C          R2E=EVAL2D(FRACT,R2,J,K)
C          Q2E=EVAL2D(FRACT,Q2,J,K)
C          RETURN
C          END
```

C VEQ Motorola-6809 ndh: 27-Sep-82

C
 C Written by - Neil D. Herbert 08-Sep-82
 C GLEER Computer & Software Systems
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472

C Modifications:

C Replaced some inteser variables with real in COMMON.
 C Added some constants to the COMMON.
 C Neil D. Herbert 13-Sep-82 ndh-010
 C Edited for Motorola-6809.
 C Neil D. Herbert 27-Sep-82 ndh-020

C *****
 C Equilibrium Voltage Ver 2.0
 C *****

C Description:

C Calculates equilibrium voltase based on
 C state of charge and temperature.

C Inputs: Battery state of charge and temperature.

C Outputs: Expected equilibrium voltase of battery.

C Subprograms called: (none)

C FUNCTION VEQ(QBAT,TEAT)

##H VEQ

C Arguments: QBAT = Battery state of charge
 C TEAT = Battery temperature

C Declarations:

C ; ndh-010 begin
 COMMON IFMODE, IMAKEF, IVLIM, IFINI
 COMMON IIBAT, IVBAT, ITBAT, ISPEED
 COMMON AMPSF, TEMPF, PWRP, SPDF
 COMMON IQBAT, IQBATX, IQLAST, IQAES
 COMMON IFRST, IFCHG, IFTHK ; ndh-020
 COMMON IFEQU, IRESET, ISPCAL
 COMMON IDSOC, IDMILE, IDCTIM, IERTIM, ICGTIM
 COMMON R1(4,3), R2(4,3), Q2(4,3)
 COMMON RK1, RK2, RK3, RK4
 COMMON VEQ1, VEQ2, VEQ3, VEQ4
 COMMON BCFQ, BCFV, BCFTIM

C ; ndh-010 end

C Main Body:

C VEQ=(VEQ1+VEQ2*TEAT)+(VEQ3+VEQ4*TEAT)*QBAT

PAGE 002 VEQ SA:1

RETURN
END

C FDELTA Motorola-6809 ndh: 27-Sep-82
 C
 C Written by - Neil D. Herbert 08-Sep-82
 C GLEER Computer & Software Systems
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472
 C

C Modifications:
 C Corrections from J. Mezera.
 C Neil D. Herbertex-82 ndh-010
 C
 C Edited for Motorola-6809.
 C Neil D. Herbertex-82 ndh-020
 C

C *****
 C FDELTA value between list points Ver 2.0
 C *****
 C

C Description:
 C Calculate the fraction of distance that the given value is
 C from the given point in the list to the next point.
 C

C Inputs: Value used in search, the list to search,
 C & the list index.
 C

C Outputs: The fraction of the distance from T(i) to T(i+1).
 C

C Subprograms called: (none)
 C
 C
 C

FUNCTION FDELTA(IPARAM,L1,L2)

\$H FDELTA

C Arguments: IPARAM = Value used in search
 C L1 = Lower array element of list
 C L2 = Upper array element of list
 C
 C

C Declarations:
 C
 C
 C

C Main Body:
 C

FDELTA=(1.0*IPARAM-L1)/(L2-L1)
 .RETURN
 END

C EVAL2D Motorola-6809 ndh:27-Sep-82

C
 C Written by - Neil D. Herbert 08-Sep-82
 C GLEER Computer & Software Systems
 C Gould, Inc., Rollins Meadows, Ill.
 C 312/640-4472
 C

C Modifications:

C Edited for Motorola-6809.
 C Neil D. Herbert 27-Sep-82 ndh-020

C
 C *****
 C Evaluate parameter of 2 dimensional table Ver 2.0
 C *****
 C

C Description:

C Using the indexes and fractions for each of the
 C two dimensions of the batters parameter table given,
 C interpolate the actual value from the 2-dimensional array.

C Inputs: Table array of fractions, Parameter array, & Indexes.

C Outputs: Interpolated value from 2-dimensional array.

C Subprograms called: (none)

C FUNCTION EVAL2D(FRACT,PARAM,J,K)

##H EVAL2D

C Arguments: FRACT = 2x2 array of fractions
 C PARAM = 2-D array of parameter to be interpolated
 C J = Index for 1st dimension
 C K = Index for 2nd dimension

C Declarations:

C DIMENSION FRACT(2,2),PARAM(4,3) ;ndh-020

C Main Body.

C EVAL2D=FRAC(1,1)*PARAM(J,K)
 & +FRAC(1,2)*PARAM(J,K+1)
 & +FRAC(2,1)*PARAM(J+1,K)
 & +FRAC(2,2)*PARAM(J+1,K+1)
 C RETURN
 C END

PAGE 001 ZRQQ1 SA:1

C ZRQQ1 Motorola-6809 ndh:27-Sep-82

C
C Written by - Neil D. Herbert 09-Sep-82
C GLEER Computer & Software Systems
C Gould, Inc., Rolling Meadows, Ill.
C 312/640-4472
C

C Modifications:
C Corrections from J. Mezera.
C Neil D. Herbert 13-Sep-82 ndh-010
C
C Edited for Motorola-6809.
C Neil D. Herbert 27-Sep-82 ndh-020
C

C *****
C Impedance Calculation Ver 2.0
C *****

C Description:
C Calculates battery impedance from internal resistance,
C capacity, & state of charge.

C Inputs: Battery internal resistance, capacity,
C & state of charge.

C Outputs: Battery impedance.

C Subprograms called: (none)

C FUNCTION ZRQQ1(R2,Q2,Q)

#H ZRQQ1

C Arguments: R2 = Internal resistance
C Q2 = Battery capacity
C Q = State of charge

C Declarations:

C Main Body:

C Q1=Q
C IF(0.999*Q2.GT.Q1) Q1=0.999*Q2 ;limit denominator ;ndh-010
C ZRQQ1=R2*Q2/(Q2-Q1)
C RETURN
C END