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BCB Evaluation of High-Performance and Low-Leakage Three-Independent-Gate Field-Effect Transistors

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ABSTRACT Three-independent-gate field-effect transistors (TIGFETs) are a promising next-generation device technology. Their controllable-polarity capability allows for superior design of arithmetic and sequential logic gates. In this paper, the TIGFET technology has been benchmarked against several beyond-CMOS devices. The benchmarking techniques followed a similar approach used by the Nanoelectronic Research Initiative Group. The performance of the 32-bit adder and the 32-bit arithmetic logic unit (ALU) was investigated using the advanced 15-nm technology node. The TIGFET devices were shown to achieve the best energy-delay product (EDP) compared with all other beyond-CMOS devices for the 32-bit adder and competitive EDP for the 32-bit ALU. In particular, TIGFETs have 3.83 times and 1.54 times lower EDP than CMOS high-performance (HP) for the 32-bit adder and the 32-bit ALU, respectively. In addition, TIGFETs were shown to have a similar throughput for the 32-bit ALU compared with CMOS HP. Finally, due to TIGFETs' ultralow leakage current and unique circuit designs, our results show that the standby energy of the 32-bit adder decreased by two orders of magnitude compared with CMOS HP and a decrease of at least one order of magnitude compared with CMOS low-voltage.

INDEX TERMS Arithmetic logic gate, beyond-CMOS, gate-all-around, silicon nanowire field-effect transistor (SiNWFET), three-independent-gate.

I. INTRODUCTION

The semiconductor industry has thrived in scaling CMOS field-effect transistors (FETs) into the nanometer regime. As this era advances, problems with dimensional scalability arise as fundamental physical limits are reached [1]. High-mobility channel materials, high-κ dielectrics, and nonplanar structures, such as fins and nanowires, are being used to increase the performance of the current CMOS technology [2], [3]. These advances have their own issues and device scaling limits still apply. Therefore, research for beyond-CMOS devices that allow performance enhancement in advanced technology nodes becomes crucial. Some promising alternatives, outlined in [7]–[9], have compelling results. Magnetoelectric spintronic devices, such as the spin wave device (SWD) [4] and the spin majority gate (SMG) [5], and tunneling devices, such as the gallium nitride FET (GaNFET) and the graphene nanoribbon FET (gnrTFET), can lead to less switching energy than CMOS high-performance (HP). However, the switching speed for these devices is generally slower than CMOS HP. The only device projected to switch faster with less switching energy is the van der Walls FET (vdWFET) [6] device.

In order to compare performances, the Nanoelectronic Research Initiative Group launched an investigation as a valuable effort to benchmark beyond-CMOS devices. The comparisons were outlined in beyond-CMOS benchmarking (BCB) versions 1.0 through 3.0 [7]–[9]. The first benchmarking (BCB 1.0 [7]) evaluated several devices with a partial set of common guidelines, while the second release (BCB 2.0 [8]) proposed a uniform method for estimating area, switching delay, and energy of various arithmetic logic circuits. The third and most recent release (BCB 3.0 [9]) improves the methodology by including standby power and sequential logic circuits. All three BCB versions cover devices from various genres, such as electronic, ferroelectric, straintronic, orbitronic, and spintronic.

At advanced technology nodes, emerging devices, such as multiple-independent-gate FETs, are promising technologies that utilize the addition of multiple gate terminals on a semiconducting channel to increase the functionality of the device [10]–[13]. Notably, the three-independent-gate FET (TIGFET) technology [12] introduces three MOS gate terminals between source and drain. This technology delivers several crucial functionalities that make it a competitive beyond-CMOS exploratory technology. In particular, the multigate design and the Schottky-barrier source and drain terminals enable dynamic reconfiguration of the polarity (*n*-type or *p*-type) [11], dynamic control of the threshold voltage (V_T) [12], and dynamic control of the subthreshold slope [13]. The dynamic control of the electrostatic properties of TIGFETs also allows for nondoping fabrication procedures. Since the materials and processes used to fabricate TIGFET transistors and standard CMOS transistors are similar, the lesser reliance on process steps makes for a more robust TIGFET transistor design [19]. TIGFET devices have been successfully demonstrated with a variety of channel materials and geometries. Particularly, nonplanar silicon geometries [11], [12] offer better electrostatic control, reduced short channel effects, and simplicity of fabrication. Silicon nanowire FETs (SiNWFETs) [10], in particular, are also a great choice as its gate-all-around (GAA) electrodes enable the best geometry for an excellent electrostatic control and have a favorable increase of I_{ON}/I_{OFF}. TIG SiNWFET devices have been demonstrated with a single nanowire [10] and multiple nanowires [11], [12].

In this paper, we evaluated the potential of the TIGFET technology following BCB 3.0 [9]'s methodology, whose best combinational and sequential circuit benchmark consists of a 32-bit adder and a 32-bit arithmetic logic unit (ALU). The adder utilizes the standard ripple-carry configuration while the ALU computes the addition, subtraction, NAND, and NOR of two 32-bit numbers. Basic logic functions were first mapped onto regular layouts to get area estimates. Critical device parameters, including ON-current, OFF-current, and nominal voltage, were extracted through TCAD simulations of a TIG SiNWFET. The parasitic capacitances for the device-dependent adjustment factor were extracted using COMSOL Multiphysics. Finally, equations were developed which approximated the switching delay, switching energy, and standby power of such logic functions. We provide the BCB methodology, with the added TIGFET architecture, online at [15]. Our results show that TIG SiNWFET devices are capable of achieving the best energy-delay product (EDP) out of all beyond-CMOS devices for the 32-bit adder and competitive EDP for the 32-bit ALU. In particular, following the performance metric of the 32-bit adder, TIG SiNWFETs have 3.83 times lower EDP, 2.05 times lower total area, and 147 times lower standby energy compared with CMOS HP. The performance metric of the 32-bit ALU shows that TIG SiNWFETs have 1.54 times lower EDP and 1.43% higher throughput compared with CMOS HP while maintaining a similar total area.

The remainder of this paper is organized as follows. Section II discusses background material of the TIGFET technology. The layout considerations are shown in Section III. Delay, energy, and standby power equations are outlined in Section IV. The results are shown and discussed in Section V, and this paper is concluded in Section VI.

II. BACKGROUND

In this section, we briefly review the structure, working principle, and circuit level implementations of TIGFET transistors.

A. GENERALITIES

TIGFET devices utilize additional independent gate terminals in order to provide unconventional control of the device electrostatic properties [12]. As illustrated in Fig. 1, a typical TIGFET device has three MOS gate contacts. The control gate (CG), in the inner region, regulates the channel conduction, whereas the polarity gate at source (PGS) and the polarity gate at drain (PGD) modulate the Schottky barrier to, respectively, allow electrons or holes to flow into the channel.

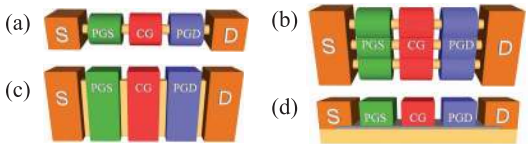

FIGURE 1. Sketches of different TIGFET topologies. (a) Single NW. (b) Stacked NWs. (c) Fin. (d) 2-D horizontal layer.

This technology has been demonstrated in the literature with multiple channel geometries and materials, such as silicon nanowire structures [10], [12], silicon fin structures [13], 2-D materials [14], [16], [17], and carbon nanotubes [18]. In addition, performance at aggressive scaling nodes was estimated using ballistic self-consistent quantum simulations [17] on 2-D materials from the transition-metal-dichalcogenide family and showed possibilities for TIGFETs to achieve high-current densities. Fully exploiting a doping-free process, TIGFETs also bear the promise of improved robustness to process variations as identified in [19]. Vertically stacked nanowires [20]–[22] are the natural extension of single nanowire channels as their increased drive current leads to reduced circuit delays. The results based in [23] have shown advantageous delay marks up to five stacked nanowires. However, to keep this paper focused and to rely on more accurate evaluations, the TIGFET technology has been evaluated under a single SiNW structure.

B. WORKING PRINCIPLE

All TIGFET devices operate along the same set of principles. Schottky barriers are created at the source/drain contacts. The potential of PGS and PGD may modulate the thickness of the Schottky barriers and allow for different types of carriers to flow. The barrier at the source side allows electrons to enter the channel, whereas the drain side allows holes to enter the channel. The CG is used to regulate the current by modulating a potential barrier in the center of the channel. The bias gate

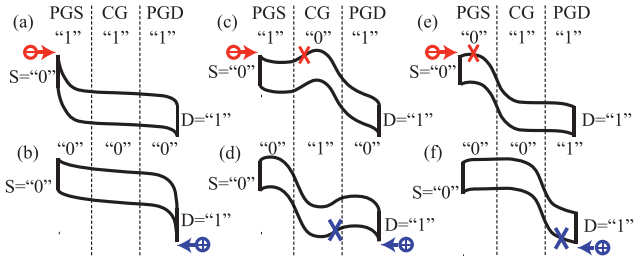

FIGURE 2. Band diagrams under different bias conditions. (a) and (b) ON-state. (c) and (d) OFF-state. (e) and (f) Low-leakage OFF-state.

conditions [G_{ND} ("0") or V_{DD} ("1")] used in this paper are illustrated by the band diagrams in Fig. 2.

1) ON STATES

As shown in Fig. 2(a) and (b), if CG = PGS = PGD, at least one of the Schottky barriers allows carriers to flow. If all are set "1," electrons flow from the source side. If all are set "0," holes flow from the drain side.

2) OFF STATES

If CG ≠ PGS and CG ≠ PGD, as shown in Fig. 2(c) and (d), then the barrier in the center of the channel will not allow carriers to flow.

3) LOW-LEAKAGE OFF STATES

If PGS = S and PGD = D, as shown in Fig. 2(e) and (f), then thick Schottky barriers at the source and drain sides are formed and prevent carriers to flow into the channel. Turning OFF the barrier injection provides a lower leakage floor compared with the traditional OFF-state.

The logic behavior of TIGFET transistors is summarized in Fig. 3. If PGD is set low, the TIGFET transistor is equivalent to two *p*-type transistors in series with CG and PGS at gates. On the other hand, if PGS is set high, the TIGFET transistor behaves as two *n*-type transistors in series with CG and PGD at gates. Finally, if both PGs are set high, the device represents an *n*-type transistor with CG as gate and if both PGs are set low, the device represents a *p*-type transistor with CG as gate. For more details, we refer the reader to [26].

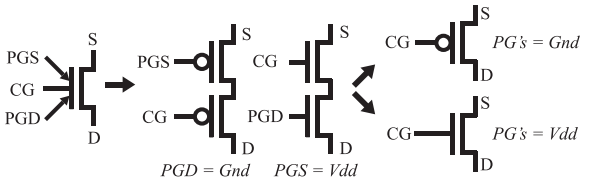

FIGURE 3. Bias configurations for TIGFET transistor. Symbol representation followed by series pFET and series nFET followed by unipolar pFET and unipolar nFET configurations.

C. CIRCUIT LEVEL OPPORTUNITIES

The benefits of TIGFETs have been largely investigated in the literature [24], [29]. Circuits can be implemented with TIGFETs by emulating unipolar transistors. Fig. 4(a) shows the schematic of a standard CMOS-style fan-out-of-1 inverter [26]. The top and bottom transistors are set as *p*-type and *n*-type by tying their polarity gates to G_{ND} and V_{DD}, respectively. While this allows a full design style compatibility with the CMOS technology, the capabilities of TIGFETs can be leveraged to create more efficient circuits. In particular, TIGFETs can emulate two series transistors as discussed earlier. As a result, it is possible to design several compact logic gates, such as a two-input NAND with three transistors [26] [Fig. 4(b)], or a two-level 4-to-1 static multiplexer [Fig. 4(c)]. TIGFET technology's rich set of operations also allow the core circuit of the exclusive OR (XOR) and the majority (MAJ) gates to be compacted within four transistors. As illustrated in Fig. 4(d), by adjusting the top (Y) and bottom (X) terminals, the realization of a two-input XOR [24], a three-input XOR [27], and a three-input MAJ [27] is possible with an identical structure. We refer the reader to [25] and [28] for further circuit opportunities, such as 6T static random-access memory (SRAM), true single-phase clocking (TSPC) flip-flop, multiplexers, and embedded power gating.

III. LAYOUT CONSIDERATION

In this section, we evaluate the area of TIGFET circuits according to BCB's design rules [9].

A. SINGLE TRANSISTOR

The layout of a single TIGFET transistor is shown in Fig. 5(a). In this paper, we follow the same standard design rules than [8]. The feature size, designated as the DRAMs half-pitch, F, was chosen to be 15 nm following the technology node in BCB 3.0 [9]. Using a maximum mask misalignment, $\lambda = (1/2)F$, the pitch (P) and width (W) of the TIGFET transistor were designed to be $8F$ and $4F$, respectively. This single transistor will be considered as the intrinsic component of the TIGFET technology from this point forward.

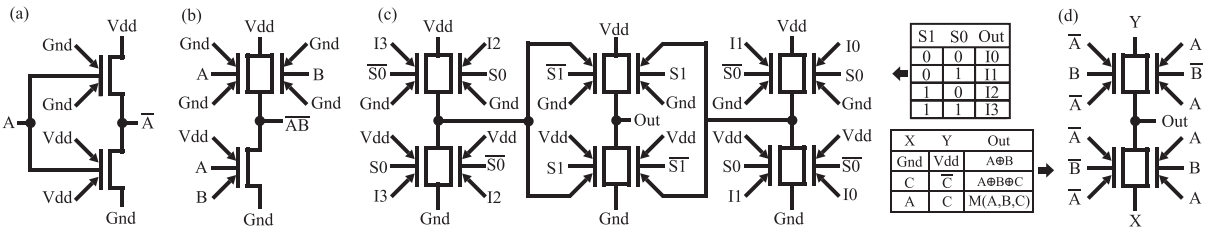

FIGURE 4. TIGFET circuit representations of (a) fan-out-of-1 inverter, (b) two-input NAND gate, (c) two-level 4-to-1 static multiplexer, and (d) two-input XOR gate, a three-input XOR gate, and a three-input MAJ gate with corresponding *X* and *Y* values to map the functions.

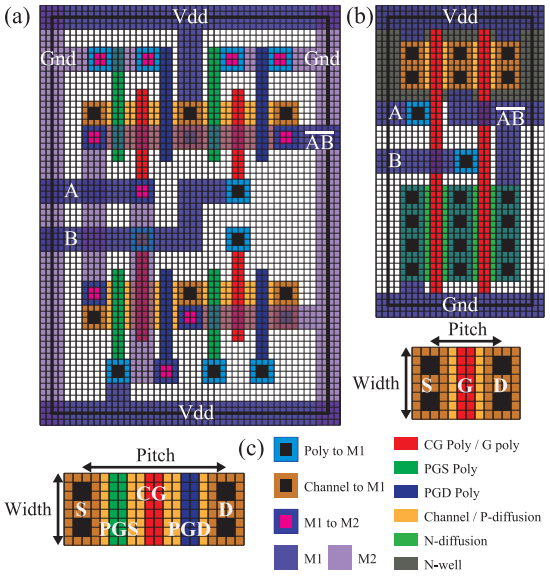

FIGURE 5. Layout view of the two-input NAND and intrinsic transistor with (a) TIGFET architecture and (b) CMOS architecture. (c) Key with designated contact and material naming.

B. PHYSICAL DESIGN CONSIDERATIONS

The multigate geometry of TIGFET devices brings more complex routing as two additional gates are required for every transistor with respect to the CMOS technology. In order to mitigate this problem, we use a regular layout tile, as shown in Fig. 5(a), that was introduced as a building block for TIGFET designs [23]. The tiles are composed of two pairs of TIGFET transistors with common S/D gates surrounded by a grid of power rails. The resulting track height is 38% larger than CMOS's two-input NAND gate with a 20% increase in usable metallic tracks. The resulting tile geometry allows for eight total metal tracks (compared with six in CMOS) and one additional metal (M2) to route signals and provides less problematic routing congestions [30] for a large range of circuits [31]. As a result, the use of this layout topology allows us to mitigate any additional routing congestions coming from the multigate geometry and achieve similar routing efficiency as the CMOS technology [30]. In addition, the uniformity of the architecture allows for homogeneous front-end production which is fundamental to achieve a high yield at advanced technology nodes. That said, the area of the TIGFET tile (A_T) as shown in Fig. 5(a) is calculated to be

$$A_T = (2P + 7F) \cdot (2W + 25F). \tag{1}$$

C. BASIC LOGIC GATES

The area of a single four-transistor tile is used as a reference to determine the areas of the various logic functions examined in BCB 3.0 [9]. Area of an inverter, A_{invFO} [Fig. 4(a)] with fan-out (FO) and of a two-input NAND, A_{NAND2}, [Fig. 4(b)] are determined to be

$$A_{\text{invFO}} = 0.5A_T \cdot \text{FO}, \quad A_{\text{NAND2}} = A_T. \tag{2}$$

Using Fig. 4(d), the areas of the two input XOR, A_{XOR2}, three-input XOR, A_{XOR3}, and three-input MAJ, A_{maj3}, are determined to be

$$A_{\text{XOR2}} = A_T + 2A_{\text{inv1}}, \quad A_{\text{XOR3}} = A_T + 3A_{\text{inv1}} \tag{3}$$

$$A_{\text{maj3}} = A_T + 2A_{\text{inv1}}. \tag{4}$$

The area of the multiplexer, A_{mux}, as shown in Fig. 4(c), the area of the state element circuit, A_{se}, realized with the TSPC flip-flop introduced in [27], and the area of the register bit, A_{rb}, based on the 6T SRAM cell discussed in [8], are determined to be

$$A_{\text{mux}} = 4A_T M_g, \quad A_{se} = 3A_T M_g, \; A_{rb} = A_T, \tag{5}$$

where M_g is the gate overhead factor used to model the space required to route interconnects [8]. This factor is back-corrected to take into account that the tile methodology leads to larger logic cells but does not require larger intercell routing area. Note that the overhead factor was not added to the XOR and MAJ gate circuits, as the tile methodology was specifically designed to include the additional spacing required for these gates. The register bit (SRAM cell) in BCB 3.0 [9] uses the optimized layout design of a six-transistor SRAM cell.

D. 1-BIT FULL ADDER

The functionality of TIGFET transistors enables a straightforward implementation of the 1-bit full adder. It requires three inverters, one three-input XOR gate, and one three-input MAJ gate as depicted in Fig. 6. The three inverters invert *A*, *B*, and carry-in (*Cin*), whereas the XOR gate outputs *Sum* and the MAJ gate outputs carry-out (*Cout*). The area of the 1-bit full adder is then shown to be

$$A_{1b} = (2A_T + 3A_{\text{inv1}})M_g = 3.5A_T M_g. \tag{6}$$

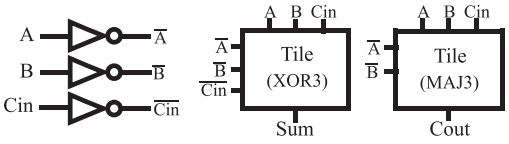

FIGURE 6. 1-bit full-adder circuit schematic.

E. 32-BIT FULL ADDER

The first important metric that is evaluated in BCB 3.0 [9] is the 32-bit adder. Here, we adopt a unique design for the 32-bit ripple-carry adder utilizing TIGFET transistors. Indeed, every stage, depicted in Fig. 7(a), relies on the efficient TIGFET 1-bit full adder design (Fig. 6) to generate Sum_n and $Cout_n$ but adds an extra three-input MAJ gate to generate $\overline{Cout_n}$. Generating both $Cout_n$ and $\overline{Cout_n}$ at the same logic level is made possible by the TIGFET technology at a low additional area cost (only two more transistors per stage) and leads to a significant performance benefit. The general structure of the 32-bit adder is shown in Fig. 7(b).

In order to restore the signal that is degraded passing through the source and drain terminals, an inverter for every five stages of the adder is added. Thus, the total area of the 32-bit adder is calculated as follows:

$$A_{32b} = 32(3A_T + 2A_{\text{inv1}})M_g M_g + 7A_{\text{inv1}}M_g \tag{7}$$

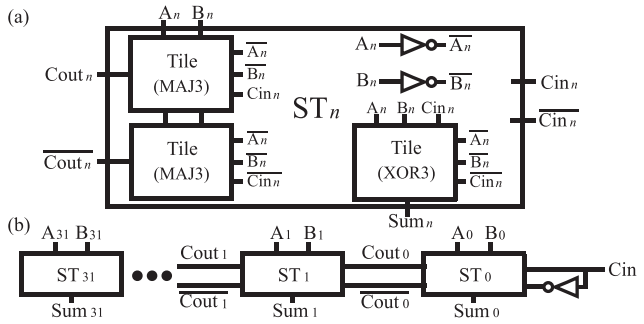

FIGURE 7. (a) Single stage, ST_n, where *n* denotes the stage number. (b) Stage diagram for the 32-bit ripple-carry adder.

F. 32-BIT ALU

The sequential gate metric used in this paper is the ALU. This circuit is capable of computing the addition, subtraction, NAND, and NOR of two 32-bit numbers as discussed in [9]. The equations that describe the area, delay, energy, and standby power for the 32-bit ALU have not been adjusted in this paper. The TIGFET technology will only affect the building blocks of the ALU.

G. AREA SUMMARY

Table 1 reports the areas evaluated in this paper. Here, we add the CMOS HP and the CMOS low-voltage (LV) areas to compare our results with BCB 3.0 [8]. The fan-out-of-1 inverter, the two-input NAND, the SRAM cell, and the flip-flop circuit lead to larger cell areas using TIGFET transistors. This was expected, since our evaluation employs conservative structures (tiles) to reduce routing congestions. Nevertheless, the two-input XOR, the two-level 4-to-1 MUX, the 1-bit full adder, and the 32-bit adder lead to decreased area thanks to the design opportunities given by TIGFETs. Such results show that the use of multiple independent gates does lead to lower areas in large systems.

TABLE 1. Total area summary expressed in F^2.

Logic Function	CMOS HP & LV	TIGFET	Comparison
FO-1 Inverter	160	380	2.37×
2-input NAND	288	759	2.64×
2-input XOR	1,728	1,518	0.88×
4-to-1 MUX	4,368	3,962	0.91×
Flip-Flop	2,448	2,972	1.21×
SRAM	320	759	2.37×
1-bit Adder	7,200	3,467	0.48×
32-bit Adder	345,600	168,920	0.49×
32-bit ALU	1,596,672	1,563,000	0.98×

IV. DELAY, ENERGY, AND STANDBY POWER

In this section, we evaluate the delay, energy, and standby power of the logic circuits implemented in BCB 3.0 [9].

A. TIGFET ELECTRICAL PROPERTIES

Device level parameters, i.e., OFF-current (I_{OFF}), ON-current (I_{ON}), and nominal voltage (V_{DD}) were extracted by commercially available TCAD Sentaurus from Synopsys Inc. The TIGFET structure under consideration is shown in Fig. 8. The materials used in this device were selected to ensure full compatibility with standard CMOS processes (e.g., CMOS HP). We also considered the same feature size of 15 nm taken from BCB 3.0 [9]. The channel (silver) is an 8-nm diameter SiNW. The dielectric layer (light orange) is HfO_2 with a thickness of 6.92 nm and an equivalent oxide thickness (EOT) of 1.08 nm. The gate length (L_g) is 15 nm while the separation between the gates are set to 15 nm.

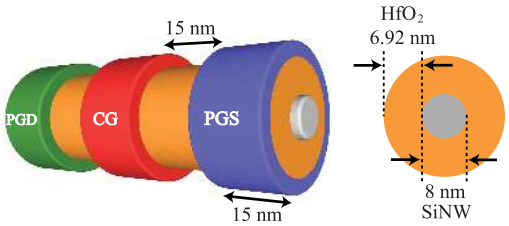

FIGURE 8. Experimental drawing of the TIG SiNWFET.

For a proper baseline comparison, the SiNW CMOS HP device (with well-designed short channel effects [32] and channel dimensions) has been simulated alongside the SiNW TIGFET device. Furthermore, Poisson's equations and continuity equations for both electrons and holes are solved self-consistently for the TIGFET device. The physical models applied to the device include Fermi statistics, the Philips unified mobility model, the Slotboom bandgap narrowing model, the band-to-band tunneling model for electrons in the source electrode and holes in the drain electrode, and finally the barrier lowering model for Schottky contacts. These settings were extracted from calibrated TCAD models performed in [11]. While these settings do not take into consideration quantum current distributions, such as using nonequilibrium Green's function formalism, we believe that such results give a good understanding of the electrical behavior of TIGFET transistors and is therefore suitable for the BCB methodology.

The I–V curve extracted from TCAD simulations is shown in Fig. 9. In order to achieve symmetric n-type and p-type ON-currents, metallic source/drain regions with mid-gap workfunction were designed. In practice, NiSi on Si may be used to achieve this condition [11]. The voltage required to create a large enough barrier on the OFF-state and, at the same time, lower the Schottky barrier enough at the source/drain terminals on the ON-state resulted in a nominal voltage of $V_{DD} = 0.9$ V. This condition allowed the I_{ON}/I_{OFF} metric to give the best performance values in terms of EDP and throughput. Different materials with lower bandgap energy are needed to further scale down the voltage while maintaining similar current densities. The extracted ON-current and OFF-current values were 12.6 μA and 0.135 pA, respectively. Using an effective width of $2\pi r$ for the SiNW transistor,

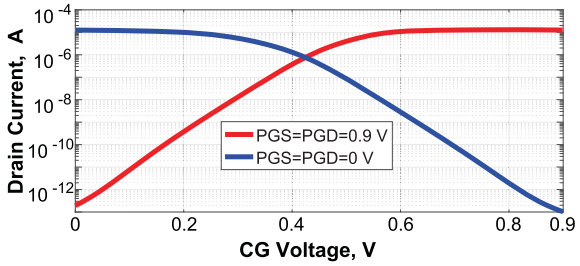

FIGURE 9. Drain current (I_D) versus CG voltage (V_{CG}) for a single TIG SiNWFET at $V_{DD} = 0.9$ V. The red and blue curves indicate the nMOS and pMOS realizations, respectively.

the ON-current density resulted in $I_{ON} = 501\ \mu A/\mu m$. Following the methodology from BCB 3.0 [9], the total current in the OFF-state mode includes both OFF-current density measured at the drain terminal and leakage current measured at the gate terminals. Using the standard gate leakage current in [9], the total OFF-current density is calculated to be $I_{OFF} = 3.8\ nA/\mu m$.

B. TIGFET TRANSISTOR EXPRESSIONS

Next, we evaluate the theoretical expressions for the delay (t_{int}), energy (E_{int}), and standby power (S_{int}) for a single TIGFET transistor. These basic equations follow the equations of an electronic-based device in [9]

$$t_{int,M_{cadj}} = \frac{C_{tot}V_{DD}}{I_{ON}} \tag{8}$$

$$E_{int,M_{cadj}} = C_{tot}V_{DD}^2 \tag{9}$$

$$S_{int} = V_{DD}I_{OFF}, \tag{10}$$

where

$$C_{tot} = \frac{\epsilon_r\epsilon_0}{EOT}L_g(M_{cadj} + M_{cpar}). \tag{11}$$

M_{cpar} is the parasitic capacitance factor which includes gate-to-source, gate-to-drain, gate-to-contact, fringing capacitance, and so on. This factor is set to 1.5 for all devices in BCB 3.0 [9]. M_{cadj} is the adjustment factor, identified by Fig. 10(a)–(d) that determines whether the intrinsic gate capacitance is larger or smaller than the capacitance of a single gate dielectric [9]. This factor is set to 1 for CMOS HP while a more thorough examination is needed for TIGFET devices.

C. CAPACITANCE ADJUSTMENT FACTOR

Three-dimensional Poisson electrostatic simulations performed in COMSOL Multiphysics were used to determine the parasitic and intrinsic capacitances of TIGFET SiNW transistors. Using FinFET (CMOS) COMSOL simulations as the baseline for comparison [33], the total capacitance difference (C_{tot}) and the corresponding adjustment factor (M_{cadj}) for the different modes of operation were calculated. These different modes of operation correspond to the different bias configurations in a TIGFET device. As shown in Fig. 10(a), if PG and CG gates are biased to a fixed voltage, then our

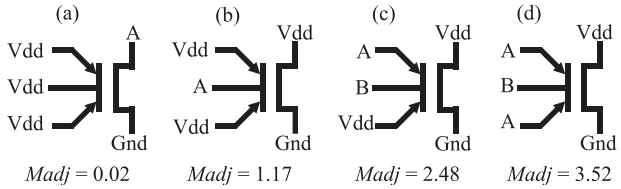

FIGURE 10. Capacitance adjustment factor (M_{cadj}) for the multiple modes of operation. A and B correspond to different inputs. The transistors in (a)–(c) are nFET configurations while the transistor in (d) may behave as an nFET or pFET configuration. The input gates set to V_{DD} may be set to G_{ND} for the pFET configurations.

simulations show that C_{tot} is 39.2% smaller than CMOS HP or $M_{cadj} = 0.019$. This configuration is only encountered in the 32-bit adder as discussed in Section IV-F. If only the CG is switching while the polarity gates are biased to a fixed voltage, then our simulations show that C_{tot} is now 6.65% larger than CMOS HP or $M_{cadj} = 1.17$, as depicted in Fig. 10(b). This configuration is, for example, encountered in the pull-up and pull-down networks of an inverter. When two inputs are switching while one polarity gate is biased to a fixed voltage, we see a 1.59 times increase in C_{tot} or $M_{cadj} = 2.48$ as shown in Fig. 10(c). This configuration is encountered in the pull-down network of a two-input NAND. Finally, when one input is tied to the CG and another input is tied to both polarity gates, then C_{tot} is 2.02 times larger than CMOS HP or $M_{cadj} = 3.52$ as depicted in Fig. 10(d). This configuration appears in the XOR and MAJ gates that are used in this paper.

D. INTERCONNECT CONDITIONS

The expressions of delay t_{ic}, energy E_{ic}, and standby power S_{ic} of a typical length interconnect are defined in [9]

$$t_{ic} = 0.7\frac{C_{ic}V_{DD}}{I_{ON}}, \quad E_{ic} = 0.5C_{ic}V_{DD}^2, \quad S_{ic} = 0, \tag{12}$$

where I_{ON} is the ON-current of the device and C_{ic} is the capacitance of a wire per length of interconnect (estimated to be five times the pitch) [9].

E. FUNDAMENTAL LOGIC GATES

Due to the similarities between TIGFET and CMOS representations of a NAND and inverter, we expect delay t, energy E, and standby power S equations to be

$$t_{inv1} = 2M_{tinv}t_{int,b} + t_{ic}L_{inv} \tag{13}$$

$$E_{inv1} = M_{Einv}E_{int,b} + E_{ic}L_{inv} \tag{14}$$

$$S_{inv1} = M_{tNAND}S_{int} \tag{15}$$

$$t_{NAND2} = 2M_{tNAND}t_{int,c} + t_{ic}L_{NAND} \tag{16}$$

$$E_{NAND2} = 2M_{ENAND}E_{int,c} + E_{ic}L_{NAND} \tag{17}$$

$$S_{NAND2} = M_{SNAND2}S_{int}. \tag{18}$$

The M_{tgate}, M_{Egate}, and M_{Sgate} factors are adjustment parameters from SPICE simulations as discussed in [9] using Arizona compact predictive technology model [34].

The length factors, L_{inv} and L_{NAND}, are defined as

$$L_{gate} = \max(1, \frac{\sqrt{A_{gate}}}{l_{ic}}), \tag{19}$$

where the subscript *gate* is the logic circuit under consideration. If the width of the logic circuit (assuming a squared layout) becomes larger than the typical length of an interconnect, then the energy and delay are corrected to account for a larger interconnect contribution. Following the methodology in BCB 3.0 [9], the interconnect energy component $E_{ic}L_{gate}$ is multiplied by the number of output signals for the gate in question.

As the subsequent circuit elements exploit one or more tiles, it becomes convenient to derive delay, t_T, energy, E_T, and standby power, S_T of a tile

$$t_{T,M_{\text{cadj}}} = 2M_{tT}t_{\text{int},M_{\text{cadj}}} + t_{ic}L_T \tag{20}$$
$$E_{T,M_{\text{cadj}}} = M_{ET}E_{\text{int},M_{\text{cadj}}} + E_{ic}L_T \tag{21}$$
$$S_T = M_{ST}S_{\text{int}}, \tag{22}$$

where the adjustment parameters M_{tT}, M_{ET}, and M_{ST} are considered to be similar to the adjusted parameters for a two-input NAND gate.

Using the tile estimations in [23], [30], and [31], we estimate the energy, delay, and standby power of the two-input XOR and three-input XOR gates using the design shown in Fig. 4(d) and the adjustment factors discussed in Section III-C

$$t_{\text{XOR2}} = t_{T,d} + t_{\text{inv1}}, \quad t_{\text{XOR3}} = t_{T,d} + t_{\text{inv1}} \tag{23}$$
$$E_{\text{XOR2}} = E_{T,d} + 2E_{\text{inv1}}, \quad E_{\text{XOR3}} = E_{T,d} + 3E_{\text{inv1}} \tag{24}$$
$$S_{\text{XOR2}} = S_T + 2S_{\text{inv1}}, \quad S_{\text{XOR3}} = S_T + 3S_{\text{inv1}}. \tag{25}$$

The three-input MAJ gate, using the design shown in Fig. 4(d), and the register bit, realized using the CMOS design of a 6T-SRAM cell, have the following expressions of delay, energy, and standby power:

$$t_{\text{maj3}} = t_{T,d} + t_{\text{inv1}}, \quad t_{rb} = 2t_{\text{inv1}} + t_{ic}L_{rb} \tag{26}$$
$$E_{\text{maj3}} = E_{T,d} + 2E_{\text{inv1}}, \quad E_{rb} = 3E_{\text{inv1}} + E_{ic}L_{rb} \tag{27}$$
$$S_{\text{maj3}} = S_T + 2S_{\text{inv1}}, \quad S_{rb} = 2S_{\text{inv1}}. \tag{28}$$

The four-input two-level static multiplexer, as shown in Fig. 4(c), uses three tiles with $M_{\text{cadj}} = 2.48$ (as discussed in Section III-C) and has its performance metrics expressed as

$$t_{\text{mux}} = t_{T,c} + 2t_{\text{inv1}} \tag{29}$$
$$E_{\text{mux}} = 2E_{T,c} + 3E_{\text{inv1}} \tag{30}$$
$$S_{\text{mux}} = 2S_T + 4S_{\text{inv1}}. \tag{31}$$

The state element circuit is realized using the design of the TSPC flip-flop introduced in [27]. This circuit uses one tile with $M_{\text{cadj}} = 2.48$, another tile that resembles two inverters, and two sets of inverters. Following the same methodology as BCB 3.0 [9], the expressions may be expressed as

$$t_{se} = t_{T,c} + 3t_{\text{inv1}} + t_{ic}L_{se} \tag{32}$$
$$E_{se} = E_{T,c} + 4E_{\text{inv1}} + 2E_{ic}L_{se} \tag{33}$$
$$S_{se} = S_T + 4S_{\text{inv1}}. \tag{34}$$

F. FULL ADDERS

The 1-bit full adder, as presented in Fig. 6, is designed using one XOR gate and one MAJ gate. The expression of the energy component, $E_{1\,\text{bit}}$, is estimated using the activity factor found in [35] and [36]. The activity factor of the three-input XOR (α_{XOR3}) and of the three-input MAJ (α_{maj3}) are calculated to be 3/16 and 1/4, respectively. Furthermore, the unique structure of a TIGFET full adder allows the delay, $t_{1\,\text{bit}}$, to be dependent on a single tile plus an inverter. The standby power, $S_{1\,\text{bit}}$, includes two tile and three inverter components

$$t_{1\,\text{bit}} = t_{T,d} + t_{\text{inv1}} + t_{ic}L_{1\,\text{bit}} \tag{35}$$
$$E_{1\,\text{bit}} = \alpha_{\text{XOR3}}E_{T,d} + \alpha_{\text{maj3}}E_{T,d} + 3E_{\text{inv1}}/2 + 2E_{ic}L_{1\,\text{bit}} \tag{36}$$
$$S_{1\,\text{bit}} = 2S_T + 3E_{\text{inv1}}. \tag{37}$$

The 32-bit ripple-carry adder adopted in this paper is shown in Fig. 7. Adding a three-input MAJ gate to each stage allows the generation of $\overline{Cout_n}$ and $Cout_n$ to be at the same logic level. The critical path delay contribution of a single stage corresponds to the delay for the propagating carry signals, $\overline{Cin_n}$ and Cin_n, to travel through a transmission gate and solely charge the parasitic capacitances. This special case allows us to consider $M_{\text{cadj}} = 0.02$ for the delay component of a tile. The energy component, on the other hand, will consider $M_{\text{cadj}} = 3.52$, since energy is spent charging the gate-to-channel capacitances. An additional interconnect component will be added for every stage in order to compensate for the additional output signal propagation ($\overline{Cout_n}$). For all the three relations, six inverters are added to restore the degraded signal passing through the XOR and MAJ gates with its corresponding activity factor. Furthermore, the energy and standby power relations include an additional inverter to invert Cin_0

$$t_{32\,\text{bit}} = t_{1\,\text{bit}} + 31(M_{tT}t_{\text{int},a} + t_{ic}L_{1\,\text{bit}}) + 6t_{\text{inv1}} \tag{38}$$
$$E_{32\,\text{bit}} = 32(E_{1\,\text{bit}} + \alpha_{\text{maj3}}E_{T,d} + E_{ic}L_{1\,\text{bit}}) - 32(E_{\text{inv1}}/2) + 7E_{\text{inv}}/2 \tag{39}$$
$$S_{32\,\text{bit}} = 32(S_{1\,\text{bit}} + S_T - S_{\text{inv}}) + 7S_{\text{inv}}. \tag{40}$$

V. BENCHMARKING RESULTS

In this section, we analyze the performance of BCB 3.0's flagship benchmarking, i.e., the 32-bit adder and the 32-bit ALU [9], for the TIG SiNWFET and for the whole set of BCB 3.0's technologies. The standby energy, switching energy, and delay are considered for the 32-bit adder, whereas the power density, throughput, switching energy, and delay are considered for the 32-bit ALU.

Fig. 11(a) and (b) shows very promising results for the 32-bit adder using the TIGFET technology. EDP is 3.83 times smaller than CMOS HP and 4.18 times smaller than CMOS LV. In fact, the EDP for the TIGFET technology surpasses every device in BCB 3.0 [9] for the 32-bit adder. Similarly, the standby energy for the TIGFET technology surpasses

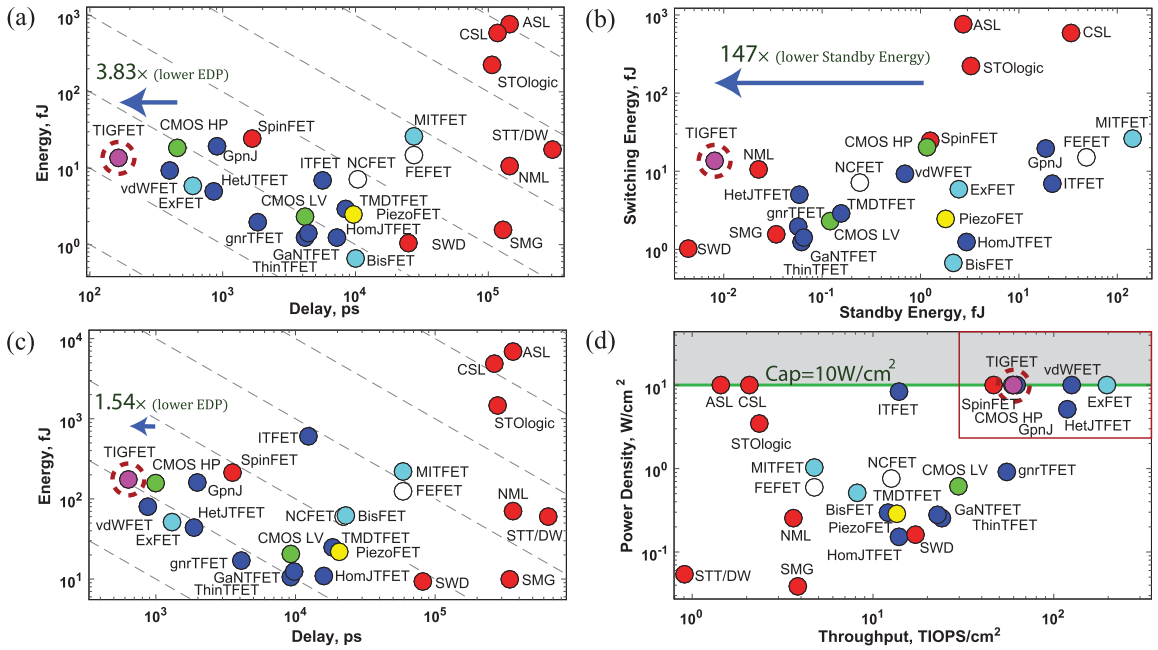

FIGURE 11. **32-bit adder with (a) *E* versus *t* and (b) *E* versus *S*. 32-bit ALU with (c) *E* versus *t* and (d) power density versus throughput.**

every silicon device and is at least two orders of magnitude smaller than CMOS HP and at least one order of magnitude smaller than CMOS LV. These results are owed to the innovations brought on by the TIGFET technology that allows for novel functionalities at the device level granting superior circuit implementations and also exhibits sufficient drive current, good *p*-type and *n*-type symmetry, easy fabrication, and low-leakage floor.

The 32-bit ALU performance metrics are shown in Fig. 11(c) and (d). While some technologies show better EDP than the TIGFET device for the 32-bit ALU, it is still a competitive beyond-CMOS device as the EDP is shown to be 1.54 times smaller than CMOS HP and 1.75 times smaller than CMOS LV. The power density for the TIGFET device and multiple other devices are capped at 10 W/cm^2. This cap limits the computational throughput and is further discussed in [8]. Despite this limiting factor, the TIGFET devices have essentially the same throughput than CMOS HP (1.43% difference) and 1.97 times higher throughput than CMOS LV. The main contribution to the large throughput used by the TIGFET technology is the small switching delay while having lower total area. While being fully silicon-based devices, TIGFETs are estimated to have the lowest energy per operation and a very appealing computational throughput for the 32-bit ALU.

VI. CONCLUSION

In this paper, the TIG SiNWFET device is investigated as an effort to compare its performance with other beyond-CMOS devices. The same feature size, channel material, and EOT were followed to ensure full compatibility with standard CMOS processes. While SiNW TIGFET devices may be less appealing from a device perspective as compared with CMOS HP (reduced current densities, increased device capacitance, and so on), the unique circuit design capabilities, coming from the dynamic control of the polarity, allow for a competitive boost in performance at the system level. Furthermore, the TIGFET technology may also benefit from device scaling, such as reduced metal/contact size, reduced oxide thickness, high-mobility, and low band-gap channel materials—similar to CMOS scaling. The benchmarking results show that SiNW TIGFET devices are well suited for large-scale circuits where its multigate functionality may be fully exploited. In particular, our estimates show that, by using our device, the 32-bit adder has 3.83 times lower EDP, 2.05 times lower total area, and 147 times lower standby energy than CMOS HP and 4.18 times lower EDP, 2.05 times lower total area, and 15.4 times lower standby energy than CMOS LV. On the other hand, the estimates show that the 32-bit ALU has 1.54 times lower EDP and 1.43% higher throughput than CMOS HP and has 1.75 times lower EDP and 1.97 times higher throughput than CMOS LV. The presented device illustrates the promises of the growing family of functionality-enhanced devices where technology's capabilities allow designers to create superior circuits and systems.

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