

# Behavior of the Flying Capacitor Converter Under Critical Operating Conditions

**Conference Paper****Author(s):**

Papamanolis, Panteleimon; Neumayr, Dominik; Kolar, Johann W.

**Publication date:**

2017

**Permanent link:**

<https://doi.org/10.3929/ethz-b-000187514>

**Rights / license:**

[In Copyright - Non-Commercial Use Permitted](#)

**Originally published in:**

<https://doi.org/10.1109/ISIE.2017.8001319>

# Behavior of the Flying Capacitor Converter Under Critical Operating Conditions

Panteleimon Papamanolis, Dominik Neumayr, and Johann W. Kolar

Power Electronic Systems Laboratory (PES)  
ETH Zurich, Physikstrasse 3  
8092 Zurich, Switzerland  
Email: papamanolis@lem.ee.ethz.ch

**Abstract**—The Flying Capacitor Converter (FCC) offers an attractive alternative to conventional 2-level converter topologies due to the easily acquired high number of voltage levels and the increased effective switching frequency. However, balancing of the flying capacitor (FC) voltages is crucial in practice since a deviation from the nominal voltage levels increases harmonics in the output voltage and, more importantly, jeopardizes the integrity of the converter due to overvoltages across the power transistors. Modulation inherent FC balancing techniques (termed natural/passive balancing) have been thoroughly analyzed in literature, however only for stationary operating conditions. In this paper, the behavior of the FCC and the effectiveness of passive balancing will be analyzed in detail regarding specific operating conditions present in typical industry applications such as converter start-up, shut-down, standby and operation under fault conditions. The basis for the analysis is a 5-level, 2kW FCC embedded in two typical industry applications: single-phase PV inverter and single-phase PFC rectifier.

## I. INTRODUCTION

The Flying Capacitor Converter (FCC) is exceptional among multilevel topologies, since it only employs a single DC source, i.e. compared to the cascaded H-bridge converter no isolated voltage sources are required and no clamping diodes like in the Neutral Point Clamped (NPC) topologies. Moreover, it can operate both in DC/DC and bidirectional DC/AC mode and there is no restriction regarding the modulation index range. In the past, multi-level converters have been employed in high voltage / high power applications to overcome the blocking voltage limitation of the involved power semiconductors [1]. Recently, it was demonstrated that the FCC might also be a preferable choice in low-voltage DC/AC applications [2]. Due to the resulting multi-level output voltage and the increased effective switching frequency, the size of passive filter components can be significantly reduced yielding high power density designs. Moreover, since low-voltage and/or low  $R_{ds,on}$  power devices can be employed and the switching frequency can be kept comparably low, also a high conversion efficiency can be achieved. However, despite the many advantages and the remarkable performance, until now, the FCC is seldom employed in industry applications. One of the reasons might be that the performance and the integrity of the FCC depends on the

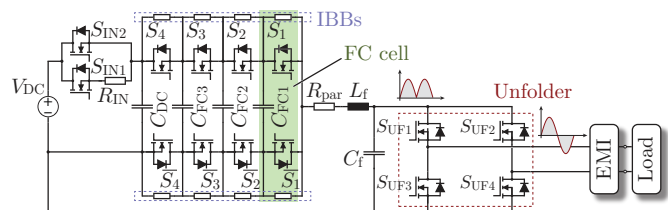


Fig. 1: 5-Level FCC half-bridge topology with LC filter and low-frequency unfold, equipped with internal balance boosters (IBBs) and pre-charge circuitry.

balancing of the individual FC voltages. A large number of scientific publications deals with modeling and control-related aspects of FC voltage balancing. The dynamics of the FC voltages under passive balancing (natural balancing) have been analyzed both in the frequency [3]–[6] and in the time domain [7]–[10] and also in a more generalized multilevel inverter topology using simulation results in [11]. In addition, several methods have been proposed on how to achieve monitored balancing operation using active techniques [12]–[14].

Although the FC dynamics have been studied in great detail in literature for stationary operation, the actual behavior of the converter during start-up, standby, shut-down and failure handling, i.e. operating conditions inherently occurring in typical industry applications, has not been investigated yet. With respect to failure handling, the ability to balance the FC voltages, while limiting the output current in case of a short-circuit, and the behavior of the FCC subject to an intermittent outage of the grid voltage is of interest. Concerning start-up of the converter, several methods to pre-charge the FC voltages have been proposed in literature so far [12]–[17].

In this paper the aforementioned critical operating modes are studied in detail for two distinct application embodiments of the FCC: i) single-phase PV inverter and ii) single-phase PFC rectifier. By means of comprehensive circuit simulation results, it is demonstrated whether or not the FCC is able to handle abnormal operating conditions present in any industry application.

The basis for the presented analysis is a 5-level, bidi-

**TABLE I: System Parameters**

Input Volt.	$U_{in} = 450$ V	Nom. Power	$P = 2$ kW
Switch. Freq.	$f_{sw} = 80$ kHz	No of Levels	$N = 5$
Nom. Out. Volt.	$U_{out} = 230$ Vrms	FCs	$C_{FC1} - C_{FC3} = 12$ $\mu$ F
Output Freq.	$f = 50$ Hz	Filter Ind.	$L_f = 22$ $\mu$ H
Mod. Scheme	iPSPWM	Eff. out. freq.	$f_{eff} = 320$ kHz

rectional, 450V DC/AC converter, which is introduced in more detail in **Sec. II**. Moreover, additionally required passive components for improving FC voltage balancing, termed *balance-boosters* in literature, will also be introduced in **Sec. II**. Subsequently, in **Sec. III** the critical operating modes are studied for the two considered applications, and practical solutions to overcome possible shortcomings are presented.

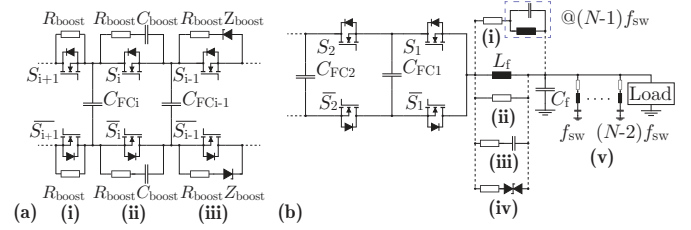
## II. ANALYZED TOPOLOGY

### A. 5-Level single-phase FCC

The topology employed for the analysis of this paper, is a 2kW 5-level single-phase FCC. It consists of a single bridge-leg connected to an LC output filter and a subsequent full-bridge unfolded operated with AC output frequency, i.e. 50 Hz (cf. **Fig. 1**). More details regarding the operation and implementation of the topology can be found in [2]. A preceding Pareto optimization with focus on high power density (omitted here for the sake of brevity) yielded the system parameters listed in **Table I**. The optimized design was implemented in hardware, achieving 98.7% efficiency at 2kW and a power density of 192 Watts/in<sup>3</sup>. The results presented herein for the studied operation modes were obtained from a co-simulation between Matlab/Simulink (sim. of the control system) and GeckoCIRCUITS (sim. of the FCC circuit). The implemented control system depends on the actual application and will be introduced in the respective sections.

### B. Internal / External balance boosters

Provided good balancing dynamics, the FC voltages remain well balanced and show no steady-state deviation (excluding the switching frequency ripple) from their respective nominal values, even if real world non-idealities are present in the circuit. The balancing dynamics are strongly affected by the employed modulation scheme and depend on the prevailing modulation index. Apart from the saturated regions (duty-cycle 0 or 1) the common phase-shifted (PS) PWM results in comparably poor dynamics also in intermediate modulating regions, as it is not effectively utilizing the redundant switching states of the FC topology. In [18] the presence of poor balancing regions in 4-7 level topologies is mathematically proven and in [16] an improved PSPWM (iPSPWM) scheme is proposed for a 5-level single-phase inverter, which increases the balancing dynamics in the intermediate modulation regions. In order to further improve balancing and to cope with all critical operating modes, additional passive components,



**Fig. 2:** (a) Internal and (b) external balance boosters to improve balancing dynamics of the FCC.

so-called *balance boosters* (BBs), can be installed [19]. These additional balancing measures can be classified in internal and external boosters and are briefly summarized in the following.

1) *Internal Balance Boosters (IBBs)*: The three most common IBB concepts are shown in **Fig. 2a**. It has to be noted that boosters including zener diodes and capacitors are increasing the effective capacitance parallel to the power transistors, thus increasing the hard-switching losses in each cell (a cell comprises of two complementary switches  $S_i/\bar{S}_i$  and an adjacent FC ( $C_{FCi}$ ) cf. **Fig. 1**). In addition, boosters including capacitors operate only during a transient and are ineffective in converter standby or if modulation indices close to the limits are present.

Regardless of the type of IBB, a passive pre-charge without ramping the DC-link is not feasible, since immediately after turn-on, the cell closest to the DC-link would share the full DC voltage. Studying the simplest case of IBBs in **Fig. 2a(i)**, the time constant of the passive RC network is:

$$T_{BB} = (N-2)R_{boost}C_{FC}. \quad (1)$$

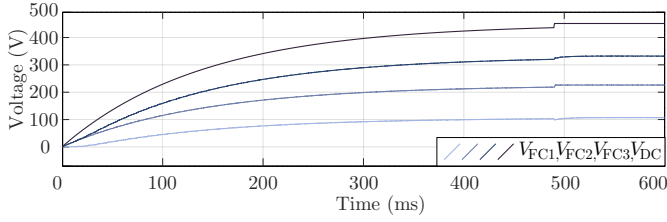
For the considered 5-level FCC, for reasons that will be discussed in **Sec. III-A2**, the permissible pre-charge time is set to 500ms. By setting the time constant of the IBB network five times smaller, it will result in an  $R_{boost}$  of approximately 700  $\Omega$ . For such a resistance, the additional losses of the circuit in steady state operation would be

$$P_{BB} = \frac{V_{cell}^2}{R_{boost}} = 18 \frac{W}{cell}, \text{ where } V_{cell} = \frac{V_{DC}}{(N-1)}. \quad (2)$$

Although IBBs cannot be used for pre-charging, they help to maintain balancing during standby, as will be shown in **Sec. III-A**.

2) *External Balance Boosters (EBBs)*: The most commonly found EBB in literature is a RLC network tuned at multiples of the switching frequency ( $f_{sw}, \dots, (N-2)f_{sw}$ ), connected in parallel to the output [3] (cf. **Fig. 2b(v)**). The idea behind this concept is to provide low impedance paths for the balancing frequencies, with losses high enough in order to improve the dynamics. The more the active power drawn at those frequencies, the better the dynamics of the FCs balancing. A possible alternative in case a high number of





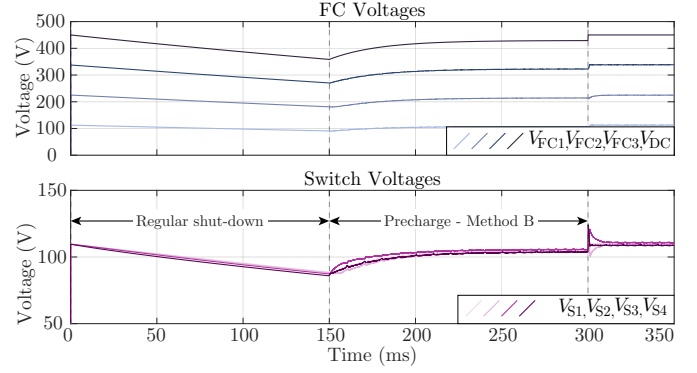
**Fig. 5:** Simulation results of the start-up procedure using method B.

5-level half-bridge with subsequent unfolders considered in this paper (cf. **Fig. 1**), in order to generate 0V at the output a duty-cycle of  $d=0$  must be selected which unfortunately disables the FC dynamics. Consequently, during the pre-charge of the FCs the load/grid must be isolated to allow a duty-cycle selection with good balancing dynamics, which will generate an output voltage (across filter capacitor  $C_f$ ) during the pre-charge; this works for all numbers of levels. In case of the island-mode PV inverter application the unfolders suffice to isolate the load. In case of the grid connected inverter, an additional bi-directional switch (relay, see also **Fig. 12**) must be inserted between the unfolders and the mains.

3) *Standby operation:* A common operating state for an inverter is the standby mode where the DC-link and the FCs are charged but no voltage must be generated at the inverter output. Moreover, if required by the application, all switching actions must be suspended during standby. As a consequence, natural balancing is disabled and the FCs are discharging due to leakage currents of the installed capacitors ( $R_{leak}$  typically larger than several hundreds of  $M\Omega$ ). The off-state resistance of the power transistors (2-3 orders of magnitude lower, operating as IBBs) tend to balance the FCs back to their nominal values, however the actual off-state resistance can vary significantly between the power transistors. To remedy this problem, IBBs of  $1 M\Omega$  (or less if needed) are installed which ensure permanent balance of the circuit while in standby, causing negligible steady state losses of 13 mW/cell (according to (2)). The value of  $R_{boost}$  (cf. **Fig. 2a(i)**) must dominate the leakage resistance of the power transistors in order to ensure equal voltage sharing.

4) *Regular shut-down (complete and incomplete):* Regular shut-down corresponds to an immediate turn-off of all switches in the circuit. Safe discharge of the FCs, as well as the ability to re-enable the converter during the shut-down process, are both essential properties. Depending on the application, it might be required to discharge the circuit within a specified amount of time (e.g. in case of a failure) which demands for an additional discharge circuit in parallel to the DC-link. As this strongly affects the shut-down process, shut-down with and without additional discharge circuit will be studied individually.

If no discharge circuit is present, electrolytic capacitors at the DC-link represent the worst case scenario. Due to the

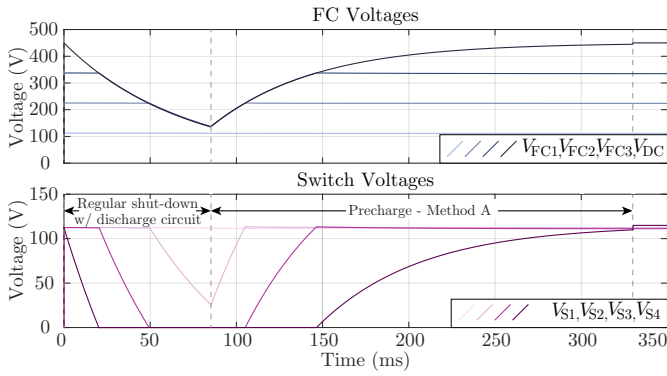


**Fig. 6:** Simulation results of incomplete regular shut-down of the 5-level FCC (time constants are adapted in order to present shut-down and re-start within a shortened time interval).

installed IBBs, a symmetric discharge of the converter is ensured as shown in **Fig. 6**, where at  $t=0$  ms a shut-down is initiated. Without having the DC-link completely discharged, the converter is re-enabled at  $t=150$  ms, symmetrically charging the FCs back to their nominal voltage values by means of natural balancing (start-up method B in **Sec. III-A2**). It should be noted that the time constants of the simulation model were adapted in order to present shut-down and re-start within a shortened time interval.

With additionally installed discharge circuit, a discharge rate of the DC-link faster than the dynamics of the IBBs is considered. In this case the converter also discharges safely, as shown in **Fig. 7**, since the FCs are tied to the DC-link via the anti-parallel diodes of the power transistors. Re-enabling the converter during the discharge process is more challenging, as the FCs have to be recharged from an unsymmetrical state (cf. **Fig. 6** at  $t=150$  ms and **Fig. 7** at  $t=80$  ms). According to [20], charging the FCs from an unbalanced initial condition by means of natural balancing causes severe voltage oscillations depending on the initial voltage deviations. Therefore, start-up of the converter according to method A (cf. **Sec. III-A2**) is advised, as it is capable of safely restarting the converter as shown in **Fig. 7** at  $t=80$  ms.

5) *Grid voltage fluctuation / load steps:* Both island-mode and grid connected operation need to be able to handle severe load steps. According to [21], depending on the amplitude of the grid voltage fluctuation (both under/overvoltage), the inverter is advised to stay connected to the grid for a proposed time period, to avoid unnecessary disconnections. As a result, it is required that a 50% decrease of the grid voltage should not constitute an issue for the topology. In order to preserve constant output power, the converter must immediately adapt the reference value of the underlying current controller, which ultimately results in an almost step-wise change of the duty-cycle. The caused voltage deviation of the FCs can be calculated by integrating the product of the load current and the duty-cycle difference of two consecutive switches,



**Fig. 7:** Simulation results of incomplete regular shut-down of the 5-level FCC with additional discharge circuit (time constants are adapted in order to present shut-down and re-start within a shortened time interval).

$$v_{FCi}(t) = \frac{1}{C_{FCi}} \int_0^t (d_{i+1}(\tau) - d_i(\tau)) i_L(\tau) d\tau, \quad (3)$$

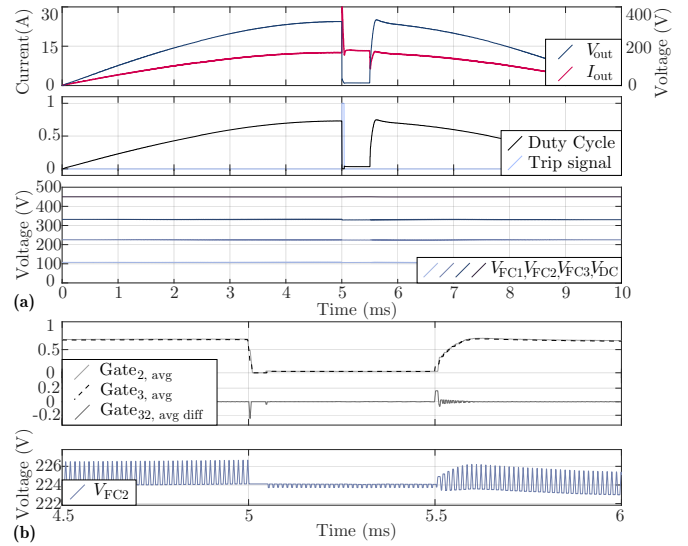
for a sampling of the duty-cycle (reference signal) synchronized to the phase-shifted carrier of the respective FC cell. For the implemented FCC, the 50% abrupt reduction in grid voltage causes a FC voltage step of just 6V, which is negligible considering the actual FC peak-to-peak voltage ripple of 2.5V.

Regarding the abrupt duty-cycle transitions, adding a moving average (MA) filter at the controller output has been proposed in [19], however, this decreases the system bandwidth.

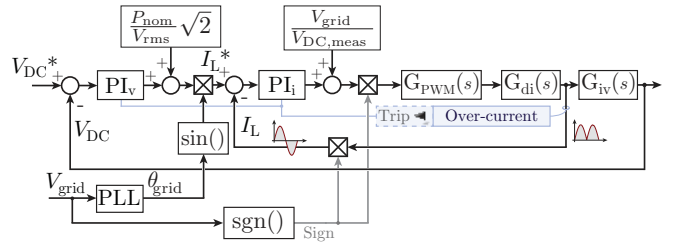
6) *Short-circuit:* The considered scenario is based on a short-circuit (SC) of 0.5 ms duration occurring in close vicinity to the converter. The SC impedance, due to the small distance from the fault location, is considered purely ohmic and equal to  $1 \Omega$ . The critical events of the SC is the moment the fault occurs and the moment the SC ceases and the converter returns back to normal operation. During these events, a step change in duty-cycle, requested by the control system to handle the fault, propagates through the individual FC cells and affects the FC voltage according to Eq.3. The operation during the fault with small duty cycle to limit the current is not critical, thus it suffices to consider a fault duration of just 0.5 ms, although a SC event may last considerably longer in reality. The simulation results are shown in **Fig. 8**, where at  $t=5$  ms a short-circuit is applied.

Once the fault has been identified, both PI controllers (cf. **Fig. 3**) along with their reference values are frozen and the duty-cycle is set to 0 in order to limit the fault current. The actual peak of the SC current depends on how quickly the fault can be identified. Once the current decreases back to the reference value of the current controller, operation under fault is continued with only the current controller enabled.

As can be seen from the detailed view in **Fig. 8b**, the FC voltages remain unaffected by the short-circuit, given that appropriate fault handling mechanisms are in place as



**Fig. 8:** (a) Simulation waveforms for a short-circuit, during passive load operation. (b) Zoomed in waveforms during the transient of FC2 and its surrounding switches (for clarity reasons only  $V_{FC2}$  is depicted).



**Fig. 9:** Controller diagram for Grid Rectifier mode (Controller gains: (i) Voltage -  $K_p = 100e-3$  A/V,  $K_i = 1.5$  A/V, (ii) Current -  $K_p = 5.6e-3$  A $^{-1}$ ,  $K_i = 1$  A $^{-1}$ ). Sgn() corresponds to the signum function and is used in order to define the measurement/duty cycle signs, hence creating a pseudo-sinusoidal controller with lower bandwidth requirement.

discussed before. A more sophisticated fault identification mechanism (eg. asynchronous trip) would result in a significantly lower SC current peak.

### B. PFC Rectifier

In this section, the 5-level FCC deployed as PFC rectifier for a single-phase 2 kW telecom supply is analyzed. The controller scheme used in the simulation models is shown in **Fig. 9**. For the sake of brevity, only operating conditions which are specific to rectifier application or show a different outcome compared to the PV inverter will be discussed in the following.

1) *Start-up procedure:* For rectifier operation, there are no official standards that define a minimum start-up time of the converter. A minimum start-up time is typically defined by the customer and depends on the specific application. Similar to the PV inverter application, two methods are proposed. For both methods, a precharge resistor is required before the unfold stage, in order to limit the inrush current. The value of this resistor is chosen such that the

peak current during the first cycle is less than the maximum tolerable current of the capacitors and, at the same time, core saturation of the boost inductor is avoided.

**Method A** is split into two main operating modes; mode 1 relies on a *quasi-passive* operation, which also employs the precharge resistor and mode 2 is an *active boost* operation, during which the precharge resistor is bypassed. The operating state of each FC cell, as well as the circuit state, during the complete start-up procedure can be found in **Table II** and **Fig. 10**, respectively. For the sake of simplicity, the unfold and the EMI stages are omitted and a rectified grid voltage is considered directly before the precharge resistor.

Mode 1 applies as long as the DC link voltage is below the maximum grid voltage (325 V). At the beginning all switches, except  $\overline{S_1}$ , are turned on. This way the system is being directly charged from the grid through the precharge resistor in a passive way. Once the DC-link voltage equals to  $V_{DC,nom}/4$  (i.e.  $V_{DC} = 112.5$  V),  $\overline{S_2}$  also turns off and the same applies to  $\overline{S_3}$  at  $V_{DC} = 225$  V. Due to this simple switching operation this mode could be termed as *quasi-passive*.

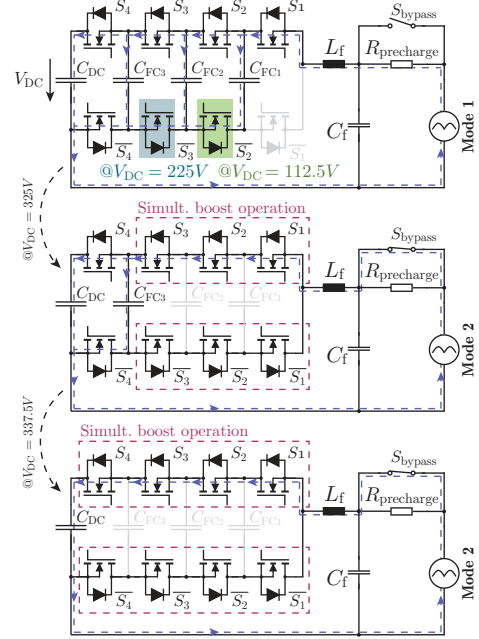
In mode 2 FCs 1 & 2 already have their nominal values. At this point, the precharge resistor is bypassed and the topology is operated as a conventional 2-level boost converter. Switches  $S_3$ ,  $\overline{S_3}$ ,  $S_4$  and  $\overline{S_4}$  are constantly on, switches  $S_1$  and  $\overline{S_2}$  are off (operating as rectifying diodes) and switches  $\overline{S_1}$  and  $S_2$  represent the boost switches, operating simultaneously. It is important to note that synchronous and not phase shifted carrier should be used during this procedure. Once the  $V_{DC} = 337.5$  V, which is the nominal voltage value of FC3, then  $S_3$  turns off and  $\overline{S_3}$  also operates in parallel to  $\overline{S_1}$  and  $\overline{S_2}$ , until  $V_{DC} = 450$  V.

This method can be applied also in a half-bridge topology with split DC-link or in a full-bridge. Moreover, depending on the nominal voltage of the DC-link and the number of levels, the transition between mode 1 and mode 2 can take place at a different time instant. In both modes, some of the top switches are used as rectifying diodes. Nevertheless, the existence of the IBBs will create a voltage difference between two consecutive FCs each time the diodes do not conduct and, as a result, uncontrolled current exchange will occur once the corresponding diodes conduct again. This can be avoided by keeping the corresponding switch permanently in the on state. Simulation results of the proposed method can be seen in **Fig. 11**.

**Method B**, whose simulation results will be omitted for the sake of brevity, would be to start-up the system operating it in mode 1 and sequentially turn off the lower switches, such that when the DC-link has reached  $V_{grid,max}$ , the complete system is already balanced, with respect to  $V_{DC} = V_{grid,max}$ . Subsequently, boost operation can bring the DC-link voltage (and as a result the complete system) to its nominal value (cf. **Fig. 12**). Compared to the method A, method B is simpler in terms of implementation, however in case of an incomplete hold-up case (cf. **Sec. III-B3**),

**TABLE II:** Rectifier start-up procedure (method A)

Stage	1	2	3	4	5
Mode	1	1	1	2	2
Max. $V_{DC}$	112.5 V	225 V	325 V	337.5 V	450 V
$\overline{S_1}$	on	on	on	boost	boost
$\overline{S_1}$	off	off	off	boost	boost
$\overline{S_2}$	on	on	on	boost	boost
$\overline{S_2}$	on	off	off	boost	boost
$\overline{S_3}$	on	on	on	boost	boost
$\overline{S_3}$	on	on	off	boost	boost
$\overline{S_4}$	on	on	on	on	boost
$\overline{S_4}$	on	on	on	on	boost
$S_{bypass}$	off	off	off	on	on

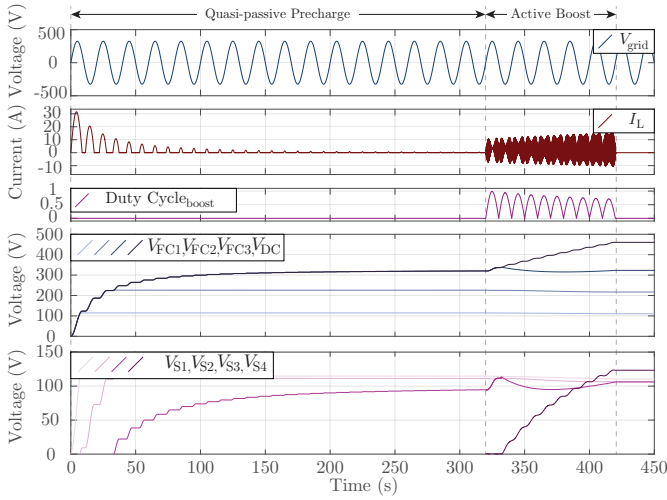


**Fig. 10:** Proposed start-up procedure employing method A, during rectifier operation. The unfold stage is omitted and a rectified grid voltage source is assumed. Depending on the DC voltage, the different mode transitions are depicted (in mode 1 the colored switches turn off at the corresponding voltage level of  $C_{DC}$ ).

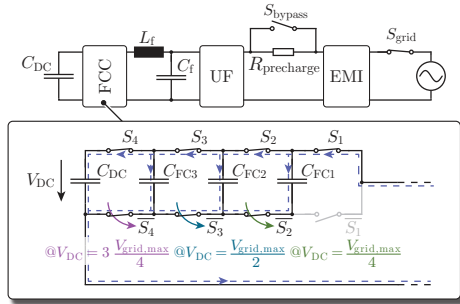
recovery of the system would not be possible, unless a complete discharge of the DC-link would take place.

2) *Standby operation:* In passive standby operation, it is assumed that the FC bridge-leg is blocked (gate signals suspended) and no voltage is generated at the AC side. In this case, the DC-link voltage will decrease to  $V_{grid,max}$  and the FCs will follow accordingly through the IBBs. Once rectifier operation is restarted, the FCC will need to charge the DC-link to its nominal voltage value, before supplying the load, using PSPWM. The FCs will symmetrically follow, due to the enabled voltage balancing dynamics.

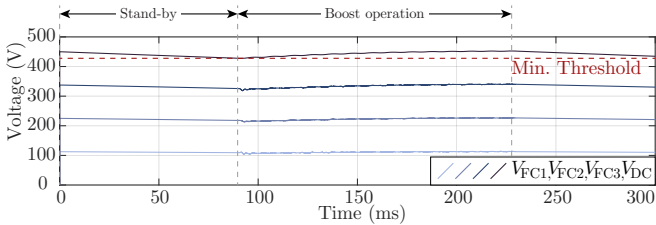
In active standby operation, the DC-link voltage is monitored. Once it drops below a pre-defined threshold, the DC-link is charged back to its nominal value and then passive standby mode is again enabled. In this way, the converter remains charged, while reducing standby power loss (cf. **Fig. 13**).



**Fig. 11:** Simulation results of start-up procedure of a FCC, employing method A. The proposed value of the precharge resistor is 30 Ohms, however in order to shorten the simulation time interval, a value of 10 Ohms is considered, which results in increased precharge currents.



**Fig. 12:** Proposed start-up procedure employing method B, during rectifier operation. The arrows depict switch turn off at the indicated voltage level of  $C_{DC}$ .



**Fig. 13:** Voltage waveforms of the FCs during standby operation of rectifier operation (time constants are adapted, for demonstration purposes).

3) *Grid voltage fluctuation / grid outage:* In case of fluctuations of the grid voltage, e.g. a sudden voltage drop to 50%, the FCs are not affected, since a proper controller will promptly adapt to the new AC input and as already discussed earlier in **Sec. III-A5**, such reference step does not jeopardize the converter. More problematic is the scenario of a complete grid outage, where the following cases must be distinguished:

- **Connected load (Hold-up case):** The DC-link rapidly discharges and the FCs follow through the anti-parallel diodes. In case of grid operation return, the system can

follow the start-up procedure of method A proposed in **Sec. III-B1**, since it represents the inverse operation. Nevertheless, it is of great importance that once the DC-link is discharged below 325V,  $S_{bypass}$  is turned off in order to limit the inrush current.

- **No load connected:** The FCs symmetrically follow the DC-link, due to the IBBs. In case grid operation returns before the DC-link has discharged below 325V, the rectifier operation can be re-enabled, bringing the DC-link back to its nominal value. However, for DC-link value below 325V, rectifier operation cannot be enabled and the proposed pre-charge method (cf. **Sec. III-B1**) can only be initiated, if the FCs are completely discharged, which requires additional discharge circuitry to be installed.

#### IV. CONCLUSION

The performance of a 5-level, bi-directional Flying Capacitor Converter (FCC) embedded in two typical industry applications, single-phase PV inverter and single-phase PFC rectifier, was assessed in this paper. It is shown, that if the circuit parameters of the FCC are correctly dimensioned and the improved phase-shifted PWM (iPSPWM) is employed, the FCC features excellent passive balancing properties, which keep the FC voltages charged to their nominal values during stationary operations. More interestingly, it is verified that passive (natural) balancing remains effective also during abnormal/critical operating modes present in the considered application. Start-up of the FCC can be handled by means of a dedicated pre-charge control routine, however, additional pre-charge circuitry must be installed in order to limit the  $dV/dt$  of the applied DC source voltage (PV inverter) or grid voltage (PFC rectifier). Regardless of the application, internal balance boosters (IBBs), i.e. high ohmic resistors in parallel to the power transistors causing negligible losses, must be installed to keep the FCs balanced during standby, where all switching actions must be suspended and therefore natural balancing is lost. Furthermore, it is shown that during shut-down of the converter, the FCs discharge symmetrically, with decreasing voltage of the DC-link capacitor (parasitic leakage resistors), if IBBs are installed. If a faster shut-down is required by the PV inverter (installation of additional discharge circuitry on the DC-link) or the connected load quickly drains the DC-link capacitor as in the case of the PFC rectifier (hold-up case), the FCs are also safely discharged (i.e. no over-voltage across the power transistors is caused) by means of the anti-parallel diodes of the power transistors. However, since the time-constant of the discharge process is now much smaller than the natural balancing time-constant or the IBBs (in case of suspended switching operation), the FCs are in an unsymmetrical state, if the converter is re-enabled before the shut-down is completed. For both considered applications, pre-charge routines are proposed that can be directly initiated in order to restart the converter. Furthermore, it was verified that with an appropriate fault-



handling mechanism and control system in place, the FCC can deal with grid voltage fluctuations and short-circuit conditions, while keeping the FC voltages balanced. It can be concluded that the considered 2kW, 5-level FCC is capable of handling typical critical operating conditions, given that the converter is equipped with internal balance boosters and additional circuitry for precharge and possibly discharge.

#### REFERENCES

- [1] S. A. Gonzalez, S. A. Verne, and M. I. Valla, *Multilevel Converters for Industrial Applications*. Taylor & Francis Group, 2014.
- [2] Y. Lei, C. Barth, S. Qin, W.-c. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. Pilawa-Podgurski, "A 2 kW, single-phase, 7-level, GaN inverter with an active energy buffer achieving 216 W/in<sup>3</sup> power density and 97.6% peak efficiency," in *Proc. of the IEEE Applied Power Electronics Conf. and Expo. (APEC)*, 2016, pp. 1512–1519.
- [3] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 356–364, 1997.
- [4] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 543–550, 1998.
- [5] R. Wilkinson, T. Meynard, and H. du Mouton, "Natural balance of multicell converters: The general case," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1658–1666, 2006.
- [6] S. Thielemans, T. Vyncke, and J. Melkebeek, "Balancing and harmonic analysis of flying capacitor multilevel converters," in *Proc. of the IEEE Convention of Electrical and Electronics Engineers in Israel*, 2008, pp. 609–613.
- [7] A. Ruderman and B. Reznikov, "Simple time domain averaging methodology for flying capacitor converter voltage balancing dynamics analysis," in *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, 2010, pp. 1064–1069.
- [8] A. Ruderman, B. Reznikov, and M. Margaliot, "Simple analysis of a flying capacitor converter voltage balance dynamics for DC modulation," in *Proc. of the IEEE Power Electronics and Motion Control Conf. (EPE-PEMC)*, 2008, pp. 260–267.
- [9] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Five-level H-bridge flying capacitor converter voltage balance dynamics analysis," in *Proc. of the IEEE International Symposium on Industrial Electronics (ISIE)*, 2010, pp. 826–831.
- [10] S. Thielemans, A. Ruderman, and J. Melkebeek, "Self-precharge in single-leg flying capacitor converters," in *Proc. of the Annual IEEE Industrial Electronics Conf. (IECON)*, 2009, pp. 812–817.
- [11] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, 2001.
- [12] M. Khazraei, H. Sepahvand, K. Corzine, and M. Ferdowsi, "A generalized capacitor voltage balancing scheme for flying capacitor multilevel converters," in *Proc. of the IEEE Applied Power Electronics Conf. and Expo. (APEC)*, 2010, pp. 58–62.
- [13] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 178–185, 2007.
- [14] B. P. McGrath, G. Gateau, T. Meynard, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," in *Proc. of the IEEE Power Electronics Specialists Conf. (PESC)*, 2005, pp. 1671–1677.
- [15] H. Obara and Y. Sato, "Development of high power density flying capacitor multi-level converters with balanced capacitor voltage," in *Proc. of the IEEE Energy Conversion Congress and Expo. (ECCE USA)*, 2012, pp. 330–336.
- [16] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five-level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658–1667, 2012.
- [17] H. Sepahvand, M. Khazraei, K. A. Corzine, and M. Ferdowsi, "Start-up procedure and switching loss reduction for a single-phase flying capacitor active rectifier," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3699–3710, 2013.
- [18] J. van der Merwe, H. du T. Mouton, and S. Thielemans, "Calculating boundaries for the natural voltage balancing time-constant of the constant duty cycle single leg flying capacitor converter," *International Journal for Computation and Mathematics in Electrical and Electronic Engineering (COMPEL)*, vol. 31, no. 6, pp. 1603–1624, 2012.
- [19] T. Meynard, *Analysis and Design of Multicell DCDC Converters Using Vectorized Models*. John Wiley & Sons, 2015.
- [20] A. Ruderman and B. Reznikov, "Five-level single-leg flying capacitor converter voltage balance dynamics analysis," in *Proc. of the IEEE Industrial Electronics Conf.*, 2009, pp. 486–491.
- [21] "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," *IEEE Std. 1547-2003*, pp. 1–28, 2003.
- [22] C. A. Teixeira, D. G. Holmes, and B. P. McGrath, "Single-phase semi-bridge five-level flying-capacitor rectifier," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5, pp. 2158–2166, 2013.
- [23] M. Khazraei, H. Sepahvand, M. Ferdowsi, and K. A. Corzine, "Hysteresis-based control of a single-phase multilevel flying capacitor active rectifier," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 154–164, 2013.