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24 August 2022

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Abstract: This paper addresses the development of accurate and efficient behavioral models of digital integrated circuit input and output ports for signal integrity simulations and timing analyses. The modeling process is described and applied to the characterization of actual devices.

1 Introduction

The development of behavioral models of digital Integrated Circuits (IC) ports is a key resource for the assessment of signal integrity (SI) effects on fast digital circuits. Such an assessment is mainly achieved by simulating the evolution of signals on interconnects and requires accurate and efficient models of IC ports. Behavioral models, that are simplified models obtained from waveforms computed or measured at devices ports, match this requirement.

In this paper we address the development of behavioral models via parametric representations, that offer interesting features. The estimation of parametric models can take into account all the physical effects relating port voltage and current, since their structure is selected by the estimation proces itself. Besides, the accuracy of such models is also weakly influenced by the external loads they are connected to.

The modeling process is described and applied to the characterization of both input and output ports of commercial IBM devices.

2 Drivers models

The modeling of a digital IC output port (*driver* hereafter) via a parametric model amounts to relate its port voltage and current by a suitable parametric equation. The equation must be nonstationary in order to take into account port logic state and state transitions. Various model representations are possible for such nonlinear time-dependent devices. After extensive search [1, 2, 6, 7], we recognized that the following discrete-time Piece-Wise (PW) representation provides an accurate model for drivers:

$$i(k) = w_1(k)f_1(k) + w_2(k)f_2(k) \qquad (1)$$

The above expression assumes that the port current i is obtained as a combination of two submodels f_1 and f_2, reproducing the behavior of the driver in the High and Low output states, respectively. The combination coefficients are w_1 and w_2, that take into account driver state switchings. Submodels f_1 and f_2 are nonlinear dynamic parametric models, based on the theory of Radial Basis Functions (RBF) [3]. They consist of sums of gaussian basis functions depending on the past r samples of the port current i (r is called the dynamic order of the model), and the present and past samples of the port voltage v. Each basis function is properly centered in the parameters space and depends on the distance from centers.

The estimation of model (1) is carried out by a simple procedure [2] and is done by matching the output of the model to the output of actual drivers for suitable input signals. Port voltage and current waveforms involved in the estimation of parametric models are named *identification signals*. Submodels f_1 and f_2 are obtained via effective estimation algorithms [4, 5] whereas the weight coefficients w_1 and w_2 are estimated by linear inversion of (1) where v and i are replaced by sampled waveforms recorded on two different loads (*identification loads*) during the Up (Low-to-High) and the Down (High-to-Low) state switchings.

This modeling process has been developed and validated by applying it to the characterization of several virtual and actual devices [1, 2]. Besides, It has also been succesfully applied to the characterization of commercial IBM drivers [6].

The last part of the process is the implementation of the estimated PW-RBF models (1) in a circuit simulation environment, like SPICE, by means of an equivalent circuit. This is achieved by converting

equation (1) into a continuous time state-space model and then by synthesizing it via RC circuits with voltage controlled sources.

In the following, we show two examples highlighting the accuracy and efficiency of PW-RBF models, estimated from detailed transistor-level models (*reference* models hereafter) of high speed IBM drivers.

Example 1: The Modeled Driver (MD1) is an IBM CMOS driver (power supply: $V_{ss} = 0$ V, $V_{dd} = 1.65$ V) used in IBM mainframe products. The identification loads for the estimation process are a 100Ω and a 50Ω resistor in series with a V_{dd} battery. The PW-RBF model estimated for MD1 has dynamic order $r = 1$ and a number of basis functions 9 for both submodels f_1 and f_2.

As a validation test, Figure 1 compares the responses of MD1 and of its PW-RBF model when they apply a 4 ns pulse (bit pattern "010") to three ideal transmission lines, with different characteristic impedance and time delay values, terminated by a 1 pF capacitor. The accuracy of the PW-RBF model in reproducing the reference behavior of MD1 for generic dynamic loads can be clearly appreciated.

Example 2: The Modeled Driver (MD2) is another IBM CMOS driver ($V_{ss} = 0$ V, $V_{dd} = 1.5$ V) used in IBM mainframe products and the identification loads are the same as those used in the Example 1. The PW-RBF model estimated for MD2 has dynamic order $r = 1$, a number of nine basis functions for submodel f_1 and seven for submodel f_2.

Figure 1: Far-end voltage waveform $v_{fe}(t)$ on three ideal transmission lines driven by MD1 (solid, reference curves) and by its PW-RBF model (dotted). Panel *(a)* refers to a line with $Z_c = 50 \Omega$, $T_d = 0.5$ ns; *(b)* $Z_c = 100 \Omega$, $T_d = 0.5$ ns; *(c)* $Z_c = 100 \Omega$, $T_d = 40$ ps.

Figure 2 shows the validation setup devised for this second example. It is based on a three-conductor lossy on-MCM interconnect (2 lands + reference plane) driven by two MD2 devices and terminated by 1 pF capacitors. The device on land #1 is active and sends a train pulse (bit pattern "011011101010000"), whereas the device on land #2 remains quiet in the Low logic state (bit pattern "000000000000000").
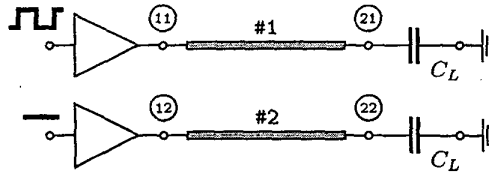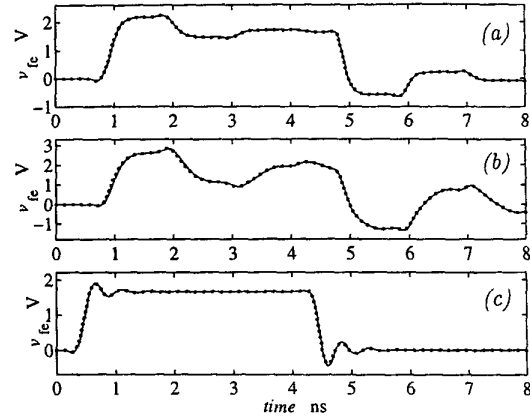

Figure 2: Coupled-line structure for the realistic test case of Example 2 (length 0.1 m, $l_{11} = l_{22} = 0.441 \mu H/m$, $l_{12} = l_{21} = 14.4 nH/m$, $c_{11} = c_{22} = 144 pF/m$, $c_{12} = c_{21} = -1.38 pF/m$, dc resistance $24.4 \Omega/m$, skin effect coefficient $11.7 \, 10^{-6} \, \Omega s^{-1/2}/m$, dielectric loss factor $2.5 \, 10^{-3}$, $C_L = 1 pF$)
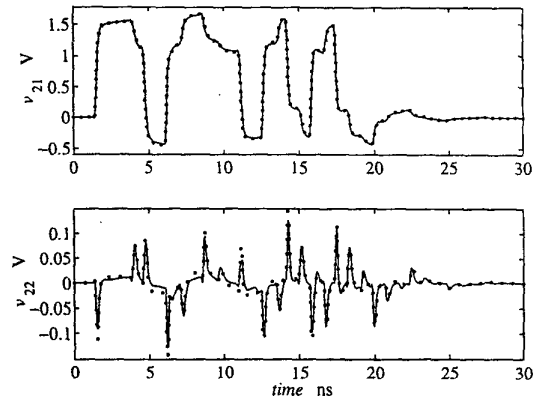

Figure 3: Far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on the active and quiet line of the structure of Fig. 2. Solid lines: reference responses; dotted lines: approximate responses obtained by PW-RBF models.

Figure 3 shows the far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on both the active and the quiet land of the setup. This comparison highlights that also the far-end crosstalk signal, which is a sensitive quantity, can be carefully predicted by using PW-RBF models.

The estimation of PW-RBF models is rather fast and their numerical efficiency is fairly good. The CPU time needed to estimate the models of the above examples is some ten seconds on a Pentium-II PC @ 350 MHz. PW-RBF models turn out to be more than 20 times faster than transistor-level models and lead to timing errors that are always less than $5 \div 20$ ps, being $T_s = 5 \div 10$ ps the sampling time used in the estimation process. The above timing errors are obtained by computing the maximum delay between the crossing of a suitable voltage treshold of PW-RBF and reference transistor-level models responses.

3 Receivers models

The development of behavioral models for input ports (receivers in the following) is rather straightforward because, in contrast with output ports, their operation is hardly influenced by the IC internal states.

For input port voltages in the range of power supply, receivers exhibit a mainly linear capacitive behavior, whereas outside such range their behavior is dominated by the nonlinear protection circuits. This property and the physical structure of receivers suggest the following model representation

$$i(k) = i_l(k) + i_{nl}(k) \qquad (2)$$

where the current i flowing into the input pin is split into two contributions. The first part, i_l, is described by a linear AutoRegression with eXtra input (ARX) parametric model [8] defined by the linear combination of the present sample of the port voltage v, and the past r samples of v and i, being r the dynamic order of the model. Submodel i_l is obtained by standard estimation routines [9, 5] and suitable identification signals, obtained by driving the receiver with a voltage multilevel waveform spanning the range of the power supply.

The second part, i_{nl}, is a nonlinear model that accounts for the nonlinear behavior of receivers in the voltage range where the effects of protection circuits are dominant. We found that a simple shunt connection of two identical circuits, each consisting of the series connection of an inductor and a nonlinear resistor, leads to models performing with a sufficient accuracy. In this case, i_{nl} is defined by the following equation

$$i_{nl} = \begin{cases} g(v - L_1 \frac{d}{dt} i_{nl}), & i_{nl} > 0 \\ g(v - L_2 \frac{d}{dt} i_{nl}), & i_{nl} < 0 \end{cases} \qquad (3)$$

where g is the $i - v$ static characteristic of the receiver and L_1 and L_2 are the series inductors taking into account the dynamic behavior of receiver in the nonlinear regions where the protection circuits dominate. The values of the series inductors L_1 and L_2 are obtained by driving the receiver with a small signal voltage step for $v > V_{dd}$ and $v < V_{ss}$, respectively, and by solving a linear least squares problem. This is done by minimizing the error between the reference response of the receiver and the model response.
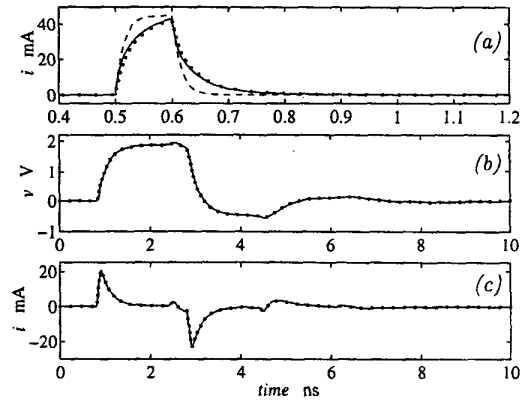
It is ought to remark that a simple circuit model

Figure 4: Results of validation tests for receivers (see text for details). Panel (a): model responses for a receiver driven directly by an equivalent source. Panel (b) and (c): model responses for a receiver driven through a transmission line. Solid lines: reference responses; dotted lines: higher-order model responses; dashed line: $i - v$ model response.

(referred to as $i - v$ model below) consisting of a shunt connection between a capacitor C_{eq} and a nonlinear resistor belongs to the class defined by (2). In fact, a capacitor and a nonlinear resistor are the simplest i_l and i_{nl} submodels taking into account both the static and dynamic behavior of receivers. However, it can be verified that a capacitor gives only a rough approximation of the quasi-linear behavior of the port, having order $r = 1$. A better accuracy can be achieved by using submodels i_l of dynamic order $r = 3 \div 7$ (higher-order models). Also, the choice of equation (3) for i_{nl} arises from qualitative analyses of the behavior of modeled receivers. If necessary, the accuracy of the proposed model can be further improved by using nonlinear parametric models.

Finally, the estimated models (2) are turned into equivalent circuits and implemented as SPICE-like subcircuits by following the same procedure described in Section 2. An example highlighting the accuracy of the above models, estimated from detailed transistor-level models of high speed IBM receivers, follows.

Example 3: The Modeled Receiver (MR) is an IBM receiver ($V_{ss} = 0\,\text{V}$, $V_{dd} = 1.5\,\text{V}$) used in the same series of IBM products as those of the previous examples. For such a MR we estimated two different models (2): a simple $i-v$ model ($r = 1$, $C_{\text{eq}} = 3\,\text{pF}$) and an higher order model ($r = 5$, $L_1 \simeq 8.39\,\text{nH}$, $L_2 \simeq 7.27\,\text{nH}$).

As a first validation test, we consider a setup consisting of the MR driven by the series connection of a $5\,\Omega$ resistor and an ideal voltage source producing a step (amplitude=1 V, transition time=100 ps). For such a setup, Fig. 4, panel (a), shows the comparison between the MR $i(t)$ reference response and estimated models responses. From the previous curves we can appreciate the improvement on the accuracy of higher-order models.

As a second and more realistic validation test, we consider a 10 cm long lossy transmission line loaded by the MR and driven by the series connection of a $30\,\Omega$ resistor and an ideal voltage source producing a 1 ns pulse (amplitude=V_{dd}, transition time=100 ps). Fig. 4, panel (b) and (c), shows the MR $v(t)$ and $i(t)$ reference responses and the responses generated by the higher-order model.

Finally, we assessed the performances of the estimated models (2) ($i.e.$, model generation time, timing errors, accuracy, efficiency), finding results similar to those obtained in Section 2.

4 Conclusion

This paper addresses the development of accurate and efficient behavioral models of both input and output ports of digital ICs. The proposed approach is based on the estimation of nonlinear parametric models from port current and voltage waveforms. The obtained models perform well on high speed actual devices. Their cost of generation is low and they can replace transistor-level models for the simulation of realistic SI problems without appreciable loss of accuracy.

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