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Behavioral Modeling of Switched-Capacitor Sigma–Delta Modulators

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***Abstract*—This paper presents a complete set of blocks implemented in the popular MATLAB SIMULINK environment, which allows designers to perform time-domain behavioral simulations of switched-capacitor (SC) sigma–delta ($\Sigma\Delta$) modulators. The proposed set of blocks takes into account most of the SC $\Sigma\Delta$ modulator nonidealities, such as sampling jitter, kT/C noise, and operational amplifier parameters (white noise, finite dc gain, finite bandwidth, slew rate and saturation voltages). For each block, a description of the considered effect as well as all of the implementative details are provided. The proposed simulation environment is validated by comparing the simulated behavior with the experimental results obtained from two actual circuits, namely a second-order low-pass and a sixth-order bandpass SC $\Sigma\Delta$ modulator.**

***Index Terms*—Analog–digital conversion, discrete-time systems, sigma–delta ($\Sigma\Delta$) modulation.**

I. Introduction

SIGMA–DELTA ($\Sigma\Delta$) modulators are the most suitable A/D converter topologies for digitizing with high-resolution analog signals characterized by a bandwidth (BW) much smaller than the sampling frequency (f_s). With these architectures, a resolution up to 19–21 bits can be reached using standard IC technologies [2]–[4]. These features make the $\Sigma\Delta$ solutions very attractive for a number of applications. For instance, they have gained increasing popularity in audio applications (where a low-pass signal BW requires a resolution up to 20 bit), in receivers for communication systems (where the modulated signal can be digitized at the interface with a bandpass $\Sigma\Delta$ modulator), in sensor interface circuits and in measurement systems. Key advantages of $\Sigma\Delta$ modulators are their inherent linearity and their robust analog implementation. Moreover, by trading accuracy with speed, $\Sigma\Delta$ modulators allow high performance to be achieved with low sensitivity to analog component imperfections and without requiring component trimming.

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$\Sigma\Delta$ modulators can be implemented either with continuous-time or with sampled-data techniques. The most popular approach is based on a sampled-data solution with switched-capacitor (SC) implementation. In fact, SC $\Sigma\Delta$ modulators can be efficiently realized in standard CMOS technology and included in complete mixed-signal systems without any performance degradation. For this reason, we will focus on the case of SC $\Sigma\Delta$ modulators in this paper.

In the design of a high-performance SC $\Sigma\Delta$ modulator, two main issues have to be addressed by the designers.

1) Which is the best architecture to fulfill the application requirements?
2) For a given architecture, which are the requirements for the building blocks?

In practice, a significant problem in the design of $\Sigma\Delta$ modulators is the estimation of their performance, since they are mixed-signal nonlinear circuits. Due to the inherent nonlinearity of the $\Sigma\Delta$ modulator loop the optimization of the performance has to be carried out with behavioral time-domain simulations. This situation is quite difficult to handle when a high-performance system is considered. Indeed, to satisfy high-performance requirements, accurate simulations of a number of nonidealities and, eventually, the comparison of the performance of different architectures are needed in order to choose the best solution. In addition to this, in the design of high-resolution SC $\Sigma\Delta$ modulators, a large set of parameters, including the performance of the building blocks embedded in the adopted structure, has to be optimized in order to achieve the desired signal-to-noise ratio (SNR) or signal-to-noise and distortion ratio (SNDR).[1]

In principle, various approaches for transient simulation which include device models (such as SPICE), finite-difference equations (such as SWITCAP), custom numerical models (typically in C++ language), etc., are already available. However, in different measures, all of them exhibit some disadvantages. Table I [5] classifies the different tools in terms of three main characteristics: accuracy, speed, and flexibility (intended as modeling capability plus reusability). Moreover, the post-processing algorithms for the evaluation of modulator performances are other qualifying features for the various tools.

SPICE is a conventional electrical simulator and, despite its precision, it is not suitable for the analysis of $\Sigma\Delta$ modulators be-

[1]Notice that the two issues mentioned above are strictly correlated because architectures which achieve optimal results with ideal block models are not necessarily the best solution in the presence of building blocks with degraded performances. Therefore, the choice of the architecture and design of the building blocks require typically concurrent optimization processes.

TABLE I
COMPARISON AMONG THE DIFFERENT TOOLS FOR THE SIMULATION OF $\Sigma\Delta$ MODULATOR

Approach	*Accuracy*	*Speed*	*Flexibility*
Device models	☺	☹	😐
Custom models (C++)	😐	☺	☹
Finite-difference equations	😐	☺	😐
Circuit-based macromodel	☺	☹	☺
Time-domain macromodel	☺	😐	☹
Table-lookup model	😐	😐	☹
Behavioral models	☺	😐	☹
Proposed solution	☺	☺	☺

cause of the extremely long simulation time. Custom models are just suited for a specific structure and cannot be easily adapted to a different modulator topology (especially regarding exotic architectures). This situation is quite difficult to handle when accurate simulations of a number of nonidealities and, eventually, the performance comparison between different architectures are needed.

The circuit-based macro model essentially represents an equivalent circuit build up with a minimum set of passive and active devices already available in electrical simulators like SPICE. Modulator building blocks are described by means of simplified circuits and specifications are used as model parameters. Nonidealities can be introduced in the models. This approach guarantees a good degree of accuracy and reusability, but the speed improvement with respect to device level simulation is poor. Time-domain macro models are based on a set of equations describing the transient behavior of a specific circuit. The specifications of the circuit represent the model parameters. Again this approach is not flexible at all, but allows us to introduce dynamic nonlinearities.

The simulators based on finite-difference equations are programs usually written in C language that exploit the z-domain description of the transfer function of sample-data networks. They can be general-purpose like SWITCAP (or its evolution AWEswit [6]) or especially devoted to oversampled modulators like MIDAS. They achieve an excellent speed of simulation, but the nonidealities modeling capabilities are poor. Moreover, both simulators operate on netlists and offer a not user-friendly human interface.

Table-lookup models [7] use a two-step procedure. First, tables of input and output points are extracted for the $\Sigma\Delta$ modulator sub-blocks by using conventional electrical simulators. Then, the obtained tables are utilized instead of the original circuit for global transients simulations. However, this approach seems not to guarantee high accuracy (< 80 dB) in SNR estimation (static errors only) and tables are not reusable. The speed of this approach depends on the size of the tables.

Further behavioral simulator with a more custom approach like simulators or those reported in [8] and [9], represent a compromise between finite-difference equations simulators and behavioral model simulators achieving intermediate performances.

In this paper, a complete set of blocks to be used in the very popular MATLAB SIMULINK [10] environment is proposed. This toolbox allows us to perform exhaustive time-domain behavioral simulations of $\Sigma\Delta$ modulators. The most significant nonidealities are modeled and building blocks for modeling sampling jitter, kT/C noise, and operational amplifier parameters (white noise, finite dc gain, finite BW, slew rate (SR) and saturation voltages) are proposed.

It is important to point out that the proposed building blocks allow us to achieve a good estimation of the SC $\Sigma\Delta$ modulator performance. The proposed models, however, are not perfect, since they are based on a number of hypothesis which are typically, but not always, verified in $\Sigma\Delta$ modulators. In the development of this particular set of blocks, taking into account the needs of the $\Sigma\Delta$ modulator designers, the basic tradeoff between accuracy and simplicity of the models has been optimized in terms of model simplicity and hence, efficiency.

The proposed behavioral simulation toolbox (available on the worldwide web [1]), together with the utilities distributed in [11], has been used for designing, simulating, and verifying the performance of two actual $\Sigma\Delta$ modulators: a second-order 15-bit low-pass and a sixth-order 12-bit bandpass modulator. The simulated performance of these circuits is compared with experimental results in order to validate the proposed simulation environment.

This paper is organized as follows. In Section II, the major nonidealities of SC $\Sigma\Delta$ modulators are described. The correspondent behavioral model blocks are then presented in Section III– V. Finally, in Section VI, we report the results obtained with the proposed blocks for a second-order low-pass and for a sixth-order bandpass $\Sigma\Delta$ modulator.

II. $\Sigma\Delta$ MODULATOR NONIDEALITIES

The block diagram of a first-order SC $\Sigma\Delta$ modulator is shown in Fig. 1. This circuit will be used in this section, to introduce the nonidealities which affect the performance of SC $\Sigma\Delta$ modulators of any order. The modulator consists of an input sampler, a

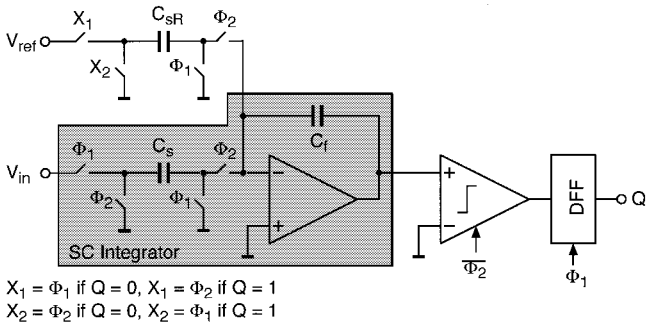

Fig. 1. Schematic of an SC first-order $\Sigma\Delta$ modulator.

SC integrator, a quantizer and a feedback digital-to-analog converter (DAC). The main nonidealities of this circuit which are considered in this paper are the following:

1) clock jitter at the input sampler;
2) switch thermal noise in the SC structure;
3) operational amplifier noise;
4) operational amplifier finite gain;
5) operational amplifier BW;
6) operational amplifier SR;
7) operational amplifier saturation voltages.

The use of the SC technique for the implementation means that all the blocks in a SC $\Sigma\Delta$ modulator are properly synchronized. Using the building blocks presented in the following sections, the simulation of any SC $\Sigma\Delta$ modulator is possible.

The basic concept of the proposed simulation environment is the evaluation of the output samples in the time domain. The nonidealities listed above produce a deviation of the output samples from their ideal values. The overall performance of the $\Sigma\Delta$ modulator is then evaluated in the frequency domain after proper fast Fourier transform (FFT) [12] of the output samples (see the Appendix).

III. Clock Jitter

The operation of an SC circuit depends on complete charge transfers during each of the clock phases [13]. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal. This also means that the effect of clock jitter on a $\Sigma\Delta$ modulator is independent of the structure or order of the modulator.

Clock jitter results in a nonuniform sampling time sequence, and produces an error which increases the total error power at the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the modulator input signal. The error introduced when a sinusoidal signal $x(t)$ with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given by

$$x(t+\delta) - x(t) \approx 2\pi f_{\text{in}} \delta A \cos(2\pi f_{\text{in}} t) = \delta \frac{d}{dt} x(t). \quad (1)$$

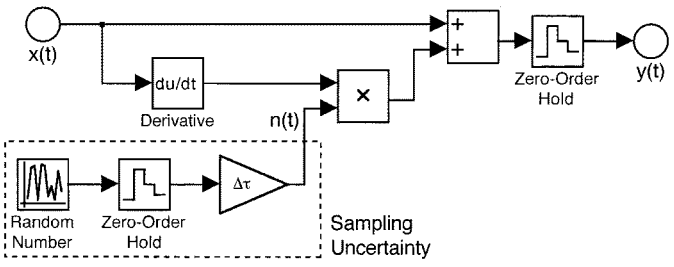

Fig. 2. Modeling a random sampling jitter.

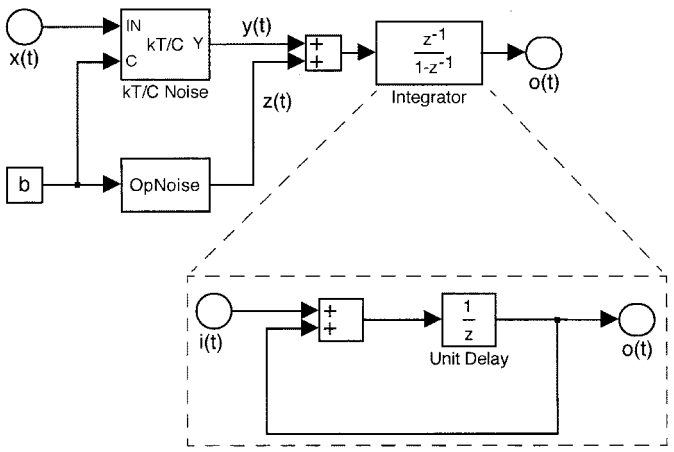

Fig. 3. Model of a "noisy" integrator.

This effect can be simulated at behavioral level by using the model shown in Fig. 2, which implements (1). The input signal $x(t)$ and its derivative (du/dt) are continuous-time signals. They are sampled with sampling period T_s by a zero-order hold. In the model, we assumed that the sampling uncertainty δ is a Gaussian random process $n(t)$ with standard deviation $\Delta\tau$. The signal $n(t)$ is implemented starting from a sequence of random numbers with Gaussian distribution, zero mean, and unity standard deviation (available in SIMULINK). Other possible distributions can be considered and consequently implemented in this block. Whether oversampling is helpful in reducing the error introduced by the jitter depends on the nature of the jitter. Since we assume the jitter white, the resultant error has uniform power-spectral density (PSD) from 0 to $f_s/2$, with a total power of $(2\pi f_{\text{in}} \Delta\tau A)^2/2$. In this case, the total error power will be reduced by the oversampling ratio [14].

IV. Thermal and Operational Amplifier Noise

The most important noise sources affecting the operation of an SC $\Sigma\Delta$ modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifiers.

These effects can be successfully simulated at the behavioral level by using the model of a "noisy" integrator shown in Fig. 3, which represents the SC integrator shown in Fig. 1 (a similar model can be used also for resonators). The z-domain transfer function of this integrator $H_I(z)$ is given by

$$H_I(z) = \frac{C_s}{C_f} \frac{z^{-1}}{1 - z^{-1}} = b \frac{z^{-1}}{1 - z^{-1}} \quad (2)$$

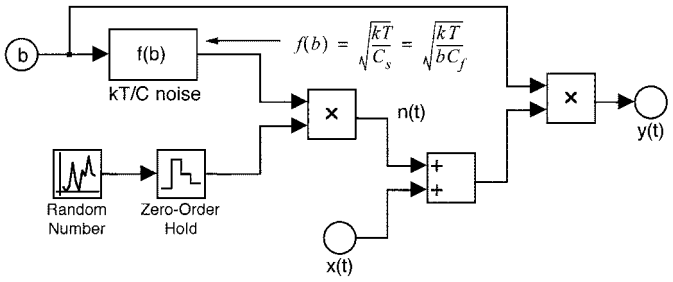

Fig. 4. Modeling switches thermal noise (kT/C block).

where the variable $b = C_s/C_f$ represents the coefficient of the integrator. The input signal $x(t)$ is multiplied by b in the kT/C block.

Each noise source and its relevant model will be described in the following paragraphs.

A. Switches Thermal Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band, limited only by the time constant of the switched capacitors or the BW of the operational amplifiers. Referring to the SC first-order $\Sigma\Delta$ modulator shown in Fig. 1, the sampling capacitor C_s is in series with a switch, with finite resistance R_{on}, that periodically opens, thus sampling a noise voltage onto C_s. The total noise power can be found evaluating the integral [5]

$$e_T^2 = \int_0^\infty \frac{4kTR_{\text{on}}}{1+(2\pi f R_{\text{on}} C_s)^2} df = \frac{kT}{C_s} \tag{3}$$

where k is the Boltzmann's constant, T the absolute temperature, and $4kTR_{\text{on}}$ the noise PSD associated with the switch on-resistance. The switch thermal noise voltage e_T (usually called kT/C noise) is then superimposed to the input voltage $x(t)$ leading to

$$\begin{aligned} y(t) &= [x(t) + e_T(t)]\, b \\ &= \left[x(t) + \sqrt{\frac{kT}{C_s}} n(t)\right] b \\ &= \left[x(t) + \sqrt{\frac{kT}{bC_f}} n(t)\right] b \end{aligned} \tag{4}$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation, while $b = C_s/C_f$ is the coefficient of the integrator. Equation (4) is implemented by the model shown in Fig. 4.

The integrators or resonators of an SC $\Sigma\Delta$ modulator may include more than one SC input branch, each contributing to the total noise power. For example, in the $\Sigma\Delta$ modulator shown in Fig. 1, there are two input branches, one carrying the signal and the other providing the feedback from the modulator output. Each branch has to be modeled with a separate kT/C noise block, including the proper coefficient b (different coefficients can be used in the different branches).

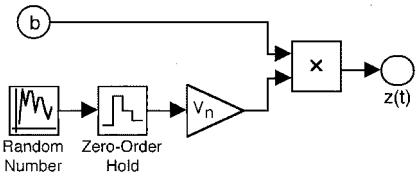

Fig. 5. Operational amplifier noise model (OpNoise block).

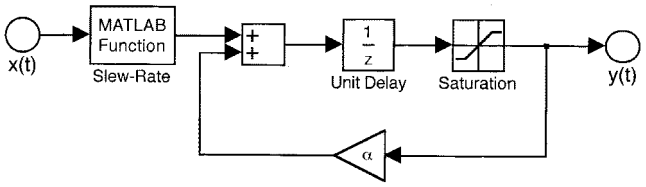

Fig. 6. Real integrator model.

B. Operational Amplifier Noise

Fig. 5 shows the model used to simulate the effect of the operational amplifier noise [15]. Here, V_n represents the total rms noise voltage of the operational amplifier referred to the integrator (or resonator) input. In this model we considered only thermal noise, while flicker $(1/f)$ noise and dc offset are neglected. Indeed, in low-pass $\Sigma\Delta$ modulators, flicker noise and dc offset are typically canceled by means of auto-zero, correlated double sampling, or chopper stabilization techniques, while they are not important in bandpass architectures. The noise power V_n^2 can be evaluated through a transistor-level noise simulation of the complete integrator in the proper clock phase, including feedback, sampling and load capacitors (clock phase Φ_2 in Fig. 1). The resulting output referred noise PSD has to be integrated over the whole frequency spectrum, eventually taking into account the degradation of the thermal noise PSD introduced by the auto-zero or correlated double sampling techniques [16], and then divided by b^2 in order to refer the obtained noise power to the integrator input.

In this model, we consider only the contribution of the sampled noise, assuming that no continuous-time paths are present across the $\Sigma\Delta$ modulator (this is typically the case in SC $\Sigma\Delta$ modulators due to the presence of a latched quantizer).

V. Operational Amplifier Nonidealities

The behavioral model of an ideal integrator with unity coefficient is shown in the inset of Fig. 3. Its transfer function is

$$H(z) = \frac{z^{-1}}{1-z^{-1}}. \tag{5}$$

Analog circuit implementations of the integrator or resonator deviate from this ideal behavior due to several nonideal effects. One of the major causes of performance degradation in SC $\Sigma\Delta$ modulators is the incomplete transfer of charge in the SC integrators. This nonideal effect is a consequence of the operational amplifier nonidealities, namely finite gain and BW, SR, and saturation voltages [17]. These will be considered separately in the following sections. Fig. 6 shows the model of the real integrator including all the nonidealities. A similar model, based on the same building blocks can also be realized for real resonators.

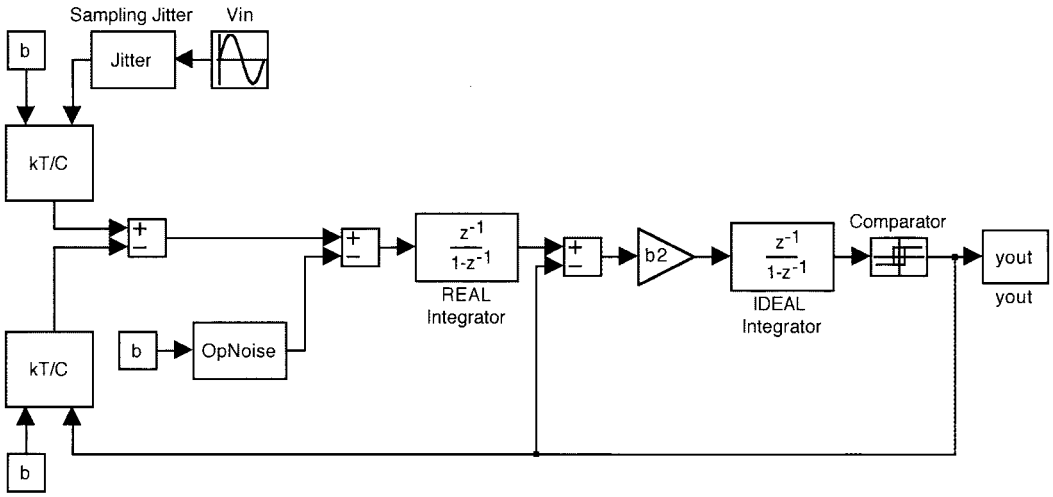

Fig. 7. Low-pass second-order $\Sigma\Delta$ modulator model.

TABLE II
PARAMETERS OF THE SECOND-ORDER LOW-PASS $\Sigma\Delta$ MODULATOR MODEL

Parameter	*Value*
Signal bandwidth	$BW = 100$ Hz
Sampling frequency	$f_s = 50$ kHz
Oversampling ratio	$R = 250$
Number of samples considered	$N = 65536$
Integrator coefficients	$b = b_2 = 0.5$

A. DC Gain

The dc gain of the integrator described by (5) is infinite. In practice, however, the actual gain is limited by circuit constraints and in particular by the operational amplifier open-loop gain A_0. The consequence of this integrator "leakage" is that only a fraction α of the previous output of the integrator is added to each new input sample. The limited dc gain of the integrator increases the in-band noise. The transfer function of the integrator with leakage becomes

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}}. \tag{6}$$

The dc gain of the integrator H_0, therefore, becomes

$$H_0 = H(1) = \frac{1}{1-\alpha}. \tag{7}$$

For example, in the SC integrator shown in Fig. 1, the parameters α and H_0 are approximately given by

$$\alpha \cong \frac{A_0 C_f}{A_0 C_f + C_s + C_{sR}} \text{ and } H_0 = \frac{C_s + C_{sR} + A_0 C_f}{C_s + C_{cR}}. \tag{8}$$

The effect of the finite open-loop dc gain on the integrator coefficient b and hence on the modulator coefficients, is considered together with the operational amplifier finite BW and SR in the next paragraph (because of A_0 the actual integrator coefficient becomes $\alpha\, b$).

B. BW and SR

The finite BW and the SR of the operational amplifier are modeled in Fig. 6 with a building block placed in front of the integrator or the resonator, which implements a MATLAB function. The effect of the finite BW and the SR are related to each other, and may be interpreted as a nonlinear gain [18]. In fact, finite BW and SR in SC circuits lead to a nonideal transient response within each clock cycle, thus producing an incomplete or inaccurate charge transfer to the output at the end of the integration period. Referring to the SC first-order $\Sigma\Delta$ modulator shown in Fig. 1, the evolution of the output node during the nth integration period (when Φ_2 is on, between $nT_s - T_s/2$ and nT_s) is given by

$$v_0(t) = v_0(nT_s - T_s) + \alpha V_s \left(1 - e^{-\frac{t}{\tau}}\right),\ 0 < t < \frac{T_s}{2} \tag{9}$$

where, $V_s = V_{\text{in}}(nT_s - T_s/2)$, α is the integrator leakage (which accounts for the operational amplifier finite gain A_0) and $\tau = 1/(2\pi\text{GBW})$ is the time constant of the integrator and GBW is the unity gain frequency of the integrator loop-gain during the considered clock phase). The slope of this curve reaches its maximum value when $t = 0$, resulting in

$$\left.\frac{d}{dt} v_0(t)\right|_{\max} = \alpha \frac{V_s}{\tau}. \tag{10}$$

We must now consider two separate cases.

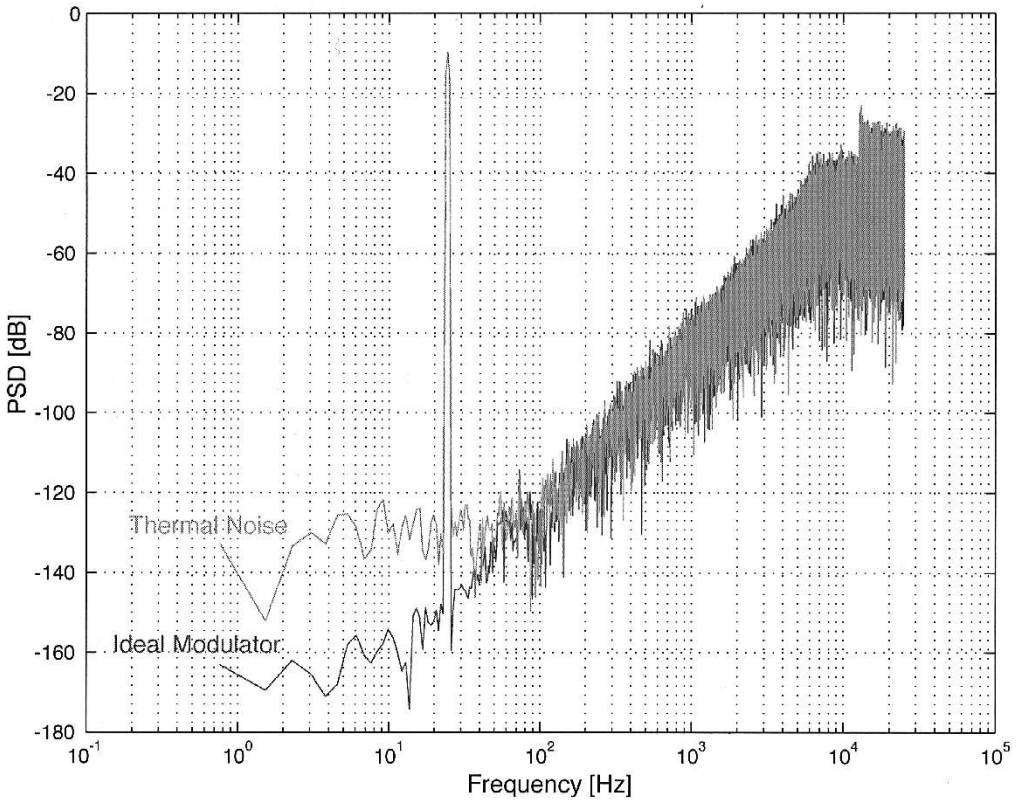

Fig. 8. PSDs of the low-pass second-order ΣΔ modulator output with ($C_s = 2.5$ pF) and without (ideal modulator) the thermal noise model.

1) The value specified by (10) is lower than the operational amplifier SR (taking into account all of the capacitors connected to the operational amplifier output during the considered clock phase). In this case, no SR limitation appears and the evolution of v_0 is described by (9) during the whole clock period (until $t = T_s/2$).
2) The value specified by (10) is larger than SR. In this case, the operational amplifier is in slewing and, therefore, the first part of the transient of $v_0(t < t_0)$ is linear with slope SR. The following equations hold (assuming $t_0 < T_s/2$):

$$t \le t_0 \qquad v_0(t) = v_0(nT_s - t_s) + SRt \tag{11}$$

$$t > t_0 \qquad v_0(t) = v_0(t_0) + (\alpha V_s - SRt_0) \times \left(1 - e^{-\frac{t-t_0}{\tau}}\right). \tag{12}$$

Imposing the condition for the continuity of the derivatives of (11)–(12) in t_0, we obtain

$$t_0 = \frac{\alpha V_s}{SR} - \tau. \tag{13}$$

If $t_0 \ge T_s/2$ Equation(11) holds for the whole clock period.

The MATLAB function in Fig. 6 implements the above equations to calculate the value reached by $v_0(t)$ at time T_s, which will be different from V_s due to the gain, BW and SR limitations of the operational amplifier. The SR and BW limitations produce harmonic distortion reducing the total SNDR of the ΣΔ modulator.

C. Saturation

The dynamic of signals in a ΣΔ modulator is a major concern. It is therefore important to take into account the saturation levels of the operational amplifier used. This can simply be done in SIMULINK using the saturation block inside the feedback loop of the integrator or the resonator, as shown in Fig. 6.

VI. Simulation Results

The proposed set of models has been used in the design of two actual circuits, namely a second-order low-pass ΣΔ modulator and a sixth-order bandpass ΣΔ modulator. Both circuits have been implemented on silicon, thus allowing the behavioral simulation results to be compared with measured data.

A. Low-Pass Second-Order ΣΔ Modulator

To validate the models of the various nonidealities affecting the operation of a low-pass SC ΣΔ modulator, we performed several simulations with SIMULINK on the second-order ΣΔ modulator shown in Fig. 7 [14]. Moreover, we compared the results achieved in simulation with the actual data obtained on an integrated prototype designed for microsensor applications [19]. In the circuit shown in Fig. 7 only the nonidealities of the first integrator are considered, since their effects are not attenuated by the noise shaping. This can be easily verified by using the proposed toolbox. The design parameters used for the simulations and the integrated prototype are summarized in Table II. These values correspond to the typical performance required for sensor applications. In particular, in this case a minimum SNDR of 96 dB (i.e. a resolution of 16 bits) is required.

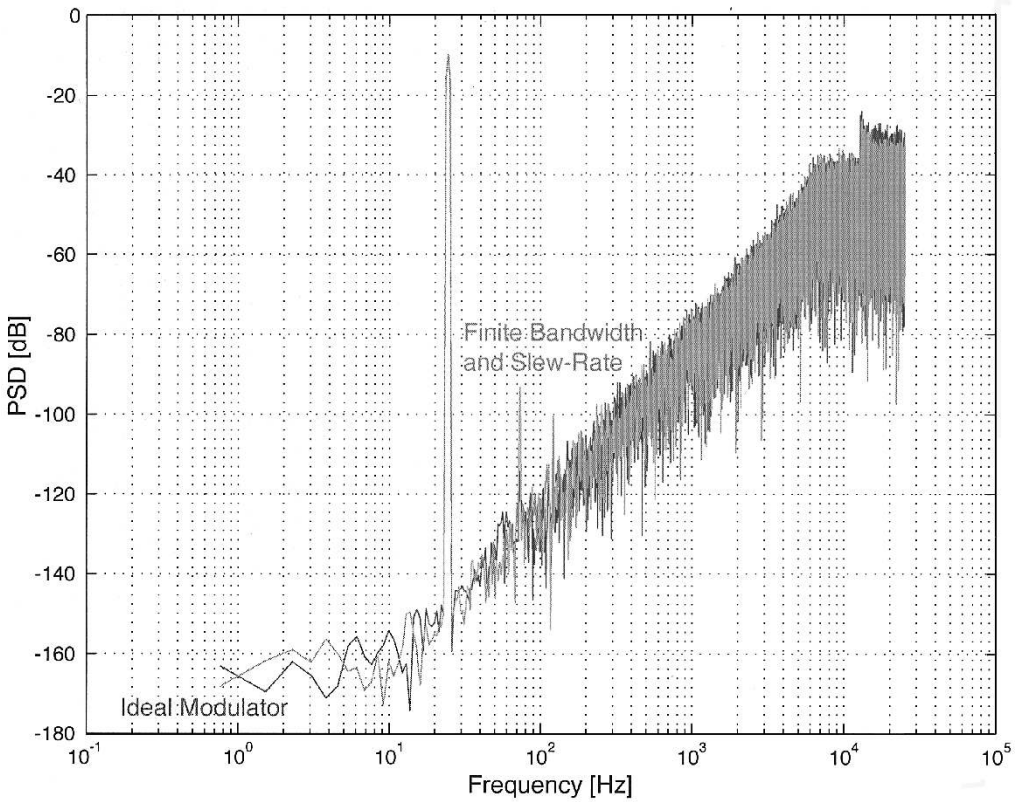

Fig. 9. PSDs of the low-pass second-order $\Sigma\Delta$ modulator output with ($SR = 0.1$ V/μs and GBW$= 100$ kHz) and without (ideal modulator) the operational amplifier finite-BW and SR model.

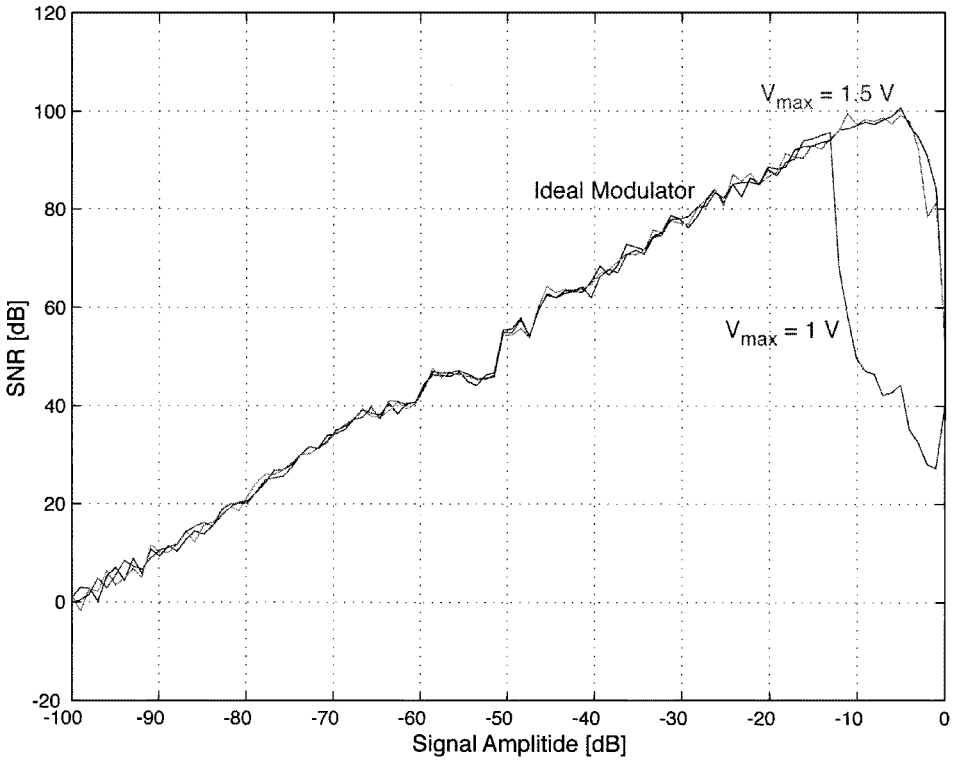

Fig. 10. SNDR of the low-pass second-order $\Sigma\Delta$ modulator as a function of the input signal amplitude for different values of the operational amplifier saturation voltage ($V_{\max}$).

Fig. 8 shows the PSDs of the modulator output bitstream obtained in simulation without (ideal modulator) and with the thermal noise (kT/C) model. The value of the sampling capacitance C_s used in the simulation is 2.5 pF. The

TABLE III
SNDR AND RESOLUTION OF SECOND–ORDER LOW-PASS ΣΔ MODULATOR

ΣΔ Modulator Parameter	*$SNDR_{-6\ dB}$ [dB]*	*Resolution [bits]*
Ideal modulator	99.1	16.17
Sampling jitter ($\Delta\tau$ = 16 ns)	98.8	16.12
Switches (kT/C) noise (C_s = 1.25 pF)	94.0	15.32
Input-referred operational amplifier noise (V_n = 73 μV_{rms})	94.8	15.46
Finite dc gain ($H_0 = 1{\cdot}10^3$)	98.9	16.13
Finite bandwidth (GBW = 11.25 MHz)	99.1	16.17
Slew-rate (SR = 4 V/μs)	99.1	16.17
Saturation voltages (V_{max} = ±1.5 V)	99.1	16.17
Modulator simulated including all of the non-idealities	91.6	14.94
Measurement results on the integrated prototype	90.2	14.69

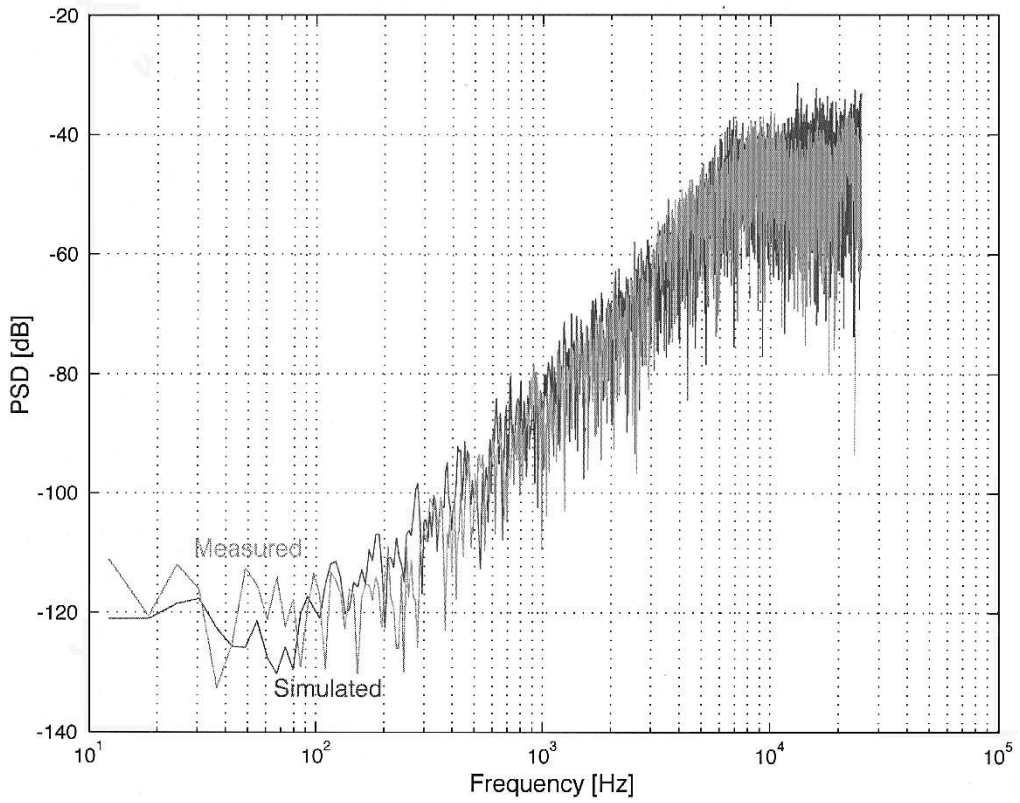

Fig. 11. Noise PSDs of the low-pass second-order ΣΔ modulator resulting from simulation (considering all of the nonidealities) and measurements.

kT/C noise produces a noise floor at low frequencies, as expected.

Likewise, Fig. 9 shows the PSDs of the modulator output obtained in simulation without (ideal modulator) and with the operational amplifier finite BW and SR model. The SR and BW (GBW) values used in the simulation are 0.1 V/μs and 100 kHz, respectively. The finite BW and SR lead to harmonic distortion, thus degrading the SNDR performance of the ΣΔ modulator.

The effect of the operational amplifier saturation voltage ($V_{\max}$) on the performance of the ΣΔ modulator is illustrated in Fig. 10, by plotting the simulated SNDR as a function of the input signal amplitude for different values of $V_{\max}$. The ideal modulator operates properly up to a signal amplitude of −6 dB, with respect to the reference voltage. A saturation voltage $V_{\max} = 1.5$ V with a reference voltage of 1 V does not degrade the performance significantly, while for $V_{\max} = 1.0$ V a significant degradation occurs for signal amplitudes larger than −13 dB, since, due to the saturation of the operational amplifiers, the modulator loop cannot follow the input signal.

TABLE IV
PARAMETERS OF THE SIXTH-ORDER BANDPASS $\Sigma\Delta$ MODULATOR MODEL

Parameter	*Value*
Sampling frequency	$f_s = 42.8$ MHz
Center (intermediate) frequency	$f_0 = 10.7$ MHz
f_s/f_0 ratio	4
Signal bandwidth	$BW = 200$ kHz
Oversampling ratio	$R = 107$
Number of samples considered	$N = 65536$

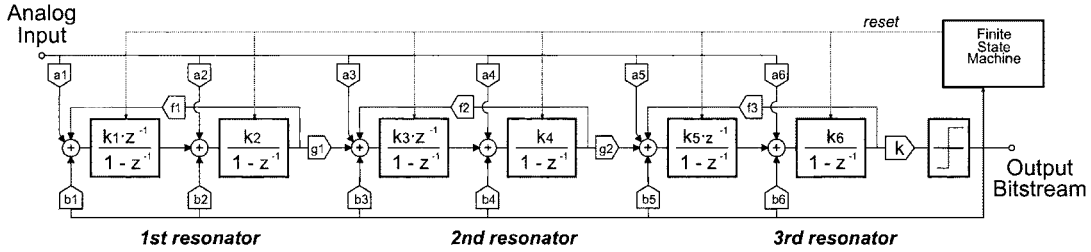

Fig. 12. Block diagram of the sixth-order bandpass $\Sigma\Delta$ modulator.

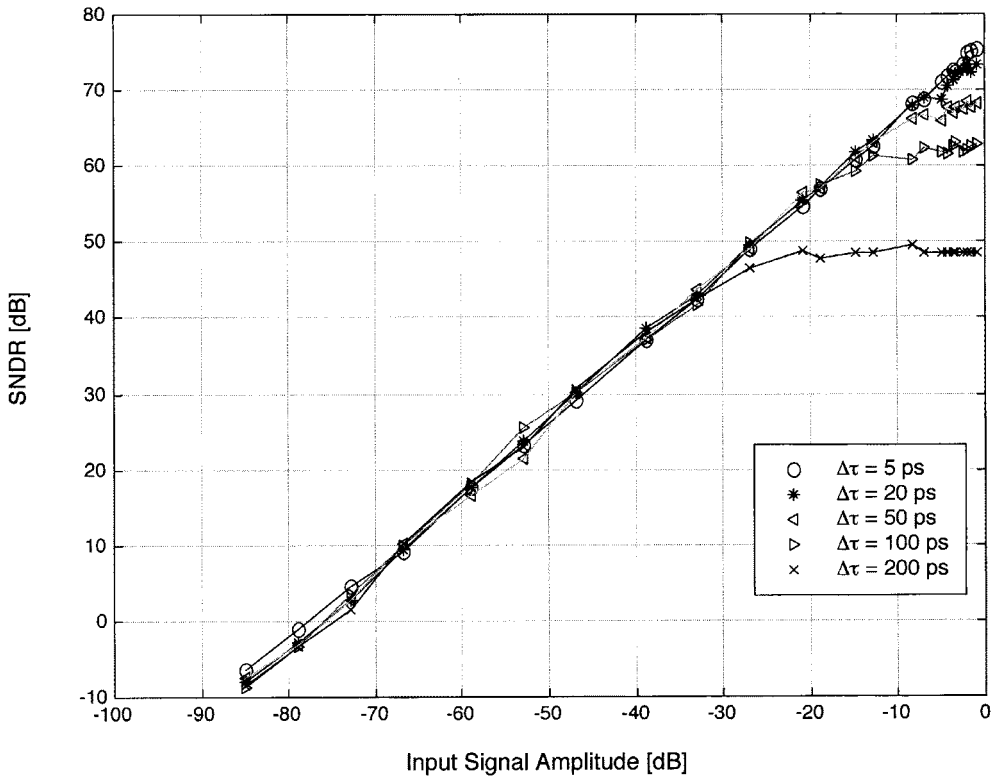

Fig. 13. SNDR as a function input amplitude for different values of the sampling jitter.

The curves shown in Fig. 8–10 show that the nonideal effects resulting from practical circuit limitations, such as thermal noise or operational amplifier nonidealities, increase the in-band noise and distortion, thus becoming potentially a severe limitation to the performance achievable with a given architecture.

Finally, Table III compares the SNDR obtained with an input signal of -6 dB ($\text{SNDR}_{-6\text{ dB}}$) with respect to full-scale and the corresponding equivalent resolution in bits of the ideal modulator, which are the maximum obtainable with the architecture and parameters used, with those achieved with the same architecture when one single nonideality at a time is introduced.

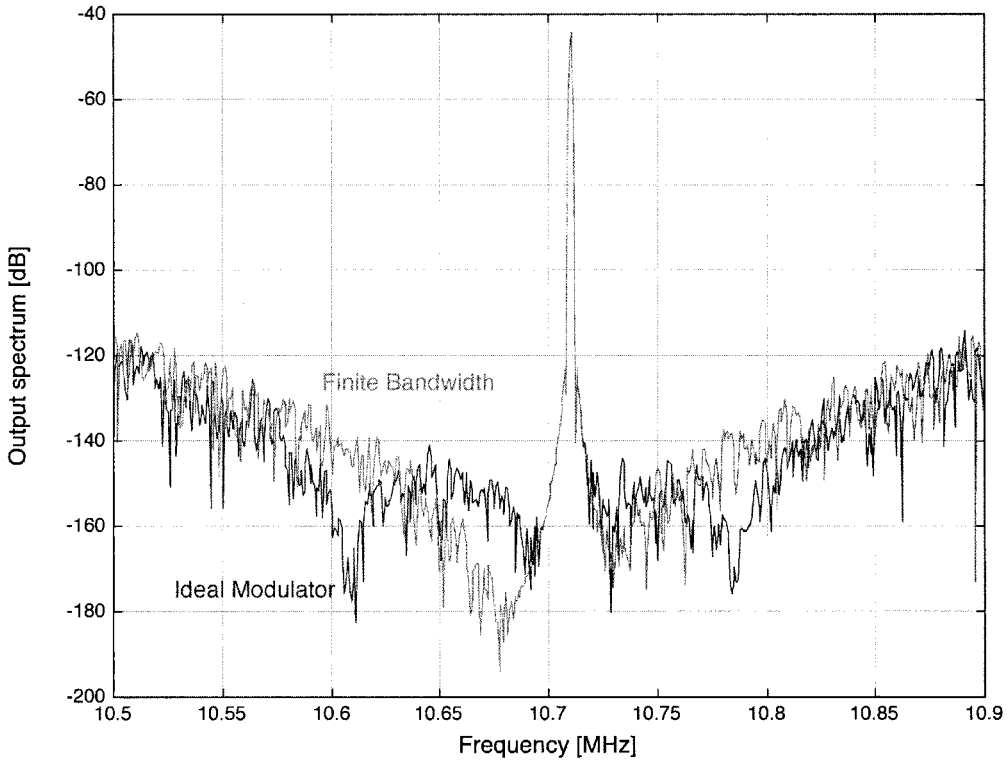

Fig. 14. PSDs of the bandpass sixth-order $\Sigma\Delta$ modulator output showing the effect of the operational amplifier finite BW (GBW$=$ 150 MHz).

TABLE V
DESIGN PARAMETERS USED FOR THE SIXTH-ORDER BANDPASS $\Sigma\Delta$ MODULATOR SIMULATION

$\Sigma\Delta$ Modulator Parameter	*Value*
Sampling jitter ($\Delta\tau$)	20 ps
Finite DC gain (H_0)	10^6
Finite bandwidth (*GBW*)	250 MHz
Slew-rate (*SR*)	300 V/μs
Saturation voltages (V_{max})	$\pm$2 V

Moreover, the overall (SNDR$_{-6\ \mathrm{dB}}$ achieved in simulation considering all of the nonidealities is compared with the measured data obtained on the integrated prototype, fabricated using a double-poly, double-metal 2-μm CMOS technology. The values of the parameters used in the simulations correspond to the design parameters of the chip. Fig. 11 compares the noise PSD obtained in simulation considering all of the nonidealities with the noise PSD resulting from the measured data.

B. Bandpass Sixth-Order $\Sigma\Delta$ Modulator

To validate the models of the various nonidealities affecting the operation of a SC bandpass $\Sigma\Delta$ modulator, we performed several simulations with SIMULINK on the sixth-order modulator shown in Fig. 12 [20], [21]. In this model, the nonidealities of all the integrators were considered. The features of the bandpass modulator and the simulation parameters are reported in Table IV.

Bandpass $\Sigma\Delta$ modulators are more sensitive to sampling jitter than low-pass ones [13]. Fig. 13 shows the simulated SNDR as a function of the input amplitude for different values of the sampling jitter ($\Delta\tau$). The limitation due to the jitter appears mainly in a limitation of the SNDR peak and not in the dynamic range (DR).

Fig. 14 shows the effect of an operational amplifier finite BW (GBW$=$ 150 MHz) on the output PSD of the SC bandpass $\Sigma\Delta$ modulator. In this case, the operational amplifier nonidealities produce a shift of the notch frequencies in the bandpass noise transfer function. However, the application requirements (and hence the decimating filter center frequency) are restricted to a given BW and therefore the shift of the notch frequencies results in an increase of the in-band quantization noise.

Fig. 15 shows the SNDR as a function of the input signal amplitude when an SR (positive and negative) of 135 V/μs and saturation voltages of $\pm$1.1 V are used. The effect of both these nonidealities is a degradation of the SNDR for large input signal amplitude, due to the saturation of the $\Sigma\Delta$ modulator loop.

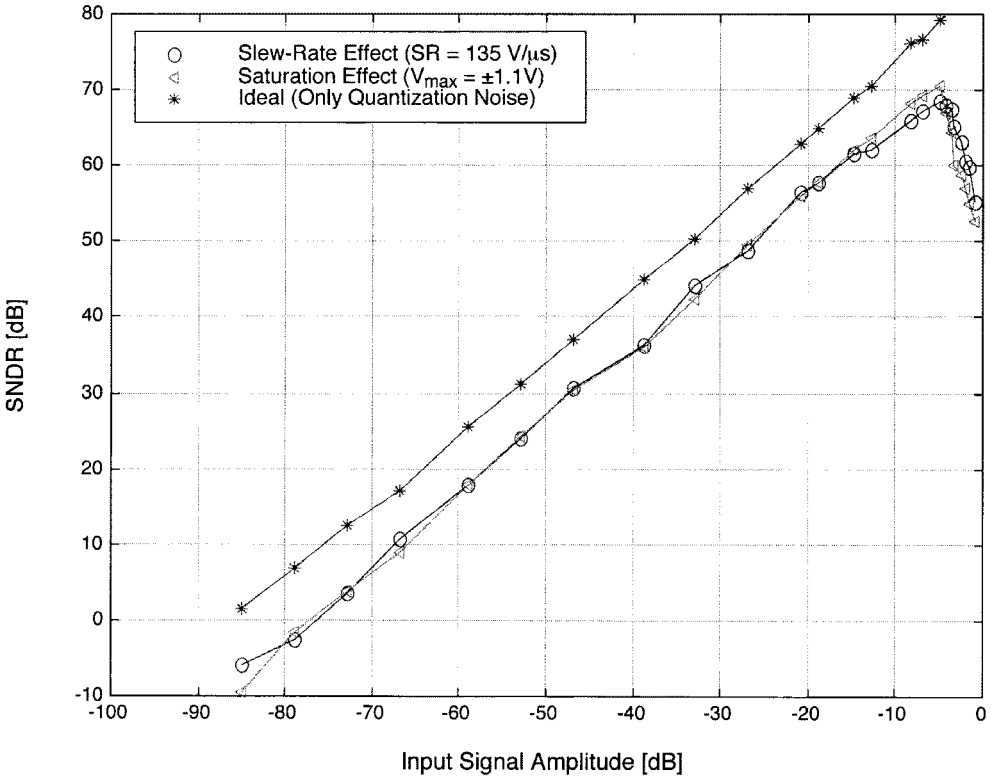

Fig. 15. SNDR as a function input amplitude with operational amplifier SR ($SR = 135$ V/μs) and saturation voltage ($V_{\max} = \pm 1.1$ V).

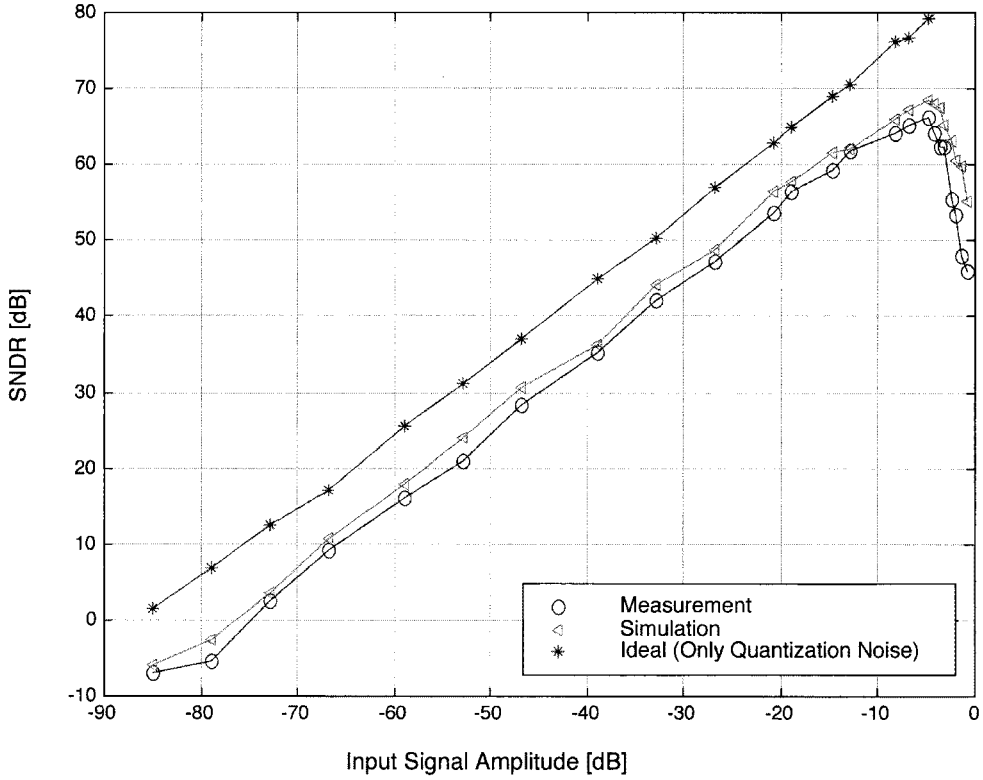

Fig. 16. SNDR as a function of the input signal amplitude of the bandpass sixth-order $\Sigma\Delta$ modulator resulting from simulation (considering all of the nonidealities) and measurements.

The modulator presented in this section has been integrated in a double-poly 0.35-μm CMOS 3.3-V technology with five metal layers. Fig. 16 compares the measured data obtained from the test chip with the simulated behavior obtained including all of the nonidealities with the parameter values reported in Table V, extracted from circuit simulation at the transistor-level.

The measured SNDR as a function of the input signal amplitude is in good agreement with the results of the behavioral simulations. By comparing Fig. 15 and Fig. 16, it appears that operational amplifier SR and saturation are the dominant effects which affect the performance of the modulator.

VII. Conclusion

In this paper, we presented a set of models implemented in the popular MATLAB SIMULINK environment suitable for time-domain behavioral simulations of SC $\Sigma\Delta$ modulators. The proposed set of models takes into account at the behavioral level most of the SC $\Sigma\Delta$ modulator nonidealities, such as sampling jitter, kT/C noise, and operational amplifier parameters (white noise, finite dc-gain, finite BW, SR and saturation voltages), thus allowing us to obtain a good estimation of the $\Sigma\Delta$ modulator performance with a short simulation time (about 4096 simulated samples per second on the second-order $\Sigma\Delta$ modulator, including post-processing of the output data). The proposed simulation environment has been validated by comparing the simulated behavior with the experimental results obtained from both a second-order low-pass and a sixth-order bandpass $\Sigma\Delta$ modulator. The proposed set of models will be expanded in the future to include additional nonidealities, such as the nonlinearity of the sampling switches and of the D/A converter.

Appendix

The SNR and the SNDR of a $\Sigma\Delta$ modulator are defined as

$$\text{SNR} = \frac{P_S}{P_N} \text{ and } \text{SNDR} = \frac{P_S}{P_N + P_D} = \frac{P_S}{P_{N+D}} \qquad (14)$$

respectively, where P_S denotes the signal power, P_N the noise power, and P_D the power of the harmonics of the signal. In an ideal $\Sigma\Delta$ modulator, the SNR is determined only by the quantization noise according to

$$\text{SNR} = \frac{\frac{\Delta^2}{8}}{P_N} = \frac{2^{2N}3(2L+1)M^{2L+1}}{2\pi^{2L}} \qquad (15)$$

where Δ denotes the input range of the $\Sigma\Delta$ modulator, N the number of bits in the quantizer, M the oversampling ratio, and L the order of the $\Sigma\Delta$ modulator.

However, the other noise or distortion sources increase the total noise power of the data converter above the quantization noise level and contribute to both the SNR and the SNDR.

The calculation of the SNR or SNDR of a $\Sigma\Delta$ modulator starting from the raw output data (output samples) is performed in two steps. In the first step, the sinusoidal signal (S) is extracted from the sequence of N_O output data (O_i, at time t_i), typically by computing a discrete Fourier transform (DFT) of O at the signal frequency (f_{in})

$$S(t_j) = \frac{1}{N_O}\left(\sum_{i=1}^{N_O} 2O_iW_i\cos(2\pi f_{\text{in}}t_i)\right)\cos(2\pi f_{\text{in}}t_j) + \frac{1}{N_O}\left(\sum_{i=1}^{N_O} 2O_iW_i\sin(2\pi f_{\text{in}}t_i)\right)\sin(2\pi f_{\text{in}}t_j) \qquad (16)$$

where W_i denotes the desired window for the data (typically the Hanning window). The obtained signal is then subtracted from the raw output signal in the time domain, thus obtaining a signal (N_T) which contains only the noise and distortion contributions. In the second step, we calculate the FFT of S and of $N_T = N + D$, obtaining the spectra of the signal (S_S) and of the noise (S_{N+D}). The same window W_i used for the DFT has to be used also for the FFT. Finally, the signal (P_S) and noise (P_{N+D}) power are calculated by integrating the power spectra

$$P_S = \sum_{i=1}^{N_B} S_S^2(i) \text{ and } P_{N+D} = \sum_{i=1}^{N_B} S_{N+D}^2(i) \qquad (17)$$

where $N_B = N_O BW/f_s$ denotes the number of samples corresponding to the desired BW (baseband, BW) with sampling frequency f_s. The SNR (or SNDR) is then obtained from (14).

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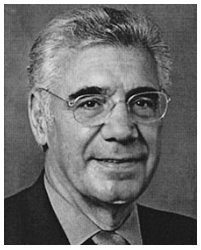

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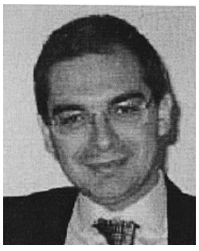

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