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Behaviour of variable speed drives under the influence of voltage sags

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BEHAVIOUR OF VARIABLE SPEED DRIVES UNDER THE INFLUENCE OF VOLTAGE SAGS

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DECLARATION

This is to certify that the work reported in this thesis has been performed by the author unless specified otherwise. No part of it has been submitted as a thesis to any other University.

R. L. Narayanan

dedicated to

My parents, Jai, Ashwin and all my beloved ones

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ABSTRACT

In ac variable speed drives (VSDs) having an uncontrolled rectifier front-end, the effect of voltage sags are mainly observed in the dc bus characteristics. These VSDs are susceptible to nuisance tripping due to dc under-voltage or ac over-current faults which result in production loss, material wastage and require manual interventions in industrial processes. This thesis is aimed at improving the voltage sag ride-through performance of ac VSDs by improving the control algorithm. The proposed strategy recommends maintaining the dc link voltage constant at the nominal value utilising two control modes (a) by recovering the kinetic energy available in the rotating mass at high motor speeds and (b) by recovering the magnetising energy available in the motor winding inductances at low speeds. By combining these two modes, the VSD can be configured to ride-through voltage sags at all speeds. Additional control loops are suggested for this dc link voltage control.

The proposed control strategy was applied on a synchronous reluctance motor (SRM) VSD and on an induction motor (IM) VSD. In the case of an SRM VSD, both modes of this control strategy are found to work satisfactorily and sag ride-through can be achieved at all motor speeds.

In an IM VSD, the first mode of the control strategy, viz. closed loop dc voltage control by recovering the kinetic energy available in the system inertia is found to work satisfactorily and sag ride-through can be achieved at high motor speeds. However, due to the inherent IM characteristics, it was found that the magnetising energy present in an IM is not recoverable. The reasons for this behaviour are analysed and an alternative ride-through scheme is suggested by accommodating the limitations encountered in the case of an IM so that the VSD is able to ride-through voltage sags at low speeds also.

This control strategy can provide a voltage sag ride-through performance at all motor speeds down to standstill. It is also shown that the transition between various control modes during a sag situation can be achieved relatively smoothly.

LIST OF SYMBOLS

C	dc bus capacitor
dt	sampling time
δ	load angle
ε	rotor angle
f	supply frequency
I_l	incoming phase current
I_{in}	capacitor charging current
I_{out}	dc current flowing between capacitor and the inverter
i_{mR}	rotor magnetising current
$\vec{i}_{mR}$	rotor magnetising current vector
$\vec{i}_r$	rotor current space phasor
i_{rd}	rotor current in d-axis
i_{rq}	rotor current in q-axis
$\vec{i}_s$	stator current space phasor
i_{sd}	stator current in d-axis
i_{sq}	stator current in q-axis
J	system inertia
$K_{p,b1}$	Bus Voltage Regulator 1 P gain
$K_{i,b1}$	Bus Voltage Regulator 1 I gain
$K_{p,b2}$	Bus Voltage Regulator 2 P gain
$K_{I,b2}$	Bus Voltage Regulator 2 I gain
$K_{p,sp}$	Speed controller P Gain
$K_{i,sp}$	Speed controller I Gain
L	per phase line inductance
L_m	mutual inductance
L_r	rotor inductance
L_s	stator inductance

L_{sd} stator inductance in d-axis

L_{sq} stator inductance in q-axis

L_t total inductance of the ac machine

$\vec{\lambda}_s$ stator leakage flux space phasor

λ_{sd}, stator flux linkage in d-axis

λ_{sq} stator flux linkage in q-axis

M mutual inductance, and

N_p number of poles

N_{pp} number of pole pairs

p power input to the motor

ρ magnetising (flux) axis position with respect to stator axis

R per phase line resistance

R_r rotor resistance

R_s stator resistance

σ total leakage factor

σ_S stator Leakage factor

σ_r rotor Leakage factor

T_L load torque

T_M motor torque

T_R rotor time constant

T_{ref} torque reference

V_{bus} bus capacitor voltage

V_{ll} line-to-line ac voltage

$\vec{V}_r$ rotor voltage vector

V_{rd} rotor voltage in d-axis

V_{rq} rotor voltage in q-axis

$\vec{V}_s$ stator voltage vector

V_{sd} stator voltage in d-axis

V_{sq} stator voltage in q-axis

ω	motor angular velocity
ω_{cutoff}	cut-off speed for control transition
ω_{mR}	angular velocity of the magnetising vector
ω_{ref}	velocity reference
X_t	total reactance of the ac machine

CHAPTER 1

INTRODUCTION

1.1 VARIABLE SPEED DRIVES IN PROCESS PLANTS

Solid State Variable Speed Drives (VSDs) have already become an integral part of many process plants and their usage is on the rise in industrial, commercial and residential applications [1]. Recent developments in the areas of design of converters, motors and control systems have contributed to a significant increase in the usage of VSDs [2,3]. It is projected that, about 50-60% of the electrical energy generated will be processed by solid state power electronic devices by the year 2010 compared to the present day levels of 10-20% [4].

As the use of power electronics keeps growing, so does the awareness of power quality issues and their impact on the performance of supply sensitive equipment. Power quality disturbances can be of several types such as interruptions, sags and swells, transients, harmonic distortion, voltage fluctuations and noise [5]. They can lead to undesired consequences such as loss of efficiency, loss of plant life, loss of product quality, maloperation and trip-out of sensitive equipment [6]. Of all power quality disturbances, voltage sag seems to be the most common type. A power quality survey conducted by Bell Telephone Laboratories reports that 87.2% of the instances recorded were voltage sags [4]. Voltage sags are reported to be the most frequent cause of disrupted operations of many industrial processes, particularly those using modern electronic equipment which are sensitive to short supply variations [7].

VSDs are one of the most common power electronics based industrial equipment and they are also vulnerable to voltage sags [7-8]. In the presence of voltage sags, VSDs can malfunction or even fail [9,10]. Many industrial processes are controlled by VSDs either individually or in groups depending on the process requirement. A single VSD trip could bring the entire plant to a standstill. An interruption to the process usually

requires manual interventions and would result in enormous wastage of material and restarting delays which lead to severe losses. In order to increase productivity and avoid losses, reliability of VSD operation is of utmost importance in process plants.

This thesis is intended to study the VSD behaviour during voltage sags and enhance the sag ride-through performance.

In this chapter, the definition of voltage sags and their causes will be discussed. The various classifications of sags experienced by VSDs will be presented and will be referred to throughout this thesis. Then the effect of voltage sags on the performance of the VSDs will be discussed. Finally, the conventional mitigation strategies that are available in the literature will be mentioned and their advantages and disadvantages will be analysed.

1.2 VOLTAGE SAGS AND THEIR CAUSES

Voltage sag is a momentary reduction in the supply voltage and not complete loss of power [11]. Sags are usually characterised by their magnitude and duration. A voltage sag is defined as a decrease in the rms voltage magnitude at the supply frequency with typical values between 0.1- 0.9 p.u. and durations ranging from 0.5 cycles to 1 minute [5,10].

Voltage sags are usually caused by faults in the transmission and/or distribution system such as lightning strikes, tree or animal contacts [10-11]. High currents flowing due to short circuits either within the plants or on utility lines in the electrical neighbourhood result in voltage sags [12]. The sag persists as long as the short circuit current flows and it disappears when a fault clearing device interrupts the fault current. Starting of large motors and welding also can cause voltage sags. Methods for predicting magnitude, duration and frequency of voltage sags in an electrical network are suggested in [12]. The sag magnitude depends on the fault impedance, network impedance and fault location with respect to a sensitive load. Sag duration depends on

the clearing time of the fault clearing equipment and any intentional delays introduced to provide coordination between devices in series. In order to predict the frequency of occurrence of voltage sags, the reliability data for all voltage sag sensitive equipment in the electrical neighbourhood is required.

1.3 TYPES OF VOLTAGE SAGS

Voltage sags experienced by three-phase VSDs are classified into four types depending on the type of fault (viz. single-phase, phase-to-phase, or three-phase), the type of transformer connection and the type of load connection (Yor Δ) as follows [13-14]:

a) **Type A:** All three phases drop voltage by the same amount in magnitude.
b) **Type B:** Only one phase voltage magnitude drops.
c) **Type C:** Two phases drop in voltage magnitude with change in their phase angles
d) **Type D:** Two phases drop in voltage magnitude with change in phase angles and the third phase drop in magnitude only.

As seen from the above definitions, voltage sags may be accompanied by phase angle jumps. Transformer connections (Δ–Y,Y–Y, etc.) also have an effect on the line voltage seen by the load during an unbalanced sag [7]. Moreover, one type of sag can transform into another type depending upon the transformer connections [11, 13].

1.4 IMPACT OF VOLTAGE SAGS ON AC VSDs

Though, dc motor drives still have a presence in the drives market, their share is being overtaken by the ac VSDs because of the recent technological advances and the comparative advantages of ac motors over their dc counterparts [2-3,15]. Hence in this thesis only ac motor VSDs are examined.

About 80% of the modern AC drives are Voltage Source Inverter type, having a diode bridge front-end, a dc link capacitor (with an optional inductor) and a PWM inverter [7, 15-16]. In this VSD configuration, because the rectifier is an uncontrolled one, any variation in the ac supply would be reflected in the dc bus characteristics. With a balanced and rated ac supply, the diodes in the three-phase rectifier are forward biased when the line voltage exceeds the bus capacitor voltage and thus the rectifier output current is a repetitive pattern of six symmetrical pulses per cycle. Similarly the dc bus voltage is a symmetrical pattern of six peaks per cycle as the capacitor charges to the peak input voltage and discharges in between the peaks while supplying energy to the motor [7]. Hence, in such ideal ac supply conditions, the dc capacitor voltage is at the nominal value with minimal ripple content. The dc capacitor delivers the power required by the motor to operate at the set speed and torque levels.

However, when subjected to voltage sags, the VSD performance, especially the dc bus characteristics, is affected. The impact of balanced as well as unbalanced sags on the VSD behaviour is discussed in the following subsections.

1.4.1 IMPACT OF A BALANCED SAG

When a balanced sag (Type A as mentioned in Section 1.3) appears on the VSD power supply, the capacitor voltage will still be a symmetrical pattern of six peaks per cycle but its average value will be lower than the nominal value depending on the sag magnitude [7]. When the dc bus voltage reduces, the energy available in the dc link also reduces and below a particular voltage, the VSD cannot deliver the rated torque at a certain speed. But the main problem with this dc voltage drop is the risk of damaging the rectifier components due to high capacitor charging currents when ac supply returns to normal level. The rectifier over-current transients can be much worse on voltage recovery than during a sag [17]. Hence the dc bus voltage is continuously monitored by the control system which trips the VSD on under-voltage fault when the bus voltage reaches a lower limit.

1.4.2 IMPACT OF AN UNBALANCED SAG

In the case of unbalanced sags (Types B, to D as defined in Section 1.3), the conduction of diodes is not a symmetrical pattern any more. The capacitor charges to the peak of the line-to-line voltage and usually one or more of these peak voltages are less than the nominal capacitor voltage. This causes the capacitor to discharge for a longer duration until the next peak voltage is sufficient to forward bias the diodes. Often, the three-phase rectifier acts as a single phase rectifier with phase current as high as 4 or more times the rated value which causes the drive to trip due to over-current protection fault [7].

The phase angle jump also results in a similar situation as an unbalanced sag since it tends to reduce one or more line-to-line voltages thereby tripping the drive on either under-voltage or over-current faults [7].

Most older VSDs have their control electronics power supply derived from the AC input and hence they are very sensitive to supply variations which caused nuisance tripping [7].

Though voltage sags do not damage the equipment, they usually result in nuisance tripping of VSDs. It is reported that, a sag of magnitude more than 20% and duration more than 12 cycles is found to trip VSDs [4].

1.5 CONVENTIONAL MITIGATION STRATEGIES

The mitigation techniques aimed at improving the sag ride-through performance of the VSDs that are available in the literature can be broadly classified into three categories, viz. (1) hardware modifications, (2) provision of alternate power supplies and (3) control algorithm modifications. The various suggestions available in each group will be discussed in the rest of this section.

1.5.1 MITIGATION TECHNIQUES BY HARDWARE MODIFICATIONS

The following strategies suggest either changes in the hardware ratings or addition of extra hardware in a VSD in order to improve the voltage sag ride-through performance:

a) increase the ac side reactance [7]
b) increase the dc bus capacitance [7,18]
c) decrease the dc bus capacitance [19]
d) provision of large L-C filter at the rectifier output [19]
e) over-dimension the diode-bridge rectifier [19]
f) derive control electronics power supply from the dc bus capacitor by means of a Switch Mode Power Supply [7,18]
g) dc bus voltage control during a sag by operating the dynamic braking IGBT in boost mode with the addition of three diodes and an inductor [20]
h) have an active rectifier front end [21]

The advantages as well as disadvantages of the above strategies are discussed as follows:

a) Increasing ac side line reactors would help to smooth the rectifier currents during an unbalanced voltage sag and improve the ride-through performance against over-current tripping but would permanently account for a drop in the input voltage especially at higher line currents [7]. Also they add to the cost and size of the VSDs.

b) Larger bus capacitor ensures smaller ripple voltage in the dc bus and also improves the ride through capability of the VSD during a sag condition. But it results in higher recharging currents when the voltage returns to normal which may lead to damage of the rectifier components or tripping of the VSD on an over-current fault.

c) Interestingly, another suggestion contrary to (b) recommends to lower the dc bus capacitance value for some specific control strategies [19]. The advantage here is the

lower current peaks in the rectifier circuit whereas this strategy results in higher dc bus voltage ripple and reduced energy storage for sag ride-through operation.

d) Addition of an L-C filter in the dc link helps smooth the current in the rectifier thereby avoid VSD over-current tripping. Apart from that, it is also useful in limiting the ac side harmonic pollution generated by a VSD [19]. The main disadvantage here again is the extra cost and space requirement.

e) Another suggestion recommends to overrate the diode bridge to twice the normal current rating [19]. This strategy helps to take care of higher capacitor charging currents during unbalanced power supply and transients but it increases the cost.

f) Many older versions of VSDs derived power for the control electronics from the incoming ac supply which was also monitored for under-voltage trips. In such cases, the control power supply being sensitive to ac supply variations, caused large number of nuisance tripping during sags and transients. Hence, it is recommended to derive the power supply for control electronics from the dc bus [7,18] and the advantage is the capacitor backs up the power supply during supply variations. Most modern drives are already incorporating this feature.

g) Another strategy suggests controlling the dc bus voltage at a required level during a sag condition by the addition of three diodes and an inductor to the standard VSD hardware used in a VSI configuration [20]. These additional components, along with the lower half of the diode rectifier and the existing dynamic braking IGBT (which is a standard component in VSDs), can be operated as a boost rectifier during a sag and the bus voltage can be maintained at the desired value. It is reported that the performance of the VSD is unaffected, without any speed fluctuations, when subjected to a sag of magnitude 50% lasting for 30 cycles [20]. In spite of the high level of sag ride-through performance, the additional cost and space requirements cannot be justified for all types of VSD applications.

h) Use of a controlled front-end rectifier is recommended which will improve the dc bus characteristics of VSDs during voltage sags with the additional advantage being

lower harmonic pollution in the power system [21]. But again, the main disadvantage is the additional cost.

It can be observed that, most of the hardware related mitigation strategies involve additional costs and increased space requirement in VSDs. Suggestions (a) to (d) are intended to delay the tripping so that VSDs can override sags of short duration. Suggestions such as (e) and (f) are already in usage in recent drives. Though strategies (g) and (h) help to improve the ride-through performance during adverse sag conditions, they are not popularly implemented mainly due to the cost and space constraints.

1.5.2 MITIGATION TECHNIQUES BY MEANS OF IMPROVED POWER SUPPLY CONDITIONS

Some sag ride-through mitigation strategies suggest to improve the power supply conditions rather than modifications in VSDs to overcome the discontinuity of operation during a voltage sag. The various suggestions alongwith their advantages as well as disadvantages are discussed below:

a) transfer of supply between two independent power sources [11,22]
b) use of thyristor controlled tap changer (CTCs) [4,23]
c) use of a Motor Generator Set to provide power supply [4]
d) use of a Power Line Conditioning Equipment [4]
e) use of Uninterruptable Power Supply (UPS) for control electronics [18]

a) Transfer of power supply to an alternative source by means of solid state switches is recommended in [11] when a sag occurs. A very smooth transition is reported without any significant speed or torque disturbances in the VSD performance when a 24 kV power supply was transferred to an alternative system [11]. However, this solution calls for a very high capital investment. But the drawback of this solution, in spite of backing up the entire plant supply, is that it can only prevent external disturbances

from entering the local system but cannot prevent sags from being generated due to internal plant electrical faults.

b) Another suggestion recommends the use of a thyristor controlled tap-changer (CTC) in order to maintain the ac supply voltage at nominal levels [4,23]. The reported advantages are fast response, low total harmonic distortion (THD) and high efficiency. The disadvantages are the high cost and space requirements.

c) The use of a Motor Generator Set is suggested in order to supply critical loads such as VSDs [4]. The advantages are the ability to withstand deeper sags, high output regulation and electrical isolation. The disadvantages are high investment costs, maintenance, low efficiency and increased space.

d) Another strategy suggests the use of power line conditioners in the ac supply which results in very fast voltage regulation and low harmonic current distortion [4]. However it is also an expensive solution.

e) Use of an Uninterruptable Power Supply (UPS) is suggested for supplying the control electronics in [18]. This suggestion may guarantee uninterrupted control supply, but cannot prevent the VSD from tripping because of dc bus under-voltage or ac over-current faults.

From the above discussions, it can be realised that the main disadvantage of the power supply related suggestions is their high costs with most of the solutions more expensive than the cost of the VSDs. Also, they occupy considerable space. Moreover, since most of these type of strategies attempt to provide a plant-wide solution to power quality problems, they cannot take care of the disturbances which occur due to internal plant faults.

1.5.3 MITIGATION TECHNIQUES BY CONTROL ALGORITHM MODIFICATIONS

So far, sag ride-through strategies either by modifying the VSD hardware or by improving ac power supply conditions have been discussed. It was found that, most of the hardware related suggestions are aimed at delaying the VSD tripping during sags and they cannot prevent VSD tripping due to longer and deeper sags. Moreover, these solutions tend to increase the cost and space requirements in the VSD. The power supply related suggestions are too expensive to consider for most of the VSD applications. Also, they have other disadvantages such as additional space requirement, poor efficiency, maintenance requirements and inability to prevent sags occurring from within the plant. The ideal solution would be to enable the VSD to ride-through the voltage sags. The best means to achieve this objective would be by improving the control algorithm in the VSD. With this type of solution, the standard VSD hardware can be retained and the disadvantages such as additional cost and space can be avoided. The suggestions available in this category are:

a) modulation index and stator frequency compensation [19]
b) maintaining the inverter output synchronised with the motor i.e. operate the VSD with minimum losses [16,24]
c) bus capacitor voltage control by recovering the kinetic energy available in the rotating mass [25]

The VSD performance characteristics when controlled by the above strategies are analysed below:

a) The first strategy suggests to compensate for the modulation index and stator frequency according to the dc bus voltage available during a sag. This leads to shifting the torque-speed characteristics towards the origin during a sag and this technique ensures maximum torque availability to the motor at all speeds despite a reduction in the motor speed [19]. But, since the dc bus characteristics are not improved by this control strategy, VSD tripping can still occur due to dc under-voltage or ac over-current faults as discussed in Section 1.4.

b) Another control based strategy recommends maintaining the supply output of the VSD synchronised with the induction machine flux and operate it at zero slip during a sag [16,24]. This means only a minimal power corresponding to the winding losses in the machine is drawn from the dc capacitor. This solution ensures that the dc voltage is reduced at a slower rate than during normal operation and thus extends the ride-through operation of the VSD during sags until the dc voltage reaches a very low level. The machine coasts towards zero speed. Since the inverter remains synchronised with the machine flux, the VSD can be automatically restarted on power supply recovery. Here, the sag ride-through performance depends on the dc bus voltage at the point of supply recovery which in turn depends on the losses in the motor.

c) Finally, another control strategy recommends maintaining the dc bus voltage at a required level by recovering the kinetic energy available in the rotating mass during a voltage sag condition [25]. This method can be employed for both field orientation and constant v/f (VVVF) controls. The kinetic energy can be recovered until the motor speed becomes zero. During this operation, the motor decelerates to zero speed at a faster rate than during normal coasting and this deceleration rate is proportional to the amount of energy regenerated and the load present on the motor. But, the kinetic energy decreases proportional to the square of the speed and it can be realised that due to this cumulative effect, the kinetic energy is highly speed dependent. So the sag ride-through performance under this strategy is limited by the load as well as motor speed. If the voltage sag persists even after the motor has come to standstill, then the capacitor voltage will start to reduce and the VSD can trip due to under-voltage or over-current faults as discussed in Section 1.4.

1.6 AIM OF THE THESIS

The main aim of the work presented in this thesis is to improve the sag ride-through performance of VSDs by modifying the control algorithm. The control strategies available in this category result in improved ride-through characteristics but their performance is limited by factors such as losses in the motor or non availability of kinetic energy at zero speed. An improved control strategy is proposed in this thesis

which will enable extended voltage sag ride-through performance of the VSDs compared to the conventional strategies. The proposed strategy is an extension of the control strategy recommended in [25] where the dc bus capacitor voltage is maintained at a desired level by recovering the kinetic energy available in the rotating mass. It can be shown that during normal operation, a considerable amount of energy is available in the motor in the form of kinetic as well as magnetising energy as compared to the energy levels present in the dc bus capacitor (refer Appendix A). Therefore, whenever a voltage sag occurs, the dc bus voltage can be maintained at a desired level, by recovering the kinetic energy available in the rotating mass at high motor speeds and by recovering the magnetising energy available in the motor winding inductances at low speeds. Though the energy available in the inductances can supply the dc bus capacitor only for a short duration, the dc voltage will be maintained at the set value even after the complete energy is recovered from the motor because no further energy will be drawn from the dc capacitor during a sag. Once the ac supply returns to nominal level, normal VSD operation can be restored. The advantage of this control strategy over the conventional ones (which were discussed in Subsection 1.5.3) is that a sag ride-through performance can be achieved even after the motor reaching zero speed. This strategy is applicable for both induction motor (IM) as well as synchronous reluctance motor (SRM) VSDs.

1.7 CONTRIBUTIONS OF THIS THESIS

1) In this thesis, a new strategy is proposed to maintain the dc capacitor voltage by recovering the magnetising energy available in the ac motor winding inductances. This is demonstrated in the case of an SRM VSD.

2) Reasons for the inability to recover the magnetising energy in the case of an IM VSD are presented.

3) Utilising the concept of the proposed control strategy, an open loop dc bus voltage control is presented with optimum reduction of motor flux so that an IM VSD can ride-through voltage sags at low speeds.

4) A controlled coordination of bus voltage control is demonstrated by initially recovering kinetic energy from the rotating mass at high motor speeds and then the magnetising energy from the motor winding inductances at low speeds until zero speed so that the VSD rides through voltage sags at all speeds.

1.8 SCOPE OF WORK AND PLAN OF THE THESIS

In this thesis, the sag ride-through performance of both an IM VSD and an SRM VSD when controlled by the proposed strategy will be presented. Forthcoming chapters are organised as follows:

In Chapter 2, the outline and details of the proposed control strategy will be presented. The control set points and the order of control sequence will be justified. Since this strategy will be applied to both IM and SRM VSDs, simulation models will be presented for both these VSD types and the basic control loops used in these VSDs will be discussed. The design and implementation of the additional control loops required for the capacitor voltage control by recovering the energy available in the ac motors will be discussed and their coordination with the existing control loops in the VSDs will be described. Finally, the power flow relationship between various sections of the VSD system will be derived.

Chapter 3 will present the performance results of the proposed control strategy in the case of an SRM VSD. Initially, the normal speed control operation of the simulation model will be verified and then the performance results with the proposed strategy at high as well as low motor speeds during a sag will be analysed. Finally, the sag ride-through performance at an intermediate speed will be presented where the coordinated transition of control from the kinetic energy recovery at high speeds to magnetising energy recovery at low speeds can be observed.

In Chapter 4, the performance of this control strategy will be analysed in the case of an IM VSD. Initially, the normal speed control operation will be verified. Then, the performance results during dc voltage control at high and low speeds in the presence

of a sag will be analysed. Because of the inability to recover the magnetising energy in the case of an induction motor, an alternative control scheme is proposed which can be utilised at low motor speeds. The combined operation using both these modes of the control strategy is presented in order to demonstrate the sag ride-through capability of the proposed strategy at all speeds.

Chapter 5 summarises the performance of this control strategy for both IM and SRM VSDs.

CHAPTER 2

PROPOSED CONTROL STRATEGY AND MODELLING OF VSDs

2.1 INTRODUCTION

In this chapter, a control algorithm based mitigation technique that can be applied to an ac VSD in order to achieve an improved voltage sag ride-through performance is proposed. Since about 80% of recent ac drives have VSI configuration with a three stage topology (Fig. 2.1), i.e. a diode bridge rectifier front-end, a dc link capacitor and a PWM inverter [7, 15-16], an ac drive with this configuration alone will be considered in this thesis. Field orientation technique will be applied and the behaviour of IM and SRM VSDs when subjected to a voltage sag condition will be examined .

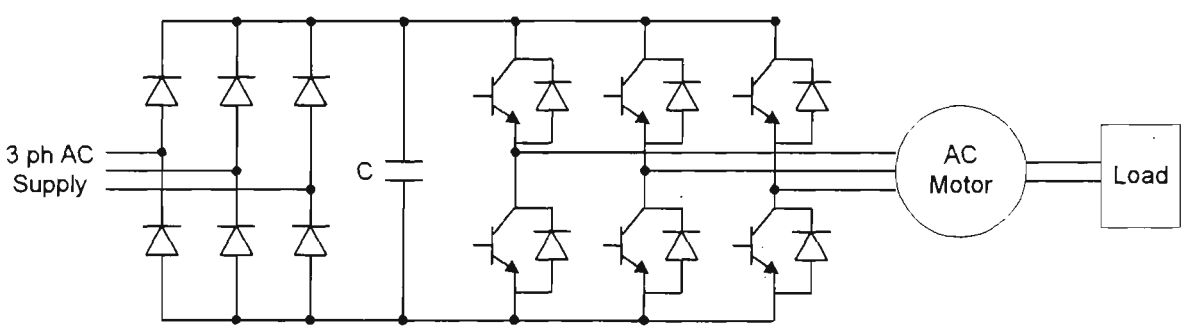


Fig.2.1. VSD with a VSI configuration having a diode bridge front-end

As already mentioned in Section 1.4, disturbances in control power supply and drop in dc bus voltage are the two main causes for the interruption of VSD during voltage sags. The stability of control circuit power supply can be ensured by deriving it from the dc bus capacitor through a Switched Mode Power Supply (SMPS) [7,18], which will buffer the impact of ac supply fluctuations from affecting the control power supply. Now, the main

task of the VSD control system is to maintain the dc bus voltage at a desired level during a voltage sag so that the drive rides-through the sag without tripping due to the fault conditions which were discussed in Section 1.4.

As shown in Appendix A, during normal operating conditions, there is a considerable amount of energy present in an ac motor in the form of kinetic energy due to system inertia and magnetising energy in the motor winding inductances. When a voltage sag occurs, the dc bus voltage can be maintained at a desired level by coordinated recovery of energy from these two sources so that the continuity of operation of the VSD can be achieved.

In this chapter, the proposed control strategy will be discussed in further detail. Because this strategy requires modifications in the VSD control algorithm, there will be a brief mention about the basic control loops used in a VSD operating under field orientation which will be followed by a simplified block diagram representation of the IM and SRM VSDs for simulation purposes. Then, the design details of the additional control loops required by this strategy and their operation sequence in coordination with the existing control loops will be elaborated. Since there is a continuous flow of energy between the ac mains, dc bus capacitor and the ac motor, and moreover because the proposed control strategy aims to recover energy from the motor to the dc capacitor during a voltage sag, the power flow equations involving the ac mains, VSD and the ac motor will be presented.

2.2 PROPOSED CONTROL STRATEGY

Out of the two sources of energy within the ac motor, viz. kinetic energy ($\frac{1}{2}J\omega^2$) and the magnetising energy ($\frac{1}{2}LI^2$), the kinetic energy is the most dominant component and at rated motor speed, it usually accounts for several times the energy stored in the capacitor (refer Appendix A). The kinetic energy can be recovered from the rotating mass by operating the PWM inverter in the regeneration mode i.e. by operating the motor as a

generator and by reversing the flow of energy from the motor to the dc bus. The magnetising energy stored in the motor inductance can be recovered by forcing the magnetising current reference to a lower value when the inductance acts as a current source and feeds the stored energy back to the dc bus. The energy thus recovered in both cases can be utilised to maintain the dc bus voltage at a desired level during a sag.

In order to establish an efficient and simpler control system, it is better to attempt energy recovery from one source at a time. The fact that the motor requires magnetic field in order to function as a generator makes kinetic energy the first choice of energy source that can be recovered. When the motor functions as a generator, its speed falls more rapidly than normal coasting, i.e. with the incoming supply cut off. The rate of speed drop during regeneration depends on factors such as the amount of energy regenerated, the load torque and system inertia. When the motor speed reaches very low values, the stored kinetic energy reaches negligible proportions and the motor cannot deliver the power required at the dc bus. There is no advantage in reducing the speed below some limit. Hence, a cut-off speed limit is defined below which, this strategy would attempt to recover the energy available in the magnetising inductances.

2.2.1 SET POINTS FOR CONTROL STRATEGY

Under normal circumstances, a voltage sag condition can be detected by the VSD control system by monitoring either the line-to-line ac supply voltage (V_{ll}) or the dc capacitor voltage (V_{bus}). Since the proposed control strategy is aimed at maintaining the dc bus voltage at a desired value during a sag, a voltage sag should be detected in this case by monitoring the incoming three-phase supply voltage only. Since as per the definition, a voltage sag is reduction in rms supply voltage between 0.1 to 0.9 p.u. of the nominal value [5,10], whenever any of the three line-to-line supply voltages to the VSD drop below 90% of the nominal ac voltage, a sag condition is declared and remedial actions are taken.

The set point for the bus voltage (V_{busref}) during a voltage sag is also very important for proper coordination of the VSD under the proposed strategy. In the case of a three phase rectifier, the dc bus voltage (V_{bus}) is normally 1.35 times the rms line-to-line voltage (V_{ll}). When a voltage sag occurs, the dc bus voltage falls below the nominal level. The deeper the sag magnitude becomes, the lower the dc bus voltage will be and the higher will be the chances of the VSD tripping due to under-voltage or over-current faults (as already explained in section 1.4). Usually in a VSD, the under-voltage trip settings are user configurable and are kept as a percentage of the nominal voltage (typically between 70% and 85%) [19]. Ideally, the bus voltage should be maintained between the nominal voltage and trip setting when a sag occurs. Here, the bus voltage reference is kept as 100% of the nominal rated dc bus voltage for reasons that will be explained during the ride-through simulations in Chapters 3 and 4.

Earlier in this section, a cut-off speed for the control transition in the energy recovery from kinetic energy to magnetising energy was mentioned. Though theoretically the motor can be operated in regeneration mode down to zero speed, in this simulation the cut off point is kept at 10% of the rated speed because less than about 1% of the rated kinetic energy is available in the motor below this speed.

2.2.2 CONTROL SEQUENCE AND FLOW CHARTING

The sequential flowchart of the VSD control during a voltage sag condition is as shown in Figure 2.2.

It can be observed from the flowchart that, as per the proposed control strategy, there are three distinct situations involved with respect to the control of the VSD. They are summarised as follows:

Control Situation 1 (CS1): *(No Voltage sag)* VSD operation with normal speed control.

Control Situation 2 (CS2): *(Voltage sag and motor speed > cut-off speed)* DC bus voltage control by recovering load kinetic energy.

Control Situation 3 (CS3): *(Voltage sag and motor speed < cut-off speed)* DC bus voltage control by recovering magnetising energy.

The above control situations, which are indicated as CS1, CS2 and CS3 in the Figure 2.2, will be referred to in the remainder of the thesis while discussing the controller design and analysing the performance results. In order to achieve the desired sag ride-through operation, additional control loops are necessary within the VSD control system and they will be discussed in the following sections. Since it is intended to demonstrate the recovery of energy from the magnetising inductances, operation below motor base speed alone will be considered in this thesis and field weakening control will not be examined.

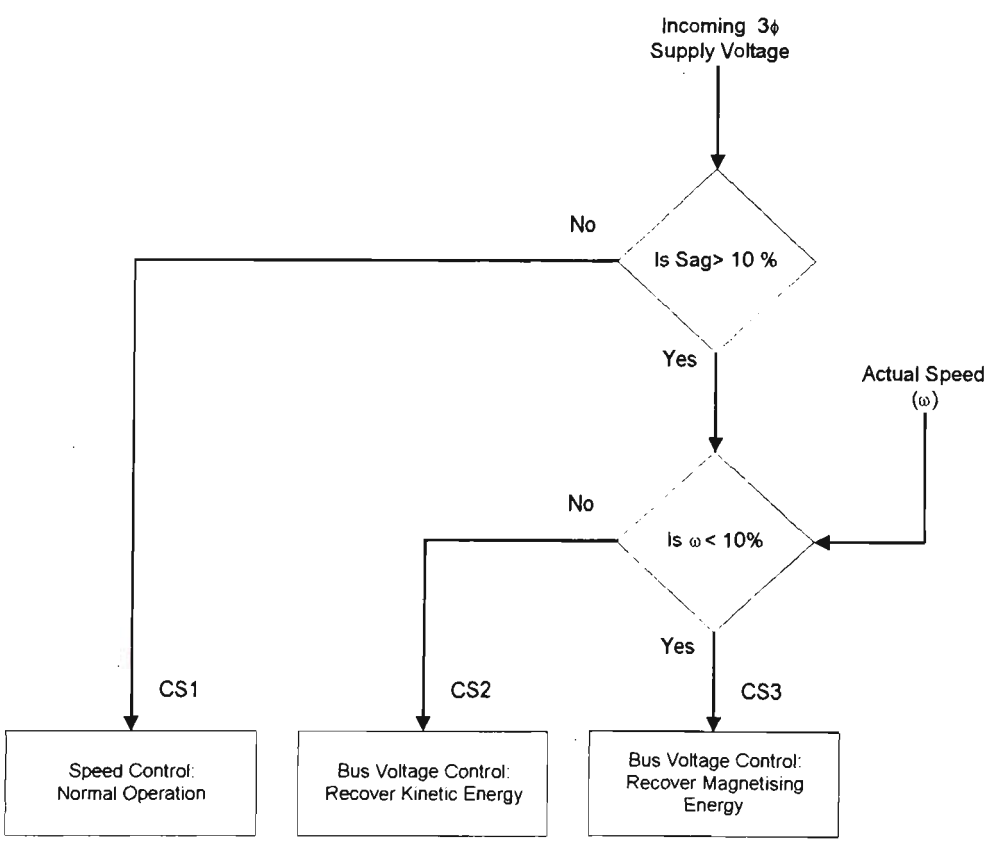


Fig.2.2. Flow chart for VSD control sequence during voltage sag condition

2.3 CONTROL LOOPS IN AC VSDs OPERATING UNDER FIELD ORIENTATION

In this section, an overview of the basic control loops in an ac VSD will be presented and the control block diagrams of IM and SRM VSDs will be discussed. In field oriented control of ac motors, the three phase motor currents are transformed into two orthogonal components in a synchronous frame of reference which moves with respect to the stator axes, and they are defined as i_{sq}, the torque producing component and i_{sd}, the flux producing component [26]. The mathematical relationships between these current vectors for IM and SRM are shown in Appendices B and C respectively. A brief overview of the control loops used in ac VSDs is as follows:

For the speed control of an ac motor, two sets of control loops are used in the VSD, viz. (a) a speed controller working in conjunction with a current controller for the torque producing current component (i_{sq}) and (b) a flux controller working in conjunction with another current controller for the flux producing current component (i_{sd}) [27]. Usually all these controllers are of proportional-integral (PI) control type operating in closed loop configuration.

The main purpose of the speed controller is to regulate the motor speed at a set reference. The speed regulator generates the torque reference to the motor depending on the instantaneous speed error and the controller gain values. In closed loop speed control, the torque reference tends to control the motor to reach the set speed by minimising the speed error to zero. In order to protect the motor from being subjected to excessive currents, the speed regulator output is limited by a torque limiter. The limited torque reference is converted to torque producing current reference (i_{sqref}) which forms the control input to the torque producing current regulator. This current regulator functions in a similar manner to the speed regulator but generates set points for motor terminal voltage so that, in closed loop control, the motor continues to run at the set speed for load torque variations between zero and the torque limit. When the load torque demand exceeds the

torque limit, the actual motor torque is clamped at this limit and the motor speed drops below the set reference.

The flux controller regulates the actual flux (or magnetising current) to the set value and it produces the flux producing current reference (i_{sdref}). The corresponding current regulator controls the flux producing current component by again influencing the set points for motor terminal voltage.

Finally, the output of the above control loops, i.e. the voltage set points, decide the switching vector selection as required by the PWM inverter at any instant. Based on the selected vector, the switches in the three inverter legs (Fig.2.1) are either opened or closed, thereby connecting the motor terminals to either the positive or negative dc bus and thus the voltage applied to the motor is controlled by the VSD control system.

The functional block diagram representation of VSD control scheme for IM and SRM VSDs operating under field orientation is discussed in the following subsections.

2.3.1 CONTROL MODEL OF AN IM VSD

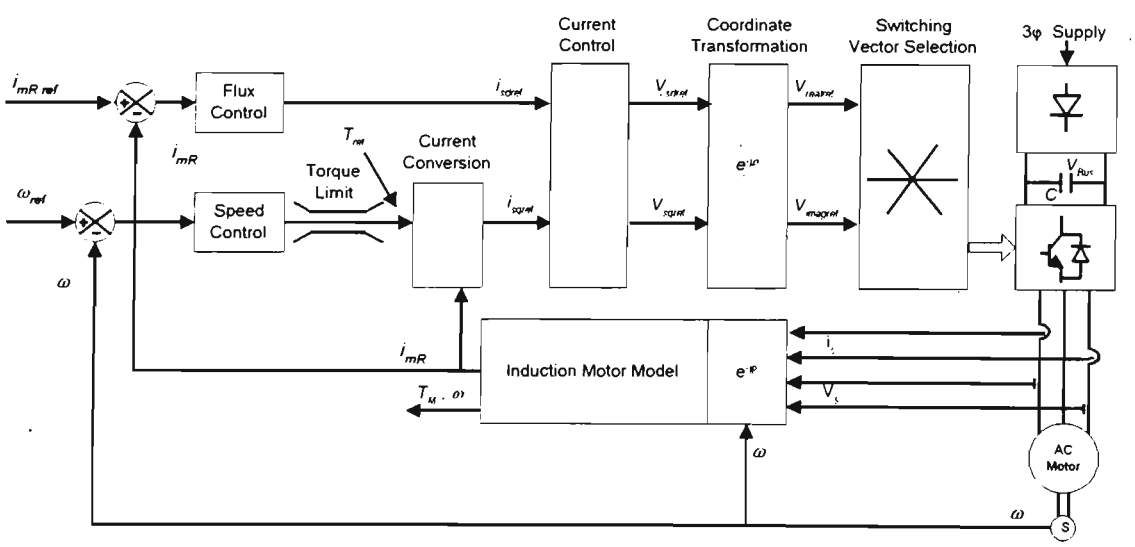


Figure 2.3 Functional block diagram of an IM VSD under field orientation control

Figure 2.3 shows the simplified block diagram representation of an IM VSD operating under field orientation, which is based on the motor modelling described in Appendix B. Tuning details of the controllers are discussed in Appendix E.

For speed control of an induction motor, the speed reference (ω_{ref}) and the magnetising current reference (i_{mRref}) are the two main control inputs. The Flux Controller generates the flux producing current reference (i_{sdref}) whereas the speed PI controller generates the torque reference, which after being limited, is converted to the torque producing current reference (i_{sqref}) in the Current Conversion block. Based on the current references (i_{sdref} and i_{sqref}), the Current Control block generates the voltage set points (V_{sdref} and V_{sqref}). In field oriented control of induction motors, the synchronous coordinates are displaced from the stator coordinates by an angle ρ as explained in Appendix B. In order to select the proper switching vector as required by the control system, it is necessary to transform these voltage reference values into real and imaginary coordinates fixed to the stator reference frame and this is done by the Coordinate Transformation block. Finally, the required switching sequence of the inverter switches is selected by the Switching Vector Selection block, the details of which are explained in Appendix D.

Based on the inverter switching sequence and the instantaneous dc bus voltage at the rectifier output, a three-phase ac voltage is applied to the motor terminals. In actual case, the flux and current controllers are of proportional-integral (PI) type and the motor speed is sensed by the control system from the speed sensor feedback (or by means of indirect speed estimation methods). Other motor variables such as voltages and currents in field coordinates and motor torque are computed from the terminal voltages and currents by the built-in motor model within the VSD as shown in the control block diagram (Figure 2.3).

However, in this simulation, the motor variables such as voltages (V_{sd} and V_{sq}), currents (i_{sd} and i_{sq}), torque (T_M) and speed (ω) are calculated based on the actual switching vector selected and the instantaneous dc capacitor voltage (V_{bus}), utilising the IM equations whose derivations are explained in Appendix B. The three-phase ac supply, diode bridge

rectifier and dc bus capacitor are also modelled in the VSD control system. The control equations used in the various control blocks are summarised as follows:

The Flux Control block calculates the motor flux producing current reference (i_{sdref}) from the magnetising current reference (i_{mRref}) utilising the following equation:

$$i_{sd} = i_{mR} + \frac{di_{mR}}{dt} T_R \tag{2.1}$$

where,

i_{sd} - stator d-axis current,

i_{mR} - rotor magnetising current,

T_R - rotor time constant

The Torque / Current Conversion block utilises the following motor torque equation in order to calculate the torque producing current set point (i_{sqset}) from the set torque reference (T_{ref}):

$$T_M = N_{pp}\, K\, i_{mR}\, i_{sq} \tag{2.2}$$

where,

$$K = \frac{2 * L_m}{3 * (1 + \sigma_r)}$$

N_{pp} - number of pole pairs in the motor,

i_{mR} - magnetising current reference,

L_m - mutual inductance between stator and rotor windings, and

σ_r - rotor leakage factor.

The Current Control block calculates the stator voltage set points in field coordinates (V_{sdref} and V_{sqref}) based on the following equations:

$$V_{sd} = R_s i_{sd} + \sigma L_s \left(\frac{di_{sd}}{dt} - \omega_{mR}\, i_{sq}\right) + (1 - \sigma) L_s \frac{di_{mR}}{dt} \tag{2.3}$$

$$V_{sq} = R_s i_{sq} + \sigma L_s \left(\frac{di_{sq}}{dt} + \omega_{mR}\, i_{sd}\right) + (1 - \sigma) L_s\, \omega_{mR}\, i_{mR} \tag{2.4}$$

where,

R_s - stator resistance,

L_s - stator inductance,

σ - total leakage factor,

ω_{mR} - angular velocity of the magnetising vector

The Coordinate Transformation block transforms the selected voltage references (V_{sdref} and V_{sqref}) from the synchronous coordinates to the stator coordinates according to equation (2.5):

$$\vec{V}_s = V_{s\_real} + jV_{s\_imag} = (V_{sd} + jV_{sq})e^{j\rho} \qquad (2.5)$$

where,

ρ - angle between the synchronous and stator coordinates.

$\vec{V}_s$ - stator voltage vector

The Switching Vector Selection block selects the appropriate operating sequence for the inverter switches, based on $V_{realref}$ and $V_{imagref}$ chosen in the Coordinate Transformation block. The details of vector selection are explained in Appendix D.

The Induction Motor Model calculates the actual motor voltages, currents (in d-q axes) and torque depending on the switching vector selected and the instantaneous capacitor voltage (V_{bus}) utilising equations (2.1) to (2.5). The motor speed is calculated by integrating equation (2.6).

$$d\omega = \frac{(T_M - T_L)dt}{J} \qquad (2.6)$$

where

T_M – motor torque,

T_L - load torque, and

J - system inertia.

2.3.2 CONTROL MODEL OF AN SRM VSD

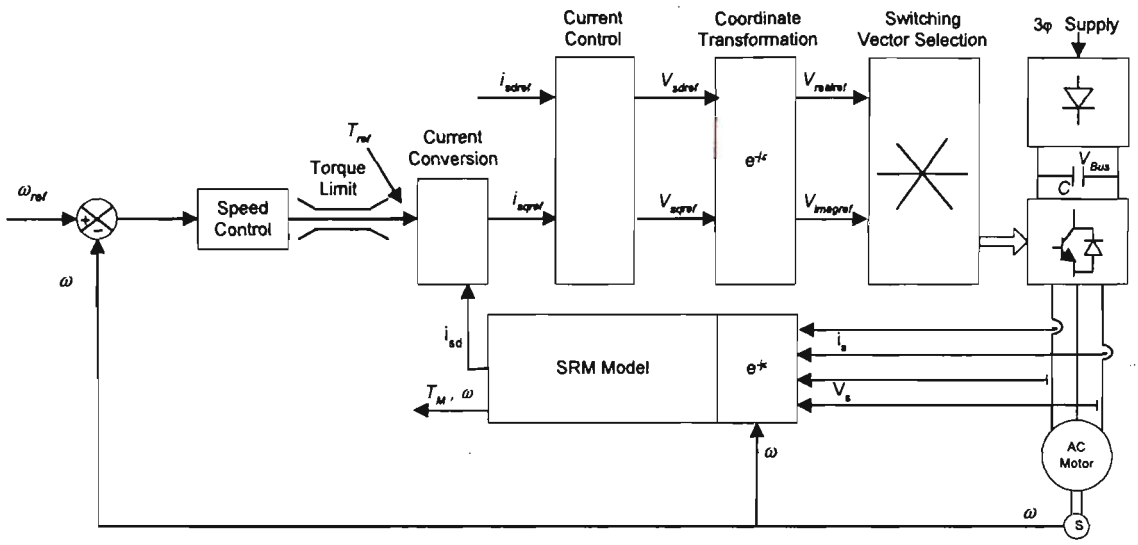


Fig 2.4 Functional block diagram of an SRM VSD under field orientation control

The simplified control block diagram of an SRM VSD under field orientation control is represented in Figure 2.4. The motor modelling and the tuning of the controllers are explained in Appendices C and F respectively.

In the case of an SRM VSD, velocity reference (ω_{ref}) and magnetising current reference (i_{sdref}) form the control inputs. The main difference in the control of SRMs as compared to the induction motors is due to the orientation of the flux axis. In the case of an SRM, the flux axis aligns itself with the rotor axis and the magnetising current is the direct component of the stator current vector (i_{sd}). The details of the current vectors and their angular relationships in the various coordinates are explained in Appendix C for an SRM. The control of an SRM is similar to that of an IM with similar control blocks as explained in Subsection 2.3.1. The following SRM equations are used in the various control blocks:

$$T_M = \frac{3}{2} N_{pp}(L_{sd} - L_{sq}) i_{sd} i_{sq} \tag{2.7}$$

$$T_M - T_L = J\frac{d\omega}{dt} \tag{2.8}$$

$$V_{sd} = R_s i_{sd} + L_{sd}\frac{di_{sd}}{dt} - \omega L_{sq} i_{sq} \quad (2.9)$$

$$V_{sq} = R_s i_{sq} + L_{sq}\frac{di_{sq}}{dt} + \omega L_{sd} i_{sd} \quad (2.10)$$

$$\vec{V}_s = V_{s\_real} + jV_{s\_imag} = (V_{sd} + jV_{sq})e^{j\varepsilon} \quad (2.11)$$

where,

T_M– motor torque

T_L- load torque

J – system inertia

N_{pp} – number of pole pairs

R_s – stator resistance

L_{sd}, L_{sq} – stator inductance in d and q axes

ε - rotor angle with respect to stator axis

ω - rotor angular velocity

$\vec{V}_s$ – stator voltage vector

i_{sd}, i_{sq} - stator currents in d and q axes

V_{sd}, V_{sq} - stator voltages in d and q axes

2.4 PROPOSED ADDITIONAL CONTROL LOOPS FOR DC BUS VOLTAGE CONTROL

It may be recalled from Section 2.2 that the main intent of the proposed control strategy is to maintain the capacitor voltage at the nominal value by recovering the kinetic as well as the magnetising energy available in the motor. Three control situations were defined, viz. (a) No sag situation (Control Situation 1), (b) A voltage sag condition with the motor running above thecut-off speed limit (Control Situation 2) and (c) A voltage sag condition with the motor running below the cut-off speed limit (Control Situation 3). An overview of the basic control loops for the speed control of IM and SRM VSDs was presented in Section 2.3. From the point of view of the proposed control strategy, these are the control

loops that will be in operation during a no sag situation (Control Situation 1). However, since there is a need to recover the energy present in the motor during a sag, additional control loops are necessary in the VSD control system. The control methodology, design and implementation of the additional control loops will be discussed in the following subsections and their sequence of operation in coordination with the existing control loops will be defined. Tuning details of the additional controllers are presented in Appendices E and F for IM and SRM respectively.

2.4.1 BUS VOLTAGE CONTROL BY RECOVERING LOAD KINETIC ENERGY

At higher motor speeds, the capacitor voltage can be controlled by recovering the kinetic energy available in the rotating mass. Kinetic energy can be recovered by operating the motor as a generator. Electrically this means reversal of the flow of current from the ac motor to the dc bus with rated flux applied to the motor. From a control point of view, this can be achieved by maintaining the flux reference to the motor constant at the rated value and by reversing the polarity of the torque reference (T_{ref}) which, in turn, will reverse the flow of i_{sq}. This operation is further explained by the power balance equation (2.12) whose derivation will be shown in Section 2.5.

$$V_{bus} I_{out} = \frac{2}{3}(V_{sd} i_{sd} + V_{sq} i_{sq}) \qquad (2.12)$$

where,

V_{bus} – bus capacitor voltage

I_{out} – dc current flowing between the bus capacitor and the inverter

V_{sd}, V_{sq} – stator voltages in synchronous coordinates

i_{sd}, i_{sq} – stator currents in synchronous coordinates

From equation (2.12), it can be noted that, by maintaining the flux (i_{sd}) constant, if i_{sq} is reversed, the flow of the dc current I_{out} can be reversed from the motor to the dc bus

which will boost the capacitor voltage. This is the basis of the control utilised in Control Situation 2.

In a voltage sag condition, the recovery of kinetic energy must be controlled so that only the required amount of energy is recovered from the motor to maintain the capacitor voltage at the desired value. This can be done by the use of a closed loop proportional-integral (PI) controller, which monitors the capacitor voltage against the set reference and produces a suitable torque reference. The polarity of the torque reference is reversed to that of normal speed control operation. A new PI controller is configured in the VSD control system for this purpose which will be referred to as Bus Voltage Controller 1 in further discussions.

As described in Section 2.3, during normal speed control operation (Control Situation 1), the torque reference is generated by the Speed Controller in order to regulate the motor speed at the set reference. When a sag occurs, if the motor speed is above the cut-off limit (i.e. Control Situation 2), the torque control is switched to the Bus Voltage Controller 1. This controller applies a reverse torque reference and controls the capacitor voltage rather than motor speed. The Current Controller as well as rest of the control blocks (which are shown in Figures 2.3 and 2.4) operate exactly in the same manner as during speed control and motor speed is not controlled in this situation. Because of the regenerative operation, the motor speed will reduce rapidly during this control. While recovering the kinetic energy, the torque limiting circuit must be in circuit to ensure that the motor currents are within the allowable levels. The transition between the Speed Controller and Bus Voltage Controller 1 is reversible when the motor speed is above the cut-off limit, i.e. when a sag occurs, torque referencing switches from Speed Controller to Bus Voltage Controller 1 and vice versa if the sag disappears when the motor speed is still above the cut-off limit. The magnetising current reference is maintained at the rated value throughout this operation. Figure 2.5 shows the sequence of operation of the control system during a sag at high motor speeds. Control Situations 1 and 2 are indicated as CS1 and CS2 respectively.

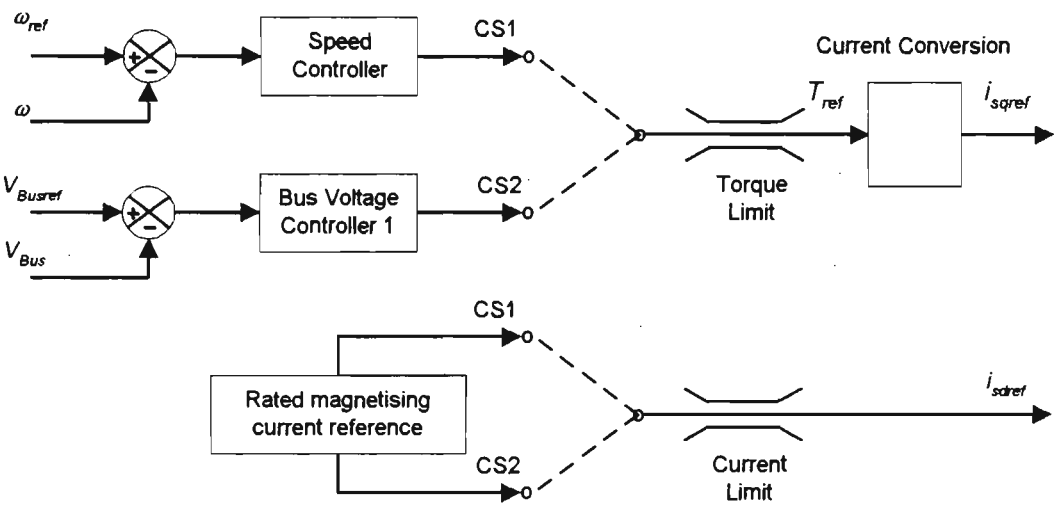


Figure 2.5 Control loop to recover kinetic energy

Since the basis of speed and torque control operation is identical for IM and SRM VSDs, as explained in Section 2.3, the proposed control scheme is applicable for both motor types. The control strategy at motor speeds lower than the cut-off speed limit is discussed in the following subsection.

2.4.2 BUS VOLTAGE CONTROL BY RECOVERING MAGNETISING ENERGY

If a voltage sag occurs when the motor speed is below the cut-off limit (Control Situation 3), the magnetising energy stored in the motor inductance can be recovered to boost the bus capacitor voltage. This energy recovery can be achieved by lowering the magnetising current, (which is i_{sd} for an SRM and i_{mR} for an IM). From the stator voltage equations, (equations (2.3) and (2.9) respectively in the case of IM and SRM), it can be found that lowering the magnetising current reference results in the polarity reversal of the applied voltage V_{sd}. There is no torque needed during this control situation and hence i_{sq} is controlled to zero. From the power flow equation (2.12), which was referred to in Subsection 2.4.1, it can be noted that, with zero i_{sq}, reversal of V_{sd} reverses the flow of the

current I_{out} from the motor to the dc bus which will boost the capacitor voltage V_{bus}. In order to achieve a controlled recovery of this magnetising energy, another PI controller (Bus Voltage Controller 2) which monitors V_{bus} against the set reference is employed to control (reduce) the flux reference. Figure 2.6 shows the sequence of operation and Control Situations 1, 2 and 3 are indicated as CS1, CS2 and CS3 respectively.

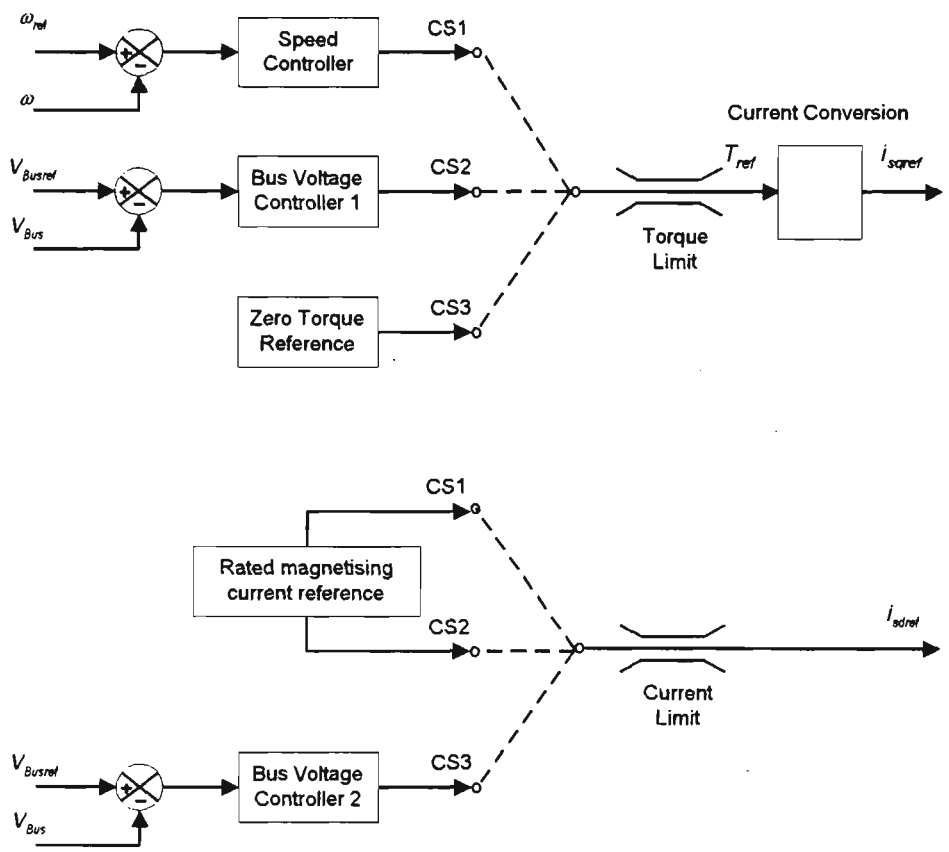


Figure 2.6 Control loop to recover magnetising energy

It can be observed that, Control Situation 3 can be initiated from either Control Situation 1 (normal speed control) or from Control Situation 2 (kinetic energy recovery). When a sag is present and if the motor speed is below the cut-off speed, Control Situation 3 comes into effect. When the power supply returns to normal, normal speed control operation resumes and the motor is speed controlled with the rated flux applied to the motor.

2.5 POWER BALANCE BETWEEN AC SUPPLY, BUS CAPACITOR AND AC MOTOR

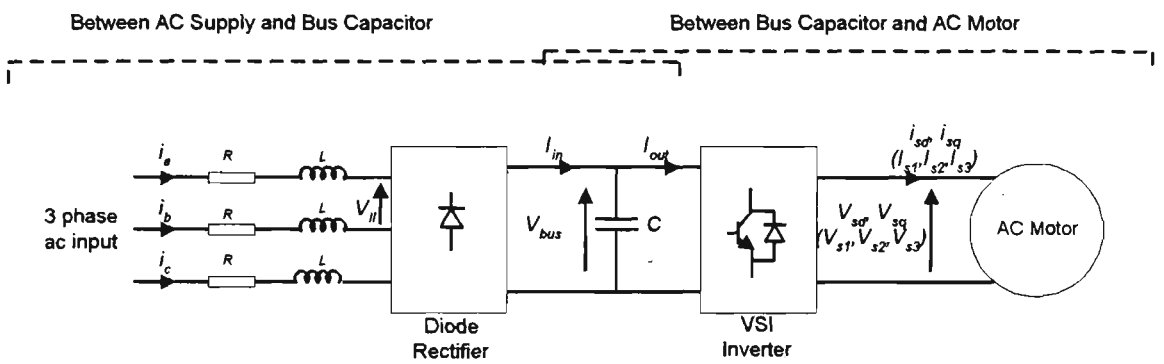


Fig. 2.7 Power flow diagram in an ac VSD

Since the proposed control strategy aims to recover energy from the motor to the dc capacitor during a voltage sag and also because there is a continuous flow of energy between the ac mains, dc link and the ac motor, the power flow equations relating the voltages and currents in these sources are discussed here. The VSD configuration considered in this thesis is shown in Figure 2.1. During motoring, power flows from the incoming ac supply to the dc bus capacitor (through the diode bridge rectifier) and from the bus capacitor to the motor (through the PWM inverter). When the motor is controlled in regeneration mode, the inverter reverses the direction of power flow from the motor to the dc capacitor. Figure 2.7 shows the power flow block diagram of the VSD configuration considered in this thesis. The currents and voltages in the ac motor are represented in synchronous coordinates. The derivation of power balance equations between ac-to-dc and dc-to-ac conversions are discussed in the following subsections.

2.5.1 POWER FLOW BETWEEN AC SUPPLY AND DC BUS CAPACITOR

In a diode-bridge rectifier, when the line-to-line ac voltage (V_{ll}) is greater than the instantaneous capacitor voltage (V_{bus}), there will be a flow of current (I_l) from the conducting phases to the bus capacitor based on equation (2.13).

$$2L\frac{dI_l}{dt} = V_{ll} - 2R\,I_l - V_{bus} \tag{2.13}$$

where,

L – per phase line inductance

R – per phase line resistance

Under balanced supply conditions with a constant load, the individual phase currents will be a repetitive pattern of two symmetrical pulses in the positive as well as the negative half cycles. Hence, the capacitor charging current (I_{in}) will be a uniform pattern of six pulses per cycle. The instantaneous capacitor voltage (V_{bus}) can be calculated as:

$$C\frac{dV_{bus}}{dt} = I_{in} - I_{out} \tag{2.14}$$

The relationship between ac and dc quantities (i.e. voltages and currents) under balanced three-phase supply conditions is,

$$I_l = 0.816\,I_{in} \tag{2.15}$$

$$V_{bus} = 1.35\,V_{ll} \tag{2.16}$$

where,

I_l - incoming phase current,

I_{in} - capacitor charging current,

V_{bus} - capacitor voltage,

V_{ll} - line-to-line ac voltage

2.5.2 POWER FLOW BETWEEN DC BUS CAPACITOR AND AC MOTOR

The relationships between the instantaneous power drawn from the bus capacitor and the power utilised by the ac motor is derived in this subsection. The angular relationships of current vectors in various reference frames are shown in Figure 2.8, which are explained in further detail in Appendices B and C for both IM and SRM.

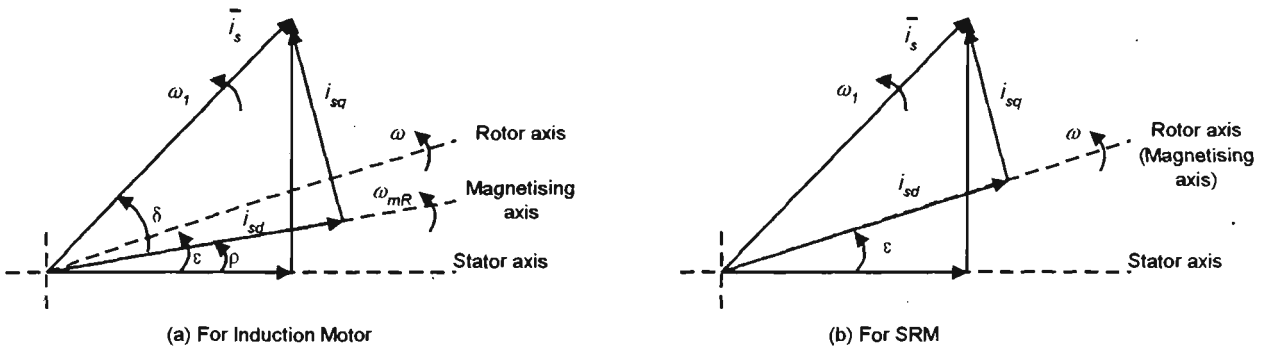


Figure 2.8 Angular relationships between current vectors in steady state [26]

The stator voltage and current vectors ($\vec{V}_s, \vec{I}_s$) can be expressed in terms of their three phase components as follows:

$$\vec{V}_s = V_{s1} + V_{s2}e^{j\frac{2\pi}{3}} + V_{s3}e^{j\frac{4\pi}{3}} \tag{2.17}$$

$$\vec{I}_s = I_{s1} + I_{s2}e^{j\frac{2\pi}{3}} + I_{s3}e^{j\frac{4\pi}{3}} \tag{2.18}$$

where,

V_{s1}, V_{s2}, V_{s3} – individual phase voltages applied to the ac motor

I_{s1}, I_{s2}, I_{s3} – individual phase currents in the ac motor

In a star connected system, $I_{s1} + I_{s2} + I_{s3} = 0$ and hence, the instantaneous power p flowing into the ac motor can be derived as:

$$p = \frac{2}{3}\mathrm{Re}(\vec{V}_s \vec{I}_s^{\,*}) \tag{2.19}$$

Also, these stator voltage and current vectors ($\vec{V}_s$ and $\vec{I}_s$) can be expressed in field coordinates. In the case of an IM, ρ is the instantaneous angle of the rotating magnetising axis with respect to the stationary frame of reference. (In the case of an SRM, this angle is ε, which is the angle of the rotor with respect to the stator axis. However the following result still holds good for both motors).

$$\vec{V}_s\, e^{-j\rho} = V_{sd} + jV_{sq} \tag{2.20}$$

$$\vec{I}_s\, e^{-j\rho} = i_{sd} + j i_{sq} \tag{2.21}$$

$$\vec{V}_s\, e^{-j\rho}\, \vec{I}_s^{*}\, e^{j\rho} = \vec{V}_s\, \vec{I}_s^{*} = (V_{sd} i_{sd} + V_{sq} i_{sq}) + j\,(V_{sq} i_{sd} - V_{sd} i_{sq}) \tag{2.22}$$

Substituting equation (2.22) into (equation (2.19),

$$p = \frac{2}{3}\mathrm{Re}(\vec{V}_s\, \vec{I}_s^{*}) = \frac{2}{3}(V_{sd}\, i_{sd} + V_{sq}\, i_{sq}) \tag{2.23}$$

From Figure 2.7, it can be seen that the input power p flowing into the motor from the capacitor (neglecting losses) is:

$$p = V_{bus}\, I_{out} \tag{2.24}$$

Combining equations (2.23) and (2.24), the power balance between the dc bus and ac motor is obtained as:

$$V_{bus}\, I_{out} = \frac{2}{3}(V_{sd} i_{sd} + V_{sq} i_{sq}) \tag{2.25}$$

2.6 SUMMARY

In this chapter, the basis and details of the proposed control strategy were described. In order to enable sag ride-through of an ac motor VSD (with a VSI configuration), it is suggested to maintain the dc bus voltage at the nominal (rated) value by recovering the kinetic and magnetisation energy available in the motor. Operation of the basic control loops used for speed and current control of IM and SRM VSDs were discussed. In order to achieve the capacitor voltage control by recovering energy from the two sources, two additional control loops were proposed and their coordination with the existing controllers in the VSD was explained. The mathematical equations for power flow between the ac mains, dc bus capacitor and the ac motor controlled by field orientation technique were presented. As seen from the control structure of both IM and SRM, the proposed strategy is applicable to both the motor types. In the forthcoming chapters the simulation results of SRM and IM VSDs when controlled by this strategy will be analysed.

CHAPTER 3

PERFORMANCE OF A SYNCHRONOUS RELUCTANCE MOTOR DRIVE

3.1 INTRODUCTION

In this chapter, the voltage sag ride-through performance of a synchronous reluctance motor variable speed drive (SRM VSD) under the proposed control strategy is presented. The details on the field orientation of an SRM can be found in Appendix C. The control of an SRM, as illustrated in Subsection 2.3.2, is modelled in MATLAB™.

Initially, there will be a brief mention on the type of voltage sags that will be applied in this simulation. Then, the performance results of the SRM VSD during normal ac supply conditions as well as during a sag will be presented. From these results, the reasons for nuisance tripping of the VSD during a voltage sag will be discussed. Finally, the voltage sag ride-through performance of the SRM VSD utilising the proposed control strategy will be verified. It may be recalled that, as per the strategy defined in Section 2.2, the bus voltage will be maintained at the nominal value during a sag by recovering the kinetic energy available in the rotating mass when motor speed is above the cut-off limit (which is 10% of the motor base speed), or by recovering the magnetising energy available in the motor winding inductances below the cut-off speed limit. Because energy is recovered from two sources under different conditions, the simulation results will be presented in three parts, viz. (a) operation above the cut-off speed by recovering kinetic energy, (b) operation below the cut-off speed by recovering magnetising energy and (c) coordinated sag ride-through at all speeds by recovering from both sources of energy.

Since kinetic energy is proportional to the square of the motor speed, it can supply the dc bus for a longer duration and thus provide a longer sag ride-through operation if the rate of speed drop is low. The speed drop of the motor during kinetic energy recovery depends on two factors, viz. (a) amount of energy regenerated and (b) the load. The regenerated energy is utilised to charge the dc bus capacitor as well as to compensate for the resistive losses in the motor windings. The effect of reducing the bus capacitance will be studied on the voltage sag ride-through behaviour of the SRM VSD later in this chapter. As far as the effect of load is concerned, the sag ride-through duration will be maximum when the load on the motor is a minimum. In this thesis, both constant torque and fan type loads are considered. Fan type loads, in which the torque reduces with square of the motor speed ($T_L \propto \omega^2$), are expected to respond to this control strategy for much longer duration as compared to constant torque loads. In this chapter, performance of the SRM VSD with a constant torque load will be discussed whereas the performance results for a fan type load will be discussed in Appendix I.

3.2 SAG TYPES UNDER STUDY

Section 1.3 presented four types of voltage sags, viz., Type A, B, C and D, which were classified on the basis of whether they are single-phase or three-phase sags and whether there are any phase shifts involved. One of the main reasons the effect of phase angle jump is not critically analysed is because this parameter is not quantified and there are no sensing equipment available to monitor phase jumps. The effect of phase angle jumps on critical equipment is not well understood [7-8] and requires further investigation. In a VSD with diode-bridge front-end, a phase shift tends to lead to a single-phasing situation [7]. In this thesis, the effect of phase shifts in the incoming supply is not studied.

Of the remaining two types of sags, viz. a three phase sag (Type A) and a single phase sag (Type B), the three phase sag accounts for a large reduction in the dc bus voltage but does not lead to a high dc voltage ripple. A single phase sag results in a reduction of two phase-

to-phase input voltages and in this case, though the average dc bus voltage is not affected as much as in a three-phase sag, it causes high ripple in the capacitor charging current and in the dc capacitor voltage. Both these types of sags can cause nuisance tripping of VSDs.

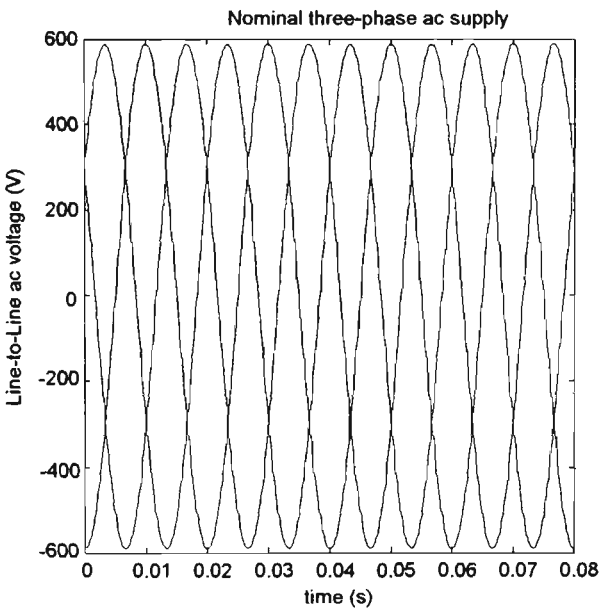
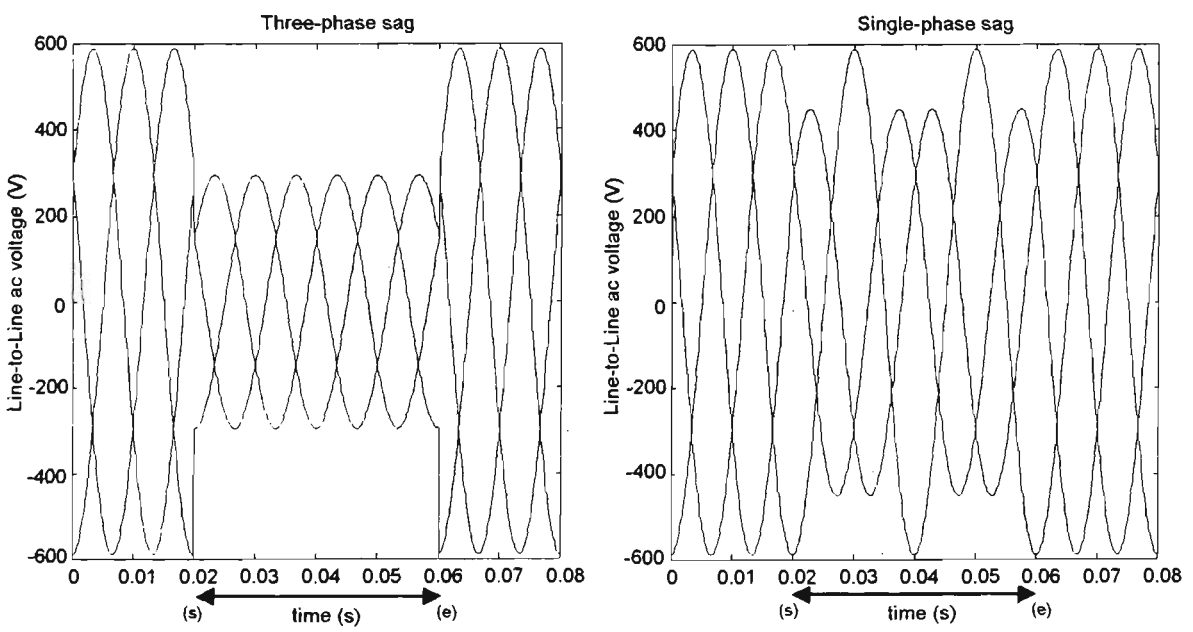


Figure 3.1 A nominal 3 phase, 415 V ac, 50 Hz power supply (Line-to-line voltages)



(a) a three-phase sag, (b) a single phase sag

Figure 3.2 A 50% Voltage sag of duration 2 cycles (Line-to-line voltages)

A nominal ac power supply of 3 phase, 415 V ac, 50 Hz is considered in the simulation work. Figure 3.1 and Figure 3.2 show a nominal power supply condition and a 50% voltage sag of duration 2 cycles (both three-phase and single-phase) respectively. The sag condition is indicated by a double-sided arrow in Figure 3.2 with the start and end of the sag indicated as (s) and (e) respectively.

As reported in [4], VSDs are likely to trip when subjected to a voltage sag of magnitude greater than 20% and duration more than 12 cycles. In this thesis, the behaviour of VSDs when subjected to both single-phase and three-phase sags of magnitude 50% and duration 50 cycles (1 second) will be studied. From the simulation results shown later in this chapter, it can be seen that the proposed control strategy provides identical sag ride-through behaviour for both types of sags. Since a three-phase sag represents the worst case situation, the performance of the proposed control strategy will be analysed by applying a three phase sag.

3.3 NORMAL SPEED CONTROL OPERATION OF AN SRM VSD

In this section, initially, the speed control behaviour of the SRM VSD will be verified under normal ac supply conditions. Then, the behaviour of the VSD when subjected to a voltage sag of both three-phase and single-phase types will be analysed. From the simulation results, the reasons for VSD tripping on a sag will be discussed.

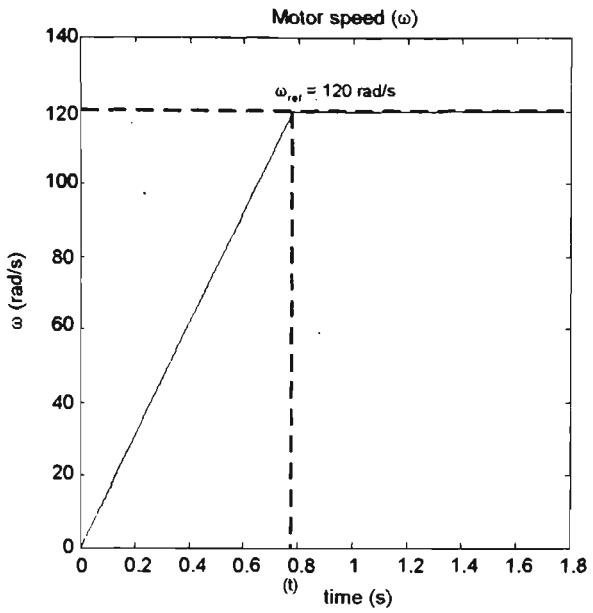
3.3.1 PERFORMANCE UNDER NORMAL OPERATING CONDITIONS – NO SAG

Here, the response of an SRM VSD, under ideal power supply conditions (as shown in Figure 3.1), is studied. This situation corresponds to Control Situation 1 as defined in the control strategy (Subsection 2.2.2). The torque reference is controlled by the Speed

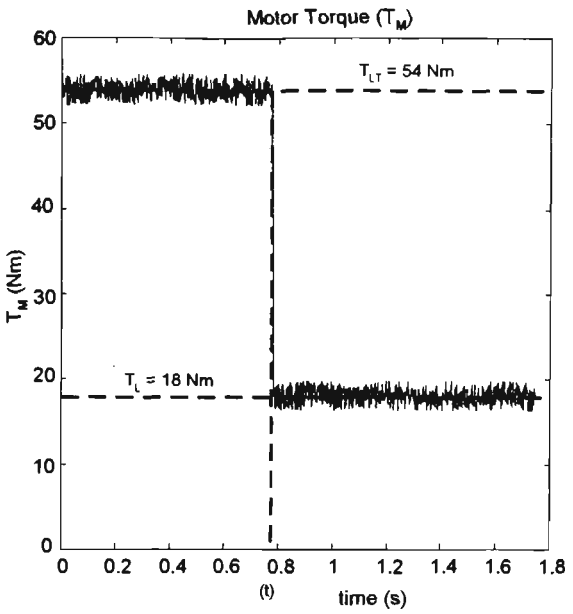
Controller which aims to control the motor speed at the set reference. The SRM parameters and VSD set points are listed in Appendix F and the details of Speed Controller tuning are given in Appendix H. The SRM VSD was tested at various operating conditions and the performance can be found to be satisfactory. The behaviour of the SRM VSD during acceleration and at steady-state speed control is analysed in this subsection.

Simulation conditions: The speed control simulation of the SRM VSD is carried out for a duration of 1.75 seconds. An inverter switching frequency of 5 kHz is considered. When a vector switching occurs, normally the transition takes place between the two inverter switches in any one inverter leg, with one switch turning on and the other turning off (refer Appendix D for details on switching sequence of the inverter switches during field orientation control). Assuming that in one switching cycle, all the six switches complete a full switching transition (i.e. on-to-off and off-to-on), a sampling frequency of 30 kHz is chosen here so that the VSD response during every transition is gathered. The motor is started from standstill and a speed reference of 120 rad/s is applied. The load torque (T_L) and the torque limit (T_{LT}) are set at 50% and 150% of the rated motor torque (36 Nm) respectively. The motor flux reference is set at the rated value (i.e. i_{sdref} = 9A). A system inertia (J) of 0.23 kgm^2 is considered.

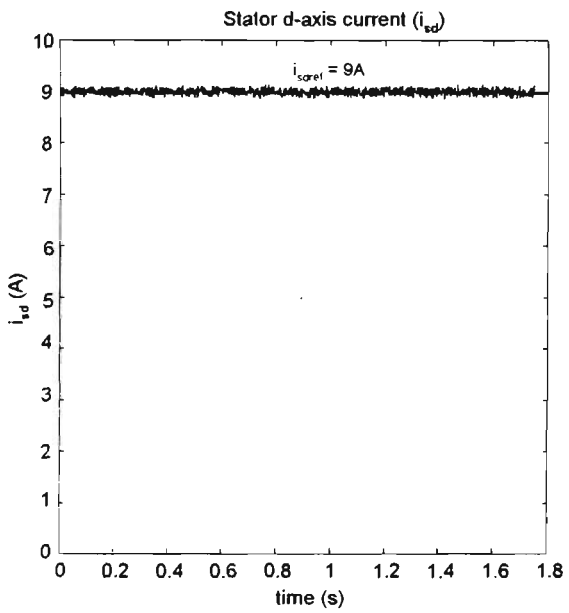
SRM VSD response: The SRM speed (ω), torque (T_M), magnetising current (i_{sd}) and torque producing current (i_{sq}) during acceleration and steady-state speed control are shown in Figure 3.3 (a) to (d) respectively. The dc bus characteristics, viz. the capacitor output current (I_{out}), the capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) are shown in Figures 3.4(a) to (c) respectively. The transition from acceleration to steady-state is indicated by a dotted vertical line (t).



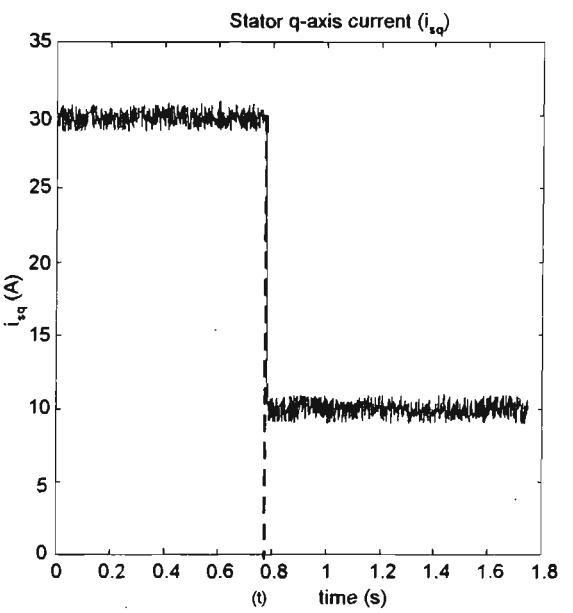
(a) Speed (ω)



(b) Torque (T_M)

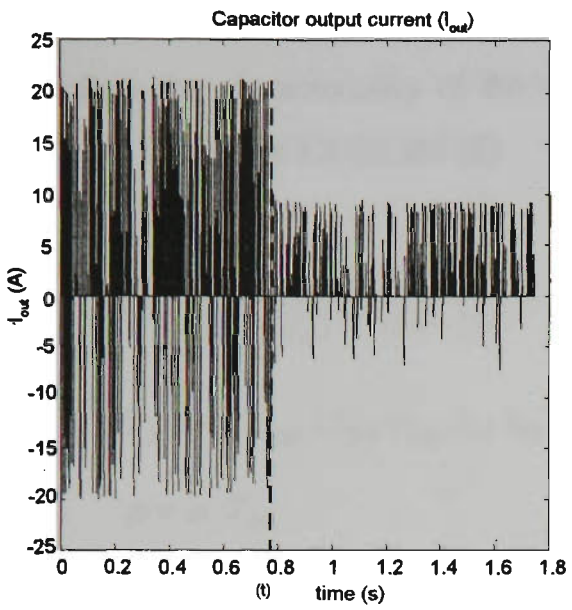


(c) Magnetising current (i_{sd})

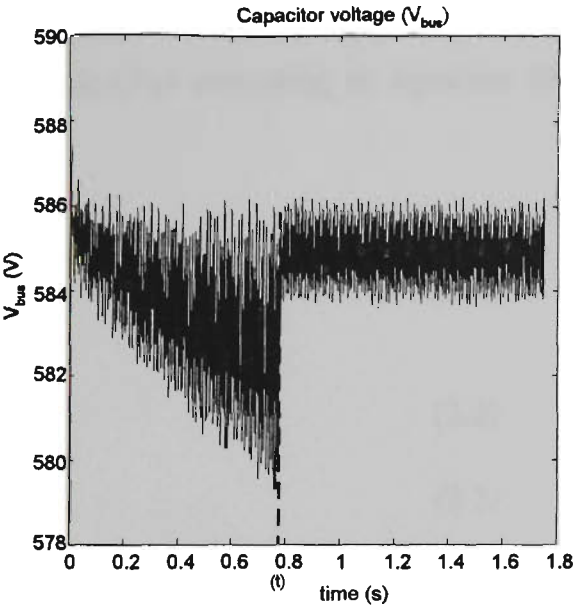


(d) Torque producing current (i_{sq})

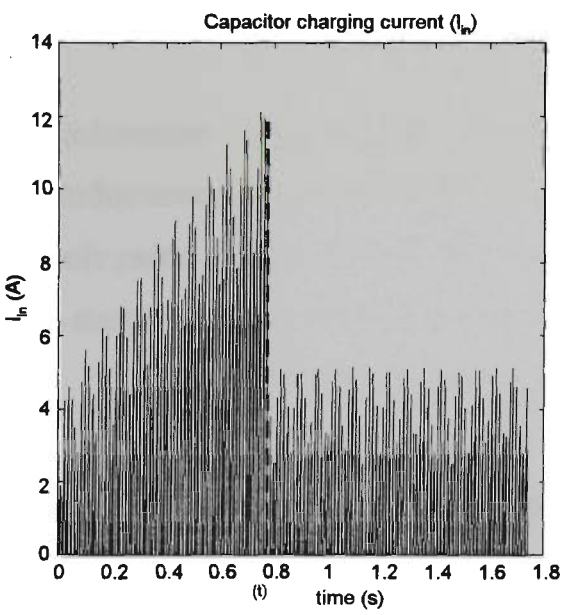
Figure 3.3 SRM response during acceleration and steady-state speed control under ideal ac supply conditions



(a) Capacitor output current (I_{out})



(b) Capacitor voltage (V_{bus})



(c) Capacitor charging current (I_{in})

Figure 3.4 SRM VSD dc bus characteristics during acceleration and steady-state speed control under ideal ac supply conditions

As shown in Figures 3.3(a) and (b), the SRM is found to accelerate to the set speed under torque limit. The observed acceleration time of about 0.75 seconds is found to coincide with the duration calculated using equation (3.1). The motor flux (i_{sd}) is found to be controlled at the rated value (Figure 3.3(c)) during both acceleration and steady-state.

Because of this constant flux control, the torque producing current component i_{sq} is found to follow the characteristics of the motor torque (T_M) according to equation (3.2) as observed in Figures 3.3 (b) and (d).

$$\Delta t = \frac{J\,\Delta\omega}{(T_M - T_L)} = \frac{0.23*120}{(54-18)} = 0.766\,\text{s} \tag{3.1}$$

$$T_M = \frac{3}{2} N_{pp}\,(L_{sd}\text{-}L_{sq})\,i_{sd}\,i_{sq} \tag{3.2}$$

$$p = \omega\ T_M \tag{3.3}$$

where,

J - system inertia,

T_M - motor torque

T_L - load torque

L_{sd} –stator d-axis inductance

L_{sq} –stator q-axis inductance

N_{pp} – number of pole pairs

p - power input to motor

ω - motor speed

The dc bus characteristics (as shown in Figure 3.4) are found to be in accordance with the motor characteristics throughout the operation. During acceleration, since the power applied to the motor (p) increases according to equation (3.3), the dc output current to the motor (I_{out}) is found to increase in Figure 3.4(a). Hence, the dc voltage ripple and the capacitor charging current are also found to increase during acceleration as observed in Figures 3.4 (b) and (c) respectively.

Once the set speed is reached, the motor speed is found to be maintained at this value as observed in Figure 3.3(a). The implementation of the integrator wind-up reset feature has ensured that no overshoot has occurred in the motor speed during the transition from acceleration to steady state, which otherwise might have occurred due to the saturation of

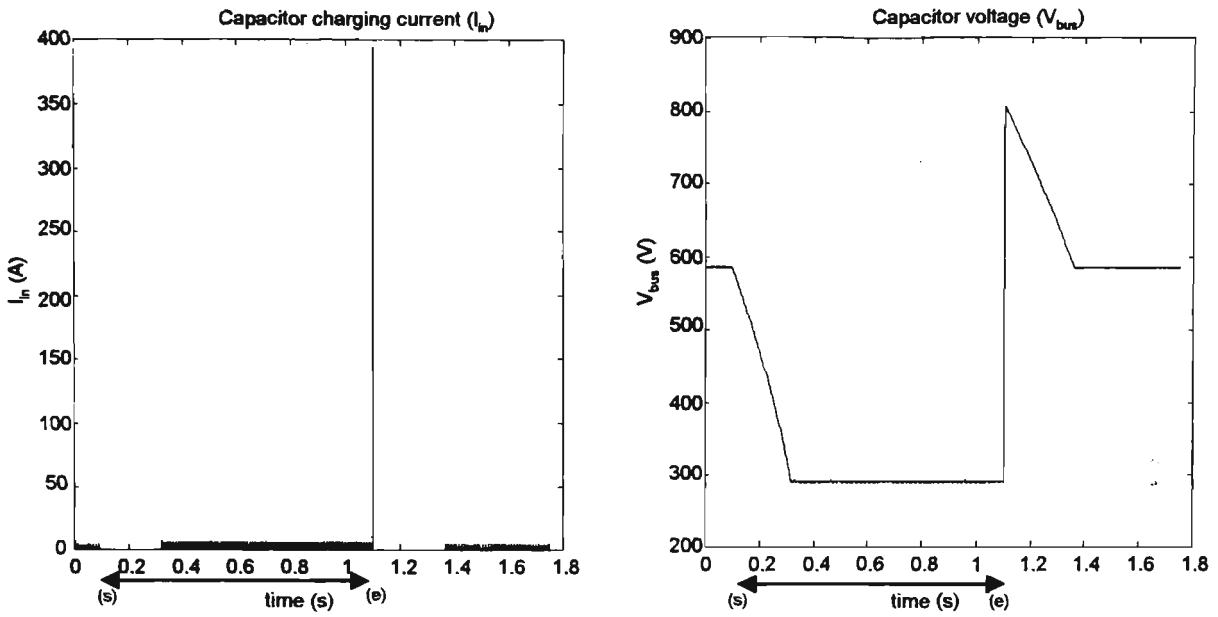
the Speed Controller because of high integrator (I) gains. On reaching steady-state, the motor torque (T_M) is found to settle down at the load torque level in Figure 3.3(b). Accordingly, the capacitor output current (I_{out}), the capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) also settle down at steady-state values corresponding to the operating conditions (speed and torque) as found in Figures 3.4 (a), (b) and (c) respectively.

3.3.2 VSD BEHAVIOUR DURING A VOLTAGE SAG

The effects of both three-phase and single-phase voltage sags on the SRM VSD operating under steady-state speed control are presented in this subsection.

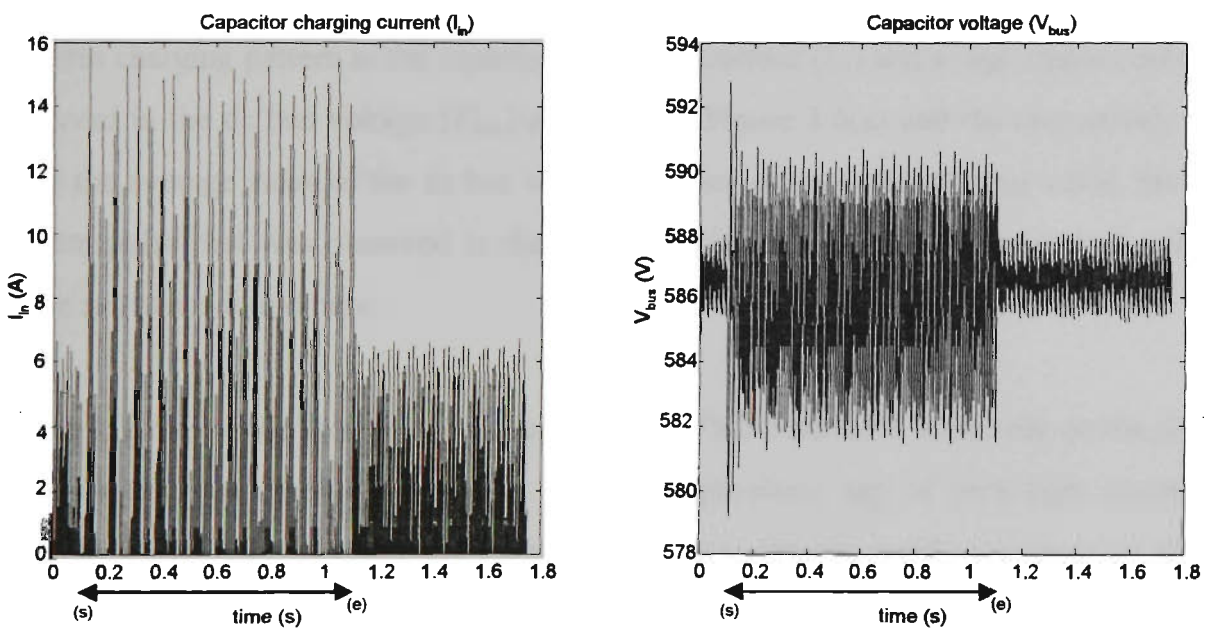
Simulation conditions: Both single-phase and three-phase voltage sags of magnitude 50% and 1 second duration were applied on the VSD when the SRM was running in steady-state at 120 rad/s with a load torque (T_L) of 18 Nm. Other operating conditions such as motor flux (i_{sd}) , torque limit (T_{LT}), switching frequency and sampling frequency are maintained at the same values as in the normal supply condition trials discussed in Subsection 3.3.1.

SRM VSD response: During sags of both types, the speed and torque behaviour of the SRM was found to be unaffected from the steady-state values observed during normal ac supply conditions (Figure 3.3(a) and (b)). Also, the SRM flux (i_{sd}) was maintained at the rated value during both sag conditions. The control system is able to take care of the ac supply variations and continue the VSD operation without any degradation in the motor performance. Since the power drawn by the motor has not changed, the characteristics of the dc output current I_{out} to the inverter are also unchanged from a no sag situation. However, the dc bus characteristics, especially the capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}), are most affected during a sag and their behaviour in the case of three-phase and single-phase sags are shown in Figures 3.5 and 3.6 respectively.



(a) Capacitor charging current (I_{in}) (b) Capacitor voltage (V_{bus})

Figure 3.5 SRM dc link characteristics during a three-phase sag



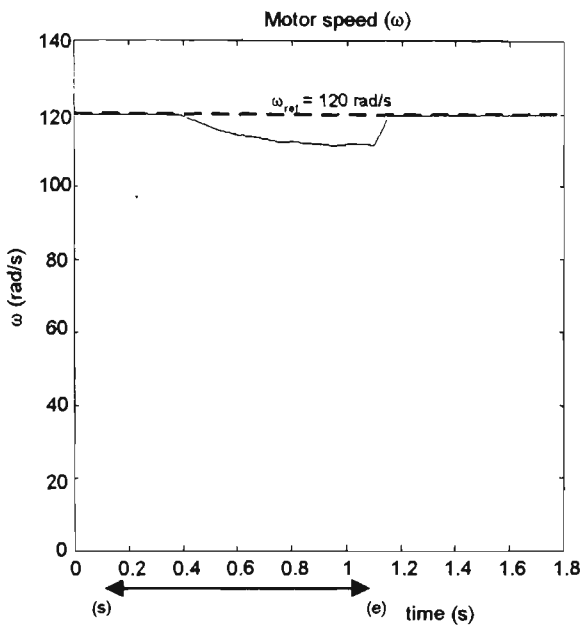
(a) Capacitor charging current (I_{in}) (b) Capacitor voltage (V_{bus})

Figure 3.6 SRM dc link characteristics during a single-phase sag

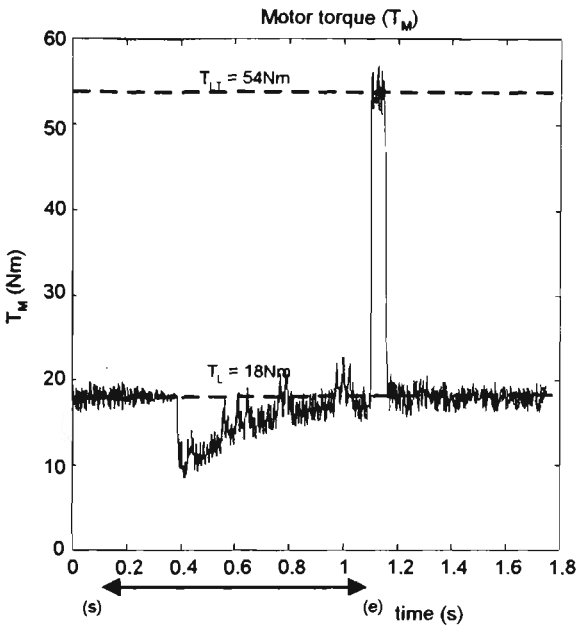
In the case of a three-phase sag, as observed in Figures 3.5(a) and (b), initially there is no flow of capacitor charging current (I_{in}) because the rectifier diodes are reverse biased and the capacitor discharges the stored energy to the motor until V_{bus} becomes lower than the line-to-line ac supply peak voltages. Once V_{bus} becomes lower than the ac supply peaks, the capacitor is charged uniformly by all the three phases with minimum dc voltage ripple. The level of the capacitor voltage V_{bus} during the sag condition depends on the magnitude of the sag and the current drawn from the dc bus (I_{out}) which depends on the load. When the ac supply returns to normal, a very high current pulse is observed in the capacitor charging current (I_{in}) with its magnitude increasing with the sag magnitude, but it is usually many times the current rating of the rectifier diodes. This high current results in an overshoot of the dc bus voltage (V_{bus}) which slowly returns to normal by discharging to the inverter load (Figure 3.5(b)).

In the case of a single-phase sag, the capacitor is charged by the unaffected line-to-line supply peaks and discharges during the rest of the supply cycle. This results in a non-uniform charging pattern in the capacitor charging current (I_{in}) and a high ripple content is observed in the dc bus voltage (V_{bus}) as shown in Figure 3.6(a) and (b) respectively. But since the average value of the dc bus voltage remains close to the nominal value, the high current pulse that was observed in the capacitor charging pattern at the end of a three-phase sag is not found here.

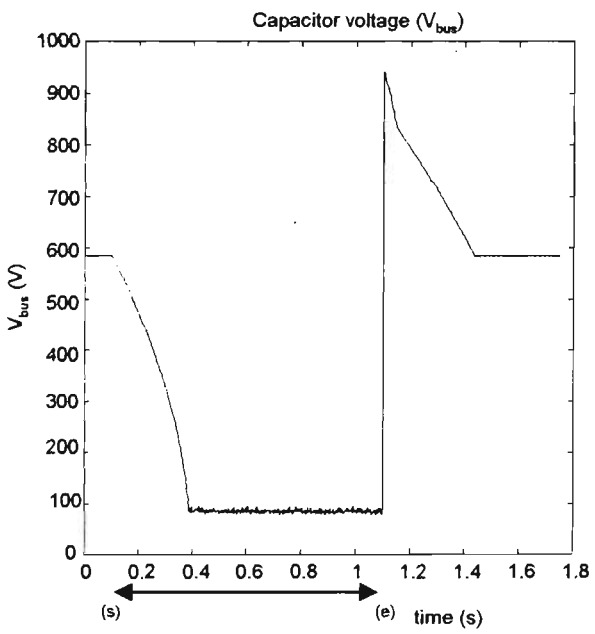
As the sag magnitude increases, its impact on the VSD behaviour, especially on the dc bus characteristics becomes more severe. With a single-phase sag of very high magnitude (such as 85%), the SRM was still found to operate at the set speed and torque levels but the dc capacitor voltage ripple and the capacitor charging current were found to increase further. However, when subjected to a three-phase sag of such high magnitude, apart from the dc bus characteristics, the speed and torque performance of the SRM was also found to be affected. Figure 3.7 shows the speed (ω), torque (T_M), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) of the SRM when subjected to a 85% three-phase sag for 1 second.



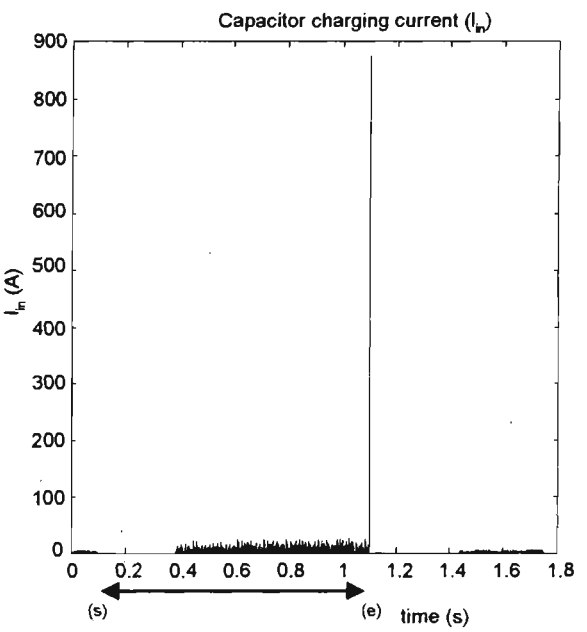
(a) Speed (ω)



(b) Torque (T_M)



(c) Capacitor voltage (V_{bus})



(d) Capacitor charging current (I_{in})

Figure 3.7 SRM VSD behaviour when subjected to a 85% three-phase sag for 1 second

It can be observed that, after the occurrence of sag, the SRM operates at the set speed for a small duration when dc capacitor is able to supply the energy required by the motor as seen in Figure 3.7(a) and (c). When the dc voltage drops below a particular value (around

100V in this case) which depends on the sag magnitude, the dc link does not have the energy required by the motor to operate at the set speed and torque levels and hence the motor speed drops below the set reference. Now, the motor torque is also found to reduce as observed in Figure 3.7(b). When V_{bus} becomes lower than the ac supply peaks, the capacitor is charged by the incoming ac supply and V_{bus} is maintained at this new level. Now, the VSD is able to drive the motor at a lower speed but with full load torque. The speed drop behaviour during the sag is explained by the power flow equation (3.4) and it can be understood that the speed drop (ω) depends on the sag magnitude (which affects the capacitor voltage V_{bus}) and the load on the motor (T_L)

$$T_L \omega_r = V_{bus} I_{out} \tag{3.4}$$

where,

I_{out} - the dc current output to the inverter load

Once the ac supply returns to normal level, very large capacitor charging current (I_{in}) appears because of the low dc bus voltage level during a sag (Figure 3.7(d)). This high charging results in the overshoot of the capacitor voltage V_{bus} which returns back to normal level by discharging to the motor load.

3.3.3 REASONS FOR VSD TRIPPING ON A SAG CONDITION

From the above results, it is clear that both three-phase and single-phase sags affect the performance of the VSD, especially the dc bus characteristics, with the impact of a three-phase sag more severe than a single-phase sag.

In the presence of a three-phase sag, the dc bus voltage reaches a low level depending on the magnitude of the sag and the load, which can cause the VSD to trip due to an under-voltage fault. When the sag condition is over, very high capacitor recharging current (I_{in}) results and in spite of being limited by the circuit impedances, it is usually several times

the current handling capacity of the rectifier diodes. In such a case, the VSD can trip due to the over-current protection fault.

In the case of a single-phase sag, the behaviour of the SRM is relatively better, but the possibility of VSD tripping cannot be ruled out. When the sag magnitude is high, the dc bus ripple voltage increases and can cause an under-voltage fault when the voltage reduces below the trip level. Also, the capacitor charging current I_{in}, which increases with the sag magnitude can also cause the VSD to trip due to an over-current fault.

In order to protect the VSD hardware, the under-voltage trip setting is typically kept between 70% and 85% of the nominal dc voltage [19]. Similarly, the over-current trip is usually set in the range of 200% to 250% of the rated motor current. As seen from the dc bus characteristics during the sag trials, it is clear that voltage sags can cause nuisance tripping of VSDs due to under-voltage or over-current faults with the probability of such events increasing at higher sag magnitudes, longer sag durations and increased load conditions.

As seen from the simulation results, the dc bus capacitor can supply energy to the motor for a few cycles. By increasing the bus capacitance (C), the rate of dc voltage drop can be reduced, i.e. an under-voltage trip occurrence can be delayed. But the main problem of increasing C would be the increased recharging currents that would occur at the end of the sag which can result in an over-current trip. Similarly, reducing C may prevent the VSD from tripping due to an over-current fault but the dc voltage reduces very rapidly in this case which can cause an under-voltage fault sooner than with a higher C. Hence, varying capacitor value alone is not an appropriate solution to this sag problem. Ride-through measures are necessary in order to achieve continuity of operation of the VSD during a sag. The performance of the proposed control strategy will be studied in an SRM VSD in the forthcoming sections.

3.4 OPERATION UNDER A SAG AT HIGH SPEEDS – BUS VOLTAGE CONTROL BY RECOVERING KINETIC ENERGY

In this section, the voltage sag ride-through performance of the SRM VSD by recovering the kinetic energy available in the rotating mass at higher motor speeds will be studied. The minimum cut-off speed for this operation is defined as 10% of the motor base speed (15.7 rad/s) because below this speed less than 1% of the kinetic energy at rated speed is only available. This corresponds to Control Situation 2 as defined in the control strategy (Subsection 2.2.2). In this situation, the control algorithm attempts to maintain the dc bus voltage at the nominal level by recovering the rotor kinetic energy. The Bus Voltage Controller 1 generates a reverse torque reference depending on the dc bus voltage error and the direction of the i_{sq} (torque producing current) is reversed. In this situation, motor speed is not controlled. The flux (i_{sd}) is maintained at the rated value to ensure proper operation of the motor in the regeneration mode. The SRM VSD behaviour during this control strategy is explained by equations (2.25), (2.9) and (2.10) which are repeated here for convenience:

$$I_{out} = \frac{2(V_{sd} i_{sd} + V_{sq} i_{sq})}{3V_{bus}} \tag{3.5}$$

$$V_{sd} = R_s i_{sd} + L_{sd} \frac{di_{sd}}{dt} - \omega \; L_{sq} i_{sq} \tag{3.6}$$

$$V_{sq} = R_s i_{sq} + L_{sq} \frac{di_{sq}}{dt} + \omega \; L_{sd} i_{sd} \tag{3.7}$$

where,

I_{out} - dc output current to the inverter

V_{sd}, V_{sq} - stator voltages in d-q axes

i_{sd}, i_{sq} - stator currents in d-q axes

L_{sd}, L_{sq} - stator inductances in d and q axes

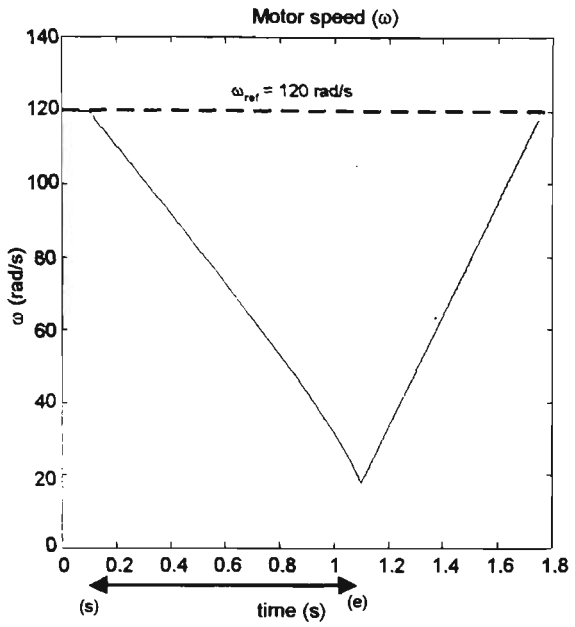
V_{bus} - capacitor voltage

ω - motor speed

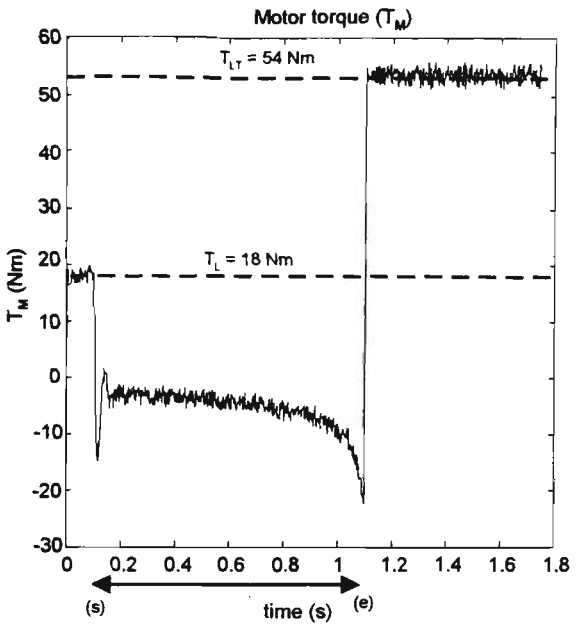
It can be seen from equations (3.5) to (3.7) that, by keeping flux (i_{sd}) constant, reversing the direction of i_{sq} would reverse the flow of I_{out} from the inverter to the dc bus capacitor as long as the motor continues to run in the same direction. It must be ensured that, only the appropriate I_{out} is recovered just to maintain the capacitor voltage at the required value and the closed loop operation of the Bus Voltage Controller 1 can take care of this requirement. The tuning of this proportional-integral (PI) controller is described in Appendix H.

Simulation conditions: In order to compare the results from the application of this control strategy with the VSD performance without any sag mitigation, simulation results are presented here when a three phase sag of magnitude 50% and duration 1 second is applied to the SRM VSD operating under the steady state conditions as previously in Subsection 3.3.2 (ω = 120 rad/s and T_L = 18 Nm).

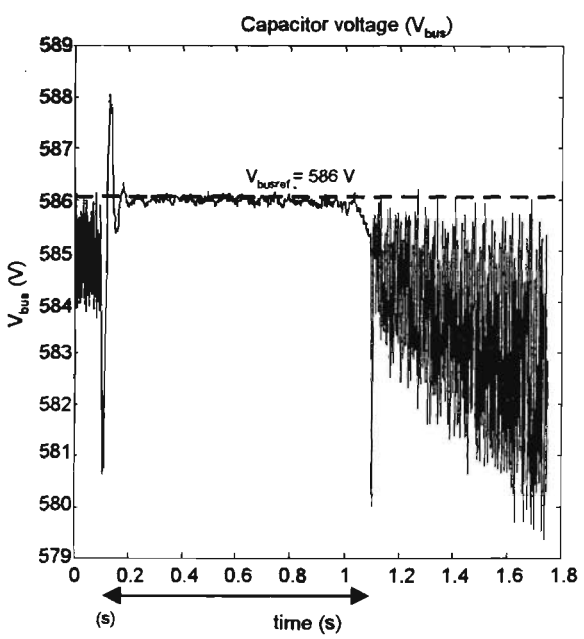
SRM VSD response: The performance results of the SRM VSD, viz. speed (ω), torque (T_M), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) during this kinetic energy recovery control is presented in Figures 3.8(a) to (d) respectively. The sag duration is indicated in these figures as previously. The motor flux is maintained at the rated value throughout this operation. When a sag is detected, the motor torque is found to reverse and is controlled at a low negative value by the Bus Voltage Controller 1 as observed in Figure 3.8(b). As seen in Figure 3.8(c), the capacitor voltage V_{bus} is controlled at the setpoint within a few milliseconds after the occurrence of the sag. Since, V_{bus} is maintained constant at the rated dc value, the rectifier diodes are reverse biased during the sag and there is no flow of capacitor charging current (I_{in}) in this period. Because of the regenerative operation of the motor, its speed is found to drop at a constant rate as observed in Figure 3.8(a). The observed speed drop of about 100 rad/s during this regeneration is more than the speed drop that would occur during normal coasting as calculated using equation (3.8). From the SRM torque response (Figure 3.8(b)), it is observed that, as the motor speed decreases, the regenerated torque (T_M) increases. This behaviour is explained by equation (3.9) because power required at the dc link is constant.



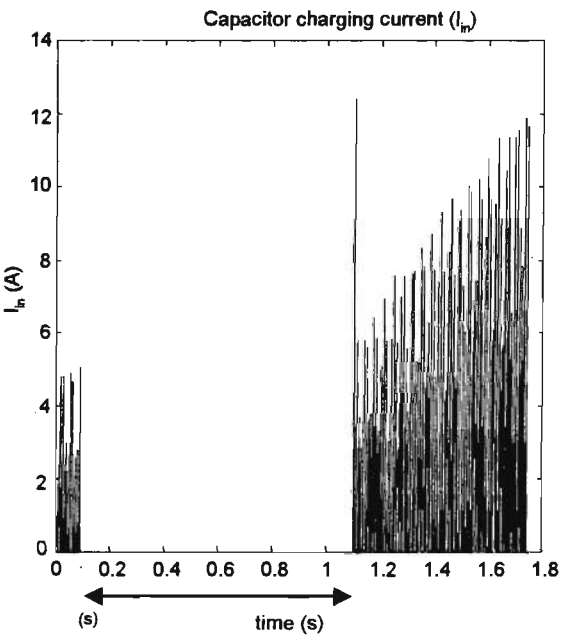
(a) Speed



(b) Torque



(c) Capacitor voltage (V_{bus})



(d) Capacitor charging current

Figure 3.8 SRM VSD response during kinetic energy recovery in a sag condition

$$d\omega = \frac{(T_M - T_L)\,dt}{J} = \frac{(0-18)}{0.23} = -78.26 \text{ rad/s} \qquad (3.8)$$

$$p = V_{bus} I_{out} = T_M \omega \qquad (3.9)$$

where,

T_M - motor torque

T_L - load torque

J - system inertia

p - power applied to the motor terminals

V_{bus} - capacitor voltage

I_{out} - current output from the dc bus to the motor

ω -motor speed

When the sag is over, normal speed control operation is resumed with the motor accelerating under torque limit towards the set speed. The large current pulse which was observed in I_{in} at the end of the sag during the trials without any control modifications (refer Figure 3.5(a)) are not present now (Figure 3.8(d)).

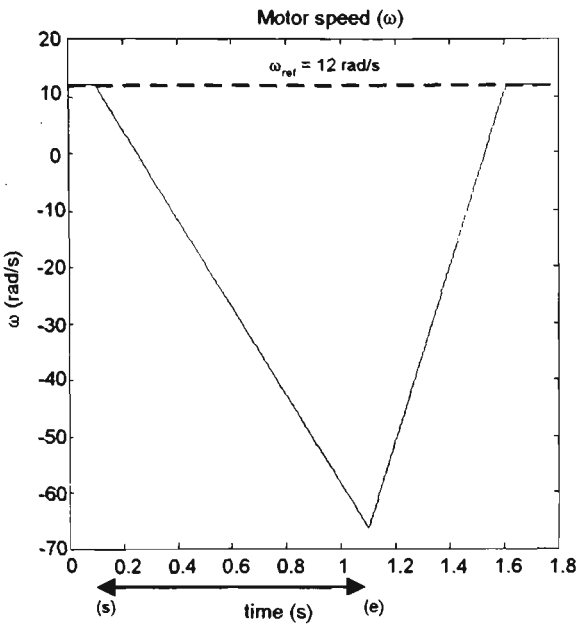
From the above simulation results, it is verified that the VSD can over-ride a voltage sag by recovering the kinetic energy available in the rotating mass. As mentioned in Section 3.2, here the ride-through behaviour was studied by applying a three-phase sag. From the observed response, it is not difficult to infer the VSD behaviour during other sag conditions when controlled by this strategy. It may be recalled from Subsection 2.2.1 that, the set point for the bus voltage controller during a sag is 100% of the nominal dc bus voltage. Since the bus voltage (V_{bus}) is maintained constant at the nominal level, the rectifier diodes are reverse biased during the entire sag duration. With this type of dc voltage control by utilising the energy from the motor, the rectifier operation and hence the dc bus characteristics would not be any different in the case of a single-phase sag or with different sag magnitudes. Hence, it can be concluded that, this proposed control strategy will provide the same type of sag ride-through performance for both single-phase and three-phase sags and for all sag magnitudes. Since a sag ride-through can be achieved only until the motor speed is above the cut-off limit, longer ride-through times can be expected by this strategy if the initial motor speed is high and/or the load on the motor is less.

3.5 OPERATION UNDER A SAG AT LOW SPEEDS – BUS VOLTAGE CONTROL BY RECOVERING MAGNETISING ENERGY

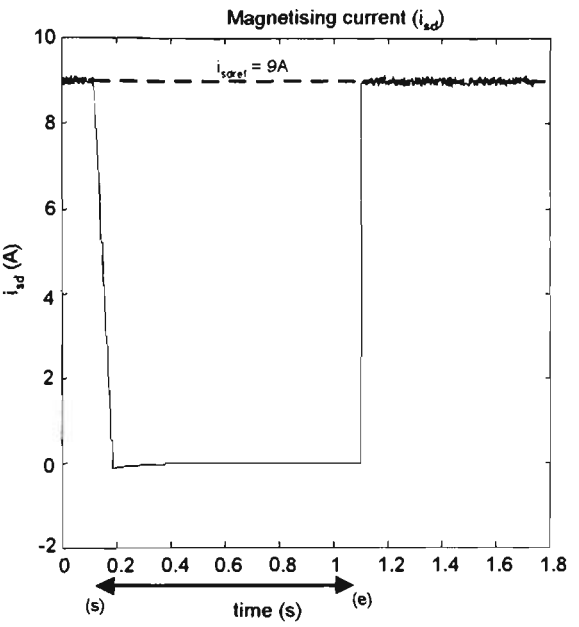
At low speeds (i.e. below 15.7 rad/s), since the kinetic energy present in the rotating mass is relatively small, this strategy aims to recover the magnetising energy ($\frac{1}{2}LI^2$) present in the motor winding inductances in order to maintain the dc bus voltage at the required level. This corresponds to Control Situation 3 as defined in Subsection 2.2.2. In this situation, the torque reference is kept as zero and the magnetising current reference (i_{sdref}) is controlled (reduced) by the Bus Voltage Controller 2. The SRM behaviour under this strategy can be analysed again by using equations (3.2) to (3.4) which were referred to in the previous section. With the torque producing current i_{sq} maintained at zero value, a reduction in the magnetising current i_{sd} would reverse the polarity of the applied voltage V_{sd} and thus the direction of flow of the dc current I_{out} would be reversed from the inverter to the dc bus which charges the dc bus capacitor. The tuning of Bus Voltage Controller 2 is described in Appendix H. In this section, the low speed performance of the proposed strategy on an SRM VSD will be analysed.

Simulation conditions: A 50% three-phase sag is applied for 1 second on the SRM VSD operating at steady-state at a speed of 12 rad/s and a load torque of 18 Nm with other simulation conditions maintained as in the previous trials.

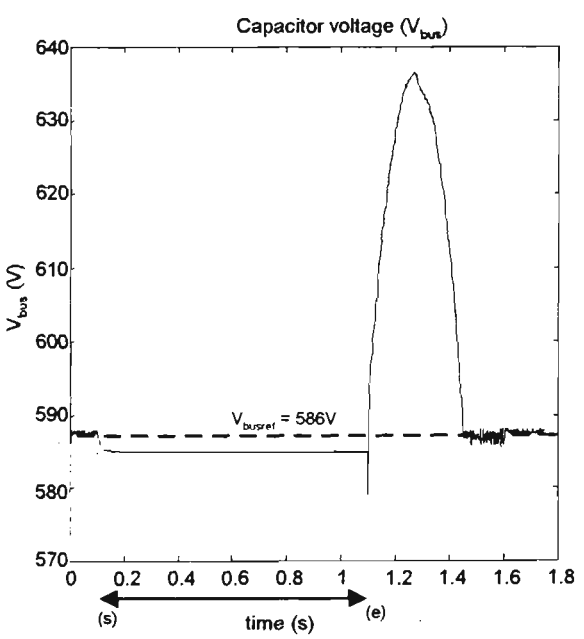
SRM VSD response: The response of the SRM speed (ω), magnetising current (i_{sd}), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}) during the bus voltage control by recovering the magnetising energy is shown in Figures 3.9 (a) to (d) respectively. As soon as the sag is sensed, the motor torque is maintained at zero level. The magnetising current, which is shown in Figure 3.9(b), is found to reduce in small steps to zero in a short duration and during this interval, the dc bus voltage is found to be controlled close to the set reference. Once the energy available in the motor winding inductances is recovered completely there is no further transfer of energy between the VSD and the motor (i.e. $i_{sd} = i_{sq} = 0$) and the dc bus capacitor voltage remains close to the



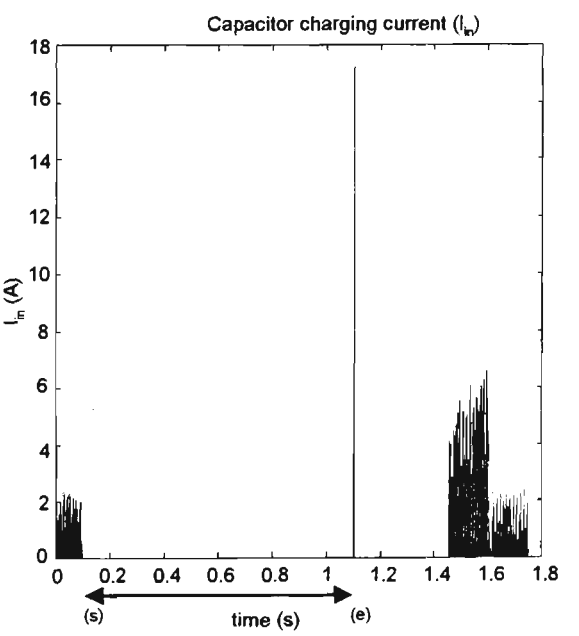
(a) Speed (ω)



(b) Magnetising current (i_{sd})



(c) Capacitor voltage (V_{bus})



(d) Capacitor charging current (I_{in})

Figure 3.9 SRM VSD characteristics during recovery of magnetising energy

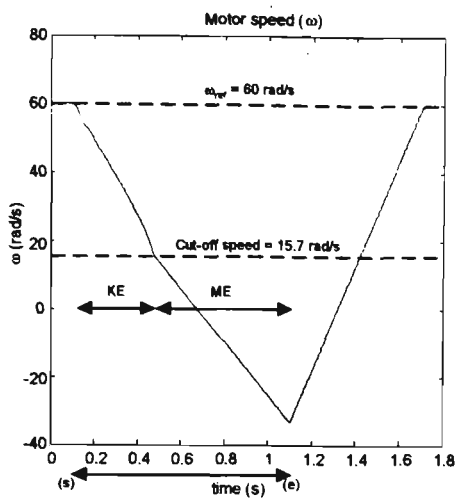
nominal level (586 V). The motor speed is found to drop to zero and then reverse as observed in Figure 3.9(a). This speed reversal happens only in types of loads such as

hoists or cranes which can rotate the motor shaft even without any power applied. In the case of frictional or fan type loads, the motor will halt after reaching zero speed. On ac supply returning to normal, the motor flux (i_{sd}) builds up to the rated value and the VSD is able to resume the speed control operation. The capacitor charging current (I_{in}) is found to be within acceptable levels as found in Figure 3.9(d). A rise in the dc bus voltage is observed in Figure 3.9(c), when the motor re-accelerates at speeds below zero because of the regenerative operation. This voltage rise will be observed only in the case of loads such as cranes and hoists and it can be discharged in the pre-charge resistor which is present in a standard VSD.

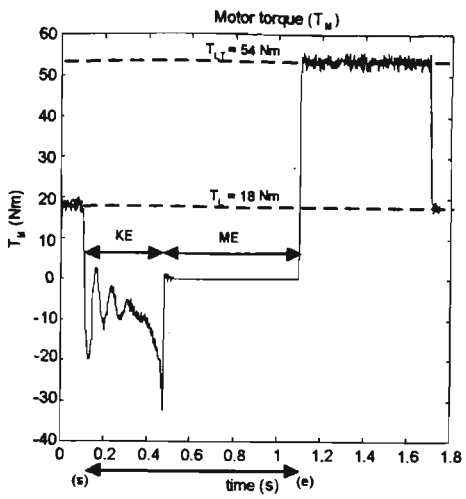
As discussed in the case of bus voltage control by kinetic energy recovery (Section 3.4), in the present control mode also the rectifier diodes are reverse biased during a sag and hence the sag ride through performance will not be affected by the sag type and the sag magnitude. Moreover, the fact that the capacitor voltage remains at the rated value even after recovering the entire energy in the motor suggests that this strategy can be employed for sags of duration longer than the applied duration in this simulation work (1 second). Also, as observed from the simulation results, this sag ride-through control is applicable even at zero speeds.

3.6 COORDINATED VSD CONTROL AT ALL SPEEDS

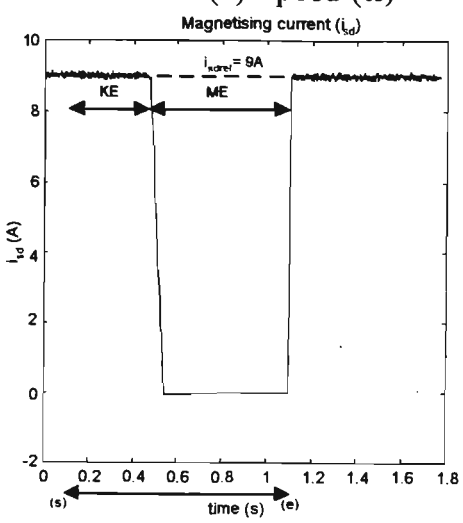
In the previous sections, the results from both modes of the proposed control strategy, viz. recovery of the kinetic energy at high motor speeds and the magnetising energy at lower speeds, were illustrated independently. It is seen that, the dc link characteristics in the VSD are improved during a sag condition and the VSD will be able to ride-through sags at both high and low motor speeds. These two operations can be combined with a smooth transition of control at the cut-off speed so that the SRM will be able to ride-through voltage sags at all ranges of speed including zero. In this section, the SRM VSD performance will be discussed at an intermediate speed where the transition of control is observed.



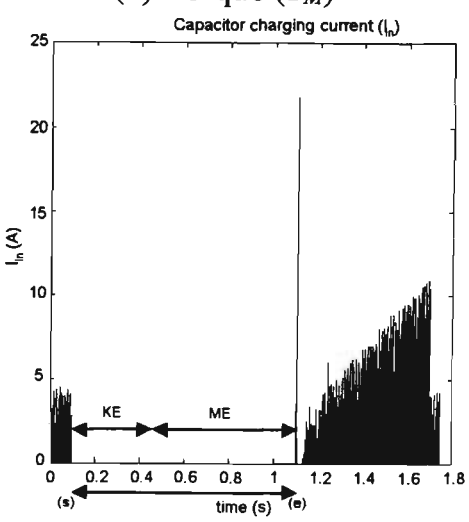
(a) Speed (ω)



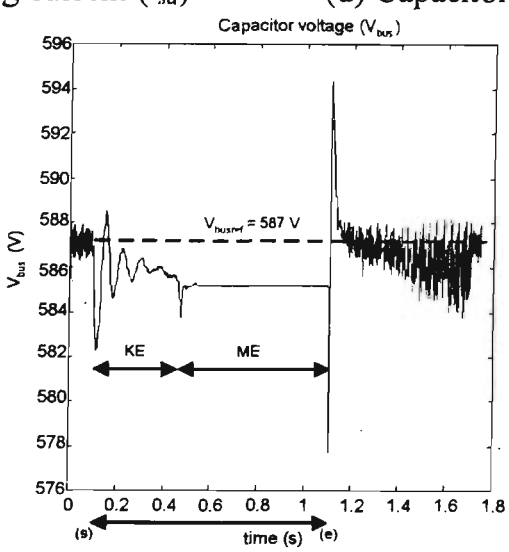
(b) Torque (T_M)



(c) Magnetising current (i_{sd})



(d) Capacitor charging current (I_{in})



(e) Capacitor voltage (V_{bus})

Figure 3.10 Behaviour of SRM VSD during combined dc bus voltage control by recovering both kinetic and magnetising energy

Simulation conditions: The inverter switching and sampling frequencies are set as previously (5 kHz and 30 kHz respectively). The initial steady state motor speed is set at 60 rad/s operating at a load torque of 18 Nm. The VSD performance during this combined control strategy is analysed by applying a 50% three-phase sag.

SRM VSD response: The characteristics of SRM during the combined operation, viz. speed (ω), torque (T_M), magnetising current (i_{sd}), capacitor charging current (I_{in}) and the capacitor voltage (V_{bus}) are shown in Figures 3.10(a) to (e). The sag condition is indicated as in previous trials and the kinetic and magnetising energy recovery periods are indicated as 'KE' and 'ME' respectively. It can be seen that the bus voltage is maintained at the set reference by initially recovering the kinetic energy until the motor speed is above the cut off speed (15.7 rad/s) and then by recovering the energy available in the inductances (by reducing i_{sd}). The motor speed is found to drop more rapidly during the regenerative operation and then coast at a slower rate during the energy recovery from the motor windings. Oscillations are observed in the motor torque response because of the non-linear relationship between torque and the bus voltage, i.e. the torque requirement increases as the motor speed decreases in order to maintain the dc bus voltage constant. Once the supply returns to normal, the motor flux reaches its rated level and the motor starts to accelerate towards the set speed. The capacitor charging current (I_{in}) is found to be within acceptable limits on normal supply recovery.

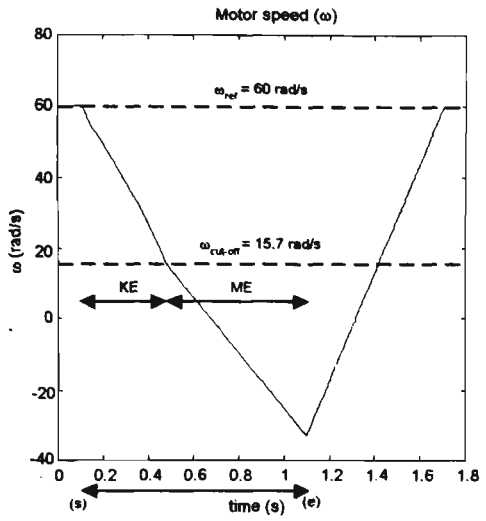
3.7 EFFECT OF LOWERING THE BUS CAPACITANCE

It was shown that, by recovering magnetising energy, the voltage sag ride-through performance can be achieved for longer durations, but while doing so, the motor speed either falls to zero or reverses. As discussed in Sections 3.1 and 3.4, during kinetic energy recovery, the rate of motor speed drop and hence the voltage sag ride-through duration of the VSD can be improved if the amount of kinetic energy recovered can be reduced. The kinetic energy recovered by the VSD control system is utilised in two ways, viz. (a) fed

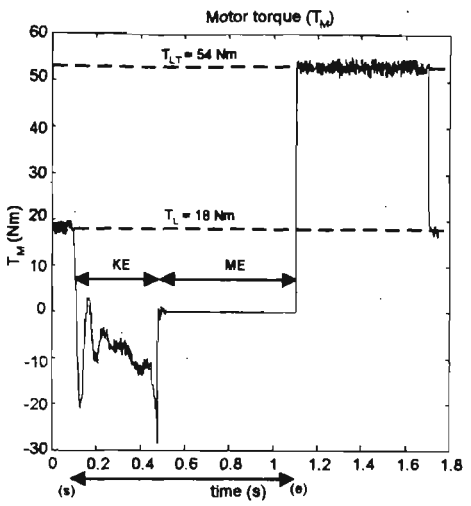
back to the motor in order to compensate the losses in the motor windings and (b) to trickle charge the capacitor in order to maintain the dc voltage at the required level. Since sag ride-through performance with less speed drop is desired, the effects of smaller dc bus capacitance on the performance of this control strategy, particularly during kinetic energy recovery, will be studied in this section.

Simulation conditions: Simulation trials, as in Section 3.6, were repeated for bus voltage control by recovering both sources of energy available in the motor. Here the bus capacitance value (C) is reduced to one-fourth the earlier value (i.e. 250 μF instead of 1000 μF). The bus voltage regulators are suitably tuned to accommodate the change in C and the tuning details of the bus voltage controllers are presented in Appendix H.

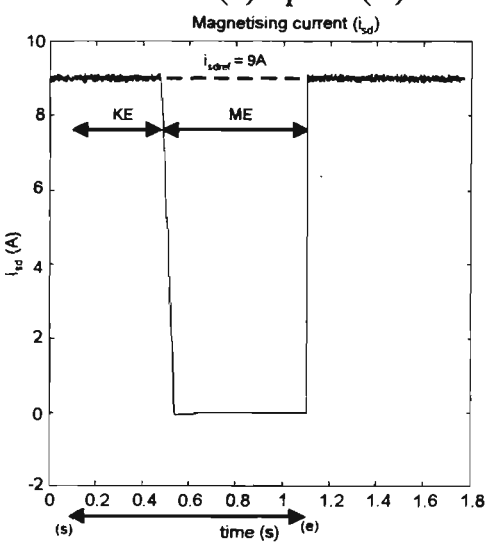
SRM VSD response: The behaviour of SRM speed, torque, magnetising current, capacitor charging current and capacitor voltage (V_{bus}) with reduced C are shown in Figure 3.11(a) to (e). It can be seen that the SRM speed response has not changed significantly from the earlier trials with a large bus capacitance (Section 3.6). In other words, sag ride through duration is found to be unaffected by the variation in C. As in the earlier trials, the motor torque reverses during the recovery of kinetic energy in order to supply the dc bus until the motor speed reaches below the cut-off speed limit (15.7 rad/s). At motor speeds below 15.7 rad/s, the flux in the motor is recovered and the dc bus voltage is maintained at the set level. Since the ride-through performance during kinetic energy recovery is of interest here, the dc current I_{out}, which shows the combined characteristics of the current recovered from the motor by regeneration as well as the current supplied to the motor in order to maintain the flux at the rated value, was studied in further detail. It was observed that, during the bus voltage control by recovering the kinetic energy, the average value of I_{out} is found to be around zero for both capacitor values, which implies that the energy recovered from the motor is utilised to mainly compensate for the losses in the motor windings. Since the capacitor voltage is maintained at the rated dc voltage by this control strategy, only a negligible current is drawn by the capacitor. In this simulation, the capacitor losses were not modelled. But even in practical



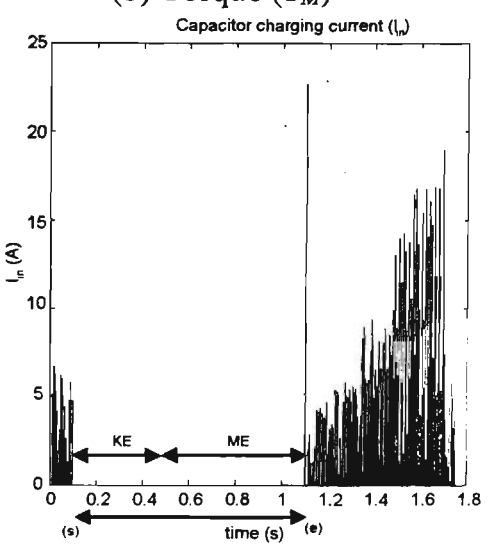
(a) Speed (ω)



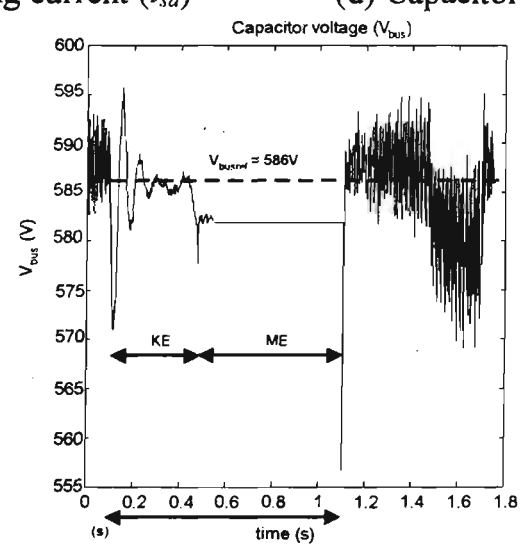
(b) Torque (T_M)



(c) Magnetising current (i_{sd})



(d) Capacitor charging current (I_{in})



(e) Capacitor voltage (V_{bus})

Figure 3.11 SRM performance under the control strategy with reduced C (250 μF).

VSDs, when the dc link voltage is maintained constant, very little trickle charging current flows into the capacitor, which is negligible compared to the energy lost in the motor windings. Hence, it can be stated that, the sag ride-through duration, when controlled by this strategy, is not influenced by the variation in the capacitor size. But, with a smaller C, the dc voltage ripple and the capacitor charging current are found to increase (as observed in Figures 3.10 and 3.11).

3.8 SUMMARY

In this chapter, the performance of an SRM VSD was studied under normal power supply conditions as well as during voltage sags. It was observed that, during a sag, the dc under-voltage and ac over-current faults are the main causes of VSD tripping and the impact of a three-phase sag is more severe on the VSD performance than a single-phase sag. The intended control strategy of maintaining the dc bus voltage at the rated value during a sag was separately demonstrated by recovering the kinetic energy at higher speeds and the magnetisation energy at lower speeds. Then, the performance was verified at an intermediate speed by combining these two control modes where a smooth control transition was observed at the cut-off speed. The under-voltage and over-current fault situations were not observed when controlled by this proposed strategy. The main advantage of this strategy is its ability to ride-through a single-phase as well as a three-phase sag and all sag magnitudes with identical performance and its ability to provide a sag ride-through even at zero motor speed.

CHAPTER 4

PERFORMANCE OF AN INDUCTION MOTOR DRIVE

4.1 INTRODUCTION

Induction motors (IMs) are the work horses of many industrial processes and are the most commonly used type of electric motors. They are preferred over other motor types because of their simpler and rugged construction and easier maintainability. But their characteristics are different from those of synchronous machines which make the control of IMs more complicated. The synchronous motors operate at a speed governed precisely by the supply frequency whereas the speed of the IMs involve a slip, which varies with the load on the motor. The tracking of the flux position is very important for the field oriented control of ac motors [26] which can be done easily in the case of synchronous motors with the help of position sensors (or indirect position sensing algorithms) whereas in the case of IMs, more complicated computations are involved. The angular relationships of flux position with respect to the stationary reference frame and their significance on the control of IMs are described in Appendix B and Subsection 2.3.1 respectively. In this chapter, the performance of the proposed strategy will be studied on an IM VSD. The control of IM VSD is simulated in MATLAB^{TM} on the basis of the model explained in Section 2.3.1.

Initially, the performance of the VSD model will be verified for normal operation under ideal ac supply conditions. Then, the response of the IM VSD when subjected to three-phase as well as single-phase sags will be presented. From the simulation results, the reasons for VSD tripping during a voltage sag condition will be analysed. Finally, the voltage sag ride-through performance of the control strategy, viz. the dc bus voltage control by recovering the energy from the rotating mass at high motor speeds and from the motor winding inductances at low speeds, will be presented. From the simulation results, it is observed that, the first mode of the control strategy, viz. kinetic energy recovery from

the rotating mass, works satisfactorily as in the case of an SRM, whereas, the dc bus capacitor voltage control by recovering the energy from the inductances is found not to work satisfactorily as envisaged by the control strategy. The reasons for this behaviour will be analysed. An improved ride-through control of induction motors at low speeds is suggested and the results will be analysed. Since, it was found in the case of an SRM VSD that the sag ride-through duration is not affected by the variation in the dc bus capacitance values when controlled by the proposed strategy, this study is not repeated here. As in the case of the SRM VSD, simulation results are presented here for constant torque loads and the sag ride-through performance results for fan type loads are shown in Appendix J.

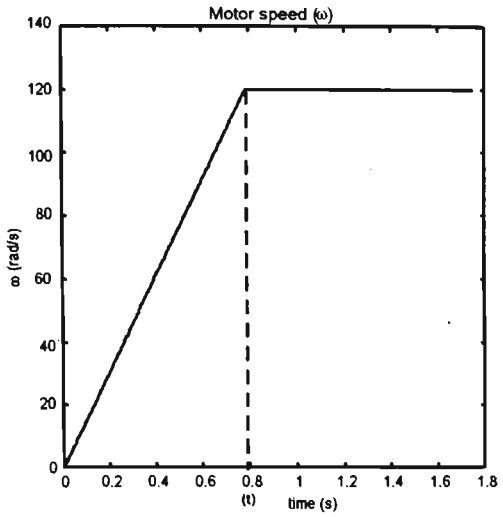
4.2 NORMAL SPEED CONTROL OPERATION OF AN IM VSD

In this section, the behaviour of an IM VSD under ideal power supply conditions as well as on voltage sag conditions (both single-phase and three-phase types) will be examined. From the results, the reasons for the VSD tripping in a sag situation will be analysed.

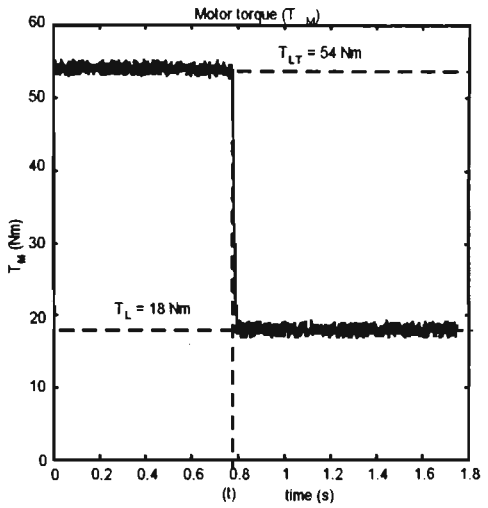
4.2.1 PERFORMANCE UNDER NORMAL OPERATING CONDITIONS – NO SAG

Here, the behaviour of an IM VSD during acceleration and steady state speed control under ideal ac supply conditions (Control Situation 1 as defined in Subsection 2.2.2) is shown. In this situation, the speed controller generates an appropriate torque reference in order to maintain the motor speed at the set value. The motor parameters are shown in Appendix E and the details of the Speed Controller tuning are explained in Appendix G.

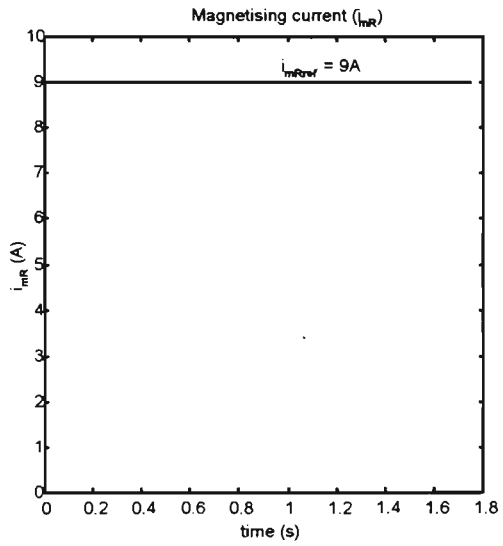
Simulation conditions: The VSD is simulated with a nominal balanced power supply, as shown in Figure 3.1. The inverter switching frequency is kept at 5 kHz and accordingly the sampling frequency is chosen as 30 kHz in order to take account of every switching transition as explained in Subsection 3.3.1. A speed reference (ω_{ref}) of 120 rad/s is applied with flux reference at the rated value (i.e. $i_{mRref} = 9$ A). The load torque (T_L) and the torque limit (T_{LT}) are set at 50% and 150% respectively of the rated motor torque (36 Nm).



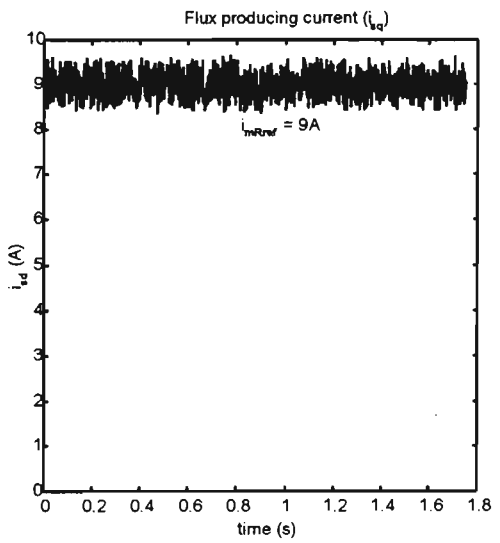
(a) Speed (ω)



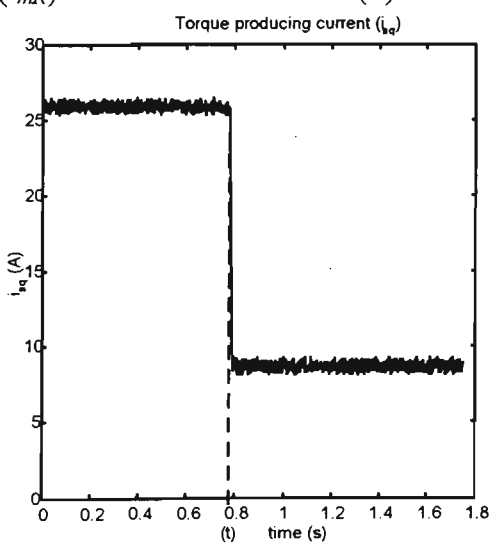
(b) Torque (T_M)



(c) Magnetisation current (i_{mR})

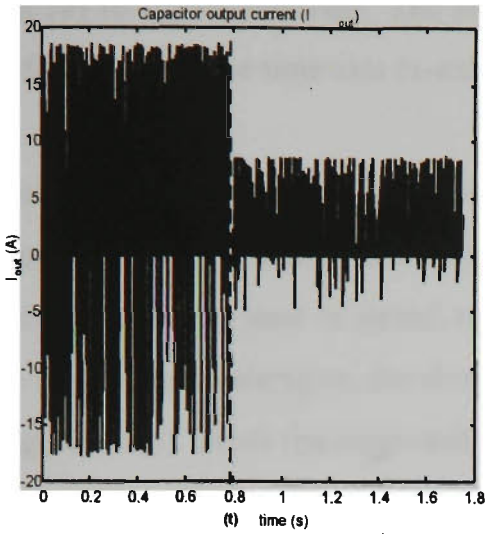


(d) Stator d-axis current (i_{sd})

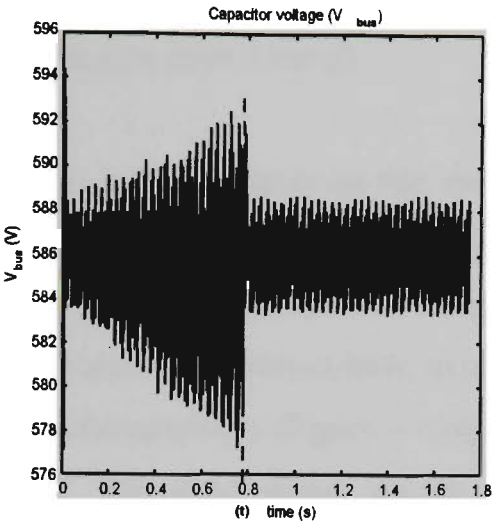


(e) Stator q-axis current (i_{sq})

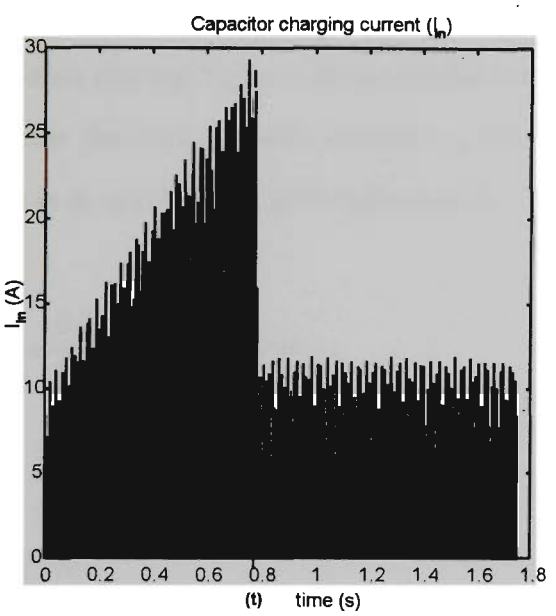
Figure 4.1 IM VSD during normal ac supply conditions



(a) dc current output to inverter (I_{out})



(b) capacitor voltage (V_{bus})



(c) capacitor charging current from rectifier (I_{in})

Figure 4.2 IM VSD dc bus characteristics during normal ac supply conditions

IM VSD Response: The main motor variables of significance to this study are the motor speed (ω), torque (T_M), magnetisation current (i_{mR}), stator d-axis current (i_{sd}) and the q-axis torque producing current (i_{sq}). Response of these quantities, during acceleration and steady state, are shown in Figures 4.1 (a) to (e) respectively. Similarly, the dc bus variables of interest in the VSD are the output dc current to the inverter (I_{out}), the dc bus voltage (V_{bus}) and the capacitor charging current from the rectifier (I_{in}) which are shown in Figures

4.2 (a) to (c) respectively. The instant of transition from acceleration to steady-state is indicated along the time axis (x-axis) in these figures by a dotted line (t).

From the speed response as shown in Figure 4.1(a), it can be observed that the induction motor accelerates from standstill to the set reference (120 rad/s) in about 0.75 seconds. This acceleration time is found to coincide with the duration calculated using equation (4.1). During acceleration, the motor is found to operate under torque limit, as observed in Figure 4.1(b). From the magnetising current (i_{mR}) characteristics (Figure 4.1(c)), it can be observed that the IM operates at the rated flux. The stator d-axis current i_{sd}, which controls the motor flux, is found to oscillate around the set value of i_{mR} (Figure 4.1(d)). This behaviour is explained using equation (4.2), where it can be noted that, the rotor flux (or i_{mR}) lags the stator d-axis current i_{sd} by a delay proportional to the rotor time constant T_R [26]. It is observed that the stator q-axis current i_{sq} has similar characteristics as the motor torque (T_M) which is in accordance with equation (4.3).

$$dt = \frac{J\,d\omega}{(T_M - T_L)} = \frac{0.23*120}{(54-18)} = 0.766 \text{ s} \tag{4.1}$$

$$T_R \frac{di_{mR}}{dt} + i_{mR} = i_{sd} \tag{4.2}$$

$$T_M = N_{pp}\, K\, i_{mR}\, i_{sq} \tag{4.3}$$

$$p = \omega\ T_M \tag{4.4}$$

where,

$$K - \frac{2}{3}(1-\sigma)L_S$$

σ- total leakage factor of the induction motor

L_S- stator inductance

J – inertia of the motor and load

T_R- rotor time constant

N_{pp} –number of pole pairs

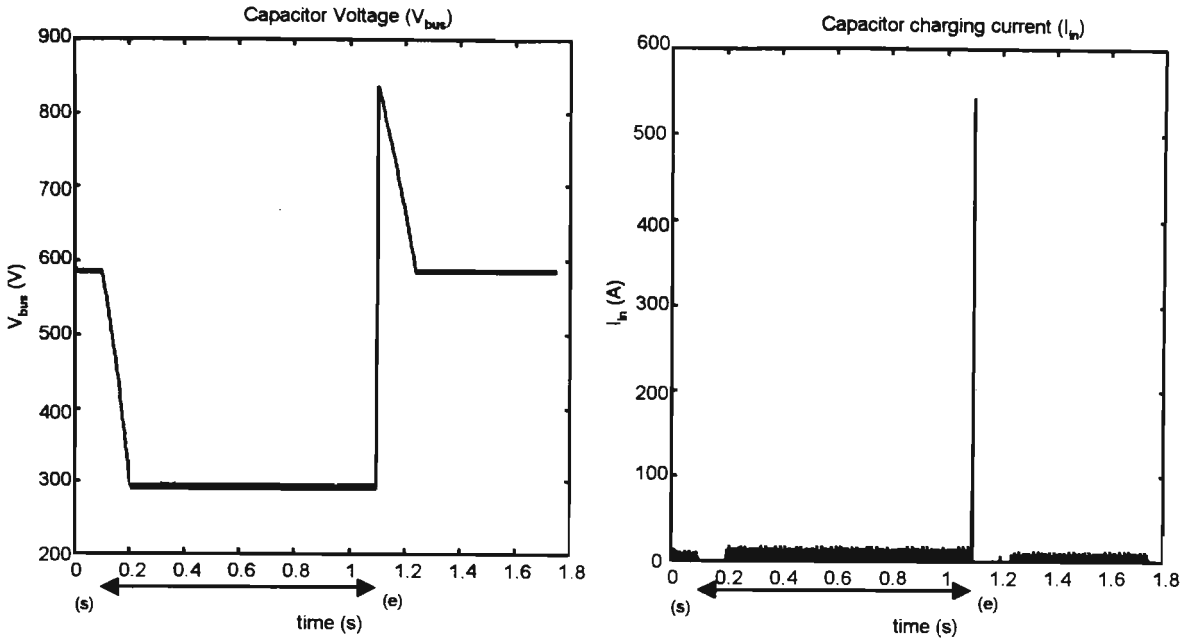
The dc bus characteristics, which are shown in Figure 4.2, are also found to respond according to the motor behaviour. During acceleration, the motor speed (ω) increases with the motor torque (T_M) limited by torque limit (T_{LT}), and hence the power (p) drawn by the motor increases as explained by equation (4.4). Because of this increased power requirement, the capacitor current to the inverter I_{out} is also found to increase during acceleration as observed in Figure 4.2(a). As a result, ripple in the dc bus voltage (V_{bus}) and the capacitor charging current (I_{in}) increase as observed in Figures 4.2(b) and (c) respectively.

Once the set speed is reached, the motor speed is maintained constant at this value as observed in Figure 4.1(a). The integrator wind-up reset feature which is implemented in the speed controller has ensured that there is no overshoot in the motor speed that may occur due to the saturation of the Speed Controller output because of high integrator gains. As seen in Figure 4.1(b), once steady state speed is reached, the motor torque is found to settle down at the set load torque levels without any oscillations, thus confirming proper tuning of the controllers. As observed in Figures 4.2(a) to (c), during this steady-state operation, the dc bus characteristics, viz. I_{out}, dc voltage ripple and I_{in}, which were increasing during acceleration, are found to settle down at lower levels corresponding to the operating conditions (load torque and speed).

4.2.2 VSD BEHAVIOUR DURING A SAG

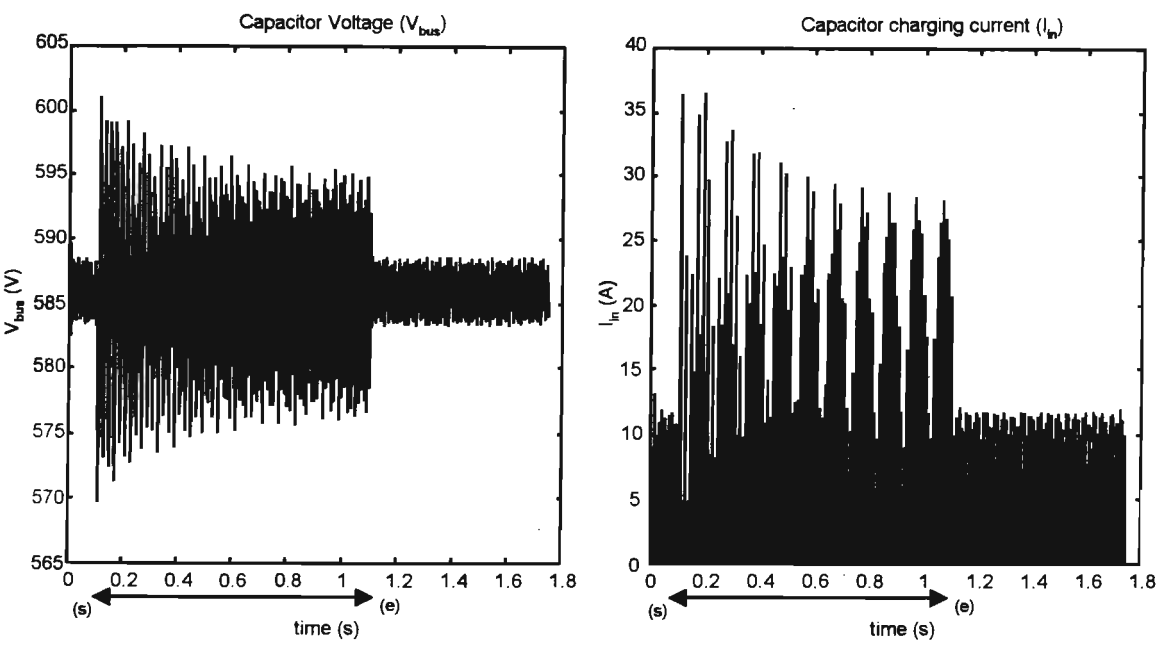
Here, the effect of a three-phase as well as a single-phase voltage sag on an IM VSD operating in steady-state is presented. In this subsection, the controllers have not been modified to take account of the voltage sags.

Simulation conditions: The steady-state operating conditions of the IM VSD are maintained at the same values as in previous trials (Subsection 4.2.1) (ie ω_{ref} = 120 rad/s, i_{mRref} = 9A and T_L = 18 Nm). Voltage sags of both three-phase and single-phase types of magnitude 50% and duration 1 second are applied and the VSD response is analysed here.



(a) Capacitor Voltage (V_{bus}) (b) Capacitor charging current (I_{in})

Figure 4.3 DC bus characteristics during a three-phase sag



(a) Capacitor Voltage (V_{bus}) (b) Capacitor charging current (I_{in})

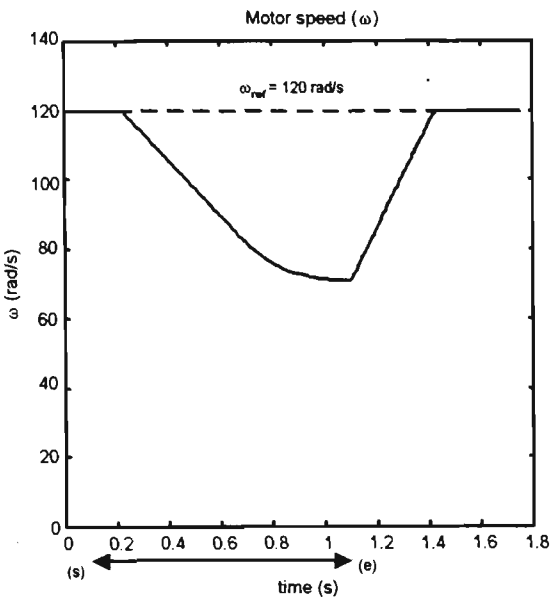
Figure 4.4 DC bus characteristics during a single-phase sag

IM VSD Response: In the presence of both three-phase and single-phase sags, the motor speed and torque responses were unaffected from the steady state behaviour with normal ac supply conditions (Figure 4.1(a) and (b)). The motor flux was maintained at the rated value. Because the motor torque and speed were maintained constant, the current drawn out of the dc capacitor (I_{out}) was found to be the same as during the steady-state condition in a no sag situation (as in Figure 4.2(a)). However, the capacitor voltage (V_{bus}) and the capacitor charging current from the rectifier (I_{in}) are the quantities that are significantly affected by the voltage sags which are shown in Figures 4.3 and 4.4 for a three-phase and a single-phase sag respectively. The start and end of the sag are indicated in these figures as previously.

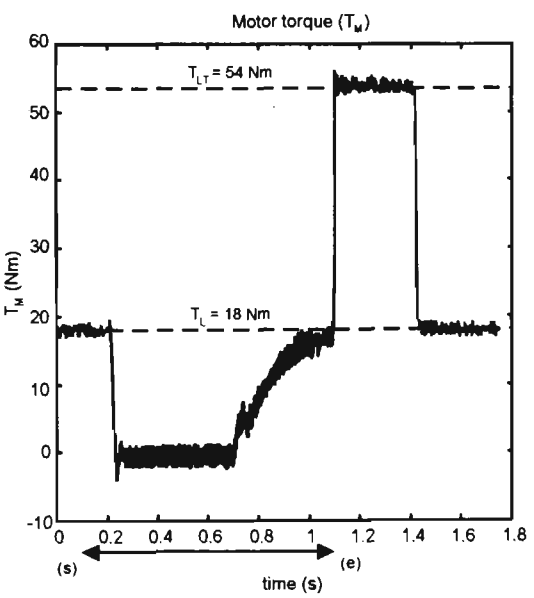
In the case of a three-phase sag, the rectifier diodes are initially reverse biased and hence there is no flow of charging current (I_{in}) to the capacitor as observed in Figure 4.3 (b). Now the capacitor discharges to supply the inverter in order to keep the motor operating at the set conditions and hence the capacitor voltage V_{bus} is found to drop as observed in Figure 4.3 (a). This discharging operation continues until V_{bus} becomes equal to the peak of the line-to-line ac supply voltage during the sag. On V_{bus} reaching this new level, the rectifier output current (I_{in}) starts flowing into the capacitor as in the case of a normal ac supply condition and the bus voltage is maintained during the sag. The drop in the capacitor voltage increases with sag magnitude and load torque. When the ac supply voltage returns to normal, a very high capacitor recharging current (I_{in}) results as observed in Figure 4.3(b). This magnitude of the current transient depends on the sag magnitude and in spite of being limited by the circuit impedances, it is usually much higher than the rating of the rectifier diodes. Because of this rapid charging of the capacitor, V_{bus} is found to overshoot to higher levels and then returns to the nominal level by discharging to supply the motor load as observed in Figure 4.3 (a).

In the case of a single-phase sag, the capacitor is charged by the unaffected line-to-line voltage peaks and it discharges during the rest of the supply cycle. Due to this intermittent charging pattern, the ripple in the dc voltage V_{bus} and the charging current I_{in} are found to

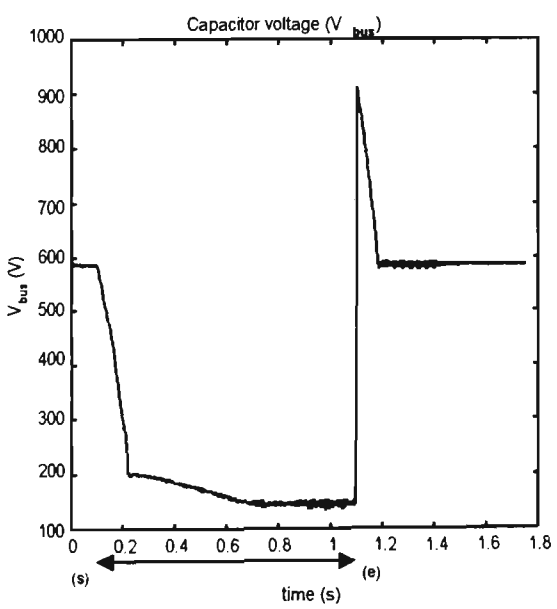
be much higher than during balanced supply conditions as shown in Figures 4.4(a) and (b) respectively. However, since the average value of V_{bus} is not affected significantly, the charging current I_{in} at the end of the sag is not as high as in the case of a three-phase sag.



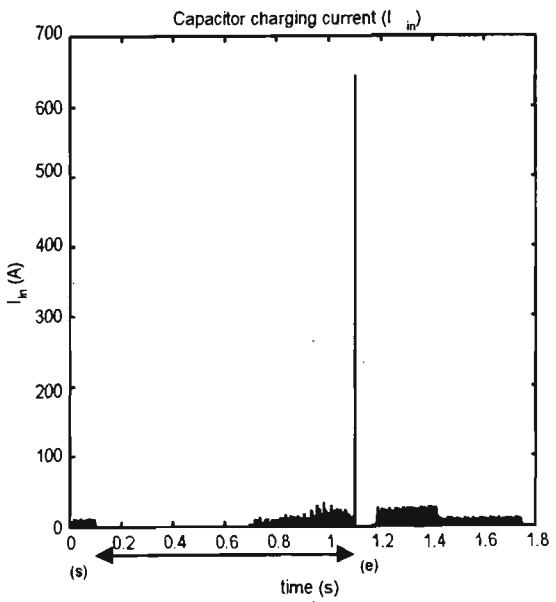
(a) Speed (ω)



(b) Torque (T_M)



(c) Capacitor voltage (V_{bus})



(d) Capacitor charging current (I_{in})

Figure 4.5 VSD behaviour in the case of a 85% three-phase sag

As the magnitude of the sag increases further, its impact on the VSD performance also increases. In the case of single-phase sags, the torque and speed performance of the VSD is not affected for all sag magnitudes, whereas the dc voltage ripple and capacitor charging current I_{in} are found to increase further. However, when subjected to a three-phase sag of very high magnitude, the motor speed and torque are also found to be affected.

The response of the IM VSD, when subjected to a balanced three-phase sag of magnitude 85% and duration 1 second with similar operating conditions as in the previous case is shown in Figure 4.5. The motor is found to operate at the set speed and torque values for a small duration after the sag occurrence (Figure 4.5(a)). During this time, the dc bus capacitor discharges to supply the load and there is no charging current I_{in} from the rectifier as observed in Figures 4.5 (c) and (d). Below a certain dc voltage (around 200 V), the capacitor does not have the energy required to drive the motor at the set speed and torque conditions and hence the motor speed is found to drop below the set reference as observed in Figure 4.5 (a). In this period, no torque is developed by the motor as found in Figure 4.5 (b). The capacitor now discharges just enough to maintain the motor flux and the rate of discharge is found to be lower than during normal motoring condition (Figure 4.5 (c)). This operation continues until V_{bus} becomes lower than the ac supply peaks when the capacitor charging current I_{in} starts flowing from the rectifier and the VSD is able to supply the required power to the motor. The motor speed is maintained at this lower level until the normal ac supply returns. The speed drop during the sag varies depending on the motor operating torque (T_M) and the dc bus voltage V_{bus} as per equation (4.5). Once the supply returns to normal condition, the motor is found to accelerate to the set speed under torque limit. However, a large recharging current pulse appears in I_{in} because of the lower capacitor voltage during the sag. This high capacitor charging results in overshoot of V_{bus} which then returns to the nominal value by discharging to the load.

$$p = \omega \ T_M = V_{bus} I_{out} \qquad (4.5)$$

where

p - power input to the motor,

I_{out} - the dc current from the capacitor to the inverter.

4.2.3 REASONS FOR VSD TRIPPING ON A SAG CONDITION

From the simulation results, it can be observed that both three-phase and single-phase sags affect the VSD performance, especially the dc bus characteristics, with the impact of a three-phase sag being more severe than a single-phase sag.

When subjected to a three-phase voltage sag, the dc bus capacitor voltage reaches a lower level, depending on the sag magnitude and the load and this can lead to a VSD trip due to an under-voltage fault. Also, when the ac supply returns to normal, a very high recharging current I_{in} occurs which can cause damage to the rectifier diodes. During such conditions, the over-current trip protection in the VSD can cause nuisance tripping. The speed drop that was observed in the case of very high three phase sags is not a major cause of concern for many VSD applications where process continuity rather than occasional speed reduction is critical.

In the case of single-phase sags, the drop in the capacitor voltage V_{bus} is not as much as in a three-phase sag condition, but a very high ripple content is present in V_{bus} which increases with the sag magnitude and load on the motor. Hence, an under-voltage trip can occur during deeper single-phase sags. Similarly, the high capacitor charging current I_{in} that occur during such deep sags can cause an ac over-current trip.

4.3 OPERATION UNDER A SAG AT HIGH SPEEDS – BUS VOLTAGE CONTROL BY RECOVERING KINETIC ENERGY

In this section, the performance of an IM VSD with dc bus voltage control by recovering the kinetic energy available in the rotating mass is demonstrated. It may be recalled from the definitions of the proposed control strategy (Section 2.2) that this mode is employed only at higher motor speeds (above 10% of the motor base speed) because the kinetic energy available in the motor at lower speeds is relatively negligible. This, corresponds to

Control Situation 2 as defined by the control strategy and during this interval, the Bus Voltage Controller 1 sets the motor torque reference with the Speed Controller bypassed. The motor flux (or magnetising current i_{mR}) is maintained at the rated value in order to ensure proper operation of the induction motor as a generator. The bus voltage controller reverses the torque reference appropriately so that the direction of torque producing current i_{sq} is reversed which in turn reverses the flow of dc current I_{out} from the motor to the dc capacitor. This operation is similar to that of an SRM and is explained by equations (4.6) to (4.8). The bus voltage controller (proportional-integral type), which monitors the actual dc bus voltage against the set reference, ensures that only the required amount of energy is recovered from the rotating mass in order to maintain the capacitor voltage at the desired nominal value. The tuning details of the Bus Voltage Controller 1 are given in Appendix G.

$$I_{out} = \frac{2(V_{sd}i_{sd} + V_{sq}i_{sq})}{3V_{bus}} \tag{4.6}$$

$$V_{sd} = R_s i_{sd} + \sigma L_s\left(\frac{di_{sd}}{dt} - \omega_{mR} i_{sq}\right) + (1-\sigma)L_s \frac{di_{mR}}{dt} \tag{4.7}$$

$$V_{sq} = R_s i_{sq} + \sigma L_s\left(\frac{di_{sq}}{dt} + \omega_{mR} i_{sd}\right) + (1-\sigma)L_s \omega_{mR} i_{mR} \tag{4.8}$$

where,

V_{sd}, V_{sq} – d and q axis stator voltages

i_{sd}, i_{sq} – d and q axis stator currents

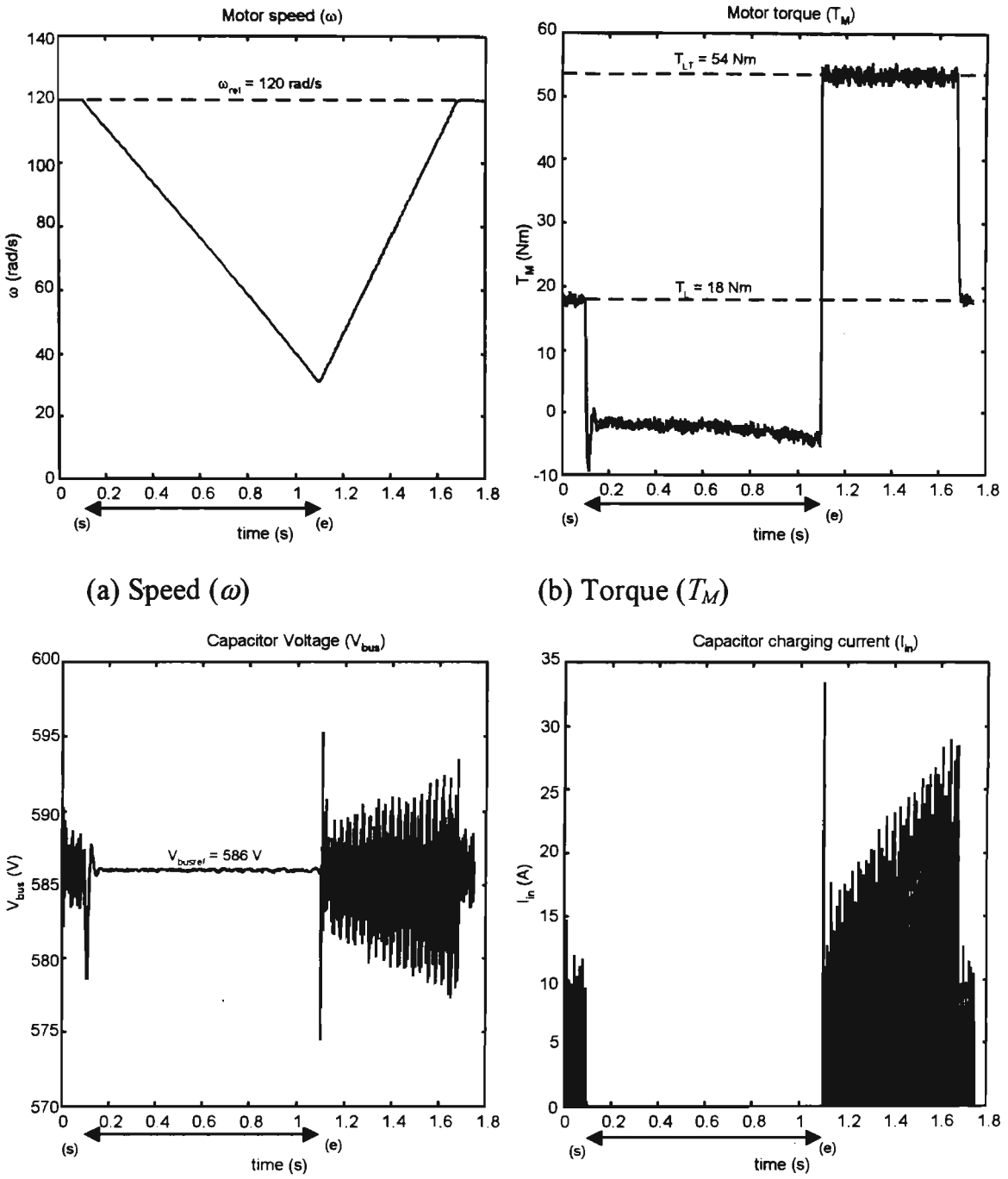
R_s - stator resistance,

L_s - stator inductance,

σ - total leakage factor of the motor,

ω_{mR} - angular velocity of the magnetising vector, and

The VSD performance when controlled by this strategy at high motor speeds is discussed here.



(a) Speed (ω) (b) Torque (T_M)

(c) Capacitor voltage (V_{bus}) (d) Capacitor charging current (I_{in})

Figure 4.6 IM VSD response during kinetic energy recovery at high motor speeds

Simulation conditions: A 50% three-phase sag is applied to the VSD when the induction motor is operating in steady state at 120 rad/s with half the rated load (18 Nm) with the other operating conditions unchanged from previous trials (refer Section 4.2.2).

IM VSD Response: The response of the motor speed (ω), torque (T_M), capacitor voltage (V_{bus}) and capacitor charging current (I_{in}) during dc link voltage control utilising rotor kinetic energy is shown in Figures 4.6(a) to (d) respectively. The sag period is indicated in these figures as previously. The motor is found to operate at full flux throughout the sag. From Figure 4.6(b), it is observed that the direction of motor torque reverses as soon as the sag is sensed and it settles down at a very low negative value as controlled by the Bus Voltage Controller 1. The capacitor voltage V_{bus} is found to reach its set point within a few milliseconds and it is maintained at this value throughout the sag condition (refer to Figure 4.6(c)). Because of this bus voltage control at the nominal level, the rectifier diodes are reverse biased and hence, there is no flow of capacitor charging current I_{in} during the sag as found in Figure 4.6(d). From motor speed response, (Figure 4.6(a)), it is observed that, the motor speed (ω) reduces at a uniform rate during this regenerative control. A speed drop of approximately 90 rad/s is observed during this 1 second sag which is more than the speed drop ($d\omega$) that would have occurred during the same period, had the motor coasted without any power applied from the VSD, which is calculated using equation (4.9).

$$d\omega = \frac{(T_M - T_L)\,dt}{J} = \frac{(0-18)}{0.23} = -78.26 \text{ rad/s} \qquad (4.9)$$

where,

T_M - motor torque,

T_L - load torque,

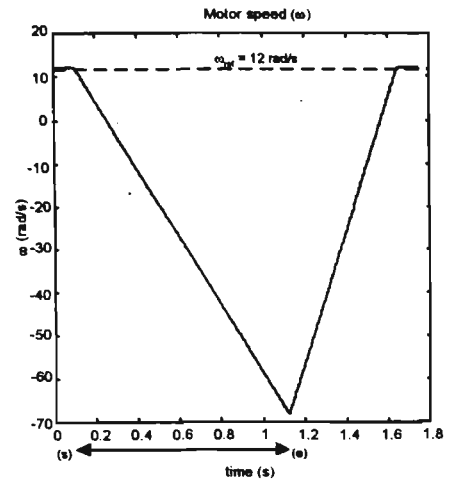
J - inertia of the rotating mass

This confirms the usual motor behaviour that, the rate of speed drop during regeneration is higher than during normal stopping. Also, it is observed that, as the motor speed drops, the reverse torque increases, in order to meet the constant power required at the dc link. On ac supply recovery, the large transient in the recharging current I_{in} which was found earlier (refer Figure 4.3(b)) is not observed during this control.

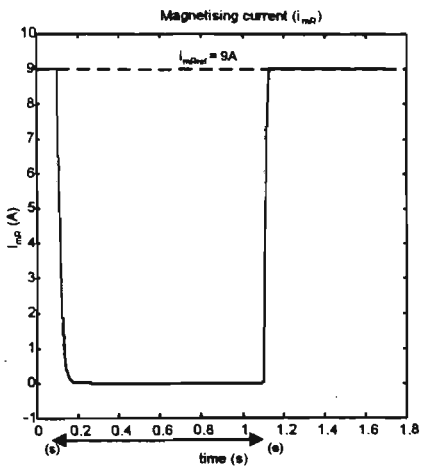
From the above simulation results, it can be concluded that a sag ride-through performance can be achieved using this strategy in the case of an IM VSD by utilising the kinetic energy available in the rotating mass until the motor speed reaches a minimum value. Also, the ride-through performance under varying sag conditions can be inferred from the dc bus characteristics. As discussed in the case of an SRM (refer Section 3.4), the rectifier diodes are reverse biased during this dc bus voltage control, and hence there is no power flow from ac mains into the VSD. This condition holds good for both sag types (single-phase as well as three-phase) irrespective of the sag magnitude. Hence, the performance of this strategy will not be affected by the sag type and sag magnitude. Also, since the motor speed drops in proportion to the load torque, longer ride-through times can be achieved at reduced loads and at high motor speeds. This strategy is more suitable in VSD applications where the operation continuity is of utmost importance and occasional speed variations can be tolerated.

4.4 OPERATION UNDER A SAG AT LOW SPEEDS – BUS VOLTAGE CONTROL BY RECOVERING MAGNETISING ENERGY

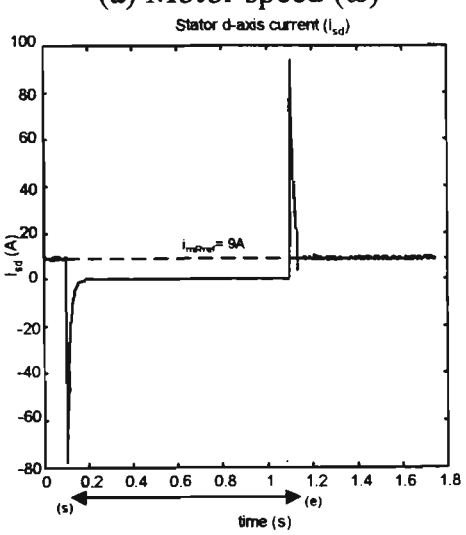
In this section, the performance results of the proposed strategy on an IM VSD during a voltage sag are discussed at low motor speeds when it is attempted to recover the magnetising energy in the motor windings for dc bus voltage control. This type of control is desired at low motor speeds when the kinetic energy available in the motor is negligible and it corresponds to Control Situation 3 as defined in the control strategy (Subsection 2.2.2). The motor torque is maintained at zero level and the flux (or i_{mR}) reference is reduced by the Bus Voltage Controller 2. The same principle as envisaged in the case of SRM is employed here, i.e. by maintaining motor torque at zero, the magnetising energy available in the inductances can be recovered by reversing the polarity of the applied voltage across the machine windings. However, it is observed that in an IM, the recovery of energy from the winding inductances does not work in the same way as in the case of an SRM. The performance results of the IM VSD under this strategy are analysed. The tuning of the Bus Voltage Controller 2 is described in Appendix G.



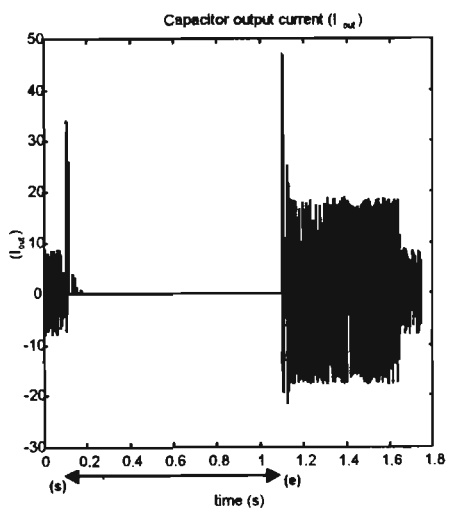
(a) Motor speed (ω)



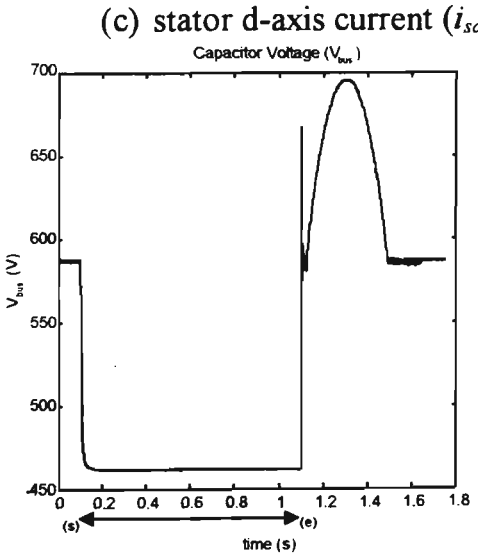
(b) Magnetising current (i_{mR})



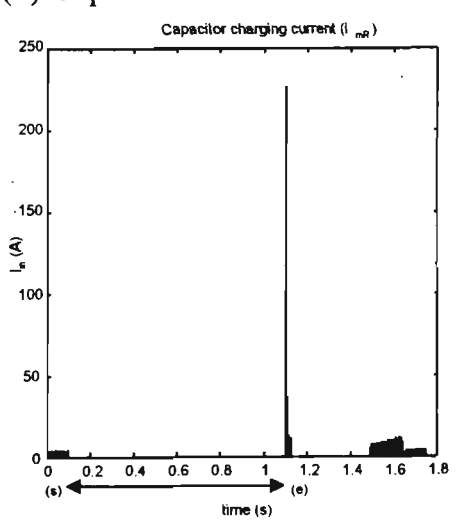
(c) stator d-axis current (i_{sd})



(d) Capacitor current to inverter (I_{out})



(e) Capacitor voltage (V_{bus})



(f) Capacitor charging current (I_{in})

Figure 4.7 IM VSD Response during attempted recovery of magnetising energy

Simulation condition: Here, an identical three-phase sag of magnitude 50% and duration 1 second is applied to the IM VSD when the motor is running in steady state at a speed of 12 rad/s with half the rated load (18 Nm). The maximum and minimum limits for stator d-axis current reference (i_{sdref}) are set at 9A and 0 A respectively.

IM VSD Response: The response of the IM VSD, viz. speed (ω), magnetisation current (i_{mR}), stator d-axis current (i_{sd}), capacitor output current to the inverter (I_{out}), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}), are shown in Figures 4.7(a) to (f). When the sag is sensed, the magnetising current (i_{mR}) is found to reduce to zero within a few milliseconds as seen in Figure 4.7(b). When the motor flux decreases, a high negative current pulse (of about 80 A) is observed in i_{sd} characteristics as seen in Figure 4.7(c). From Figure 4.7(d), it is observed that, the dc current I_{out}, instead of being fed back into the capacitor, has been drawn out of the capacitor by the motor. This has resulted in the reduction of capacitor voltage (V_{bus}) rather than it being maintained at the desired level as seen in Figure 4.7(e). As a result, when normal ac supply returns, large current pulses are observed in the capacitor charging current (I_{in}) as shown in Figure 4.7(f). During the sag period, the motor speed is found to have coasted towards zero and reversed further as seen in Figure 4.7(a). But this speed reversal, as explained in the case of the SRM, happens only in the case of loads such as hoists or cranes whereas with frictional loads, the motor stops after reaching zero speed.

When the sag is over, the flux returns to normal rated value and the motor starts to accelerate towards the set speed. The motor operates in regeneration mode until the motor reaches zero speed and thereafter normal motoring operation starts. Because of this regeneration, the capacitor voltage V_{bus} is found to increase to a higher value than normal. This voltage can be discharged at the pre-charge resistors available in a standard VSD.

Obviously, it is clear from the simulation results that, the energy recovery from the magnetising inductances has not worked with an IM VSD as envisaged by the control strategy and the reasons for this behaviour are analysed further.

4.5 ENERGY LOSS IN AN INDUCTION MOTOR DURING FLUX VARIATIONS

The derivation of stator and rotor currents in field coordinates is described in Appendix B and are repeated here for convenience.

$$i_{sd} = i_{mR} + T_R \frac{di_{mR}}{dt} \tag{4.10}$$

$$di_{sd} = \frac{L_R}{R_R}\frac{di_{mR}}{dt} = L_m \frac{(1+\sigma_r)}{R_R}\frac{di_{mR}}{dt} \tag{4.10(a))}$$

$$i_{sq} = T_R i_{mR}(\omega_{mR} - \omega) = \frac{L_m(1+\sigma_r)}{R_R}(\omega_{mR} - \omega) \tag{4.11}$$

$$i_{rd} = -\frac{L_m}{R_R}\frac{di_{mR}}{dt} \tag{4.12}$$

$$i_{rq} = -\frac{L_m\, i_{mR}}{R_R}(\omega_{mR} - \omega) \tag{4.13}$$

where,

i_{sd} - stator d-axis current,

i_{mR} - rotor magnetising current,

L_R - rotor air-gap inductance

R_R - rotor resistance

T_R - rotor time constant,

L_m - mutual inductance

i_{sd}, i_{sq} - stator currents in d and q axes (flux coordinates)

i_{rd}, i_{rq} - rotor currents in d and q axes (flux coordinates)

ω - motor angular velocity

ω_{mR} - angular velocity of the flux axis

As given by equation (4.10), the rotor flux of an induction motor, which is represented by the magnetisation current i_{mR}, is controlled by the stator d-axis current i_{sd}. During steady-state flux conditions, the average value of i_{sd} is the same as that of i_{mR}. According to equation (4.10(a)), under dynamic condition, the incremental current (di_{sd}) is proportional

to the rate of change of rotor flux (proportional to di_{mR}/dt and the rotor time constant ($T_R=L_R/R_R$)). By comparing equations (4.10(a)) and (4.12), it can be realised that, di_{sd} flows out of the dc bus into the rotor as d-axis current (i_{rd}) leading to energy dissipation in the rotor circuit. This is verified by the response of i_{sd} and i_{rd}, from Figures 4.7(c) and 4.8 respectively, which was observed during the flux reduction by Bus Voltage Controller 2 as reported in Section 4.4. Again, from equation (4.10), it can be realised that, if the motor flux is reduced to zero in a duration smaller than the rotor time constant (T_R), i_{sd} would increase beyond its nominal level (here it is 9A) and consume more power from the dc link leading to a faster discharge of the bus capacitor. This behaviour was observed during the simulation trials reported in Section 4.4 (as shown in Figures 4.7 (d) and (e)). Hence, during a sag, it is not a good idea to reduce the induction motor flux in a duration shorter than the rotor time constant.

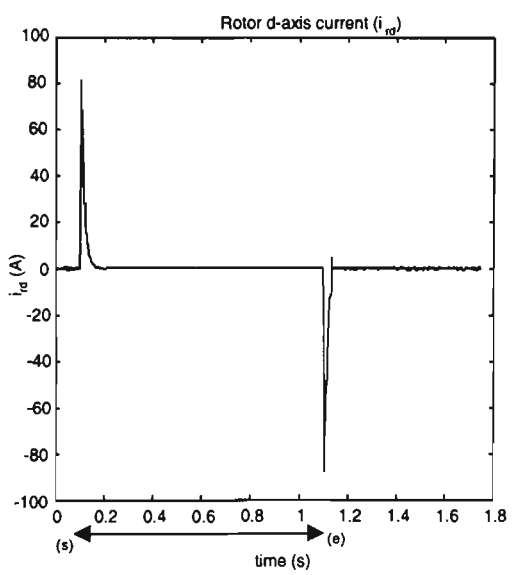


Figure 4.8 Rotor d-axis current response during flux change

One strategy, that can be applied to an IM VSD at low motor speeds, is to maintain the flux constant at the rated value with zero torque reference. In this case also, energy will still be lost in the motor in the form of stator and rotor losses, which will again lead to dc capacitor voltage drop, however, at a rate smaller than during fast flux change. Since energy is dissipated in the rotor during a flux change, it is not possible to recover the magnetising energy by reducing the flux in the case of an IM VSD. As it may be recalled,

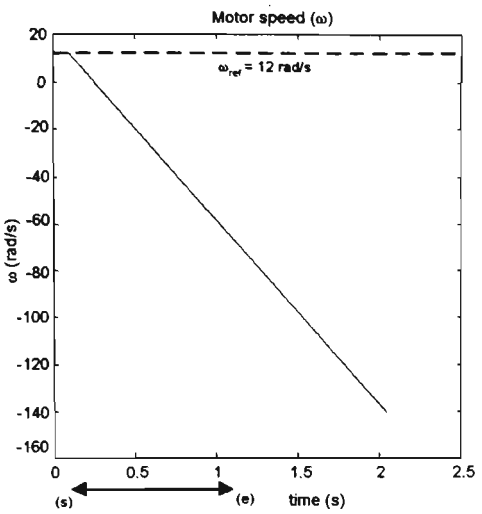
the intent of the proposed control strategy is to maintain the dc bus voltage constant at the nominal level by recovering the magnetising energy, and this being not possible in the case of an IM VSD, it must be ensured that the rate of decay of the capacitor voltage is as small as possible for an extended sag ride-through performance. An optimum dc bus voltage control can be achieved by reducing the flux to zero in a duration marginally longer than the rotor time constant and this can be achieved by an open loop flux control scheme. The advantage of this control is that, the energy drawn from the dc bus capacitor would not only be less than during constant flux control but would also continue to reduce further. Hence, the dc bus voltage would reduce at a smaller rate which will enable the VSD to ride-through sags of longer durations at low motor speeds down to zero speed.

Similar to d-axis currents, it can be found from equations (4.11) and (4.13) that, the stator q-axis current (i_{sq}) flows into the rotor as q-axis current (i_{rq}) with a small percentage impeded in the rotor leakage factor σ_r.

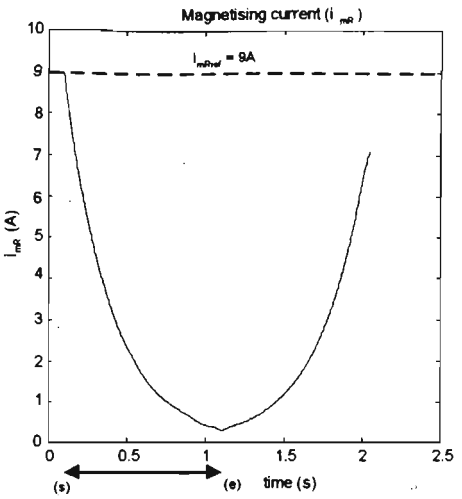
4.6 OPTIMUM SAG RIDE-THROUGH CONTROL AT LOW SPEEDS

In this section, the behaviour of the VSD will be studied during a sag at low motor speeds by reducing the flux to zero in a duration longer than the rotor time constant.

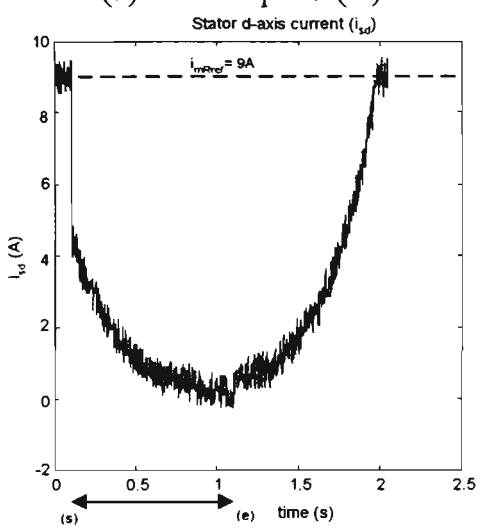
Simulation conditions: The same operating conditions as in the magnetising energy recovery trials presented in Section 4.5 are maintained. Simulation results are shown for a period of 2.05 seconds and a 1 second three-phase sag of 50% magnitude is applied to the VSD. During flux weakening, i_{mR} was reduced to zero in a duration corresponding to twice the rotor time constant. On normal ac supply recovery, the flux is increased at the same slow rate in order to avoid high currents (i_{sd}). The normal speed control operation of the VSD is restarted on supply recovery only when the motor flux becomes more than 97.5% of the rated value.



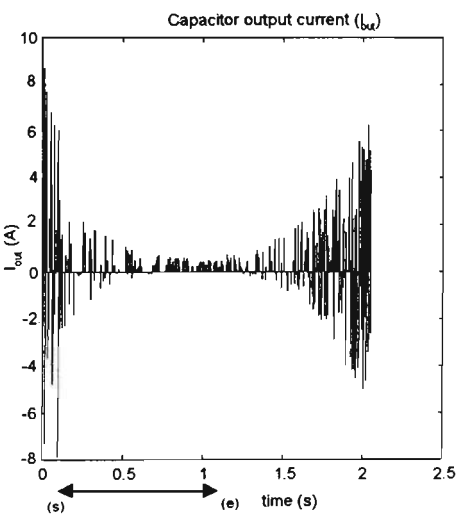
(a) Motor speed (ω)



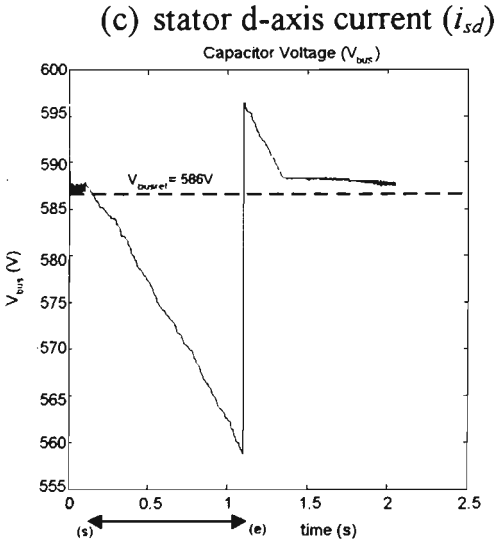
(b) Magnetising current (i_{mR})



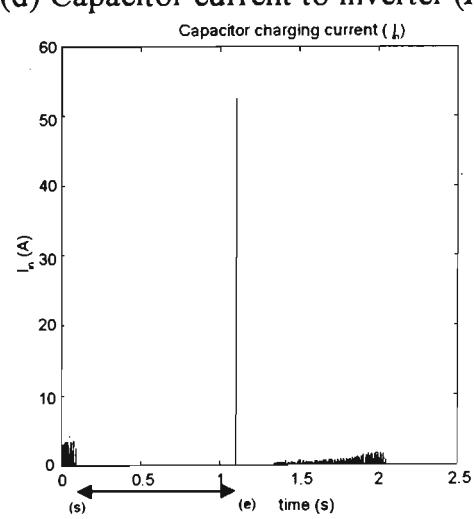
(c) stator d-axis current (i_{sd})



(d) Capacitor current to inverter (I_{out})



(e) Capacitor voltage (V_{bus})



(f) Capacitor charging current (I_{in})

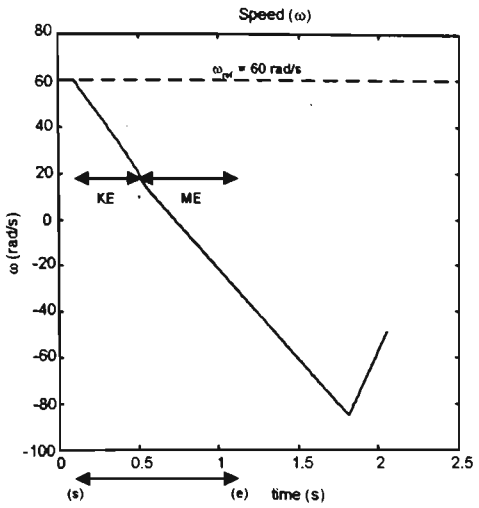
Figure 4.9 IM VSD Response during slow recovery of magnetising energy

IM VSD Response: The response of the IM VSD, viz. speed (ω), magnetising current (i_{mR}), stator d-axis current (i_{sd}), capacitor output current to the inverter (I_{out}), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}), during this slow flux reduction control are shown in Figures 4.9(a) to (f). The sag period is indicated as in the previous trials and the duration of kinetic energy recovery and flux control are indicated as 'KE' and 'ME' respectively. From the magnetising current characteristics (refer Figure 3.9(b)), it can be observed that the flux is reduced at a much smaller rate compared to the closed loop flux control as shown in Figure 3.7(b). During this control, i_{sd} is also found to reduce gradually and does not reverse its polarity (Figure 3.9(c)). Only a small amount of energy is drawn from the dc capacitor corresponding to the reduced losses in the motor windings which can be verified from the dc output current (I_{out}) characteristics as shown in Figure 3.9(d). The capacitor voltage reduces at a much smaller rate during this control in a sag condition and this results in reduced charging current at the instant of ac supply recovery as found in Figures 3.9(e) and (f). When the ac supply returns to normal, an overshoot is observed in the capacitor voltage because the motor operates in regeneration mode until zero speed is reached. This excess voltage occurs only in the case of loads such as hoists or cranes and it can be discharged by the standard resistors available in the drive.

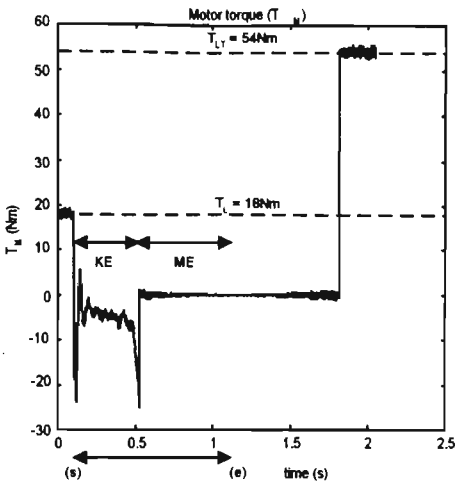
4.7 COORDINATED SAG RIDE-THROUGH CONTROL AT ALL SPEEDS

By combining the closed loop dc bus voltage control operation by recovering the kinetic energy at higher speeds with the slow open loop flux control at lower speeds, the IM VSD can be configured to ride-through voltage sags of longer durations at all operating speeds. In this section, the VSD performance at a moderate speed is simulated such that the coordinated transition between the two control modes is observed.

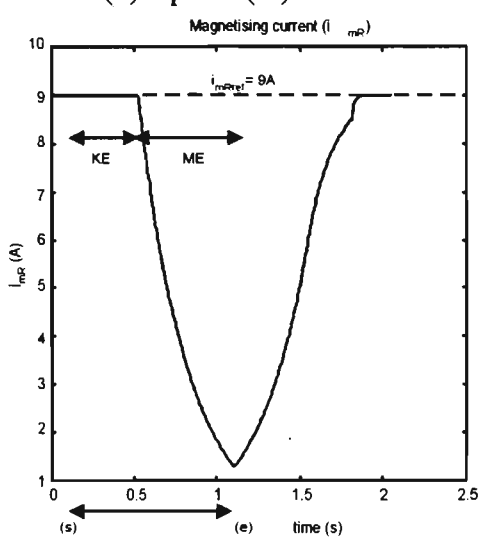
Simulation conditions: A 50% three-phase sag is applied to the IM VSD operating at a speed of 60 rad/s at half load (18Nm). Simulation results are shown for a period of 2.05 seconds. On supply recovery, the VSD operation is restarted only when the flux reaches 97.5% of the rated value.



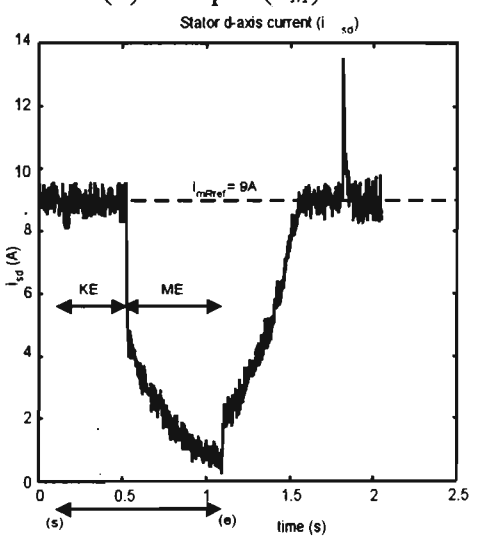
(a) Speed (ω)



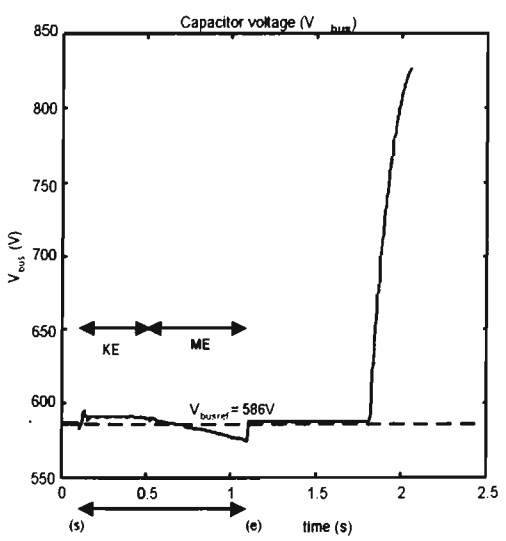
(b) Torque (T_M)



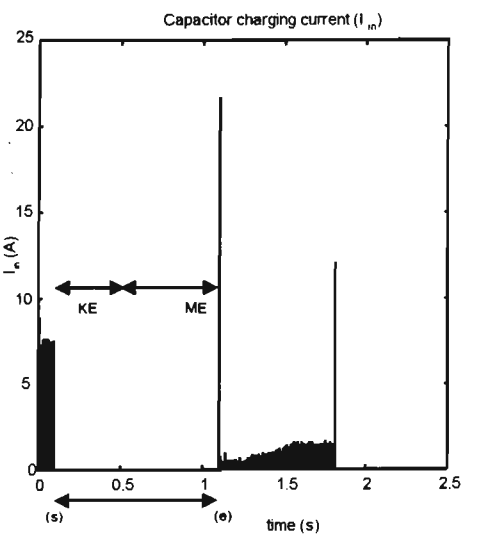
(c) Magnetisation current (i_{mR})



(d) Stator d-axis current (i_{sd})



(e) Capacitor voltage (V_{bus})



(f) Capacitor charging current (I_{in})

Figure 4.10 IM VSD sag ride-through response at an intermediate speed

IM VSD Response: The response of the induction motor VSD, viz. the motor speed (ω), torque (T_M), magnetisation current (i_{mR}), stator d-axis current (i_{sd}), capacitor voltage (V_{bus}) and the capacitor charging current (I_{in}), during this combined sag ride-through operation are shown in Figures 4.10(a) to (f). The sag period and the durations of kinetic energy recovery and flux reduction control are indicated as previously. For motor speeds above 15.7 rad/s, the kinetic energy recovery is observed as shown in Section 4.2 earlier. The dc voltage is maintained at the set value (586 V). Once the cut off speed is reached, the motor flux is found to reduce at a slower rate as observed from i_{mR} characteristics. The capacitor voltage is found to reduce at a smaller rate because a very small current is drawn by the motor in order to compensate the winding losses. When normal ac supply returns, the flux is found to increase at the same slower rate and i_{sd} is also found to increase gradually without any high transients. The capacitor charging current (I_{in}) on ac supply recovery is found to be within acceptable levels. An overshoot is observed in the capacitor voltage because the motor is regenerating until zero speed is reached.

4.8 SUMMARY

In this chapter, the normal behaviour of an IM VSD was demonstrated and its performance when affected by a voltage sag was shown. It was observed that, in the case of IM VSDs having a diode bridge rectifier, voltage sags affect the dc bus characteristics and cause nuisance tripping due to dc under-voltage and ac over-current faults. The performance of the proposed control strategy was studied on an IM VSD and it was found that, at high motor speeds, the dc bus voltage control by recovering the kinetic energy from the rotating mass works satisfactorily. However, due to the inherent characteristics of an IM, it is found that, the magnetising energy present in the winding inductances cannot be recovered and if flux is reduced to zero at a smaller duration than rotor time constant, the IM draws excessive energy from the dc bus which is dissipated in the rotor circuit. Here, a slow flux weakening scheme by an open loop control is proposed by which the dc bus characteristics are found to have improved and this type of sag ride-through control can be applied to an IM VSD at low motor speeds.

CHAPTER 5

CONCLUSIONS

5.1 CONCLUSIONS

When considering the effects of power quality aspects in the industrial process environment, voltage sags are found to be the primary source of concern causing nuisance tripping of critical equipment such as Variable Speed Drives (VSDs). Nowadays, VSDs are very commonly used in process plants and their tripping results in substantial financial losses due to reasons such as wastage of raw materials, production downtime and restarting delays. Hence, it is essential that the VSDs ride-through such sag situations to the maximum possible extent. Several suggestions have been made in the literature which are mostly hardware related solutions such as addition of extra circuitry, overrating the existing components or provision of an alternative power supply. These solutions are usually expensive and moreover they increase the size of the equipment. Very few of the published strategies suggest solutions that would improve the control algorithm in a VSD while retaining the standard hardware. This thesis was aimed at studying the behaviour of VSDs during voltage sag conditions and to improve the ride-through performance by modifying the control strategy.

Presently, ac VSDs with voltage source inverter (VSI) topology are the most commonly used type of drives and hence this configuration was examined in this thesis with field orientation applied to the motor control. Simulation models were developed and the performances of synchronous reluctance motor VSDs (SRM VSDs) and induction motor VSDs (IM VSDs) were examined under normal ac supply conditions as well as under sags (of both three-phase and single-phase types). It was observed that the speed and torque performance of both motors were not affected during most sag situations, except for a minor speed drop observed during very deep three-phase sags. However, the main impact

of the voltage sags was observed in the dc link (bus) characteristics of the VSDs. In the case of a three-phase sag, the dc capacitor voltage reduces to a lower level, depending on the magnitude of the sag, and when the ac supply returns to normal, a very high capacitor charging current results. If left unprotected, the rectifier diodes would be damaged and this situation usually results in VSD tripping due to either dc link under-voltage or ac over-current protection faults which are built into the VSD control system in order to protect the components. The probability of these trips increases with the sag magnitude and load on the motor. In the case of a single-phase sag, the impact of the sag was found to be less severe on the dc bus characteristics than a three-phase sag, due to the intermittent capacitor charging by the unaffected phases. However, the voltage ripple and the capacitor charging currents were found to increase with the sag magnitude. Though the high recharging current peaks were not present at the end of a single-phase sag, VSDs can still trip due to the faults mentioned earlier when subjected to sags of very high magnitude, especially when operating under high load conditions.

The control strategy proposed in this thesis suggests maintaining the dc bus voltage at the nominal level corresponding to the rated three-phase input supply conditions. From the published literature, it can be found that this objective can be achieved by recovering the kinetic energy available in the rotating mass by means of controlled regeneration. Since the kinetic energy falls rapidly during regeneration in proportion to the square of the motor speeds, this source can be utilised only until the motor speed is above a minimum limit. If the sag condition persists even after the motor reaching zero speed, the bus voltage will begin to drop leading to similar fault conditions, viz. under-voltage or over-current, as mentioned earlier. The power supply for the control system is assumed to be derived from the dc capacitor instead of ac mains which will buffer the effect of supply variations affecting the control supply. The control strategy proposed in this thesis recommends maintaining the dc capacitor voltage at the nominal value during a sag, initially by recovering the kinetic energy available in the rotating mass when the motor speed is above a minimum speed (here, the cut-off speed is chosen as 10% of the rated motor speed) and then by recovering the energy available in the motor winding inductances. Though the

energy available in the inductances is relatively small compared to the energy present in the capacitor under normal circumstances, the advantage of this strategy is that, it can be applied at low speed and standstill. There will be no further losses in the motor apart from the low voltage power supplies which will still draw power from the dc bus. Another advantage of this strategy is that the voltage sag ride-through performance is not affected by the type of the sag (three-phase or single-phase) or the sag magnitude because the rectifier diodes are reverse biased during either type of sag and hence the dc link characteristics are immune to the sag characteristics.

The performance of this proposed control strategy was studied on both SRMs and IMs of similar ratings (5.5 kW). It was observed that the closed loop voltage control by recovering the kinetic energy works satisfactorily with both types of machines. Longer sag ride through times are achieved by this control mode when the motor speed is high and the load on the motor is low. Hence this strategy is more suitable for high inertia loads. Better ride-through performance with smaller speed drop was observed in the case of fan type loads as compared to constant torque loads.

However the other part of the control strategy, viz. closed loop dc voltage control at low motor speeds by recovering the energy available in the motor winding inductances, is found to work satisfactorily only in the case of SRM VSD as envisaged by the control strategy. It was observed that this energy is recovered within a few milliseconds but from then on, the capacitor voltage remains close to the nominal value since there is no further energy drawn from the dc link. When the supply recovers to normal, the SRM VSD is able to restart and reach the set speed without any abnormal capacitor charging current transients.

When a closed loop dc bus voltage control was attempted on an IM VSD by recovering the stored magnetic energy, it was observed that energy is drawn from the dc capacitor rather than being fed back into it. When analysed further, the reason for this behaviour was found to be the inherent characteristics of the IM, according to which, whenever the

motor flux is changed, additional energy is drawn from the dc bus capacitor which is lost in the rotor circuit. If the rotor flux is reduced to zero in a duration smaller than the rotor time constant, the current drawn from the dc bus is more than the rated value which reduces the dc link voltage at a rapid rate. Even when the motor flux is maintained constant, energy is found to be lost in the stator and rotor circuits. Hence, the proposed control strategy was modified to accommodate this limitation and an open loop flux control scheme was examined which reduces the induction motor flux in a duration longer than the rotor time constant. In this control, the energy drawn from the dc link and hence the rate of dc bus voltage drop would be quite small. This strategy was found to work reasonably well at low motor speeds and the capacitor recharging current at the end of the sag was also found to be within acceptable limits.

In both types of motors, the transition between the two modes of the control strategy, viz. recovery of energy from rotating mass as well as from the motor winding inductances, was found to pass relatively easily between the appropriate control loops. The simulation results of the combined control show that this strategy can be utilised to ride-through voltage sags at all speeds.

According to the control strategy adopted in this thesis, as the input rectifier is not in conduction during a sag, it effectively decouples the VSD load from the ac mains and hence does not exacerbate the supply situation on the mains.

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APPENDIX A

ENERGY LEVELS IN AN AC VSD

Here, an overview of the energy levels present in an induction motor VSD (IM VSD). of rating 5.5 kW is presented. These values are also applicable for a synchronous reluctance motor VSD (SRM VSD).

Energy in motor winding inductance (L):

Assuming a star connected motor,

$$1 \text{ p.u. volts } = \frac{415}{\sqrt{3}} = 240 \text{ V rms} \qquad \text{(A.1)}$$

Considering a power factor of 0.85,

$$1 \text{ p.u. current } = \frac{5500}{\sqrt{3} * 415 * 0.85} = 9 \text{ A} \qquad \text{(A.2)}$$

$$\text{Hence, 1 p.u. impedance, } Z = \frac{240}{9} = 26.67\ \Omega \qquad \text{(A.3)}$$

$$\text{Let us assume that } X_t = \omega L_t = 2.5 \text{ p.u. } Z = 66.675\ \Omega \qquad \text{(A.4)}$$

where,

X_t – total reactance of the ac machine

L_t – total inductance of the ac machine

$$\text{Then, } L_t = \frac{66.675}{2\pi 50} = 212 \text{ mH} \qquad \text{(A.5)}$$

$$\text{Peak current in } L_t = \frac{9 * \sqrt{2}}{2.5} = 5.09 \text{ A} \qquad \text{(A.6)}$$

At the same time, current in other phases = -2.55 A

$$\text{Hence, energy stored in } L_t = \frac{1}{2} L\,(5.09^2 + 2.55^2 + 2.55^2) = 4.12 \text{ J} \qquad \text{(A.7)}$$

Energy in Motor Inertia (*J*), i.e. kinetic energy:

$$\text{Rated speed of the motor} = \frac{120 * f}{p} = 157 \text{ rad/s} \quad \text{(A.8)}$$

where,

f – supply frequency,

p – number of poles in the motor

$$\text{Energy present in the rotating mass at rated speed} = \frac{1}{2} J\omega^2 = 2834.6 \text{ J} \quad \text{(A.9)}$$

where,

J – Moment of inertia (in this case, 0.23 kgm^2)

The kinetic energy varies proportional to the square of the motor speed.

Energy in dc Bus Capacitor (*C*):

With 415 V, 3 phase AC supply,

$$\text{dc voltage} = 415 * \sqrt{2} = 587 \text{ V} \quad \text{(A.10)}$$

$$\text{Rated dc current at full load of the motor} = \frac{5500}{587} = 9.37 \text{ A} \quad \text{(A.11)}$$

Let us assume that the bus capacitance C is chosen for 5 % ripple

$$C = i\frac{dt}{dV} = \frac{9.37}{50 * 6 * 587 * 0.05} = 1064 \ \mu\text{F} \approx 1000 \ \mu\text{F} \quad \text{(A.12)}$$

$$\text{Energy stored in the capacitor} = \frac{1}{2} CV^2 = 172.28 \text{ J} \quad \text{(A.13)}$$

If we do not require the capacitor to reduce the 300 Hz ripple in the ac supply frequency, it will nevertheless have to be large enough to keep switching frequency ripple to, say 5%. If the switching frequency of each of the six IGBTs is 5 kHz, then a switching event takes place at an average interval of $\frac{1}{30 * 10^3} = 33.33 \ \mu\text{s}$.

In this case,

$$C = i\frac{dt}{dV} = \frac{9.37}{30*10^3*587*0.05} = 10.64\ \mu\text{F} \approx 10\ \mu\text{F} \qquad \text{(A.14)}$$

$$\text{Energy stored in the capacitor} = \frac{1}{2}CV^2 = 1.72\ \text{J} \qquad \text{(A.15)}$$

It can be seen that there is considerable amount of energy available in the motor inductances and the rotating mass as compared to the energy levels present in the bus capacitor. These sources of energy shall be utilised in order to maintain the dc bus voltage at a required level during a voltage sag.

APPENDIX B

MATHEMATICAL MODELLING OF AN INDUCTION MOTOR

Field orientation control modelling of cage induction motors [IM] is discussed in [26-35]. The basic equations of the IM, viz. the equations corresponding to the stator voltage, rotor voltage, torque and speed, whose derivations are presented in [26] are as follows:

$$R_s\vec{i}_s + L_s\frac{d\vec{i}_s}{dt} + L_m\frac{d}{dt}\left(\vec{i}_r e^{j\varepsilon}\right) = \vec{V}_s \tag{B.1}$$

$$R_r\vec{i}_r + L_r\frac{d\vec{i}_r}{dt} + L_m\frac{d}{dt}\left(\vec{i}_s e^{-j\varepsilon}\right) = 0 \tag{B.2}$$

$$T_M = \frac{2}{3}L_m\,\mathrm{Im}\left[\vec{i}_s\left(\vec{i}_r e^{j\varepsilon}\right)^*\right] \tag{B.3}$$

$$J\frac{d\omega}{dt} = T_M - T_L \tag{B.4}$$

$$\frac{d\varepsilon}{dt} = \omega \tag{B.5}$$

where,

R_s, R_r – stator and rotor resistances

L_s, L_r - stator and rotor inductances

L_m – mutual inductance

ε – rotor position

ω - rotor angular velocity

$\vec{i}_S$, $\vec{i}_r$ - stator and rotor current vectors

T_M, T_L – motor and load torques

J – moment of inertia of the rotating mass

It can be seen from the motor torque equation (B.3) that, the motor generates a torque (T_M) based on the interaction between the rotor and stator current vectors. Since, rotor currents are not measurable in the case of squirrel cage motors, it should be replaced by an equivalent measurable quantity. The best alternative is the magnetising current

vector (i_{mR}) which is defined in equation (B.6) in terms of the stator coordinates [26]. The stator current vector ($\vec{i}_s$) is defined by equation (B.7) which is seen as moving with respect to the flux axis. The angular relationships of the moving current vectors are shown in Figure B.1.

$$\vec{i}_{mR} = i_{mR}e^{j\rho} = \vec{i}_s + (1+\sigma_r)\vec{i}_r e^{j\varepsilon} \tag{B.6}$$

$$\vec{i}_s e^{-j\rho} = i_s e^{j\delta} = i_{sd} + j i_{sq} \tag{B.7}$$

where,

$\vec{i}_{mR}$ - magnetising current vector

i_{mR} - magnetising current

ρ – magnetising (flux) axis position with respect to stator axis

σ_r – rotor leakage factor

δ - load angle

i_{sd}, i_{sq} – stator currents in d and q axes

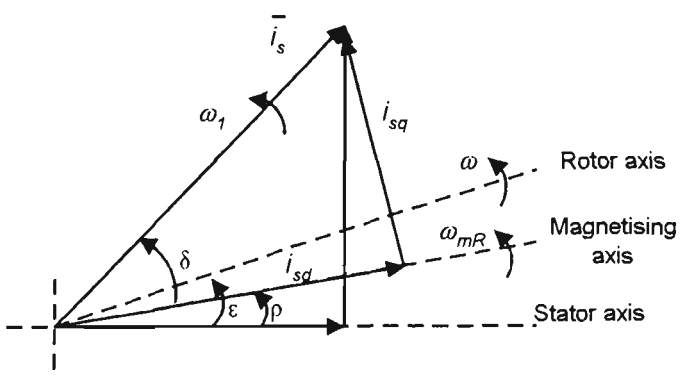


Figure B.1 Angular relationships of stator current vectors in an IM in steady state [26]

Based on equation (B.7), we get

$$i_{sd} = \mathrm{Re}\left[\vec{i}_s e^{-j\rho}\right] = i_s \cos\delta \tag{B.8}$$

$$i_{sq} = \mathrm{Im}\left[\vec{i}_s e^{-j\rho}\right] = i_s \sin\delta \tag{B.9}$$

Hence, in Figure B.1, i_{sd} is found to align with the magnetisation axis and i_{sq} is perpendicular to it.

By replacing $\vec{i}_r e^{j\varepsilon}$ from equation (B.6) in the torque equation (B.3), we get

$$T_M = \frac{2}{3}\frac{L_m}{1+\sigma_r}\,\mathrm{Im}\left[\vec{i}_s\left(\vec{i}_{mR}-\vec{i}_s\right)^*\right] = \frac{2}{3}\frac{L_m}{1+\sigma_r}\,\mathrm{Im}\left[\vec{i}_s\,\vec{i}_{mR}^{\,*}\right] \qquad \text{(B.10)}$$

But, from equation (B.6),

$$\vec{i}_{mR}^{\,*} = i_{mR}e^{-j\rho}$$

Hence, equation (B.10) becomes,

$$T_M = \frac{2}{3}\frac{L_m}{1+\sigma_r} i_{mR}\,\mathrm{Im}\left[\vec{i}_s e^{-j\rho}\right] \qquad \text{(B.11)}$$

By substituting equation (B.9), equation (B.11) becomes,

$$T_M = K i_{mR} i_{sq} \qquad \text{(B.12)}$$

where,

$$K = \frac{2}{3}\frac{L_m}{1+\sigma_r}$$

Here, i_{mR} is the magnetising current and is controlled by the stator d-axis current i_{sd} whereas the q-axis current i_{sq} is the torque producing component. Hence, i_{sd} and i_{sq} are the two independent quantities that control the flux and torque of the IM. Here, the flux axis, which is defined by the orientation of the magnetising current vector $\vec{i}_{mR}$, forms the frame of reference and it rotates across the stator axis at the stator frequency and across the rotor at the slip frequency [26].

Stator currents:

By substituting equation (B.6) into rotor voltage equation (B.2) and re-organising the real and imaginary terms, the equations representing the stator currents in field coordinates are derived as follows:

$$T_R\frac{di_{mR}}{dt} + i_{mR} = i_{sd} \qquad \text{(B.13)}$$

$$\frac{d\rho}{dt} = \omega_{mR} = \omega + \frac{i_{sq}}{T_R\, i_{mR}} \qquad \text{(B.14)}$$

or $$i_{sq} = (\omega_{mR} - \omega)\, T_R\, i_{mR} \qquad \text{(B.14a)}$$

where,

ω – rotor angular velocity

ω_{mR} – angular velocity of the magnetisation axis

From equation (B.13), it can be observed that the rotor flux (i_{mR}) lags i_{sd} by a delay equivalent to rotor time constant (T_r).

Stator voltages (V_{sd} and V_{sq}):

The stator voltages in field coordinates for an IM are derived from the stator voltage equation as shown below:

The stator voltage equation is

$$R_s\vec{i}_s + L_s\frac{d\vec{i}_s}{dt} + L_m\frac{d}{dt}\left(\vec{i}_r e^{j\varepsilon}\right) = \vec{V}_s \qquad \text{(B.1)}$$

By substituting for $\vec{i}_r e^{j\varepsilon}$ from equation (B.6), equation (B.1) becomes,

$$R_s\vec{i}_s + L_s\frac{d\vec{i}_s}{dt} + \frac{L_m(1+\sigma_s)}{(1+\sigma_s)(1+\sigma_r)}\frac{d}{dt}\left(\vec{i}_{mR} - \vec{i}_s\right) = \vec{V}_s \qquad \text{(B.15)}$$

Since, stator inductance $L_s = L_m(1+\sigma_s)$ and

total leakage factor $\sigma = 1 - \frac{1}{(1+\sigma_s)(1+\sigma_r)}$,

equation (B.15) becomes,

$$R_s\vec{i}_s + L_s\sigma\frac{d\vec{i}_s}{dt} + (1-\sigma)L_s\frac{d\vec{i}_{mR}}{dt} = \vec{V}_s \qquad \text{(B.16)}$$

From equation (B.7), the stator current vector can be represented as

$$\vec{i}_s = (i_{sd} + i_{sq})\, e^{j\rho}$$

Hence, $$\frac{d\vec{i}_s}{dt} = e^{j\rho}\left[\left(\frac{di_{sd}}{dt} - \omega_{mR}\, i_{sq}\right) + j\left(\frac{di_{sq}}{dt} + \omega_{mR}\, i_{sd}\right)\right] \qquad \text{(B.17)}$$

where,

$\omega_{mR} = \frac{d\rho}{dt}$ - speed of the flux axis

Also from equation (B.6), we know that the magnetising current vector

$$\vec{i}_{mR} = i_{mR}\, e^{j\rho}$$

Hence,

$$\frac{d\vec{i}_{mR}}{dt} = e^{j\rho}\left[\frac{di_{mR}}{dt} + j\,\omega_{mR}\, i_{mR}\right] \qquad \text{(B.18)}$$

The stator voltage vector can be represented as:

$$\vec{V}_s = \left(V_{sd} + jV_{sq}\right) e^{j\rho} \qquad \text{(B.19)}$$

By substituting equations (B.17) to (B.19) into equation (B.16) and by equating the real and imaginary components, we get:

$$V_{sd} = R_s\, i_{sd} + \sigma L_s\left(\frac{di_{sd}}{dt} - \omega_{mR}\, i_{sq}\right) + (1-\sigma)L_s\,\frac{di_{mR}}{dt} \qquad \text{(B.20)}$$

$$V_{sq} = R_s\, i_{sq} + \sigma L_s\left(\frac{di_{sq}}{dt} + \omega_{mR}\, i_{sd}\right) + (1-\sigma)\,\omega_{mR}\, i_{mR} \qquad \text{(B.21)}$$

Rotor currents:

The orientation of rotor current vector $\vec{i}_r$ in the magnetising frame of reference is shown in Figure B.2.

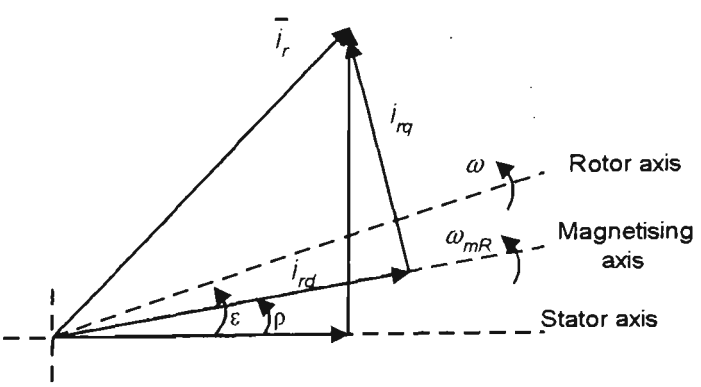


Figure B.2. Angular relationships of rotor current vectors in steady-state in an IM

By transforming the coordinates of the rotor current vector with respect to the magnetising axis, we get:

$$\vec{i}_r = \left(i_{rd} + ji_{rq}\right)e^{-j(\varepsilon-\rho)} \qquad \text{(B.22)}$$

Replacing $\vec{i}_r$ from rotor equation (B.2) utilising equation (B.6),

$$R_r\vec{i}_r + L_m e^{-j\varepsilon}\frac{d\vec{i}_{mR}}{dt} - j\omega L_m \vec{i}_{mR} e^{-j\varepsilon} = 0 \qquad \text{(B.23)}$$

Substituting equations (B.6), (B18) and (B.22) into equation (B.23),

$$i_{rd} + ji_{rq} = -\frac{1}{R_r}\left[L_m\left(\frac{di_{mR}}{dt} + j\omega_{mR} i_{mR}\right) - j\omega L_m i_{mR}\right] \qquad \text{(B.24)}$$

By equating the real and imaginary components from above equation, the rotor currents are obtained as follows:

$$i_{rd} = -\frac{L_m}{R_r}\frac{di_{mR}}{dt} \qquad \text{(B.25)}$$

$$i_{rq} = -\frac{L_m i_{mR}}{R_r}(\omega_{mR} - \omega) \qquad \text{(B.26)}$$

APPENDIX C

MATHEMATICAL MODELLING OF A SYNCHRONOUS RELUCTANCE MOTOR

Synchronous Reluctance Motors (SRMs) effectively have a salient pole rotor configuration and the rotor tries to align itself in the minimum reluctance position with respect to the synchronously rotating air-gap flux wave, (i.e.) along the magnetising axis [27]. They do not have rotor excitation and run at a synchronous speed governed by the supply frequency.

Stator voltage equations:

The stator voltage space phasor $\vec{V}_s$ in an SRM can be defined as:

$$\vec{V}_s = R_s \vec{i}_s + \frac{d\vec{\lambda}_s}{dt} \qquad \text{(C.1)}$$

where,

$\vec{i}_s$ - stator current space phasor

$\vec{\lambda}_s$ - stator flux space phasor

R_s - stator resistance

The angular position of the stator currents in the flux frame of reference is shown in Figure B.2.

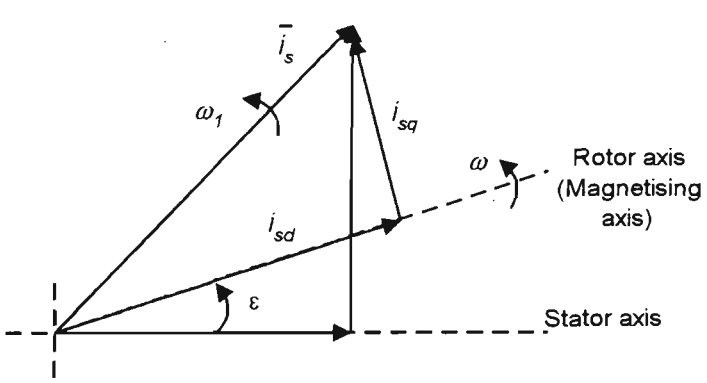


Figure B.2. Angular relationships of stator current vectors in steady-state in an SRM

In the rotor (magnetising) frame of reference, the stator current, voltage and flux space phasors can be represented as:

$$\vec{i}_s = (i_{sd} + ji_{sq})e^{j\varepsilon} \tag{C.2}$$

$$\vec{V}_s = (V_{sd} + jV_{sq})e^{j\varepsilon} \tag{C.3}$$

$$\vec{\lambda}_s = (\lambda_{sd} + \lambda_{sq})e^{j\varepsilon} \tag{C.4}$$

where,

ε – rotor position with respect to stationary reference frame

i_{sd}, i_{sq} – stator currents in d and q axes

V_{sd}, V_{sq} – stator voltages in d and q axes

λ_{sd}, λ_{sq} – stator flux linkages in d and q axes

Substituting equations (C.2) to (C.4) in (C.1), we get:

$$\begin{aligned}(V_{sd} + jV_{sq})e^{j\varepsilon} &= R_s(i_{sd} + ji_{sq})e^{j\varepsilon} + \frac{d}{dt}\left(\lambda_{sd} + j\lambda_{sq}\right)e^{j\varepsilon} \\ &= R_s(i_{sd} + ji_{sq})e^{j\varepsilon} + j\omega(\lambda_{sd} + j\lambda_{sq})e^{j\varepsilon} + \frac{d}{dt}(\lambda_{sd} + \lambda_{sq})e^{j\varepsilon}\end{aligned} \tag{C.7}$$

The d and q axis flux linkages can be expressed in terms stator currents [29] as:

$$\lambda_{sd} = L_{sd}i_{sd} \tag{C.5}$$

$$\lambda_{sq} = L_{sq}i_{sq} \tag{C.6}$$

Replacing λ_{sd} and λ_{sq} in equation (C.7) from equations (C.5) and (C.6), we get:

$$V_{sd} + jV_{sq} = R_s(i_{sd}+ji_{sq}) + j\omega L_{sd}i_{sd} - \omega L_{sq}i_{sq} + L_{sd}\frac{di_{sd}}{dt} + jL_{sq}\frac{di_{sq}}{dt} \tag{C.8}$$

By equating the real and imaginary terms in equation (C.8), the stator voltage equations in field coordinates are obtained as follows:

$$V_{sd} = R_s i_{sd} - \omega L_{sq}i_{sq} + L_{sd}\frac{di_{sd}}{dt} \tag{C.9}$$

$$V_{sq} = R_s i_{sq} + \omega L_{sd}i_{sd} + L_{sq}\frac{di_{sq}}{dt} \tag{C.10}$$

Torque and speed equations:

The SRM torque and speed equations are:

$$T_M = \frac{3}{2} N_{pp}(L_{sd} - L_{sq}) i_{sd} i_{sq} \tag{C.11}$$

$$T_M - T_L = J\frac{d\omega}{dt} \tag{C.12}$$

$$\omega = \frac{d\varepsilon}{dt} \tag{C.13}$$

where,

N_{pp} – number of pole pairs

T_M – motor torque

T_L – load torque

λ_{sd}, λ_{sq} – stator flux linkages in d and q axes

Appendix D

Switching Vector Selection

Here, the switching sequence of the voltage source inverter when controlled by field orientation technique (vector control) is analysed.

The PWM inverter, which is employed in the VSD configuration chosen in this thesis, has 6 switches, with two of them on each of the three inverter poles (legs). The inverter supplies power to the ac motor by connecting the three motor terminals to either the positive or negative terminal of the dc bus. A simplified representation of a three-phase voltage source inverter circuit is shown in Figure D.1.

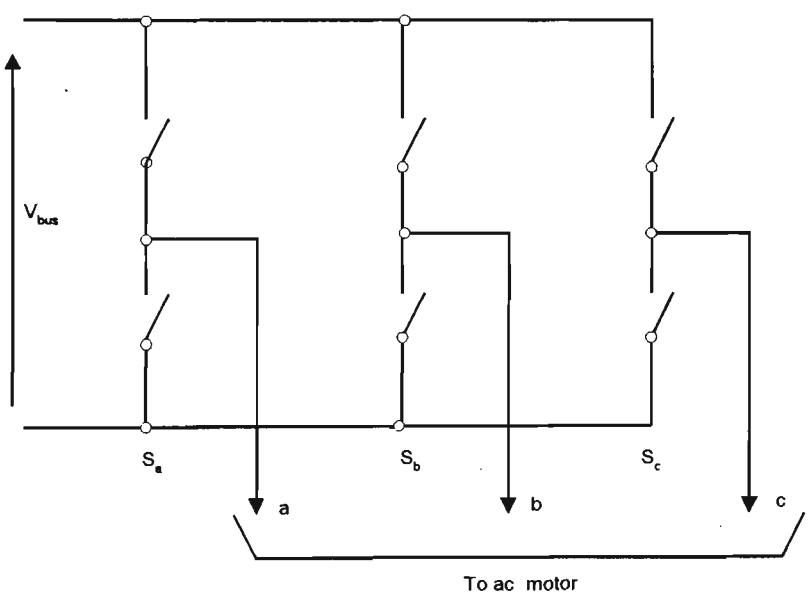


Figure D.1. A three-phase inverter

Both switches on a pole must not be turned on at the same time, in order to avoid short circuiting of the dc supply. Similarly, both switches in a leg must not be opened at the same time. The control system must ensure that each phase of the ac motor is connected to either the positive or the negative terminal of the dc bus.

Since, there are two possible connections for each of the three phases, there are 2^3 possible connections, i.e. 8 combinations of switching vectors are available to the control system.

By representing the connection of the motor terminals to the positive and negative dc bus terminals as '1'and '0' respectively, and by designating the switching pattern of each of the inverter poles as S_a, S_b and S_c, the terminal voltages of each phase with respect to the star point in the motor can be mentioned as,

$$V_a = V_{bus}\, S_a - V_{star} \tag{D.1}$$

$$V_b = V_{bus}\, S_b - V_{star} \tag{D.2}$$

$$V_c = V_{bus}\, S_c - V_{star} \tag{D.3}$$

where,

V_{bus} - bus capacitor dc voltage

V_{star} - star point voltage

The voltage space phasor is given by,

$$\vec{V} = V_a + V_b\, e^{j2\pi/3} + V_c\, e^{j4\pi/3} \tag{D.4}$$

$$= V\left(S_a + S_b\, e^{j2\pi/3} + S_c\, e^{j4\pi/3}\right) - V_{star}\left(1 + e^{j2\pi/3} + e^{j4\pi/3}\right)$$

$$= V\,\vec{S}$$

where,

$$\vec{S} = S_a + S_b\, e^{j2\pi/3} + S_c\, e^{j4\pi/3} \tag{D.5}$$

is called the "Switching Vector".

For the 8 possible combinations of $\vec{S}$ (S_a S_b S_c), the values of $\vec{S}$ and $\vec{V}$ in the real and imaginary coordinates and their angle with respect to the real axis are,

S_a S_b S_c	Re($\vec{S}$)	Im($\vec{S}$)	Re($\vec{V}$)	Im($\vec{V}$)	Angle
000	0	0	0	0	
001	$-\frac{1}{2}$	$-j\frac{\sqrt{3}}{2}$	$-\frac{1}{2}V_{bus}$	$-j\frac{\sqrt{3}}{2}V_{bus}$	240°
010	$-\frac{1}{2}$	$j\frac{\sqrt{3}}{2}$	$-\frac{1}{2}V_{bus}$	$j\frac{\sqrt{3}}{2}V_{bus}$	120°
011	-1	0	$-V_{bus}$	0	180°
100	1	0	V_{bus}	0	0°
101	$\frac{1}{2}$	$-j\frac{\sqrt{3}}{2}$	$\frac{1}{2}V_{bus}$	$-j\frac{\sqrt{3}}{2}V_{bus}$	300°
110	$\frac{1}{2}$	$j\frac{\sqrt{3}}{2}$	$\frac{1}{2}V_{bus}$	$j\frac{\sqrt{3}}{2}V_{bus}$	60°
111	0	0	0	0	

Two of the switching vectors, viz. 000 and 111, are zero vectors and the other six outer vectors are unit vectors on the complex plane and they are called the "active vectors".

The position of the switching vectors on the complex plane are shown in Figure D.2.

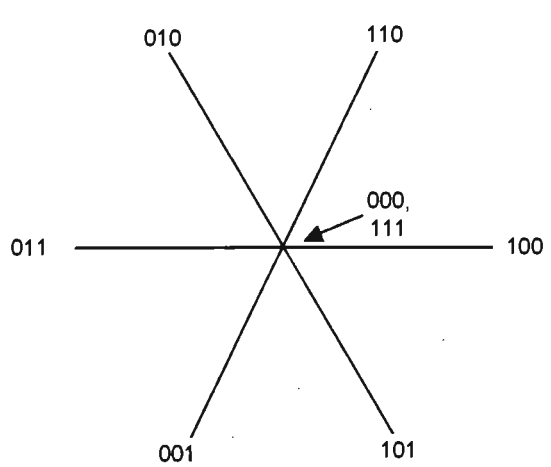


Figure D.2. Switching vectors in the complex plane

As discussed in Sections 2.3.1 and 2.3.2 regarding the control of IM and SRM VSDs respectively, the current controllers generate the reference voltage $\vec{V}_{ref}$ depending on the set points (viz. speed, torque and rotor flux) and operating conditions.

$$\vec{V}_{ref} = V_{realref} + j\,V_{imagref} \qquad \text{(D.6)}$$

where,

$V_{realref}$ - Voltage set-point in real coordinates fixed to stator

$V_{imagref}$ - Voltage reference in imaginary coordinates fixed to stator

The control system chooses the appropriate switching vector based on the voltage reference vector $\vec{V}_{ref}$ in order to ensure proper VSD operation. The position of the reference vector in the complex plane is shown in Figure D.3.

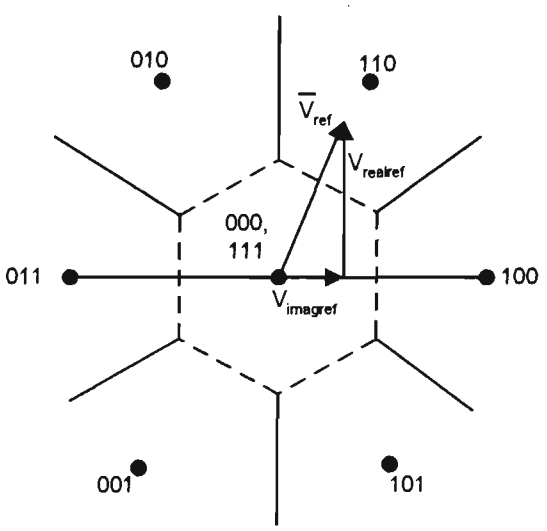


Figure D.3. Switching vector selection

If the magnitude of the selected vector $\vec{V}_{ref}$ is less than half the dc link voltage (V_{bus}), then one of the zero vectors is chosen, otherwise, one of the active vectors closest to the position of $\vec{V}_{ref}$ is selected and the inverter switching sequence is controlled by the control system.

Notice that, as we travel around the non-zero active vectors, the switching pattern changes by only one switch at a time. The sequence is 100, 110, 010, 011, 001, 101,

100). Also, to move from any of these vectors to a zero vector, only one switch needs to be changed, since either of the two zero vectors (000 or 111) can be chosen. So, to select a neighbouring vector, only one pair of switches in an inverter pole need to be changed. However, to move from one non-zero vector to another by two steps, two pairs of switches need to be changed. To move to the directly opposite vector, we need to change all the inverter switches. Therefore, the switching frequency can be kept to a minimum by limiting the choice of voltage vectors as below:

a) If the present vector is one of the outer active vectors, only the two immediate neighbours or a zero vector may be chosen.

b) If the present vector is one of the zero vectors, only the 3 active vectors require only one switching transition, can be selected. (i.e. from 000, only 100, 010 or 001 can be chosen. Similarly from 111, only 110, 011 or 101 can be chosen).

The movement from one voltage vector to another requires one switch in a pole be turned ON while the other turned OFF. If in 1 second there are N vector transitions, then on the average, each switch will turn ON $\frac{N}{6}$ times and turn OFF $\frac{N}{6}$ times. Hence, the average switching frequency will be $\frac{N}{6}$.

APPENDIX E

PARAMETERS OF INDUCTION MOTOR VSD (IM VSD)

Motor Parameters:

Power Rating	- 5.5 kW
Input supply conditions	- 415 V AC, 3ph, 50 Hz
Rated speed (ω)	- 1500 rpm (157 rad/s)
Rated torque (T_M)	- 36 Nm
Number of pole pairs (N_{pp})	- 2
Stator resistance (R_s)	- 0.673 Ω
Rotor resistance (R_r)	- 1.2964 Ω
Mutual Inductance (L_m)	- 0.2925 H
Stator Leakage factor (σ_S)	- 0.0484
Rotor Leakage factor (σ_r)	- 0.0484
Moment of inertia (J)	- 0.23 Kg m^2

VSD Parameters/Settings:

Torque Limit (T_{LT})	- 54 Nm
Bus capacitor (C)	- 1000 μF
Speed controller proportional gain ($K_{p,sp}$)	- 148
Speed controller integral gain ($K_{i,sp}$)	- 31671
Magnetising current ref. (i_{mRref})	- 9 A
Minimum limit of i_{mR} (i_{mRmin})	- 0 A
Maximum limit of i_{sd} (i_{sdmax})	- 9 A
Minimum limit of i_{sd} (i_{sdmin})	- 0 A
Cut-off speed for control transition (ω_{cutoff})	- 15.7 rad/s
Bus Voltage Regulator 1 proportional gain ($K_{p,b1}$)	- 2.68
Bus Voltage Regulator 1 integral gain ($K_{i,b1}$)	- 573.75
Bus Voltage Regulator 2 proportional gain ($K_{p,b2}$)	- 0.3585
Bus Voltage Regulator 2 integral gain ($K_{i,b2}$)	- 128.45

Simulation parameters:

Per-phase line resistance (R_a)	- 0.0085 Ω
Per-phase line inductance (L_a)	- 0.1 mH
IGBT Switching frequency	- 5 kHz
Sampling time (dt)	- 33 μs
Velocity reference (ω_{ref})	- 0 to 157 rad/s

APPENDIX F

PARAMETERS OF SYNCHRONOUS RELUCTANCE MOTOR VSD (SRM VSD)

Motor Parameters

Power Rating	- 5.5 kW
Input supply conditions	- 415 V AC, 3ph, 50 Hz
Rated speed (ω)	- 1500 rpm (157 rad/s)
Rated torque (T_M)	- 36 Nm
Number of pole pairs (N_{pp})	- 2
Stator resistance (R_s)	- 0.6 Ω
Moment of inertia (J)	- 0.23 Kg m^2
Stator d-axis inductance (L_{sd})	- 76.8 mH
Stator q-axis inductance (L_{sq})	- 9.8 mH

VSD Parameters / Settings

Torque Limit (T_{LT})	- 54 Nm
Bus capacitor (C)	- 1000 μF
Speed controller proportional gain ($K_{p,sp}$)	- 115.4
Speed controller integral gain ($K_{i,sp}$)	- 19293
Magnetising current ref. i_{sd} (i_{sdref})	- 9 A
Minimum limit of i_{sd} (i_{sdmin})	- 0 A
Cut-off speed for control transition (ω_{cutoff})	- 15.7 rad/s
Bus Voltage Regulator 1 proportional gain ($K_{p,b1}$)	- 1.8155
Bus Voltage Regulator 1 integral gain ($K_{i,b1}$)	- 303.6
Bus Voltage Regulator 2 proportional gain ($K_{p,b2}$)	- 0.0849
Bus Voltage Regulator 2 integral gain ($K_{i,b2}$)	- 72.1

Simulation parameters:

Per-phase line resistance (R_a)	- 0.0085 Ω
Per-phase line inductance (L_a)	- 0.1 mH
IGBT Switching frequency	- 5 kHz
Sampling time (dt)	- 33 μs
Velocity reference (ω_{ref})	- 0 to 157 rad/s

APPENDIX G

TUNING OF CONTROLLERS FOR INDUCTION MOTOR VSD (IM VSD)

(a) Speed Controller

The simplified block diagram of the speed control loop of an IM VSD is shown in Figure G.1. Only full flux operation is considered in this thesis and field weakening is not considered.

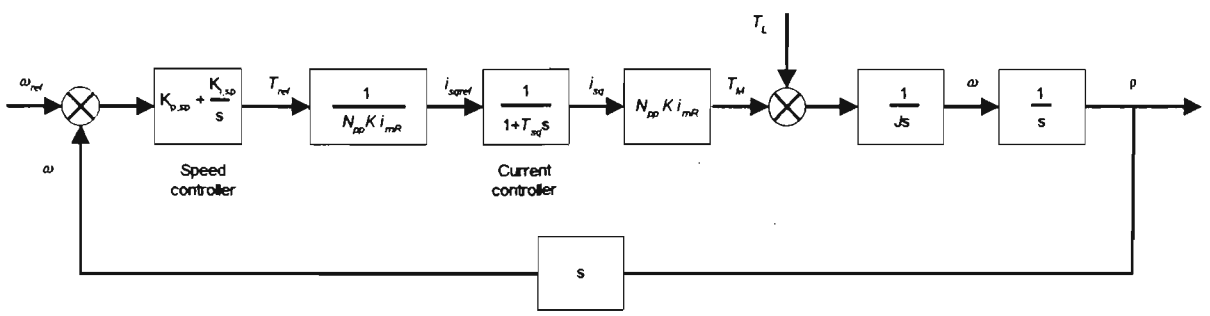


Figure G.1. Speed control loop block diagram of an IM VSD

It can be observed that, the above control block diagram shown in Fig. G.1. represents the functional behaviour of the IM VSD during speed control which is described in Subsection 2.3.1. The speed regulator, which is a proportional-integral (PI) controller, generates a torque reference (T_{ref}) based on the speed error, which is converted into a current reference (i_{sqref}) based on motor torque equation (G.1). The closed loop operation of the current controller is modelled by the transfer function $\frac{1}{1+T_{sq}s}$ [26], where the time constant T_{sq} is the time taken for 100% change in the torque producing current i_{sq} by applying the rated dc voltage V_{bus} and assuming that half the rated voltage is already available in the motor as back emf. The calculation of T_{sq} is shown by equation (G.2). The motor torque, speed and position calculations are based on equations (G.1), (G.3) and (G.4).

$$T_M = N_{pp} K i_{mR} i_{sq} \qquad \text{(G.1)}$$

$$T_{sq} = \sigma_S L_m \frac{i_{sq,rated}}{0.5 * V_{dc,rated}} = \frac{0.0484 * 0.182 * 17.28}{0.5 * 587} = 518.623\ \mu s \quad \text{(G.2)}$$

$$T_M - T_L = J\frac{d\omega}{dt} \quad \text{(G.3)}$$

$$\omega = \frac{d\rho}{dt} \quad \text{(G.4)}$$

where,

$$K = \frac{2}{3}(1-\sigma)L_s$$

N_{pp} – number of pole pairs

i_{mR} – rotor magnetising current

i_{sq} – stator q-axis torque producing current

σ_s – stator leakage inductance

L_m – mutual inductance of the motor

$i_{sq,rated}$ – i_{sq} at rated motor torque

$V_{dc,rated}$ – rated dc bus capacitor voltage

T_M - motor torque

T_L - load torque,

J – moment of inertia of rotating mass

ρ - rotor position

The open loop transfer function [OLTF] can be written as,

$$\text{OLTF} = \left[\frac{K_{p,sp}s + K_{i,sp}}{s}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{1}{Js}\right] \quad \text{(G.5)}$$

$$= \left[\frac{G(1+T_s s)}{s}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{1}{Js}\right]$$

where,

$$G = K_{i,sp} \quad \text{(G.6)}$$

$$G\,T_s = K_{p,sp} \quad \text{(G.7)}$$

The bode plot of the open loop gain has a slope of -40 db/decade except between the two corner frequencies. The controller corner frequency is chosen such that the slope in this interval is -20 db/decade.

The controller gains G and T_s can be chosen such that the zero db point, i.e. cross-over frequency ω_{cross}, is in the centre of the section with -20 db/decade slope. This gives the maximum phase margin (which is 53°).

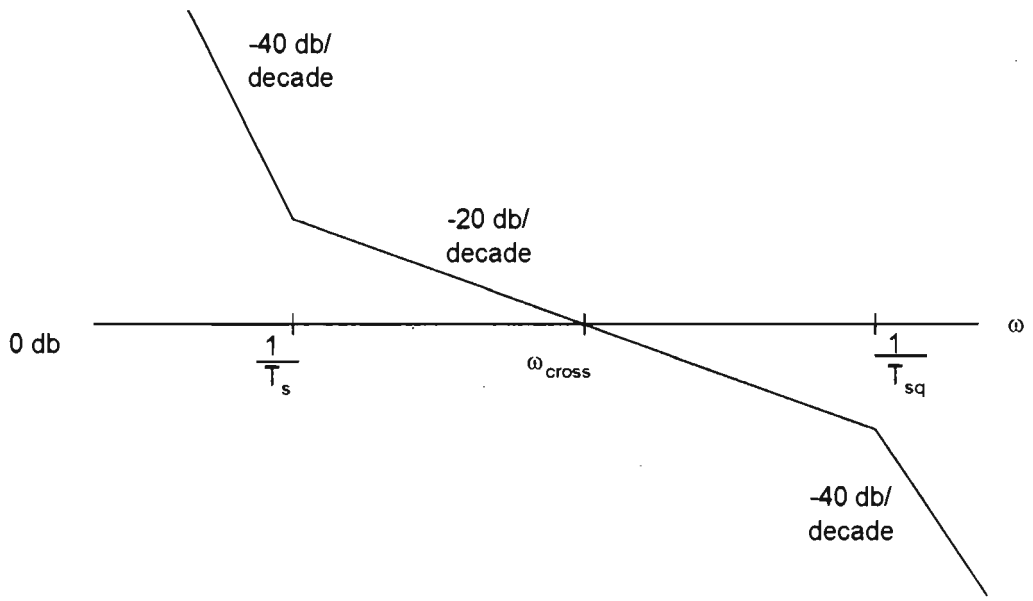


Figure G.2. Bode plot of the speed loop

In terms of the corner frequency, the optimum values of T_s and ω_{cross} are [26],

$$\frac{1}{T_{sq}} = \frac{9}{T_s} \tag{G.8}$$

$$\omega_{cross} = \frac{3}{T_s} = \frac{1}{3T_{sq}} = \frac{1}{3*518.623*10^{-6}} = 642.72 \text{ rad / s} \tag{G.9}$$

At ω_{cross},

OLTF =1

i.e.
$$\left[\frac{G|1+j3|}{\left|1+j\frac{1}{3}\right|}\right]\left[\frac{3T_{sq}3T_{sq}}{J}\right] = 1 \tag{G.10}$$

By solving equation (G.10), we get:

$$G = \frac{J}{27T_{sq}^2} \tag{G.11}$$

$$T_S = 9T_{sq} \tag{G.12}$$

The proportional (P) and integral (I) gains of the speed loop are obtained as:

$$K_{p,sp} = G\,T_S = \frac{J}{3\,T_{sq}} = \frac{0.23}{3*518.623*10^{-6}} = 148 \tag{G.13}$$

$$K_{i,sp} = G = \frac{J}{27\,T_{sq}^2} = \frac{0.23*10^{12}}{27*518.623^2} = 31671 \tag{G.14}$$

Bus Voltage Controller 1 (for kinetic energy recovery):

This voltage controller generates the torque reference for the motor during kinetic energy recovery from the rotating mass corresponding to Control Situation 2, when the motor speed is above the minimum limit (i.e. 10% of the rated speed) during a sag condition. The control block diagram is shown in Figure G.3.

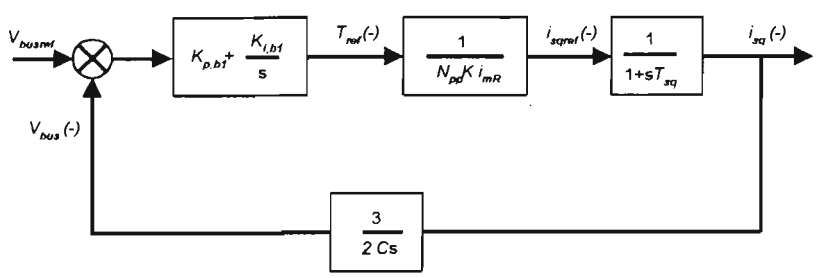


Figure G.3 Control block diagram of an IM VSD during bus voltage control by recovering load kinetic energy

As explained in Subsection 2.4.1 earlier, it can be seen that this controller generates a reverse torque reference in order to reverse the power flow from the motor to the dc bus. This torque reference is converted into a current reference (i_{sqref}) as per equation (G.1) which is referred to in the speed loop tuning. For the motor considered in this thesis, the torque-to-current conversion factor is calculated as:

$$\frac{1}{N_{pp}K i_{mR}} = \frac{1}{2*0.1157*9} = 0.48 \qquad \text{(G.15)}$$

where,

$$K = \frac{2}{3}(1-\sigma)L_s = \frac{2}{3}(1-0.090199)*0.1908 = 0.1157$$

i_{mR} = rated magnetising current = 9A

The closed loop current controller is once again modelled by the transfer function $\frac{1}{1+T_{sq}s}$ similar to the speed loop tuning. In this control, the magnetising current i_{mR} (and hence i_{sd}) is maintained at the rated value and the reversal of i_{sq} reverses the flow of the current (I_{out}) from the motor to the capacitor (C) which results in the increase of the capacitor bus voltage V_{bus} according to equation (G.16). Assuming that, the product $V_{sd}i_{sd}$ is constant and V_{sq} applied is equivalent to V_{bus}, the relationship between i_{sq} and I_{out} is shown in equation (G.17).

$$I_{out} = \frac{2(V_{sd}i_{sd} + V_{sq}i_{sq})}{3V_{bus}} \qquad \text{(G.16)}$$

$$I_{out} = \frac{2}{3}i_{sq} \qquad \text{(G.17)}$$

The open loop transfer function (OLTF) becomes:

$$\text{OLTF} = \left[\frac{K_{p.bl}s + K_{i.bl}}{s}\right]\left[\frac{1}{N_{pp}Ki_{mR}}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{3}{2Cs}\right] \qquad \text{(G.18)}$$

$$= \left[\frac{G(1+T_s s)}{s}\right]\left[\frac{1}{N_{pp}Ki_{mR}}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{3}{2Cs}\right]$$

where,

$$G = K_{i.bl} \qquad \text{(G.19)}$$

$$G\,T_s = K_{p.bl} \qquad \text{(G.20)}$$

In this case also, the bode plot is similar to the case of the speed loop (Figure G.2). The gains (G and T_s) are chosen such that the cross-over frequency ω_{cross} (i.e. the zero db point) is at the center of the section with a slope of -20 db/decade. A maximum phase margin of 53° is obtained at this frequency.

In this case also, the optimum values of Ts and ω_{cross} [26] are:

$$\frac{1}{T_{sq}} = \frac{9}{T_s} \tag{G.21}$$

$$\omega_{cross} = \frac{3}{T_s} = \frac{1}{3T_{sq}} = \frac{1}{3*518.623*10^{-6}} = 642.72 \text{ rad / s} \tag{G.22}$$

At the cross-over frequency ω_{cross},

$$\text{OLTF} = 1 \tag{G.23}$$

i.e.
$$\left[\frac{G\left|1+j3\right|}{\left|1+j\frac{1}{3}\right|}\right]\left[\frac{3T_{sq}3T_{sq}0.48}{2C}\right] = 1 \tag{G. 24}$$

By solving the above equation, the proportional (P) and integral (I) gains of the Bus Voltage Controller 1 are obtained for a bus capacitance of 1000 μF as,

$$K_{p.b1} = \text{G Ts} = 2.68 \tag{G.25}$$

$$K_{i.b1} = 573.75 \tag{G.26}$$

For C=250 μF, the P and I gains become:

$$K_{p.b1} = 0.67 \tag{G.27}$$

$$K_{i.b1} = 143 \tag{G.28}$$

Bus Voltage Controller 2 (Magnetisation Energy recovery):

This controller generates the flux (i_{mR}) reference during control situation 3, i.e. when a voltage sag occurs and the motor speed becomes less than 10% of its rated speed, as defined in Subsection 2.2.2. The motor flux (i.e. i_{mR} and hence i_{sd}) is reduced until zero

in order to recover the energy available in the winding inductances. The intended strategy is to reverse the direction of flow of I_{out} from the motor to the dc bus and maintain the dc bus capacitor voltage at the desired level. No torque reference is applied to the motor during this control (i.e. $i_{sq} = 0$). The relationship between i_{sd} and I_{out} during this situation can be obtained from equation (G.16) by assuming that the average V_{sd} applied during this control is equivalent to the bus voltage V_{bus}.

$$I_{out} = \frac{2}{3} i_{sd} \tag{G.29}$$

In this case, the d-axis current controller is optimised by the transfer function $\frac{1}{1 + T_{mR} s}$ where the magnetising time constant of the motor, T_{mR}, is the time taken for a 100% change in the magnetising current by applying the rated capacitor voltage (V_{bus}). The relevant calculation is shown by equation (G.30):

$$T_{mR} = \frac{L_m \, i_{mR,rated}}{V_{bus,rated}} = \frac{0.182 * 9}{586} \approx 2.79 \text{ ms} \tag{G.30}$$

In this case, the transfer of energy between the magnetising inductance L_m and the capacitor C is non-linear as shown by the following equations. Assuming that, a small change in i_{mR} (i.e. di_{mR}) corresponds to a change dV_{bus} in the capacitor voltage,

$$\text{Energy flowing into } C = \frac{1}{2}\left(\frac{3}{2}\right) C \, dV_{bus}^2 = \frac{3}{4} C \, 2V_{bus} \, dV_{bus} = \frac{3}{2} C V_{bus} \, dV_{bus} \tag{G.31}$$

$$\text{Similarly, energy out of } L_m = \frac{1}{2} L_m \, di_{mR}^2 = L_m \, i_{mR} \, di_{mR} \tag{G.32}$$

Equating (G.31) and (G.32) and replacing V_{bus} and i_{mR} by their average values on the basis of a gross assumption, we get,

$$\frac{3}{2} C V_{bus,av} \frac{dV_{bus}}{dt} = L_m i_{mR,av} \frac{di_{mR}}{dt} \tag{G.33}$$

$$\text{i.e.} \quad \frac{3}{2} C V_{bus,av} \, s \, V_{bus,av} = L_m i_{mR,av} \, s \, i_{mR} \tag{G.34}$$

$$\text{or} \quad V_{bus} = \frac{2 \, L_m \, i_{mR,av}}{3 \, C \, V_{bus,av}} \, i_{mR} \tag{G.35}$$

The control block diagram can now be modelled as shown in Figure G.4.

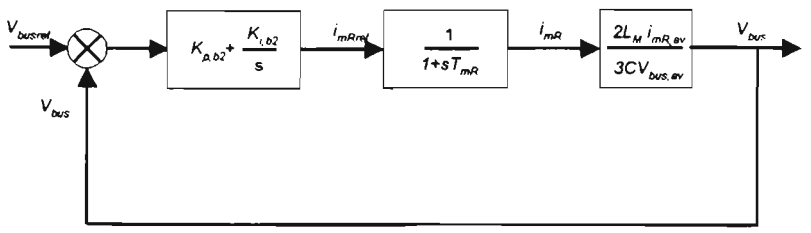


Figure G.4 Control block diagram of an SRM VSD during bus voltage control by recovering magnetisation energy.

The open loop transfer function (OLTF) becomes:

$$\text{OLTF} = \left[\frac{K_{p,b2}\, s + K_{i,b1}}{s}\right]\left[\frac{1}{1+s\, T_{sd}}\right]\left[\frac{2L_{sd}\, i_{sd,av}}{3\, C\, V_{bus,av}}\right] \qquad \text{(G.36)}$$

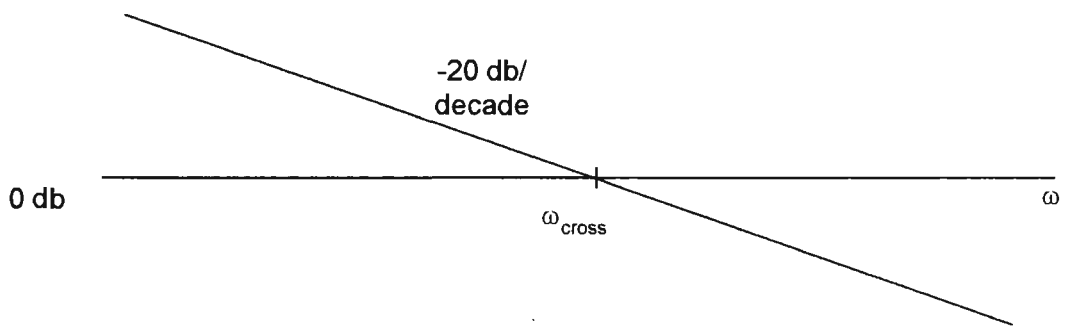


Figure G.5 Bode plot of Bus Voltage Controller 2

In this case, the bode plot has an uniform slope of -20 db/decade. The controller zero can be placed anywhere within the allowable limits for the control to cancel the pole and then the phase margin is always 90°. The proportional (P) and integral (I) gains are calculated for a unity gain and a bandwidth of 119.45 rad/s, which is one-third the corner frequency of the current loop. With a 1000 μF bus capacitor,

$$\text{OLTF} = 1\angle -90^\circ$$

$$\text{(i.e.)} \qquad \left[\frac{K_{p,b2}\, j119.45 + I}{j119.45}\right]\left[\frac{1}{1+0.002355\, j119.45}\right]\left[\frac{2*0.182*4.5}{3*0.001*587}\right] = -j$$

By solving the above equation, we get:

$K_{p,b2} = 0.3585$

$K_{i,b2} = 128.45$

In the case of a 250 μF capacitor, the controller gains become:

$K_{p,b2} = 0.09$

$K_{i,b2} = 32$

APPENDIX H

TUNING OF CONTROLLERS FOR SYNCHRONOUS RELUCTANCE MOTOR VSD (SRM VSD)

(a) Speed Controller

The control loop block diagram for speed control of an SRM VSD is shown in Figure H.1. Full flux operation of the motor alone is considered here and field weakening is not considered.

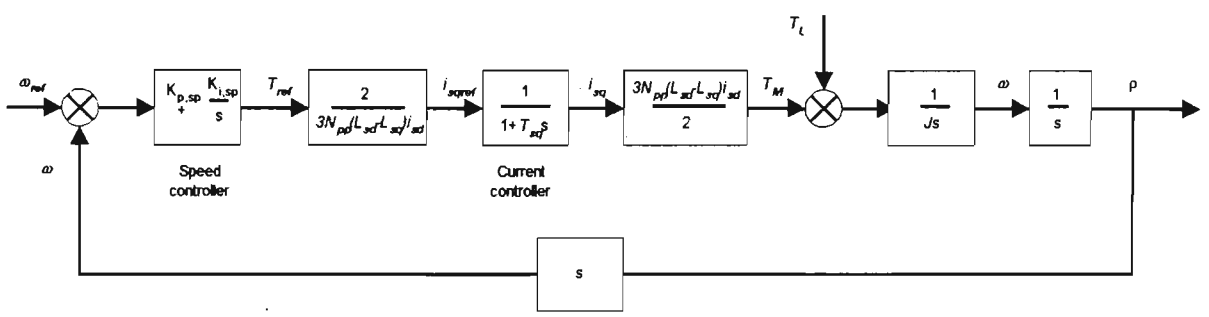


Figure H.1. Speed control loop block diagram of an SRM VSD

From the above block diagram, it can be observed that the various control blocks represent the operational behaviour of the SRM during speed control as described in Subsection 2.3.2. The proportional-integral (PI) controller of the speed loop, which is being optimised here, generates a suitable torque reference (T_{ref}) in order to maintain the motor at the set speed during the closed-loop control. T_{ref} is then converted into a current reference (i_{sqref}) as per motor torque equation (H.1) and applied to the current controller as the control input. The closed loop operation of the current controller is optimised by the transfer function $\frac{1}{1+T_{sq}s}$ [26]. Here the time constant T_{sq} is the time taken for a 100% change in the torque producing current i_{sq} by applying the rated voltage (V_{bus}) to the motor assuming that half the voltage is already available in the motor as back emf. The calculation of T_{sq} is shown by equation (H.2).

$$T_M = \frac{3}{2} N_{pp}(L_{sd} - L_{sq}) i_{sd} i_{sq} \qquad \text{(H.1)}$$

$$T_{sq} = L_{sq} \frac{i_{sq,rated}}{0.5 * V_{bus,rated}} = \frac{9.8 * 10^{-3} * 19.9}{0.5 * 587} = 664.479\ \mu s \tag{H.2}$$

$$d\omega = \frac{(T_M - T_L)dt}{J} \tag{H.3}$$

$$\omega = \frac{d\varepsilon}{dt} \tag{H.4}$$

where,

N_{pp} – number of pole pairs

L_{sd} – stator d-axis inductance

L_{sq} – stator q-axis inductance

i_{sd} – magnetising current

i_{sq} – torque producing current

$i_{sq,rated}$ –stator q-axis current at rated motor torque,

$V_{bus,rated}$ – rated dc bus capacitor voltage

T_M - motor torque

T_L - load torque,

J – moment of inertia of rotating mass

ε - rotor position

The motor torque (T_M), speed (ω) and position (ε) are calculated using equations (H.1), (H.2) and (H.4) respectively and are represented in the relevant blocks of Figure H.1.

The open loop transfer function (OLTF) can be written as:

$$\begin{aligned} \text{OLTF} &= \left[K_{p,sp} + \frac{K_{i,sp}}{s}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{1}{Js}\right] \\ &= \left[\frac{G(1+T_s s)}{s}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{1}{Js}\right] \end{aligned} \tag{H.5}$$

where,

$$G = K_{i,sp} \tag{H.6}$$

$$G\,T_s = K_{p,sp} \tag{H.7}$$

The bode plot of the open loop gain has a slope of -40 db/decade except between the two corner frequencies. The controller corner frequency is chosen such that the slope in this interval is -20 db/decade.

The controller gains G and T_s can be chosen such that the zero db point, i.e. cross-over frequency ω_{cross}, is of the center of the section of slope -20 db/decade which gives the maximum phase margin (53°).

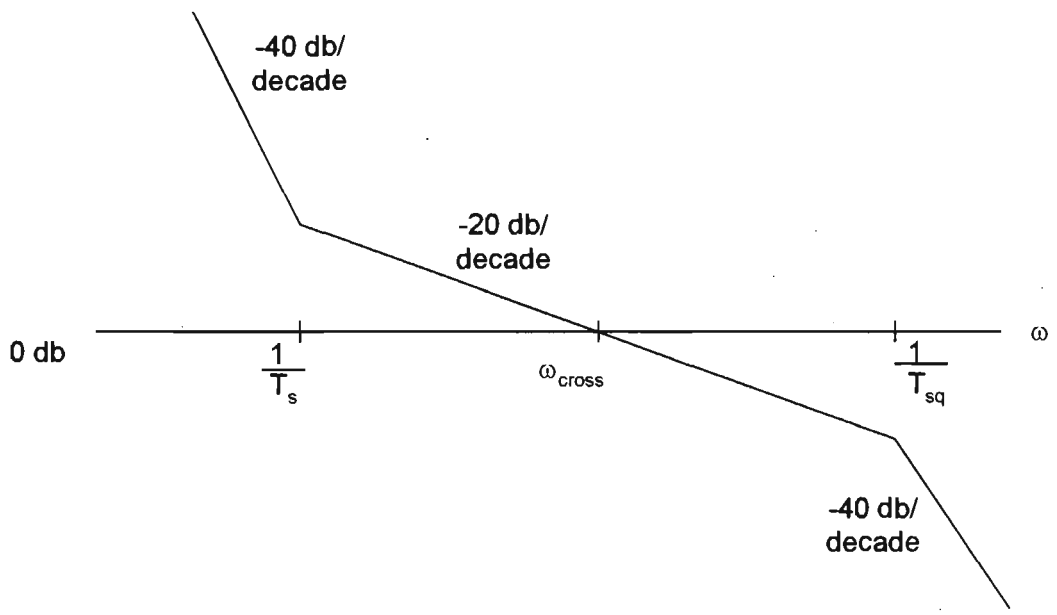


Figure H.2. Bode plot of the speed loop

In terms of the corner frequency, the optimum values of T_s and ω_{cross} are [26]:

$$\frac{1}{T_{sq}} = \frac{9}{T_s} \tag{H.8}$$

$$\omega_{cross} = \frac{3}{T_s} = \frac{1}{3T_{sq}} = \frac{1}{3 * 664.479 * 10^{-6}} = 501.65 \text{ rad / s} \tag{H.9}$$

At ω_{cross},

OLTF =1

i.e. $$\left[\frac{G\left|1+j3\right|}{\left|1+j\frac{1}{3}\right|}\right]\left[\frac{3T_{sq}3T_{sq}}{J}\right] = 1 \tag{H.10}$$

By solving (H.10), we get:

$$G = \frac{J}{27T_{sq}^2} \tag{H.11}$$

$$T_s = 9T_{sq} \tag{H.12}$$

The P and I gains of the speed loop are obtained as follows:

$$K_{p,sp} = G\,T_s = \frac{J}{3\,T_{sq}} = \frac{0.23}{3*664.479*10^{-6}} = 115.4 \tag{H.13}$$

$$K_{i,sp} = G = \frac{J}{27\,T_{sq}^2} = \frac{0.23*10^{12}}{27*664.479^2} = 19293 \tag{H.14}$$

Bus Voltage Controller 1 (for kinetic energy recovery):

This controller generates torque reference to the motor during Control Situation 2 as defined in the control strategy (Subsection 2.2.2). In this situation, the capacitor voltage is maintained at the nominal value of 586 V by recovering the kinetic energy available in the rotating mass. The control block diagram is shown in Figure H.3.

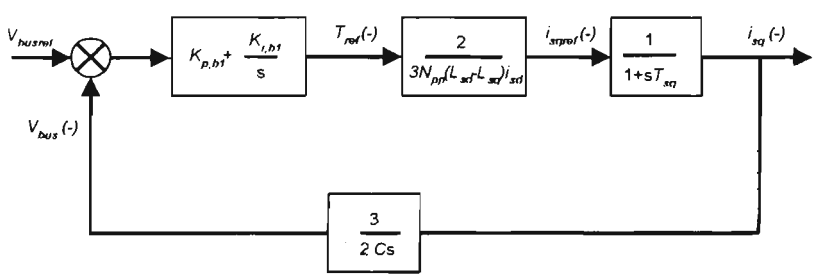


Figure H.3 Control block diagram for bus voltage control of an SRM by recovering kinetic energy

As explained in the control strategy (Subsection 2.4.1), this PI controller generates a reverse torque reference during a sag condition in order to reverse the power flow from the motor to the dc bus. A corresponding current reference (i_{sqref}) is calculated as shown in the block diagram based on equation (H.1) and it forms the input to the current controller. For the 5.5 kW SRM considered here (with parameters as shown in

Appendix F), the torque-to-current conversion factor is calculated as shown by equation (H.7).

$$\frac{2}{3N_{pp}(L_{sd}-L_{sq})i_{sd}} = \frac{2}{3*2*(76.8-9.8)*10^{-3}*9} \approx 0.5528 \qquad \text{(H.15)}$$

where,

N_{pp} – number of pole pairs

i_{sd} - rated magnetising current (9A)

L_{sq} – stator q-axis inductance

L_{sd} – stator d-axis inductance

The closed loop current controller operation is once again optimised by the transfer function $\frac{1}{1+T_{sq}s}$ similar to the case of the speed loop tuning. Since the magnetising current i_{sd} is maintained at the rated value and i_{sq} is reversed during this control, the dc current I_{out} flows from the motor to the capacitor (C) which results in an increase of the capacitor bus voltage V_{bus} according to equation (H.8). Assuming $V_{sd}i_{sd}$ as constant and on the average V_{sq} to be the same as V_{bus}, the relationship between I_{out} and i_{sq} is approximated by equation (H.17). The reversed current I_{out} charges the bus capacitor. This action is represented in the control block diagram of Figure H.3.

$$I_{out} = \frac{2(V_{sd}i_{sd}+V_{sq}i_{sq})}{3V_{bus}} \qquad \text{(H.16)}$$

$$I_{out} = \frac{2}{3}i_{sq} \qquad \text{(H.17)}$$

The open loop transfer function (OLTF) of the voltage controller is:

$$\text{OLTF} = \left[\frac{K_{p.bl}s+K_{i.bl}}{s}\right]\left[\frac{2}{3N_{pp}(L_{sd}-L_{sq})i_{sd}}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{3}{2Cs}\right] \qquad \text{(H.18)}$$

$$= \left[\frac{G(1+T_s s)}{s}\right]\left[\frac{2}{3N_{pp}(L_{sd}-L_{sq})i_{sd}}\right]\left[\frac{1}{1+T_{sq}s}\right]\left[\frac{3}{2Cs}\right]$$

where,

$$G = K_{i.bl} \qquad \text{(H.19)}$$

$$G\,T_s = K_{p.bl} \qquad \text{(H.20)}$$

In the case of Bus Voltage Controller 1 also, the bode plot is similar to that the speed loop (Figure H.2). The gains (G and T_s) are chosen such that the cross-over frequency ω_{cross} (i.e. the zero db point) is at the center of the section with a slope of -20 db/decade. A maximum phase margin of 53° is obtained.

The optimum values of T_s and ω_{cross} [26] are:

$$\frac{1}{T_{sq}} = \frac{9}{T_s} \tag{H.21}$$

$$\omega_{cross} = \frac{3}{T_s} = \frac{1}{3T_{sq}} = \frac{1}{3 * 664.479 * 10^{-6}} = 501.65 \text{ rad / s} \tag{H.22}$$

At the cross-over frequency ω_{cross},

$$\text{OLTF} = 1 \tag{H.23}$$

Utilising equations (H.15) and (H.18), OLTF becomes,

$$\text{i.e.} \quad \left[\frac{G\left|1+j3\right|}{\left|1+j\frac{1}{3}\right|}\right]\left[\frac{3T_{sq}\,3T_{sq}\,0.5528}{2C}\right] = 1 \tag{H. 24}$$

By solving the above equation, the proportional (P) and integral (I) gains of the Bus Voltage Controller 1 are obtained for a bus capacitance of 1000 μF as:

$$K_{p,b1} = \text{G Ts} = 1.8 \tag{H.25}$$

$$K_{i,b1} = 303.6 \tag{H.26}$$

For C=250 μF, the P and I gains become:

$$K_{p,b1} = 0.45 \tag{H.27}$$

$$K_{i,b1} = 75.9 \tag{H.28}$$

Bus Voltage Controller 2 (Magnetisation Energy recovery):

This controller comes into picture during Control Situation 3, i.e. in a voltage sag condition when the motor speed is less than 10% of its rated speed, as defined in the control strategy earlier in Subsection 2.2.2. In this situation, this controller reduces the

magnetisation current i_{sd} until zero and thereby regenerate the energy available in the winding inductances into the dc bus capacitor by reversing the flow of I_{out}. The torque reference is maintained at zero during this control (i.e. $i_{sq} = 0$). The relationship between i_{sd} and I_{out} during this situation can be arrived at from equation (B.8) by assuming that the average V_{sd} applied during this control is equivalent to the bus voltage V_{bus}.

$$I_{out} = \frac{2}{3} i_{sd} \tag{H.29}$$

In this control, the d-axis current controller is optimised by the transfer function $\frac{1}{1+T_{sd}s}$ where the magnetising time constant of the motor T_{sd} is calculated using equation (H.30):

$$T_{sd} = \frac{L_{sd} i_{sd,rated}}{0.5 * V_{sd,rated}} = \frac{76.8 * 10^{-3} * 9}{587} \approx 1.1775 \text{ ms} \tag{H.30}$$

The flow of energy between the magnetising inductance L_{sd} and the capacitor C is found to be a non-linear function as shown in the following equations. Assuming that, a small change in i_{sd} (i.e. di_{sd}) corresponds to a change dV_{bus} in the capacitor voltage,

$$\text{Energy flowing into } C = \frac{1}{2}\frac{3}{2} C\, dV_{bus}^2 = \frac{3}{4} C\, 2V_{bus}\, dV_{bus} = \frac{3}{2} C V_{bus}\, dV_{bus} \tag{H.31}$$

The $\frac{3}{2}$ factor is included to justify the relationship between i_{sd} and I_{out} as shown in equation (H.31) and their effect on the capacitor voltage.

$$\text{Similarly, energy out of } L_{sd} = \frac{1}{2} L_{sd}\, di_{sd}^2 = L_{sd} i_{sd} di_{sd} \tag{H.32}$$

Equating (H.31) and (H.32) and by assuming that V_{bus} and i_{sd} can be replaced by their average values during this control, we get,

$$\frac{3}{2} C V_{bus,av} \frac{dV_{bus}}{dt} = L_{sd} i_{sd,av} \frac{di_{sd}}{dt} \tag{H.33}$$

i.e. $$\frac{3}{2}CV_{bus,av}\, s\, V_{bus,av} = L_{sd} i_{sd,av}\, s\, i_{sd} \qquad \text{(H.34)}$$

or $$V_{bus} = \frac{2L_{sd} i_{sd,av}}{3CV_{bus,av}} i_{sd} \qquad \text{(H.35)}$$

The control block diagram can now be shown as in Figure H.4.

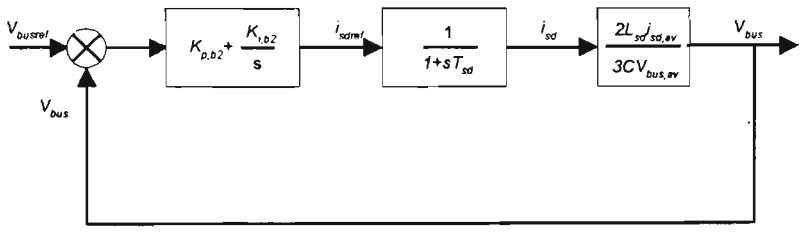


Figure H.4 Control block diagram of an SRM VSD during bus voltage control by recovering magnetisation energy.

The open loop transfer function (OLTF) is:

$$\text{OLTF} = \left[\frac{K_{p,b2}s + K_{i,b1}}{s}\right]\left[\frac{1}{1+sT_{sd}}\right]\left[\frac{2L_{sd} i_{sd,av}}{3CV_{bus,av}}\right] \qquad \text{(H.36)}$$

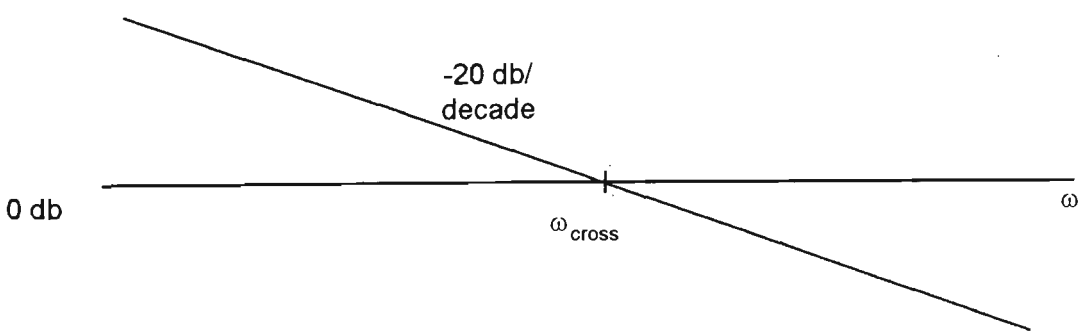


Figure H.5 Bode plot of Bus Voltage Controller 2

In this case, the bode plot has an uniform slope of -20 db/decade. The controller zero can be placed anywhere within the allowable limits for the control to cancel the pole and then the phase margin is always 90°. The proportional (P) and integral (I) gains are calculated for a unity gain and a bandwidth of 283rad/s, which is one-third the corner frequency of the current loop. With a 1000 μF bus capacitor,

$$\text{OLTF} = 1 \angle -90^{\circ}$$

i.e. $$\left[\frac{K_{p,b2} j283 + I}{j283}\right]\left[\frac{1}{1 + 0.00115 j283}\right]\left[\frac{2 * 76.8 * 10^{-3} * 4.5}{3 * 0.001 * 586}\right] = -j$$

By solving the above equations, the controller gains are obtained as:

$$K_{p,b2} = 0.085$$
$$K_{i,b2} = 72.1$$

In the case of a 250 μF capacitor, the controller gains become:

$$K_{p,b2} = 0.021$$
$$K_{i,b2} = 18.025$$

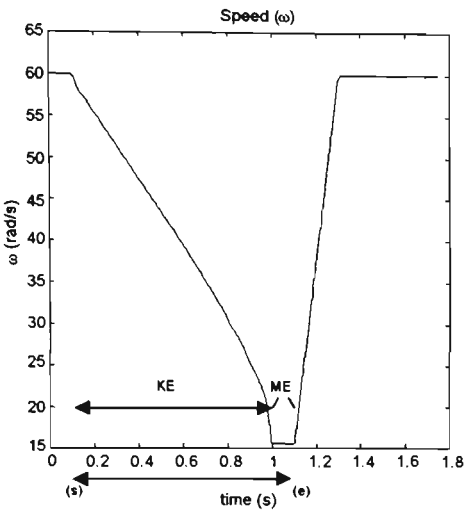
APPENDIX I

PERFORMANCE OF SRM VSD WITH FAN TYPE LOADS

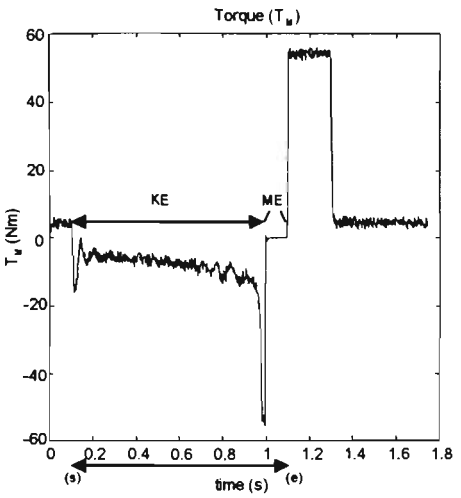
Here, the sag ride-through performance results of the proposed control strategy are presented in the case of a Synchronous Reluctance Motor VSD (SRM VSD) for fan type loads. Combined sag ride-through performance due to both kinetic and magnetising energy recovery is analysed. The results can be compared with the results with constant torque loads which were presented in Section 3.6 of Chapter 3.

Simulation conditions: The initial motor speed is set at 60 rad/s and the load is configured to be proportional to the square of the motor speed with a value of 18 Nm at a speed of 120 rad/s. For a switching frequency of 5 kHz, the simulation sampling frequency is set at 30 kHz. A 50% three-phase sag is applied for 1 second.

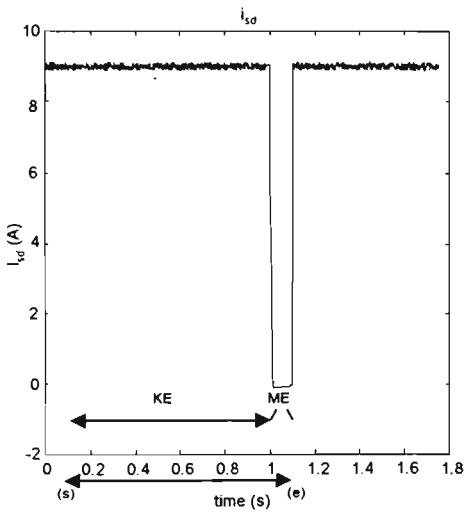
Performance analysis: The performance characteristics, viz. motor speed (ω), torque (T_M), magnetising current (i_{sd}), capacitor voltage (V_{bus}) and capacitor charging current (I_{in}) of the SRM during the sag are shown in Figure I.1. The sag condition is indicated with a double-ended arrow along the time axis with (s) and (e) representing the start and end of the sag. The durations of kinetic energy recovery and magnetisation energy recovery are also indicated as 'KE' and 'ME' respectively. By comparing these results with the constant load performance (refer Figure 3.10), it can be observed from Figure I(a) that, the motor speed drops at a much reduced rate with fan type loads and hence the durations of both the control modes, viz. kinetic energy and the magnetisation energy recovery, are much longer. During magnetisation energy recovery, the observed speed drop is very low because the load torque values at such low speeds are close to zero. The torque and the magnetisation current response confirm the proper operation of the control strategy during both control modes. (Figure I (b) and (c)). The capacitor voltage is found to be close to the set-point in both modes as observed in Figure I(d). The capacitor recharging currents at the end of the sag are found to be within the limits as observed in Figure I(e). Being a fan type load, the motor speed does not go below zero speed during this control strategy unlike constant torque loads.



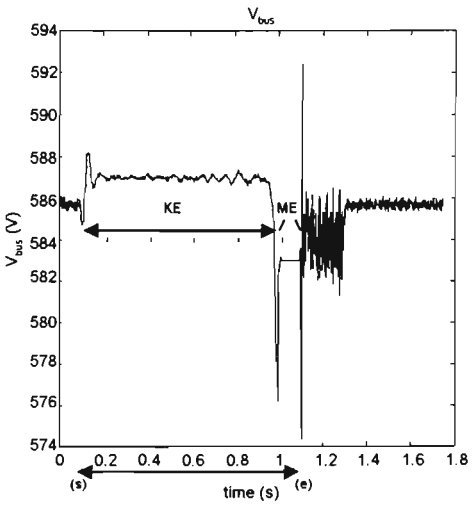
(a) Speed (ω)



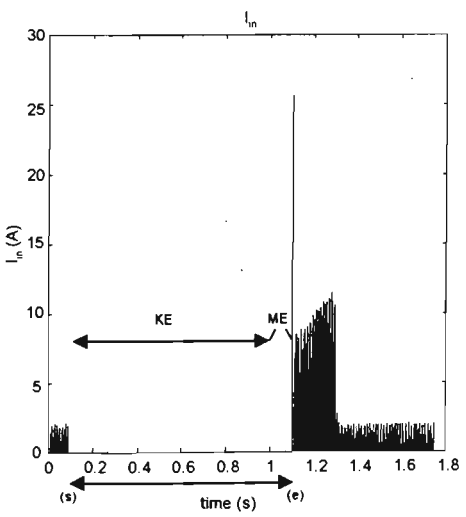
(b) Torque (T_M)



(c) Magnetising current (i_{sd})



(d) Capacitor voltage (V_{bus})



(e) Capacitor charging current (I_{in})

Figure I.1. Performance of the SRM VSD with fan type load under the proposed control strategy

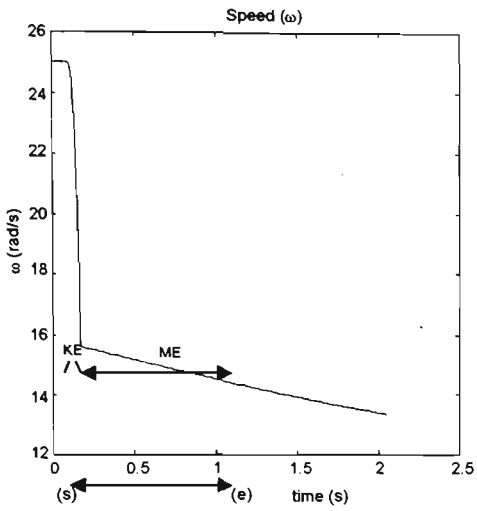
APPENDIX J

PERFORMANCE OF AN IM VSD WITH FAN TYPE LOADS

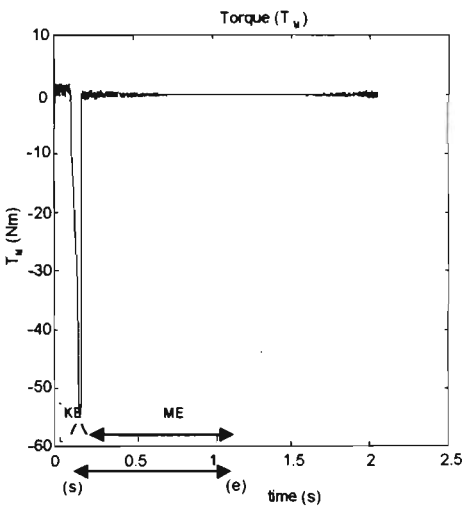
Here, the performance results of an induction motor VSD (IM VSD) are discussed when controlling fan type loads using the proposed strategy. Sag ride-through performance by the two control modes, viz. recovering kinetic energy at high speeds and the open loop flux control at lower speeds, is presented. The results can be compared with the performance of the IM VSD with constant load torque which was presented in Section 3.7 of Chapter 3.

Simulation conditions: A 50% three-phase sag was applied for 1 second on the IM VSD when the motor was operating at 25 rad/s. (Here a lower initial speed was chosen from the trials in Section 4.5 in order to observe the control transition within the 1 second sag period). A fan type load is configured with a torque of 18 Nm at 120 rad/s.

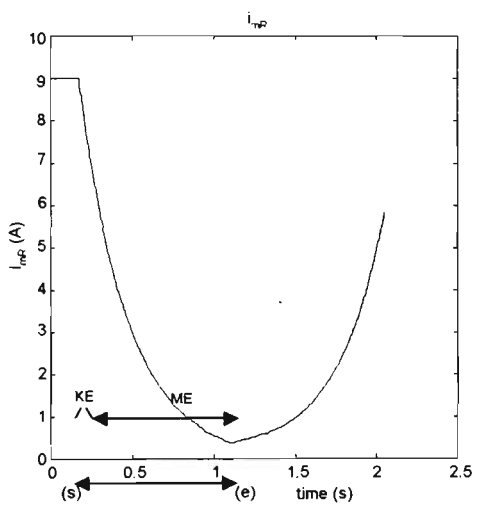
Performance results: The performance characteristics, viz. motor speed (ω), torque (T_M), magnetising current (i_{mR}), capacitor voltage (V_{bus}) and capacitor charging current (I_{in}) are shown in Figure J.1. The sag condition is indicated as in previous cases and the durations of kinetic energy recovery and open loop flux control are indicated as 'KE' and 'ME' respectively. By comparing the VSD performance with the constant load torque performance (as shown in Figure 4.10), it can be observed that, the motor speed drops at a much reduced rate with fan type loads which is more evident during the magnetisation energy recovery. At such low speeds, the load torque is very low. The operation of the two control modes are verified from the response of the torque and the magnetising current. The bus voltage is maintained at the set value during kinetic energy recovery and drops at a slower rate during the flux reduction. Being a fan type load, the motor speed is found not to reverse during the sag ride-through control.



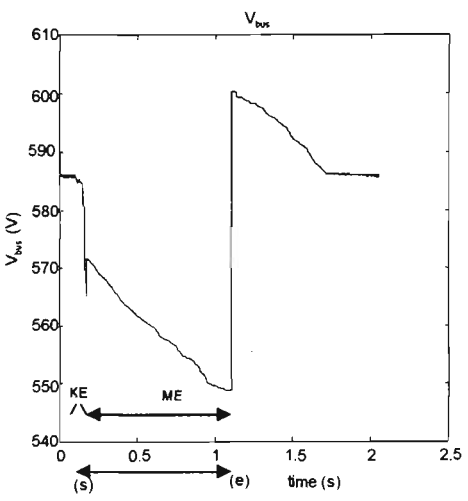
(a) Speed (ω)



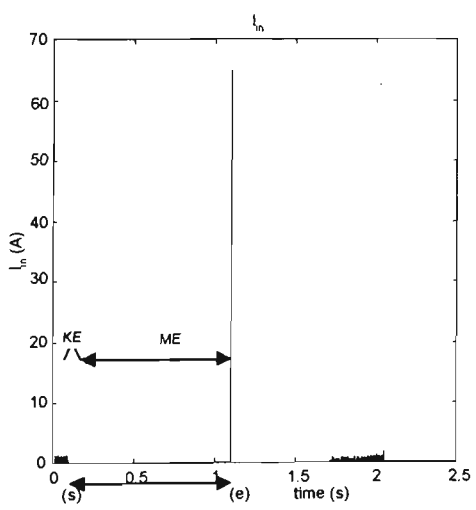
(b) Torque (T_M)



(c) Magnetising current (i_{mR})



(d) Capacitor voltage (V_{bus})



(e) Capacitor charging current (I_{in})

Figure J.1. Induction motor performance with fan type load under the control strategy

APPENDIX K

MATLAB PROGRAMS

a) SIMULATION OF SRM VSD

(Rating: 5.5 kW, 3 ph, 415 V AC, 50 Hz)

```
%
clc; clf; clear all;
%                                   CONSTANTS
%
Vpp=415;                            % line-to-line rms voltage
Vpk=Vpp*sqrt(2)/sqrt(3);            % line-to-neutral peak voltage
Vsag=0.5*Vpk;                       % line-to-neutral peak voltage on sag
Npp=2;                              % Number of pole pairs
freq=50;                            % AC Supply frequency
Ra=0.0085;                          % Per-phase line resistance
La=0.0001;                          % Per-phase line inductance
C=0.001;                            % Bus capacitance
dt=0.000033;                        % Sampling frequency
wref=120;                           % Velocity reference
idset=9.0;                          % Magnetising current (flux) reference
idmin=0.0;                          % Minimum flux reference
Kp=115.4;                           % Speed regulator P gain
Ki=19293;                           % Speed regulator I gain
TorqLt=54;                          % Torque limit
Tl=18;                              % Load torque
Rs=0.6;                             % Stator resistance
Ld=0.0768;                          % Stator d-axis inductance
Lq=0.0098;                          % Stator q-axis inductance
J=0.23;                             % System inertia
Vbusref=586;                        % Bus Voltage reference
wcutoff=15.7;                       % Cut-off velocity reference
Bus1Kp=1.8155;                      % Bus Voltage Regulator 1 P gain
Bus1Ki=303.6;                       % Bus Voltage Regulator 1 I gain
Bus2Kp=0.0849;                      % Bus Voltage Regulator 2 P gain
Bus2Ki=72.1;                        % Bus Voltage Regulator 2 I gain
%
%                                   INITIAL VALUES
%
Vbus(1)=586;                        % Capacitor voltage
time(1)=0;                          % Simulation time
IWRST=0;                            % Integrator wind-up reset (1-reset, 0-set)
Iab=0;                              % Line current with phases a and b
Ibc=0;                              % Line current with phases b and c
Ica=0;                              % Line current with phases c and a
Iout(1)=0;                          % Capacitor output current to inverter
wact(1)=0;                          % Motor speed
idact(1)=idset;                     % Stator d-axis current
iqact(1)=9.75;                      % Stator q-axis current
w=0;                                % Motor speed
TQop=Tl;                            % Torque regulator output
Tref=Tl;                            % Torque reference
Pwerr=0;                            % Previous speed error
PVbuserr=0;                         % Previous dc bus voltage error
id=idset;                           % Stator d-axis current
iq=9.75;                            % Stator q-axis current
Eact(1)=0;                          % Rotor angle
E=0;                                % Rotor angle
did(1)=0;                           % Change in stator d-axis current
diq(1)=0;                           % Change in stator q-axis current
Vdact(1)=0;                         % Stator d-axis voltage
Vqact(1)=0;                         % Stator q-axis voltage
%
%                                   SIMULATION
%
%                                   Supply and sag generation
%
for i=2:1.75/dt
    time(i)=dt*i;
    if i<3030
        Vpeak=Vpk;
    elseif i>33333
```

```
        Vpeak=Vpk;
    else
        Vpeak=Vsag;
    end;
%                                                   ac voltage waveforms (Vll)
    Va=Vpeak*sin(2*pi*freq*time(i));
    Vb=340*sin(2*pi*freq*time(i)-(2*pi/3));
    Vc=340*sin(2*pi*freq*time(i)-(4*pi/3));
    Vab(i)=Va-Vb;
    Vbc(i)=Vb-Vc;
    Vca(i)=Vc-Va;
    %                                               Sense if Vll > Vbus
    if Vab(i)<=0
        Cab1=0;
    elseif Vab(i)>=Vbus(i-1)
        Cab1=1;
    elseif Vab(i)<=Vab(i-1)
        Cab1=1;
    else
        Cab1=0;
    end;
    %
    if Vab(i)>=0
        Cab2=0;
    elseif -Vab(i)>=Vbus(i-1)
        Cab2=1;
    elseif Vab(i)>=Vab(i-1)
        Cab2=1;
    else
        Cab2=0;
    end;
    %
    if Vbc(i)<=0
        Cbc1=0;
    elseif Vbc(i)>=Vbus(i-1)
        Cbc1=1;
    elseif Vbc(i)<=Vbc(i-1)
        Cbc1=1;
    else
        Cbc1=0;
    end;
    %
    if Vbc(i)>=0
        Cbc2=0;
    elseif -Vbc(i)>=Vbus(i-1)
        Cbc2=1;
    elseif Vbc(i)>=Vbc(i-1)
        Cbc2=1;
    else
        Cbc2=0;
    end;
    %
    if Vca(i)<=0
        Cca1=0;
    elseif Vca(i)>=Vbus(i-1)
        Cca1=1;
    elseif Vca(i)<=Vca(i-1)
        Cca1=1;
    else
        Cca1=0;
    end;
    %
    if Vca(i)>=0
        Cca2=0;
    elseif -Vca(i)>=Vbus(i-1)
        Cca2=1;
    elseif Vca(i)>=Vca(i-1)
        Cca2=1;
    else
        Cca2=0;
    end;
    %                                               Line current sensing
    %
    PIabp=Iab+((Vab(i)-2*Ra*Iab-Vbus(i-1))*dt/(2*La));
    PIabn=Iab+((Vab(i)-2*Ra*Iab+Vbus(i-1))*dt/(2*La));
    if ((PIabp>0)&(Cab1>0))
```

```
    Iab=PIabp;
elseif ((PIabn<0)&(Cab2>0))
    Iab=PIabn;
else
    Iab=0;
end;
%
PIbcp=Ibc+((Vbc(i)-2*Ra*Ibc-Vbus(i-1))*dt/(2*La));
PIbcn=Ibc+((Vbc(i)-2*Ra*Ibc+Vbus(i-1))*dt/(2*La));
if ((PIbcp>0)&(Cbc1>0))
    Ibc=PIbcp;
elseif ((PIbcn<0)&(Cbc2>0))
    Ibc=PIbcn;
else
    Ibc=0;
end;
%
PIcap=Ica+((Vca(i)-2*Ra*Ica-Vbus(i-1))*dt/(2*La));
PIcan=Ica+((Vca(i)-2*Ra*Ica+Vbus(i-1))*dt/(2*La));
if ((PIcap>0)&(Cca1>0))
    Ica=PIcap;
elseif ((PIcan<0)&(Cca2>0))
    Ica=PIcan;
else
    Ica=0;
end;
%
Ia(i)=Iab-Ica;
Ib(i)=Ibc-Iab;
Ic(i)=Ica-Ibc;
Iin(i)=abs(Iab)+abs(Ibc)+abs(Ica);
%                                          Capacitor voltage sensing
Vbus(i)=Vbus(i-1)+((Iin(i)-Iout(i-1))*dt/C);
Vb=Vbus(i);
%                                          Speed Controller I gain selection
%                                          on integrator windup reset

if IWRST==1
    KI=0;
else
    KI=Ki;
end;
%
%                                          Speed Controller
werr=wref-w;
PIop=Tref+Kp*(werr-Pwerr)+werr*KI*dt;
Pwerr=werr;
%                                          Torque and flux referencing
%                                          during normal ac supply
%%TQop=PIop;
%%id_set=idset;
%                                          Torque and flux referencing
%                                          during sag
Vbuserr=Vbusref-Vb;
if Vpeak==Vpk
    TQop=PIop;
    id_set=idset;
elseif w>wcutoff
    Bus1PIop=Tref-Bus1Kp*(Vbuserr-PVbuserr)-Vbuserr*Bus1Ki*dt;
    TQop=Bus1PIop;
    id_set=idset;
else
    Bus2PIop=idref-Bus2Kp*(Vbuserr-PVbuserr)-Vbuserr*Bus2Ki*dt;
    FluxPIop=-Vbuserr*FluxKp;
    TQop=0;
    id_set=Bus2PIop;
end;
PVbuserr=Vbuserr;
%                                          Torque limiting/ Integrator
%                                          windup reset selection
if TQop>TorqLt
    Tref=TorqLt;
    IWRST=1;
elseif TQop<-TorqLt
    Tref=-TorqLt;
    IWRST=1;
```

```
    else
        Tref=TQop;
        IWRST=0;
    end;
    %                                                    Flux reference limiting
    if id_set>idset
        idref=idset;
    elseif id_set<idmin
        idref=idmin;
    else
        idref=id_set;
    end;
    %                                                    Current control
    iqref=(2*Tref)/(3*Npp*(Ld-Lq)*idset);
    dididеal=idref-id;
    diqideal=iqref-iq;
    Vdideal=Ld*(dididеal/dt)-w*Lq*iq;
    Vqideal=Lq*(diqideal/dt)+w*Ld*id;
    idealVreal=Vdideal*cos(E)-Vqideal*sin(E);
    idealVimag=Vqideal*cos(E)+Vdideal*sin(E);
    %                                                    Vector selection
    Videal=sqrt((idealVreal.^2)+(idealVimag.^2));
    if Videal<%Vbus(i)/2
        S=0; Real_S=0; Imag_S=0;
    elseif idealVreal>0
        if (sqrt(3)*idealVimag)>idealVreal
            S=6; Real_S=0.5; Imag_S=0.866;
        elseif (sqrt(3)*idealVimag)>-idealVreal
            S=4; Real_S=1; Imag_S=0;
        else
            S=5; Real_S=0.5; Imag_S=-0.866;
        end;
    else
        if (sqrt(3)*idealVimag)>-idealVreal
            S=2; Real_S=-0.5; Imag_S=0.866;
        elseif (sqrt(3)*idealVimag)>idealVreal
            S=3; Real_S=-1; Imag_S=0;
        else
            S=1; Real_S=-0.5; Imag_S=-0.866;
        end;
    end;
    %                                                    Motor voltage calculation
    RealV=Vbus(i)*Real_S;
    ImagV=Vbus(i)*Imag_S;
    Vdact(i)=RealV*cos(E)+ImagV*sin(E);
    Vd=Vdact(i);
    Vqact(i)=ImagV*cos(E)-RealV*sin(E);
    Vq=Vqact(i);
    %                                                    Motor current calculation
    did=(Vd-Rs*id+w*Lq*iq)*dt/Ld;
    idact(i)=idact(i-1)+did;
    id=idact(i);
    diq=(Vq-Rs*iq-w*Ld*id)*dt/Lq;
    iqact(i)=iqact(i-1)+diq;
    iq=iqact(i);
    %                                                    Capacitor output current calculation
    Iout(i)=2*(Vd*id+Vq*iq)/(3*Vbus(i));
    %                                                    Motor torque calculation
    Torqact(i)=(3/2)*Npp*(Ld-Lq)*id*iq;
    Torq=Torqact(i);
    %                                                    Motor speed calculation
    dw=(Torq-Tl)*dt/J;
    wact(i)=wact(i-1)+dw;
    w=wact(i);
    %                                                    Rotor position sensing
    dE=w*Npp*dt;
    Eact(i)=Eact(i-1)+dE;
    E=Eact(i);
end;
%                                                        Plot motor speed response
NN=max(size(time));MM=15;
plot(time(1:MM:NN),wact(1:MM:NN));
%
```

b) SIMULATION OF IM VSD

(Rating: 5.5 kW, 3 ph, 415 V AC, 50 Hz)

```
%
clc; clf; clear all;
%
%                                   CONSTANTS
%
Vpp=415;                            % line-to-line rms voltage
Vpk=Vpp*sqrt(2)/sqrt(3);            % line-to-neutral peak voltage
Vsag=0.5*Vpk;                       % line-to-neutral peak voltage on sag
Npp=2;                              % Number of pole pairs
freq=50;                            % AC Supply frequency
Ra=0.0085;                          % Per-phase line resistance
La=0.0001;                          % Per-phase line inductance
C=0.001;                            % Bus capacitance
dt=0.000033;                        % Sampling frequencywref=120;
wref=120;                           % Velocity reference
imRref=9.0000;                      % Magnetising current (flux) reference
imRmin =0.0;                        % Minimum flux reference
Kp=148;                             % Speed regulator P gain
Ki=31671;                           % Speed regulator I gain
TorqLt=54;                          % Torque limit
Tl=18;                              % Load torque
Rs=0.673                            % Stator resistance
Rr=1.2964;                          % Rotor resistance
J=0.23;                             % System inertia
Vbusref=586;                        % Bus Voltage reference
wcutoff=15.7;                       % Cut-off velocity reference
sigs=0.0484;                        % Stator leakage factor
sigr=0.0484;                        % Rotor leakage factor
Lm=0.182;                           % Mutual inductance
Bus1Kp=2.68;                        % Bus Voltage Regulator 1 P gain
Bus1Ki=573.75;                      % Bus Voltage Regulator 1 I gain
Bus2Kp=0.3585;                      % Bus Voltage Regulator 2 P gain
Bus2Ki=128.45;                      % Bus Voltage Regulator 2 I gain
%
%                                   CALCULATED VALUES
%
%                                   Leakage inductances
Ls=Lm*(1+sigs);
Lr=Lm*(1+sigr);
%                                   Rotor time constant
Tr=Lr/Rr;
%                                   Total leakage factor
sigma=1-(1/((1+sigs)*(1+sigr)));
%                                   Torque constant
K=2*Lm/(3*(1+sigr));
%
%                                   INITIAL VALUES
%
Vbus(1)=586;                        % Capacitor voltage
time(1)=0;                          % Simulation time
IWRST=0;                            % Integrator wind-up reset (1-reset, 0-set)
Iab=0;                              % Line current with phases a and b
Ibc=0;                              % Line current with phases b and c
Ica=0;                              % Line current with phases c and a
Iout(1)=0;                          % Capacitor output current to inverter
wact(1)=0;                          % Motor speed
w=0;                                % Motor speed
idact(1)=idset;                     % Stator d-axis current
iqact(1)=9.75;                      % Stator q-axis current
id=idset;                           % Stator d-axis current
iq=9.75;                            % Stator q-axis current
irqact(1)=0;                        % Rotor q-axis current
imRact(1)=imRref;                   % Rotor magnetising current
imR=imRref;                         % Rotor magnetising current
imR_ref=imRref;                     % Rotor magnetising current reference
TQop=Tl;                            % Torque regulator output
Tref=Tl;                            % Torque reference
Pwerr=0;                            % Previous speed error
PVbuserr=0;                         % Previous dc bus voltage error
Eact(1)=0;                          % Rotor angle
E=0;                                % Rotor angle
did(1)=0;                           % Change in stator d-axis current
```

```
diq(1)=0;                    % Change in stator q-axis current
Vdact(1)=0;                  % Stator d-axis voltage
Vqact(1)=0;                  % Stator q-axis voltage
wmRact(1)=0;                 % Speed of magnetising reference frame
P=0;                         % Position of magnetising reference frame
dP=0;                        % Change in flux velocity
wmR=0;                       % Speed of magnetising reference frame
dimR=0;                      % Change in magnetising current
PdimRideal=0;                % Previous required change in imR
Pidref=imRref;               % Previous Stator d-axis current reference
imRset=imRref;               % magnetising current reference
PimRset=imRref;
%
%                            SIMULATION
%
%                                  Supply and sag generation
for i=2:0.2/dt
    time(i)=dt*i;
    if i<3030
    Vpeak=340;
    elseif i>33333
    Vpeak=340;
    else
    Vpeak=340;
    end;

    %                              Line-to line ac voltages (Vll)
    Va=Vpeak*sin(2*pi*freq*time(i));
    Vb=340*sin(2*pi*freq*time(i)-(2*pi/3));
    Vc=340*sin(2*pi*freq*time(i)-(4*pi/3));
    Vab(i)=Va-Vb;
    Vbc(i)=Vb-Vc;
    Vca(i)=Vc-Va;
    %                              Sensing when Vll > Vbus
    if Vab(i)<=0
    Cab1=0;
    elseif Vab(i)>=Vbus(i-1)
    Cab1=1;
    elseif Vab(i)<=Vab(i-1)
    Cab1=1;
    else Cab1=0;
    end;
    if Vab(i)>=0
    Cab2=0;
    elseif -Vab(i)>=Vbus(i-1)
    Cab2=1;
    elseif Vab(i)>=Vab(i-1)
    Cab2=1;
    else Cab2=0;
    end;
    if Vbc(i)<=0
    Cbc1=0;
    elseif Vbc(i)>=Vbus(i-1)
    Cbc1=1;
    elseif Vbc(i)<=Vbc(i-1)
    Cbc1=1;
    else Cbc1=0;
    end;
    if Vbc(i)>=0
    Cbc2=0;
    elseif -Vbc(i)>=Vbus(i-1)
    Cbc2=1;
    elseif Vbc(i)>=Vbc(i-1)
    Cbc2=1;
    else Cbc2=0;
    end;
    if Vca(i)<=0
    Cca1=0;
    elseif Vca(i)>=Vbus(i-1)
    Cca1=1;
    elseif Vca(i)<=Vca(i-1)
    Cca1=1;
    else Cca1=0;
    end;
    if Vca(i)>=0
    Cca2=0;
```

```
elseif -Vca(i)>=Vbus(i-1)
Cca2=1;
elseif Vca(i)>=Vca(i-1)
Cca2=1;
else Cca2=0;
end;
%                                                    Line current sensing
%
PIabp=Iab+((Vab(i)-2*Ra*Iab-Vbus(i-1))*dt/(2*La));
PIabn=Iab+((Vab(i)-2*Ra*Iab+Vbus(i-1))*dt/(2*La));
if ((PIabp>0)&(Cab1>0))
Iab=PIabp;
elseif ((PIabn<0)&(Cab2>0))
Iab=PIabn;
else Iab=0;
end;
PIbcp=Ibc+((Vbc(i)-2*Ra*Ibc-Vbus(i-1))*dt/(2*La));
PIbcn=Ibc+((Vbc(i)-2*Ra*Ibc+Vbus(i-1))*dt/(2*La));
if ((PIbcp>0)&(Cbc1>0))
Ibc=PIbcp;
elseif ((PIbcn<0)&(Cbc2>0))
Ibc=PIbcn;
else Ibc=0;
end;
PIcap=Ica+((Vca(i)-2*Ra*Ica-Vbus(i-1))*dt/(2*La));
PIcan=Ica+((Vca(i)-2*Ra*Ica+Vbus(i-1))*dt/(2*La));
if ((PIcap>0)&(Cca1>0))
Ica=PIcap;
elseif ((PIcan<0)&(Cca2>0))
Ica=PIcan;
else Ica=0;
end;
%Ia(i)=Iab-Ica;
%Ib(i)=Ibc-Iab;
%Ic(i)=Ica(i)-Ibc(i);
Iin(i)=abs(Iab)+abs(Ibc)+abs(Ica);
%                                                    Capacitor voltage sensing
Vbus(i)=Vbus(i-1)+(Iin(i)-Iout(i-1))*dt/C;
Vb=Vbus(i);
%                                                    Speed Controller I gain selection
%                                                    on integrator windup reset
if IWRST==1
KI=0;
else
KI=Ki;
end;
%                                                    Speed Controller
werr=wref-w;
PIop=Tref+Kp*(werr-Pwerr)+werr*KI*dt;
Pwerr=werr;
Vbuserr=Vbusref-Vb;

%                                                    Bus Voltage Controllers 1 & 2
%
Bus1PIop=Tref-Bus1Kp*(Vbuserr-PVbuserr)-Vbuserr*Bus1Ki*dt;
Bus2PIop=imR_ref-Bus2Kp*(Vbuserr-PVbuserr)-Vbuserr*Bus2Ki*dt;
PVbuserr=Vbuserr;
if Bus2PIop>imRref
B2PIop=imRref;
elseif Bus2PIop<imRmin
B2PIop=imRmin;
else
B2PIop=Bus2PIop;
end;
%                                                    Torque and flux referencing
%                                                    during normal ac supply
%TQop=PIop;
%imR_ref=imRref;
%                                                    Torque and flux referencing
%                                                    during a sag
if ((Vpeak==Vpk)&(imR>=imRref*0.975))
TQop=PIop;
imR_ref=imRref;
elseif Vpeak==Vpk
TQop=0;
imR_ref=imR+((imR*dt)/(2*Tr));
```

```
elseif w>wminref
TQop=Bus1Plop;
imR_ref=imRref;
else
TQop=0;
%   imR_ref=imR+((B2Plop-imR)*dt/Tr);
imR_ref=imR-((imR*dt)/(2*Tr));
end;
%
%                                                    Torque limiting/ Integrator
%                                                    windup reset selection
if TQop>TorqLt
Tref=TorqLt;
IWRST=1;
elseif TQop<-TorqLt
Tref=-TorqLt;
IWRST=1;
else
Tref=TQop;
IWRST=0;
end;
%                                                    Flux reference limiting
if imR_ref>imRref
imR_set=imRref;
elseif imR_ref<imRmin
imR_set=imRmin;
else
imR_set=imR_ref;
end;
%                                                    Current control
iqref=Tref/(Npp*K*imR);
%dimRideal=imRset-imR;
dimRideal=imR_set-imR;
%id_ref=Pidref+Kpflux*(dimRideal-PdimRideal)+dimRideal*Kiflux*dt;
id_ref=imR_set+(dimRideal/dt)*Tr;
if id_ref>idmax
idref=idmax;
elseif id_ref<idmin
idref=idmin;
else
idref=id_ref;
end;
Pidref=idref;
PdimRideal=dimRideal;
dididеal=idref-id;
diqideal=iqref-iq;
Vdideal=(Rs*id)+(sigma*Ls)*((dididеal/dt)-(wmR*iq))+((1-sigma)*Ls*dimRideal/dt);
Vqideal=(Rs*iq)+(sigma*Ls)*((diqideal/dt)+(wmR*id))+((1-sigma)*Ls*wmR*imR);
idealVreal=Vdideal*cos(P)-Vqideal*sin(P);
idealVimag=Vqideal*cos(P)+Vdideal*sin(P);
%
%                                                    Vector selection
%
Videal=sqrt((idealVreal.^2)+(idealVimag.^2));
if Videal< Vbus(i)/2
    S=0;Real_S=0;Imag_S=0;
elseif idealVreal>0
    if (sqrt(3)*idealVimag)>idealVreal
    S=6;Real_S=0.5;Imag_S=0.866;
    elseif (sqrt(3)*idealVimag)>-idealVreal
    S=4;Real_S=1;Imag_S=0;
    else
    S=5;Real_S=0.5;Imag_S=-0.866;
    end;
else
    if (sqrt(3)*idealVimag)>-idealVreal
    S=2;Real_S=-0.5;Imag_S=0.866;
    elseif (sqrt(3)*idealVimag)>idealVreal
    S=3;Real_S=-1;Imag_S=0;
    else
    S=1;Real_S=-0.5;Imag_S=-0.866;
    end;
end;
%                                                    Motor voltage calculations
RealV=Vbus(i)*Real_S;
ImagV=Vbus(i)*Imag_S;
```

```
Vd=RealV*cos(P)+ImagV*sin(P);
Vq=ImagV*cos(P)-RealV*sin(P);


%                                                    Motor current calculations
%
did=(((Vd-Rs*id-((1-sigma)*Ls*dimR/dt))/(Ls*sigma))+wmR*iq)*dt;
idact(i)=idact(i-1)+did;
id=idact(i);
diq=(((Vq-Rs*iq-((1-sigma)*Ls*wmR*imR))/(Ls*sigma))-wmR*id)*dt;
iqact(i)=iqact(i-1)+diq;
iq=iqact(i);
%                                                    Capacitor output current  calculation
Iout(i)=2*(Vd*id+Vq*iq)/(3*Vbus(i));
%                                                    Magnetising current calculation
dimR=(id-imR)*dt/Tr;
imRact(i)=imRact(i-1)+dimR;
imR=imRact(i);
%                                                    Motor torque calculation
Torqact(i)=Npp*K*imRact(i)*iqact(i);
Torq=Torqact(i);
%                                                    Motor velocity calculation
dw=(Torq-Tl)*dt/J;
wact(i)=wact(i-1)+dw;
w=wact(i);
%                                                    Slip and flux velocity calculation
slip=iqact(i)/(Tr*imRact(i));
wmRact(i)=wact(i)+slip;
wmR=wmRact(i);
%                                                    Flux axis position calculation
dP=wmR*Npp*dt;
P=P+dP;
%                                                    Rotor current calculations
%irdact(i)=-Lm*dimR/(Rr*dt);
%irqact(i)=Lm*imR*(w-wmR)/Rr;
%                                                    Motor terminal current waveform
%isreal=(id*cos(P)-iq*sin(P));
%isimag=iq*cos(P)+id*sin(P);
%is1(i)=2*isreal/3;
%is2(i)=-(isreal/3)+(isimag/1.732);
%is3(i)=-(isreal/3)-(isimag/1.732);
%
%
%

end;
%                                                    Plot motor velocity
NN=max(size(time));MM=15;
plot(time(1:MM:NN),wact(1:MM:NN));
```