Benchmark of AC and DC Active Power Decoupling Circuits for Second-Order Harmonic Mitigation in Kilowatt-Scale Single-Phase Inverters

Qin, Zian; Tang, Yi; Loh, Poh Chiang; Blaabjerg, Frede

Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2015.2490199

Publication date:
2016

Document Version
Accepted author manuscript, peer reviewed version

Benchmark of AC and DC Active Power Decoupling Circuits for Second Order Harmonic Mitigation in kW-scale Single-Phase Inverters

Zian, Qin; Yi, Tang; Poh Chiang, Loh; Frede, Blaabjerg;

Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2015.2490199,

Publication date:
2015

Benchmark of AC and DC Active Power Decoupling Circuits for Second Order Harmonic Mitigation in kW-scale Single-Phase Inverters

Zian Qin, *Student Member, IEEE*, Yi Tang, *Member, IEEE*, Poh Chiang Loh, Frede Blaabjerg, *Fellow, IEEE*

***Abstract*— This paper presents the benchmark study of ac and dc active power decoupling circuits for second order harmonic mitigation in kW scale single-phase inverters. First of all, a brief comparison of recently reported active power decoupling circuits is given, and the best solution that can achieve high efficiency and high power density is identified and comprehensively studied, and the commercially available film capacitors, the circuit topologies, and the control strategies adopted for active power decoupling are all taken into account. Then, an adaptive decoupling voltage control method is proposed to further improve the performance of dc decoupling in terms of efficiency and reliability. The feasibility and superiority of the identified solution for active power decoupling together with the proposed adaptive decoupling voltage control method are finally verified by both the simulation and experimental results obtained on a 2 kW single-phase inverter.**

Index Terms*— *single-phase inverter, active power decoupling, film capacitor, power density, adaptive voltage control

I. INTRODUCTION

In single-phase systems, the ac side instantaneous power may contain both a dc component and a double line frequency power oscillation. This power oscillation will then induce a significant current or voltage ripple on the dc side. Depending on applications, the input ripples may cause different problems, e.g. reduced Maximum Power Point Tracking (MPPT) efficiency in photovoltaic inverters and reduced lifetime in battery powered Uninterruptible Power Supplies (UPSs) [1] [2]. To cope with this issue, the most widely used approach so far is to connect an Electrolytic Capacitor (E-cap) bank to the dc bus to passively decouple the power oscillation. The drawbacks of this method are obvious because of the bulky size and short lifetime of the E-caps. The demand for higher power density and higher efficiency has never stopped, and Google has recently initiated a technological program aiming to find an excellent solution to a 2 kW single-phase inverter. One of the most challenging targets is to achieve a compact design (<655.5 cm^3 volume in total) while keep the input ripple currents in a low level [3], and this objective cannot be simply realized by the passive decoupling approach. Therefore, Active Power Decoupling (APD), which uses inductors or film capacitors with much lower capacitance to replace the bulky electrolytic capacitor bank [4]-[21], becomes one of the key techniques to conquer this design challenge.

Zian Qin, Poh Chiang Loh and Frede Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg DK-9220, Denmark. Yi Tang is with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.

The Corresponding author is Yi Tang (yitang@ntu.edu.sg)

The APD technique is commonly implemented by using an auxiliary circuit composed of power switches and energy storage devices such as capacitors or inductors. Therefore, the efficiency reduction induced by this method becomes one of the main concerns. The inductor based APD losses its competitiveness because of the inherent high loss of the inductor, including the core loss and the copper loss [5] [6]. Besides, the volume of the inductor required for APD is also sizeable. The film capacitor based APD is more attractive from efficiency and power density points of view. A set of circuit topologies and corresponding control strategies of film capacitor based APD have been proposed in the literature, and most of them are shunt type [8]-[21] instead of connecting the auxiliary circuit in series into the dc bus [7]. The shunt film capacitor based APD methods can be basically categorized into dc decoupling [9]-[15] and ac decoupling [16]-[21] according to the polarity of the decoupling capacitor voltage, where the former has unipolar capacitor voltage while the latter has bipolar one. Dc decoupling methods can be realized by flyback converter based single-phase inverters [9]-[11] or rectifiers [12], which are simple and effective. However, these methods may be more suitable for micro inverters or LED drivers due to the power limitation of the flyback converter. A bidirectional boost-type dc decoupling method [13]-[15] is more appropriate for kW-scale single-phase applications. Since the boost converter is connected to the dc bus of the single-phase converter, the power decoupling function can be easily implemented by controlling the input current of the boost converter to be a sinusoidal with a double line frequency. The dc offset of the decoupling capacitor voltage is a variable that can be freely tuned, and it is normally fixed at a certain value in previous papers for simplicity [14], [15]. In this paper, an adaptive control algorithm will be proposed to optimize the dc offset voltage so that the efficiency and reliability of the decoupling circuits can be greatly improved during light load operation. In contrast, ac decoupling methods may need an components, the decoupling capacitor can be connected

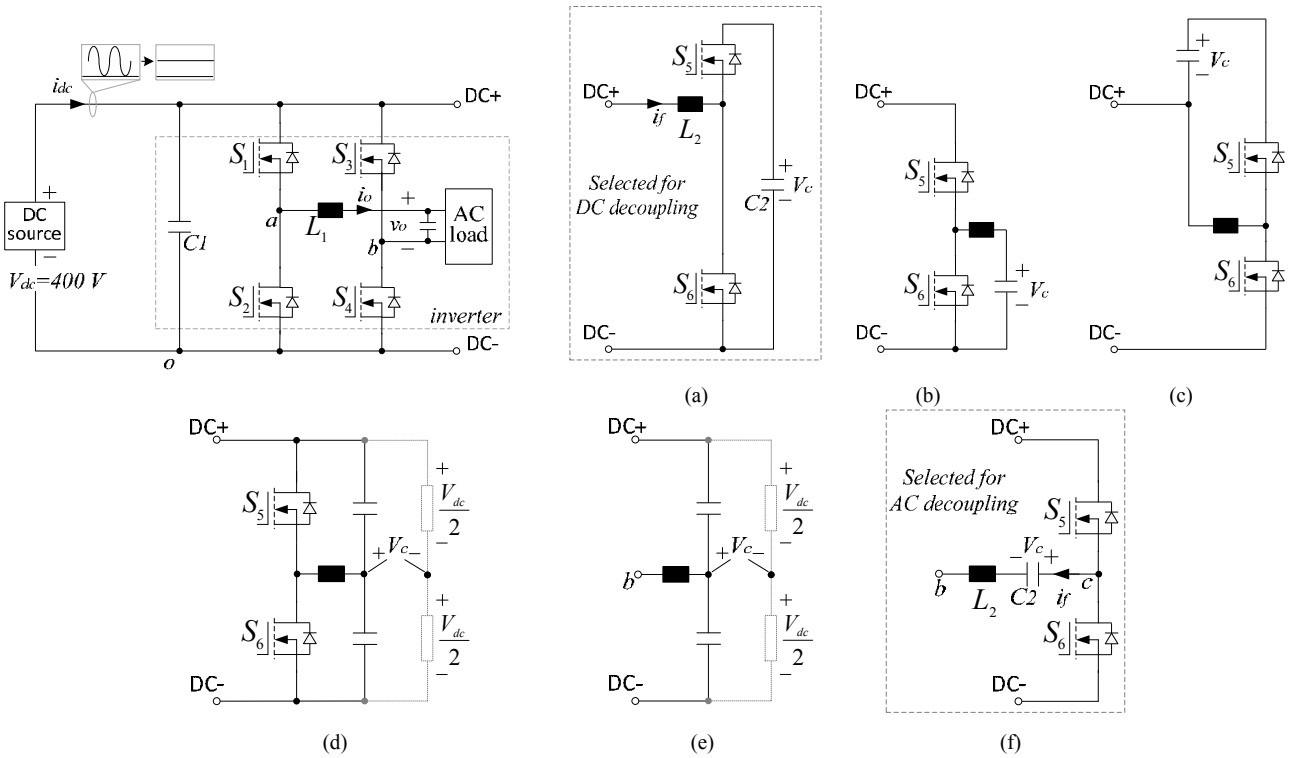


Fig. 1. A single-phase voltage source inverter with (a) boost-type, (b) buck-type, (c) buck-boost-type dc active power decoupling and (d) half bridge + flying capacitors, (e) flying capacitors, (f) half bridge ac active power decoupling.

between extra full-bridge converter to independently control the bipolar capacitor voltage [16]. In order to reduce the number of active an extra half-bridge and one leg of the single-phase full-bridge converter as proposed in [17]. However, the modulation of the original circuit may interact with that of the power decoupling circuit. Therefore, higher dc bus voltage may be required in order to produce the same ac side voltage [17]. Fortunately, by using the Space Vector Pulse-Width Modulation (SVPWM) method, the dc bus voltage utilization can be maximized, and more ripple power can be decoupled without increasing the dc bus voltage [18]. Other methods to reduce the number of components in ac decoupling include using a half bridge plus two flying capacitors [19], [20] or solely using two flying capacitors [21]. In these methods, two identical film capacitors are connected in series between the plus and minus dc rails with their neutral point controlled to be a sinusoidal. In this case, the power decoupling function can be realized without using extra dc bus capacitors to handle the transition of the switching patterns and load change. The only drawback is the relatively lower modulation index and thereby a higher voltage stress during light load operation. The minimum capacitance required for APD was analyzed in [16], however the volume of the film capacitors used for APD is not discussed, and it is actually a more important performance indicator from power density perspective.

With the research works reviewed above, it is still not clear that which types of power decoupling capacitors and circuit topologies can achieve the highest power density and efficiency for a kW-scale single-phase inverter. Most of these papers only present the capacitance required for power decoupling, but as revealed by the datasheets of the capacitors [22]-[25], the volume of the capacitors can be quite different depending on the types of the film capacitors used for power decoupling. Even with the same type of film capacitors, the ripple power they can supply may also vary depending on the operating voltage as well as the circuit topology used for power decoupling. To answer these questions, the objective of this paper is to provide a benchmark evaluation to the existing APD circuits, where the commercially available film capacitors and the control strategies adopted for power decoupling are also taken into consideration. The most promising APD solution will be identified for a kW scale single-phase inverter. Moreover, an adaptive decoupling voltage control method is also proposed for the dc decoupling circuit in order to further improve the light load efficiency as well as the lifetime of the inverter. The remaining part of the paper is organized as follows. Section II discusses the selection of the decoupling capacitors and the auxiliary circuits. Section III illustrates the control strategies of the auxiliary circuits. Section IV and Section V respectively present the simulation and experimental results of the designed ac and dc decoupling circuits to demonstrate their effectiveness. Section VI finally concludes the contributions of this paper.

II. SELECTION OF THE DECOUPLING CAPACITORS AND THE AUXILIARY CIRCUITS

The basic circuit diagram of the studied single-phase inverter is illustrated in Fig. 1, and its specifications are partially referred to the Little Box Challenge [3], where the dc

bus voltage V_{dc} is 450 V connected in series with a 10 Ω resistor as the impedance, the ac output voltage v_o is 240 Vrms with its fundamental frequency ω_n being fixed at 2π×60 rad/s. The nominal output power P_n is 2 kW, and the design constraint is that the input dc bus peak-to-peak current and voltage ripples should be less than 20% and 3% of the nominal values, respectively. In order to avoid unnecessary power losses, the 10 Ω resistor is removed in the design, and the dc bus voltage V_{dc} is purposely dropped from 450 V to 400 V. It should be noted that the topology of the inverter is optional and can be other ones than a full-bridge. The following equations can be easily derived for its ac output,

$$\begin{cases} v_0 = \sqrt{2}V_o sin(\omega_n t) \\ i_o = \sqrt{2}I_o sin(\omega_n t + \varphi) \end{cases} \quad (1)$$

$$p_o = v_o i_o = \underbrace{V_o I_o cos\varphi}_{dc\ item\ \overline{p_o}} + \underbrace{[-V_o I_o cos(2\omega_n t + \varphi)]}_{ripple\ power\ p_r} \quad (2)$$

where i_o is the ac output current, and only linear loads are considered in this case. φ is the load phase angle, V_o and I_o are the rms values of the ac output voltage and current, respectively, and p_o is the instantaneous output power. As seen in (2), the output power p_o is composed of a dc item $\overline{p_o}$ and a sizable second-order ripple power p_r. In order to keep 20 % peak-to-peak current ripple on the input side, the dc source should supply (20 %)/2=10 % of the ripple power if a constant dc input voltage is assumed. The remaining 90% of the ripple power will then be fed by the dc link capacitor C_1, and the ripple power of C_1 is simply given by (3), as illustrated in Fig. 2.

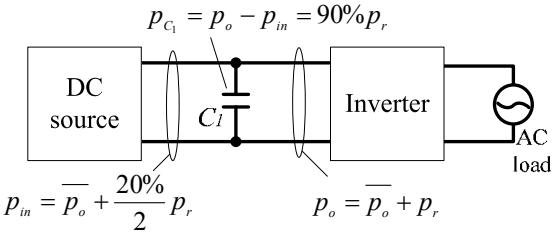


Fig. 2. Schematic diagram showing the ripple power on the dc link.

$$\left(1 - \frac{20\,\%}{2}\right) P_r = V_{dc} \cdot I_r \quad (3)$$

where I_r is the current ripple amplitude of capacitor C_1 in case of passive power decoupling, and P_r is the amplitude of the second-order ripple power p_r. According to Ohm's law in C_1 and the constraint of the dc bus voltage ripple, it is possible to derive that,

$$I_r = 2\omega_n C_1 V_r = 2\omega_n C_1 \frac{3\,\%}{2} V_{dc} \quad (4)$$

where V_r is the amplitude of the dc bus voltage ripple. According to (3) and (4), the capacitance of C_1 needed for passive power decoupling is 0.99 mF. In order to have enough design margins, the 450V E-caps cannot directly be used, and two E-caps with a lower voltage value, e.g. 350V should be connected in series in the dc bus. Moreover, the E-caps should normally be over designed in order to have satisfactory lifetime. Therefore, the size of the required E-caps could be considerable, and it will be very difficult to simultaneously meet the compact design and low input ripples requirements. The APD methods, which can significantly reduce the capacitance requirement in single-phase systems thus become the life-saving straws.

A. Decoupling capacitors

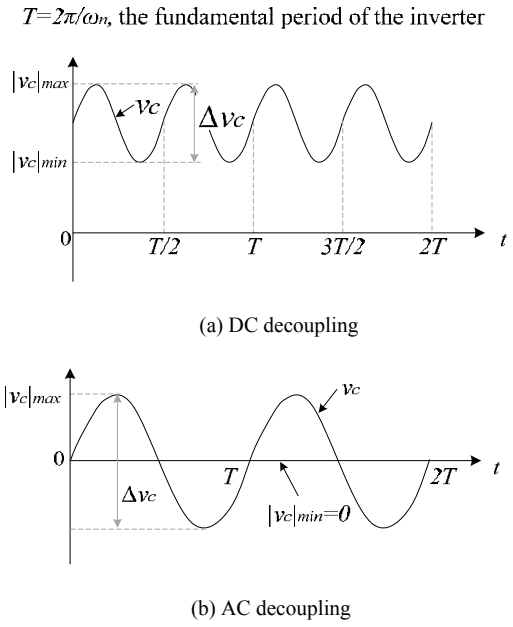


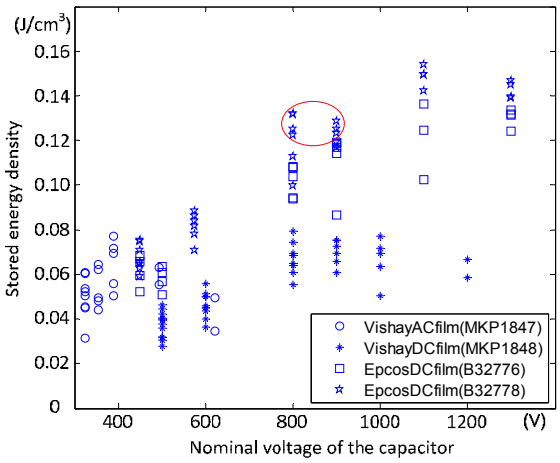
Fig. 3. Typical voltage profiles of the decoupling capacitors.

The auxiliary circuits for APD are composed of power switches, chokes, and film capacitors. For power switches and chokes, they can be optimized through the use of wide band gap devices with high frequency switching, while for film capacitors, they may dominate the volume of the overall system due to the requirement for low frequency ripple power compensation. The operation modes of APD can be classified into dc decoupling and ac decoupling, depending on whether the decoupling capacitor voltage will change its polarity or not as shown in Fig. 3. Another difference between dc decoupling and ac decoupling is the frequency of the ripple voltage in the decoupling capacitor. For the dc decoupling capacitor, the frequency of voltage ripple is twice the fundamental frequency of the ac output, while for the ac decoupling capacitor it is the same as the fundamental frequency [14], [18]. The stored energy of the capacitor in dc decoupling is obviously higher than that in ac decoupling according to the definition of the capacitor's stored energy shown in (5).

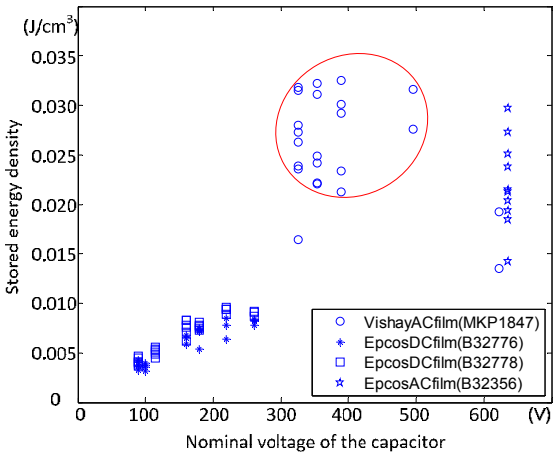
$$\Delta E = \frac{1}{2} C_2 (|v_C|^2_{max} - |v_C|^2_{min}) \quad (5)$$

where C_2 is the capacitance of the decoupling capacitor, and $|v_C|_{max}$ and $|v_C|_{min}$ are respectively the maximum and minimum values of v_C during operation.

In order to evaluate the performance of film capacitors used for power decoupling, some of the state-of-the-art film capacitors are studied and compared, and their stored energy



(a) DC decoupling



(b) AC decoupling

Fig. 4. Stored energy density versus nominal voltage of the film capacitors.

densities, i.e. the ratio between the stored energy in (5) and the volume of the capacitor, are presented in Fig. 4. For dc decoupling, the dc voltage offset and voltage variation of the capacitors are pushed to the nominal values, and the specifications of the capacitors are obtained from the datasheets [22]-[25]. As seen in Fig. 4 (a), the EPCOS dc film capacitors (B32778) always have the best performance even the nominal voltage changes from 400 V to 1300 V. Moreover, the stored energy density generally increases as the nominal voltage rises. The 800 V EPCOS dc film capacitors (B32778) are deemed as the best candidate for dc decoupling, because in this case 1200 V SiC MOSFET can be used with certain margins. However, there are very few types of B32778 film capacitors commercially available in the market, and 800 V B32776 series capacitors are finally chosen for dc decoupling and the power density will be slightly compromised. In contrast, the stored energy density of capacitors in ac decoupling is much lower, as seen in Fig. 4 (b). Despite, Vishay ac film capacitors (MKP 1847) are found to be the best choice with the highest energy density, and its nominal voltage is 250 Vrms. This ac voltage can be easily achieved by using buck-type decoupling methods as the dc bus voltage is 400 V. Vishay ac film capacitors (MKP 1847) are thus chosen for ac decoupling.

B. Circuit topologies

Generally, there are buck (Fig. 1(b)), boost (Fig. 1(a)), and buck-boost type (Fig. 1(c)) topologies available for dc power decoupling. The buck type auxiliary circuit is not considered because it may require at least two conversion stages in order to have a high dc offset voltage. The buck-boost-type topology "seems" to be a good choice, because it can output a high dc offset as well as a wide voltage variation so that the volume of the decoupling capacitor can be minimized. Unfortunately, the voltage stress of the switches in the auxiliary circuit is the sum of the decoupling capacitor voltage and the dc bus voltage as shown in Fig. 1(c). Therefore, it will significantly increase the switching loss and even make the voltage stress of the auxiliary circuit go beyond 1200 V (800 V + 400 V). The boost-type topology shown in Fig. 1(a) is finally chosen, and the required decoupling capacitance can be approximated to be [16],

$$C_{2\_dc} = \frac{P_r}{2\omega_n \Delta v_{r2}\left(v_{c\_max} - \Delta v_{r2}\right)} = \frac{2000}{2\times377\times160\times(800-160)} uF \approx 25.9\ \mu F \quad (6)$$

where Δv_{r2} is the allowed voltage ripple (amplitude) of the decoupling capacitor C_2, which is $0.2v_{c\_max}$ for the EPCOS B32776 series [22]. A single 30 µF/ 800 V film capacitor (B32776E8306K) is used together with the boost-type dc power decoupling circuit to mitigate the second-order ripple power. The volume of this capacitor is only 30mm×45mm×42mm = 56.7 cm^3.

The ac power decoupling is normally of buck type, as shown in Fig. 1(d), (e) and (f). The maximum peak value of the ac decoupling capacitor voltage v_{ac} is thus the dc link voltage, which can only be realized through the circuit shown in Fig. 1(f) with SVPWM. The required capacitance can be evaluated as described in [18],

$$C_{2\_ac} = \frac{P_r}{\frac{1}{2}\omega_n V_{ac}^2} = \frac{2000}{\frac{1}{2}\times377\times400^2} \approx 66.3\ \mu F \quad (7)$$

where V_{ac} is the amplitude of the capacitor voltage v_{ac}. In this case, three 25 uF/ 250 Vrms AC film capacitors (MKP1847625254P2) should be used, whose volume is 3×30mm×45mm×42mm = 170.1 cm^3, and it is two times larger than the dc decoupling design. Actually, in addition to the larger volume, the ac decoupling circuit may have lower efficiencies, especially under light load conditions. This is because the current stress of the decoupling switches does not linearly decrease with the load power, and this will be explained in the following section.

III. CONTROL STRATEGIES OF THE AUXILIARY CIRCUITS

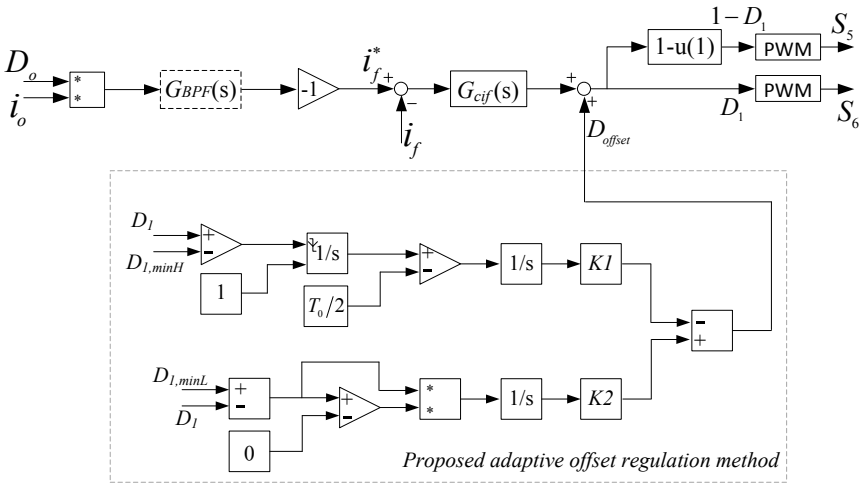


Fig. 5. Control strategy of the boost-type auxiliary circuit with proposed adaptive offset voltage control for dc decoupling.

A. DC Decoupling

According to (2) and Fig. 1(a), with the boost-type dc decoupling circuit, the ripple power can be compensated by simply regulating the decoupling current i_f to be a sinusoidal with $2\omega_n$ as following,

$$i_f^* = \frac{-p_r}{V_{dc}} = \frac{V_o I_o cos(2\omega_n t+\varphi)}{V_{dc}} = \frac{\overline{p_o}}{V_{dc}} - \frac{v_o i_o}{V_{dc}} \quad (8)$$

where i_f^* is the decoupling current reference. $\frac{\overline{p_o}}{V_{dc}}$ is actually used to cancel the dc component in $\frac{v_o i_o}{V_{dc}}$, which can also be realized by applying a band pass filter $G_{BPF}(s)$. Thus i_f^* can be expressed as,

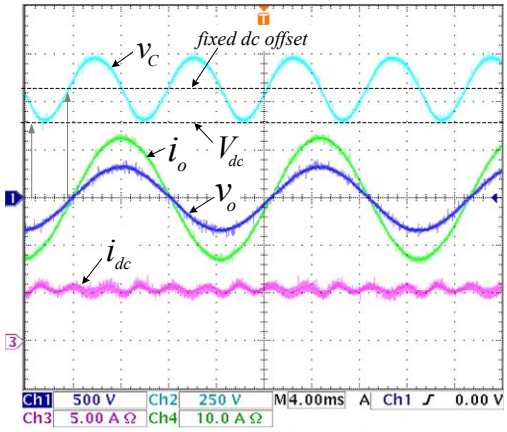
$$i_f^* = -\frac{v_o i_o}{V_{dc}} G_{BPF}(s) = -D_o i_o G_{BPF}(s) \quad (9)$$

$$G_{BPF}(s) = \frac{2*0.33*2\omega_n s}{s^2+2*0.33*2\omega_n s+(2\omega_n)^2} \quad (10)$$

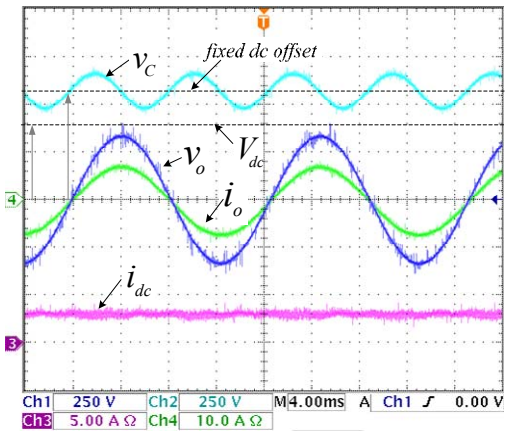
where $D_o = \frac{v_o}{V_{dc}}$ is the instantaneous duty ratio of the inverter. The error of the decoupling current is then input into a Proportional Resonance (PR) controller $G_{cif}(s)$ to obtain the duty ratio of the boost converter. The PR controller is given by (11), and its associated decoupling current control is illustrated in Fig. 5.

$$G_{cif}(s) = 0.02 + \frac{5s}{s^2+(2\omega_n)^2} + \frac{5s}{s^2+(4\omega_n)^2} + \frac{5s}{s^2+(6\omega_n)^2} \quad (11)$$

It should be noted that the dc offset of v_C is a parameter that can be freely tuned. In [13], the decoupling capacitor is fed by the ac output voltage via a transformer and a rectifier in order to keep $v_C > V_{dc}$. A relatively simpler and more cost-effective method is to set a fixed dc offset voltage for the decoupling capacitor to guarantee $v_C > V_{dc}$ for any load conditions as done in [14], [15]. However, with a fixed dc offset voltage, the ac component in v_C gets smaller under light load, and v_C becomes unnecessarily high as shown in Fig. 6(a) (full load) and Fig. 6(b) (half load). This directly translates into higher switching losses of S_5 and S_6 as well as faster lifetime



(a) full load



(b) half load

Fig. 6. Experimental results showing the decoupling capacitor voltage, output voltage and current, and dc link current with fixed dc offset in decoupling capacitor voltage.

consumption of the capacitor C_2 [26]. In order to solve these issues and meanwhile maintain the simple circuit configuration, this paper proposes an adaptive offset regulation to optimize V_C as much as possible, and the implemented

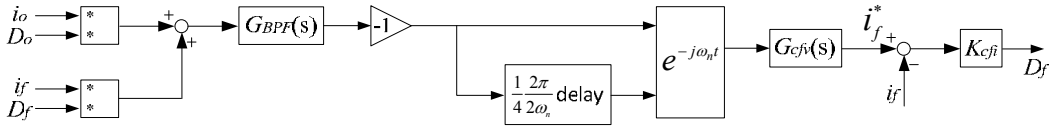


Fig. 7. Control diagram of the auxiliary circuit for ac decoupling.

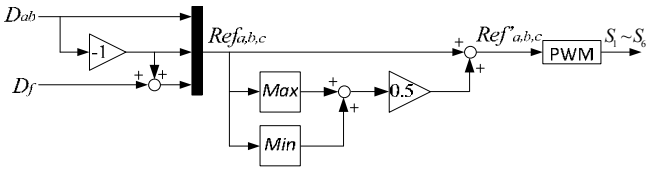


Fig. 8. Modulation strategy for B6 converter with ac decoupling to maximum the dc link voltage utilization.

control algorithm can be illustrated in the dashed box in Fig. 5. As seen, instead of having a fixed dc offset voltage, the idea is to maintain a fixed minimum value of v_C which is always slightly higher than the dc bus voltage regardless of load changes. In order to avoid adding another voltage sensor for measuring and controlling of v_C, the adaptive offset regulation method is realized by applying a hysteresis controller to keep the bottom value of D_1 into a small interval $[D_{1,minL},\ D_{1,minH}]$, because D_1 has a one-to-one mapping with v_C as simply indicated by (12). The interval is very small so that the bottom value of D_1 and v_C can be considered to be fixed.

$$v_C = \frac{1}{1-D_1} V_{dc} \tag{12}$$

- Hysteresis controller

In order to keep the minimum value of D_1 into $[D_{1,minL},\ D_{1,minH}]$, D_1 is compared with the upper and lower boundary values, as seen in Fig. 5. Once $D_1 < D_{1,minL}$ is detected, the D_{offset} will be increased to push D_1 up, thus $D_1 \geq D_{1,minL}$ can be simply guaranteed. To maintain the upper boundary of minimum D_1 is relatively more complicated, which cannot be directly implemented by comparing D_1 with $D_{1,minH}$. Instead, the duration of the continuous interval $D_1 \geq D_{1,minH}$ is detected, and it will be referred to as $T_{D_1 \geq D_{1,minH}}$. Once $T_{D_1 \geq D_{1,minH}} \geq \frac{T_o}{2} = \frac{\omega_n}{\pi}$ (T_o is a fundamental period of the inverter) is detected, the bottom value of D_1 larger than $D_{1,minH}$ can be confirmed. Therefore, D_{offset} will be decreased to pull the bottom value of D_1 back into the interval. The timer for the duration of the continuous interval $D_1 \geq D_{1,minH}$ will be reset as long as $D_1 < D_{1,minH}$ is detected. The two coefficients $K_1 = 3$ and $K_2 = 2000$ are used to adjust the dynamic response of the adaptive offset regulator. It should be noted that, the dc component in $D_o i_o$ will finally cause an offset in the duty ratio, because there is only a proportional gain for the dc component in the forward path of the controller (Fig. 5), and the effect of this offset can be automatically cancelled by the adaptive offset regulation. Therefore, the band pass filter $G_{BPF}(s)$ used to mitigate the dc component in $D_o i_o$ can be avoided, and it is eliminated in the simulation and experimental test.

B. AC Decoupling

In ac decoupling, the terminal voltage of the decoupling capacitor is theoretically a sinusoidal as defined by (13). For ripple power cancellation purpose, the decoupling capacitor voltage is necessary to be $\frac{\pi}{4}$ ahead of the inverter output voltage if the load is assumed to be resistive [18]. However in reality, the phase displacement may need a small change θ_c, because the load could be non-resistive, and the ripple power caused by the filtering inductor or capacitor should also be considered. Similarly based on the instantaneous power balancing, the required voltage and current for ac decoupling can be depicted by the following equation.

$$\begin{cases} v_C = \sqrt{2} V_c sin(\omega_n t + \frac{\pi}{4} + \theta_c) \\ i_f = \sqrt{2} I_f sin(\omega_n t + \frac{3\pi}{4} + \theta_c) \end{cases} \text{where} \begin{cases} V_C = \frac{I_f}{\omega_n C_2} \\ I_f = \sqrt{V_o I_o \omega_n C_2} \end{cases} \tag{13}$$

The above equation shows that, being different with the dc decoupling case, the inductor current here does not linearly decrease with the load power. Therefore, higher current stress and lower system efficiency may be expected for ac decoupling under light load conditions.

Instead of using open loop power decoupling, which is simple but has relatively poor decoupling performance especially under load changes, a closed-loop decoupling method is designed in this paper according to the one proposed in [20]. Since the inverter is fed by a constant dc source, the duty ratios of the converter D_o and D_f can be regarded as the normalized output voltages. In this case, the output power and the decoupling capacitor power can be estimated from the duty ratios and the inductor currents as shown in Fig. 7. The sum of these two power is then processed by the same band pass filter $G_{BPF}(s)$ as shown in (10) to cancel the dc component introduced by the output power and derive only the ripple power. A minus sign is then applied to obtain the error of the ripple power because the reference of the ripple power should be zero. Since the ripple power is of second order, while in the inner current control loop, the inductor current is a fundamental component, a transformation matrix defined by (14) is required to assist in the reference frame transformation. The second input to the matrix is obtained by adding a quarter cycle delay to the ripple power, and in this case a virtual $\alpha\beta$ coordinate can be created. Afterwards, a proportional resonant controller $G_{cfv}(s)$ is used to ensure a zero error tracking of the ripple power. The decoupling capacitor current is not necessary to be sinusoidal, and a fast dynamic performance is more preferred. Thus, only a proportional controller $K_{cfi} = 0.02$ is used.

$$T = [cos(\omega_n t) \quad sin(\omega_n t)] \tag{14}$$

$$G_{cfv}(s) = 3 + \frac{750s}{s^2+{\omega_n}^2} \tag{15}$$

For the ac decoupling circuit presented in Fig. 1 (f), another concern is the modulation method adopted for the B6 converter. A unipolar modulation method is normally used for the full bridge of the inverter, and the reference of phase C is obtained by adding the duty ratio of the decoupling capacitor D_f to the reference of phase B [17]. In this case, three-phase duty ratios can be obtained as the $Ref_{a,b,c}$ shown in Fig. 8. The drawback of this method is that the modulation index of the output voltage v_o and the decoupling capacitor voltage V_C cannot achieve unity at the same time and, therefore, the utilization of the dc link voltage or the reduction of the decoupling capacitor cannot be optimized. In order to solve this problem, a Space Vector PWM (SVPWM) method was proposed in [18], which is effective but a bit complicated due to the sector selection and dwell time calculation. Instead of using the space vectors, a reference offset injection is applied for simplification, and it is illustrated in Fig. 8. The reference offset injection method is the same with the carrier-based SVPWM method, where the only difference is that the former is an unbalanced PWM method while the latter is a balanced one.

IV. SIMULATED RESULTS

TABLE I. PARAMETERS USED FOR SIMULATED AND EXPERIMENTS.

Parameters	Values	
	AC	DC
DC-link voltage	*400 V*	
AC output voltage v_{ab}	*240 V (RMS) (Resistive load)*	
Switching frequency f_s	*30 kHz*	
Nominal power P_n	*2 kW*	
AC filter inductor L_1	*1 mH*	
AC filter capacitor C_o	*4.7 uF*	
Nominal load R_o	*28.8 Ω*	
Decoupling Cap. C_2	*75 uF*	*30 uF*
Boundary of the hysteresis controller $[D_{1,minL}, D_{1,minH}]$	---	[0.01, 0.05] ($v_{C,min} \in [404\,V, 421\,V]$)
Power switches S_1~S_6	*C2M0080120D*	

In order to verify the feasibility of the proposed solution for power decoupling, simulations of the inverter circuits shown in Fig. 1(a) and Fig.1 (f) were carried out with PLECS, and the parameters are listed in Table I. The simulated results are presented in Fig. 9 to Fig. 12. As seen, the second order harmonic in the dc link current is significantly mitigated by both dc decoupling (Fig. 9) and ac decoupling (Fig. 11). Moreover, the decoupling current i_f in ac decoupling is higher than that in dc decoupling, and thus the efficiency reduction caused by ac decoupling might be higher than the dc decoupling case, which will later be proved by the experimental results in Section V. In addition to the steady-state operation, the dynamic performances of the two power decoupling solutions are verified by the simulation as well, and

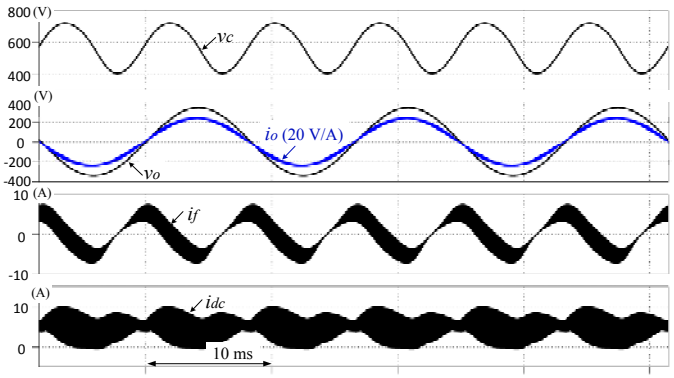


Fig. 9. Simulated results showing the steady state performance of dc decoupling with proposed adaptive control in full load condition.

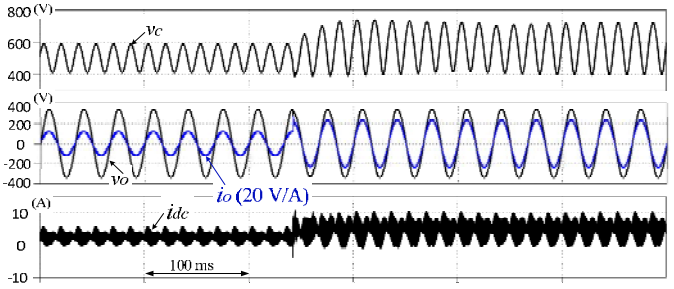


Fig. 10. Simulated results showing the transient response of dc decoupling with proposed adaptive control during load step-up.

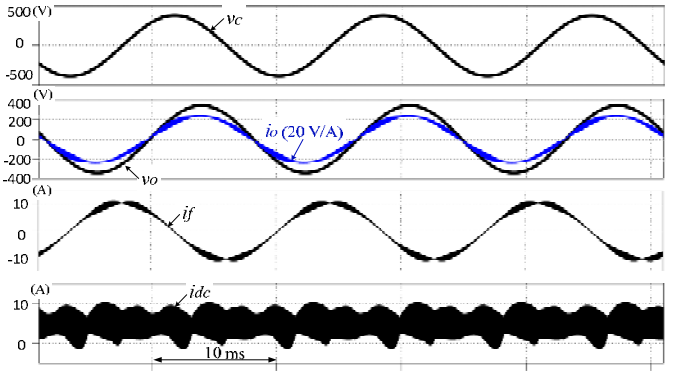


Fig. 11. Simulated results showing the steady state performance of ac decoupling in full load condition.

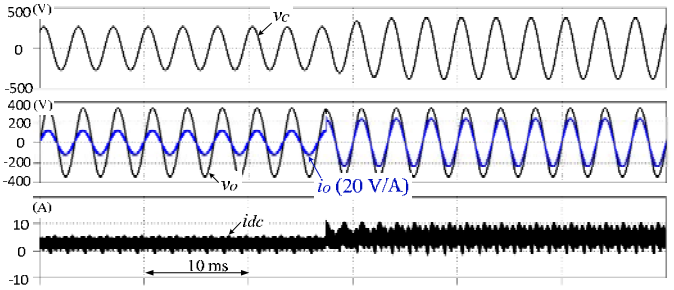


Fig. 12. Simulated results showing the transient response of ac decoupling during load step-up.

they are shown in Fig. 10 and Fig. 12, respectively. As seen in Fig. 10, with dc decoupling a fixed bottom value is ensured for the decoupling capacitor voltage v_C by using the proposed adaptive offset regulation. In this case, the voltage stress of the decoupling switches S5 and S6 will always be lower than the case when a fixed dc offset is applied to v_C. Therefore, the switching losses can be reduced.

V. EXPERIMENTAL RESULTS

The proposed APD solution was also verified on a 2 kW prototype as shown in Fig. 12, whose parameters are the same with those used for simulations in Section IV. The controller is implemented in dSPACE 1006. As seen, the volume of the capacitor for dc decoupling is only 1/3 of the total volume of the three capacitors for ac decoupling. This is in consistence with the investigations shown in Fig. 4, where the stored energy density of dc decoupling is about 3 times of the ac decoupling case.

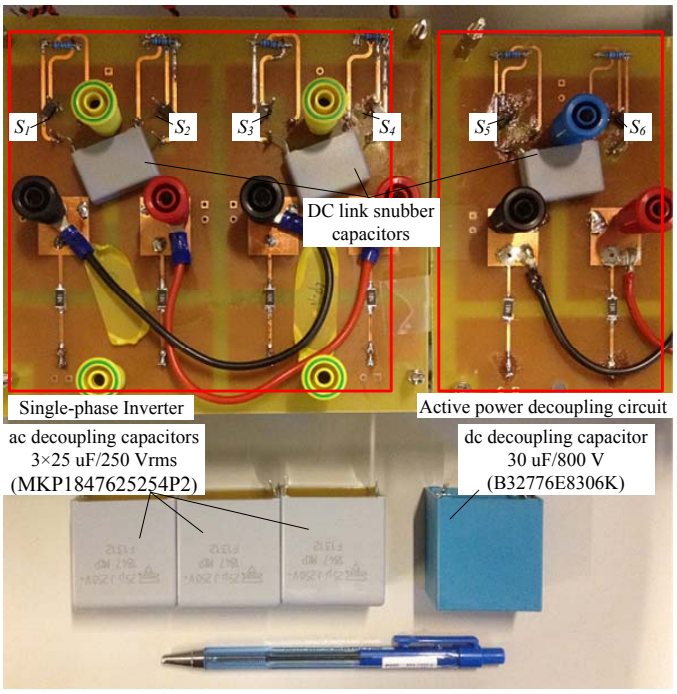


Fig. 13. The prototype for test together with the film capacitors used for dc and ac decoupling.

The obtained experimental results are presented in Fig. 14 to Fig. 18. The steady state performances of the dc and ac decoupling are shown respectively in Fig. 14 and Fig. 16, where the second order harmonic in the dc link current i_{dc} is well mitigated no matter in half or full load condition. Fig. 15 and Fig. 17 show the transient responses of the dc and ac decoupling during decoupling function enabling and load step-up respectively, which as seen are smooth and fast. Moreover, a fixed bottom value of the decoupling capacitor voltage can be observed in Fig. 14 and Fig. 15 even during the load change (Fig. 15 (b)), and this matches well with the simulation results presented in Fig. 9 and Fig. 10. The efficiency of the system and the lifetime of the decoupling capacitor are expected to be

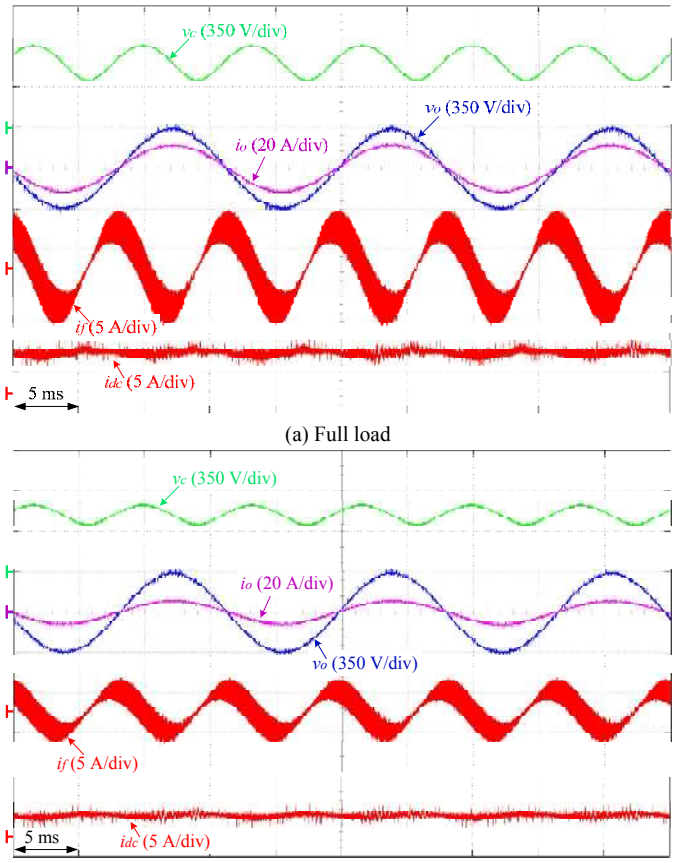


Fig. 14. Experimental results showing the steady state performance of dc decoupling with proposed adaptive control.

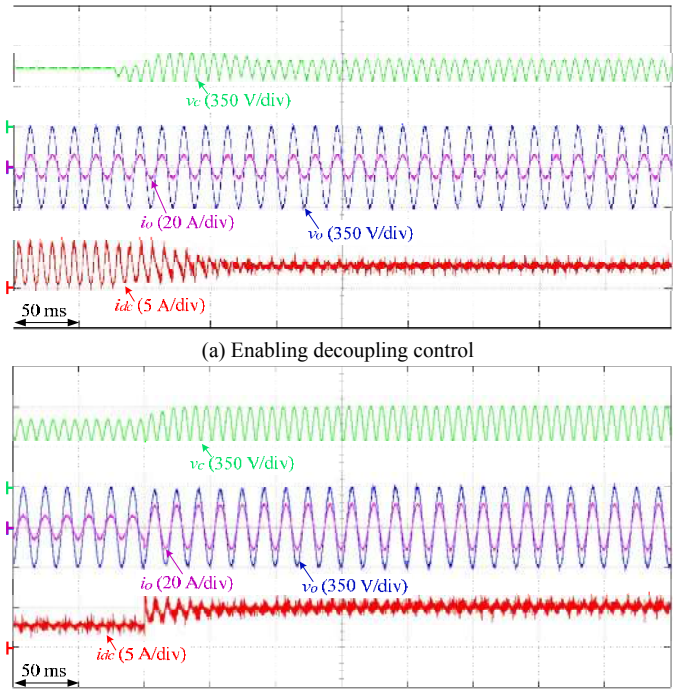
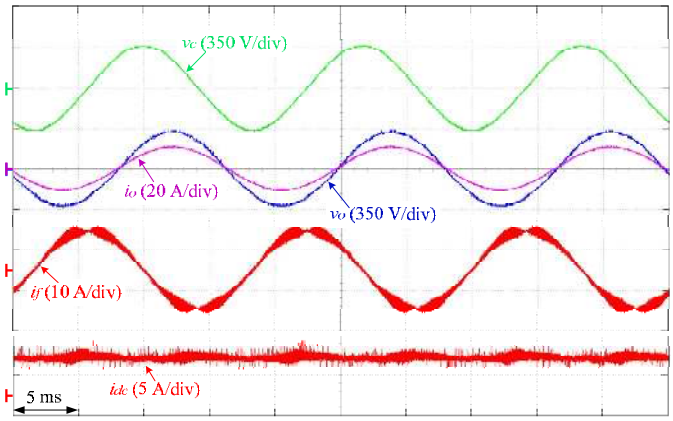
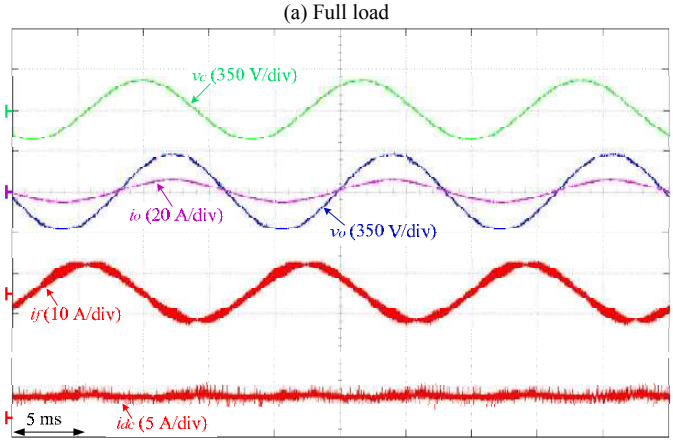


Fig. 15. Experimental results showing the transient responses of dc decoupling with proposed adaptive control.

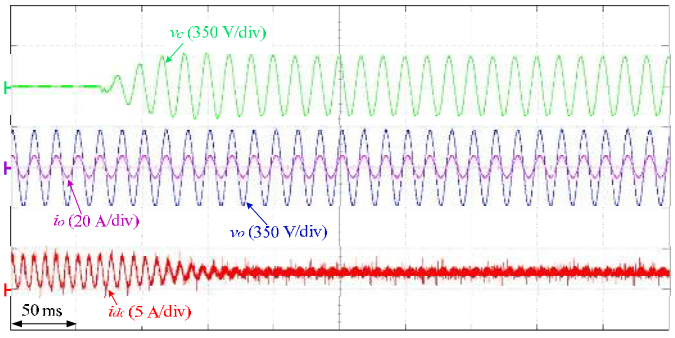


(a) Full load

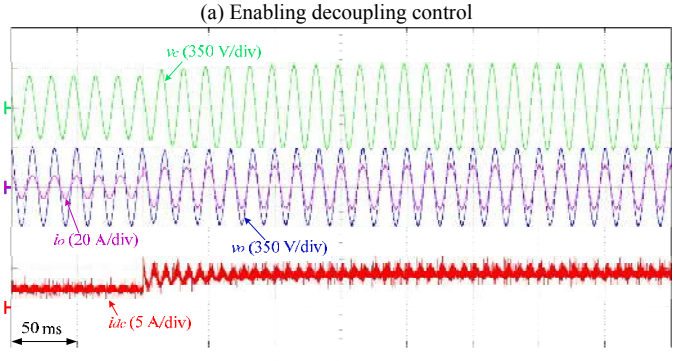


(b) Half load

Fig. 16. Experimental results showing the steady state performance of ac decoupling.



(a) Enabling decoupling control



(b) Load step-up

Fig. 17. Experimental results showing the transient responses of ac decoupling.

improved as compared to the dc decoupling without using the proposed adaptive control shown in Fig. 6, where a fixed dc offset $D_{offset} = 0.3$ is used and the corresponding dc component of v_C is $V_{dc} \times \frac{1}{1-0.3} = 575\,V$. It should be noted that, the dc link current i_{dc} has different high frequency components between simulated and experimental results. This is because in experiments the impedance of the dc source naturally exists and will provide attenuation to the high frequency components of i_{dc} as seen in Fig. 14 to Fig. 16. However in simulations, the impedance of the dc source is not modeled, and the high frequency components in the dc link current i_{dc} may become more significant as seen in Fig. 9 to Fig. 12.

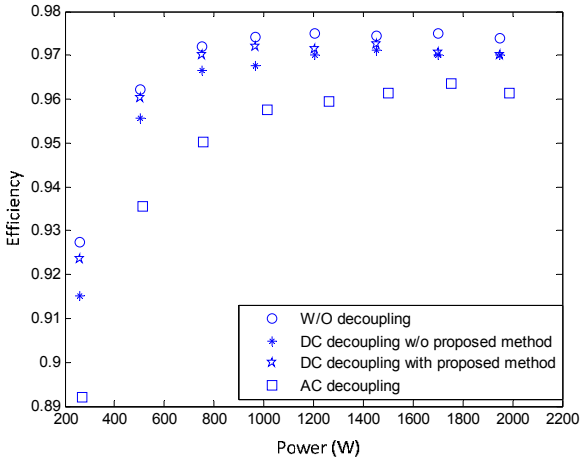


Fig. 18. Efficiency of the inverter together with the power decoupling circuit versus the load power.

The efficiency curves of the system under different control schemes and decoupling circuits were also measured by a Voltech PM3000A Universal Power Analyzer, and the results are summarized and presented in Fig. 18. It is clear that the dc decoupling method with the proposed adaptive control will stand out, because its efficiency reduction is the least as compared to the other two decoupling solutions. Thanks to the adaptive decoupling voltage control, under light load conditions, the current and voltage stresses of the decoupling circuit are low, and the efficiency reduction is basically negligible. Under high load conditions, the maximum efficiency drop can be observed, but it is still less than 0.5 %. When the proposed adaptive voltage control is disabled, the offset of the decoupling voltage is fixed at 575 V. With such a high dc-link voltage operation, the system efficiency drop will become more obvious, and it can be up to 1.2 % when 1/8 of the nominal load is applied to the system as shown in Fig. 18. In addition to the dc decoupling tests, the efficiency of the ac decoupling circuit shown in Fig. 1 (f) was also tested and presented in Fig. 18 for comparison. As seen, it is much lower than the dc decoupling case no matter the proposed adaptive voltage control is activated or not. The efficiency reduction is around 1 % under full load condition and 2 % ~ 3 % under light load condition. As mentioned, the main reason is that the

current in the ac decoupling circuit does not linearly decrease with the load power.

VI. CONCLUSIONS

In this paper, the benchmark of ac and dc APD circuits is presented in order to achieve high power density and high efficiency for kW scale single-phase inverters. Different APD topologies are evaluated and compared, among which, the boost-type dc power decoupling circuit is found to be best suited for this specific application. The results show that, with the proposed solution, the dc bus current ripple of a 2 kW prototype can be significantly reduced by utilizing only a single 30 uF/800 V film capacitor in dc decoupling, instead of a large electrolytic capacitor bank. Moreover, the efficiency drop caused by the power decoupling circuit is sizably reduced under light load conditions by implementing the proposed adaptive control strategy. Since the proposed adaptive control strategy leads to a lower voltage of the decoupling capacitor in light load condition, the lifetime consumption of the film capacitor is also reduced and thereby a higher reliability of the capacitor can be expected. Besides, the ac decoupling circuit is also studied for comparison, where the best solution is to use three 25 uF/250 Vrms film capacitors in parallel. However, the capacitor volume for ac decoupling is about 3 times of that for dc decoupling, and the efficiency of the former is much lower as well.

REFERENCES

[1] W. Kim, V.H. Duong, T.T. Nguyen, and W. Choi, "Analysis of the effects of inverter ripple current on a photovoltaic power system by using an AC impedance model of the solar cell," *Renewable Energy*, Vol. 59, pp. 150–157, 2013.

[2] Emerson Network Power, "Effects of ac ripple current on VRLA battery life," http://www.emersonnetworkpower.com/documentation/en-us/brands/liebert/documents/white%20papers/effects%20of%20ac%20ripple%20current%20on%20vrla%20battery%20life.pdf [Online: accessed 10-MAR-2015].

[3] Little Box Challenge "Detailed Inverter Specifications, Testing Procedure, and Technical Approach and Testing Application Requirements for the Little Box Challenge," https://www.littleboxchallenge.com/pdf/LBC-InverterRequirements-20141216.pdf [Online: accessed 18-JAN-2015].

[4] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," *IEEE. Trans. Power Electron.,* vol.28, no.6, pp.2711-2726, June 2013.

[5] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," *IEEE Trans. Ind. Appl.*, vol. 36, no. 4, pp. 1419–1429, Sep./Oct. 2000.

[6] K. Tsuno, T. Shimizu, and K. Wada, "Optimization of the DC ripple energy compensating circuit on a single-phase voltage source PWM rectifier," *in Proc. IEEE Power Elecron. Spec. Conf.,* Jun. 2004, pp. 316–321.

[7] H. Wang, H. S. H. Chung, and W. Liu, "Use of a series voltage compensator for reduction of the DC-Link capacitance in a Capacitor supported system," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1163–1175, Mar. 2014.

[8] S. Li, G. Zhu, S. Tan, and S. Hui, "Direct AC/DC Rectifier with Mitigated Low-Frequency Ripple Through Waveform Control," *IEEE Trans. Power Electron.*, DOI: 10.1109/TPEL.2014.2360209.

[9] T. Shimizu, K. Wada, and N. Nakamura, "A flyback-type single phase utility interactive inverter with low-frequency ripple current reduction on the dc input for an ac photovoltaic module system," *in Proc. of PESC' 2002*, pp. 1483–1488, 2002.

[10] S. B. Kjær and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," *in Proc. of PESC'03*, pp. 1183–1190, 2003.

[11] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen, and I. Batarseh, "A single-stage microinverter without using electrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2677–2687, Jun. 2013.

[12] W. Chen, and S. Y. Ron Hui, "Elimination of an Electrolytic Capacitor in AC/DC Light-Emitting Diode (LED) Driver With High Input Power Factor and Constant Output Current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1598-1607, Mar. 2012.

[13] A. C. Kyritsis, N. P. Papanikolaou, and E. C. Tatakis, "A novel Parallel Active Filter for Current Pulsation Smoothing on single stage grid-connected AC-PV modules," *in Proc. of EPE' 2007*, pp.1-10, 2007.

[14] S. Wang, X. Ruan, K. Yao, S.-C. Tan, Y. Yang, and Z. Ye, "A Flicker-Free Electrolytic Capacitor-Less AC–DC LED Driver," *IEEE Trans. Power Electron.,* vol. 27, no. 11, pp. 4540-4548, Nov. 2012.

[15] Y. Yang, X. Ruan, L. Zhang, J. He, and Z. Ye, "Feed-Forward Scheme for an Electrolytic Capacitor-Less AC/DC LED Driver to Reduce Output Current Ripple," *IEEE Trans. Power Electron*. vol. 29, no. 10, pp. 5508-5517, Oct. 2014.

[16] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.,* vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[17] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.,* vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[18] R. Chen, Y. Liu, and F.Z. Peng, "DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.,* vol. 30, no. 10, pp. 5499–5507, Oct. 2015.

[19] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuation power in single-phase systems through a symmetrical half-bridge circuit," *IEEE. Trans. Power Electron.,* vol. 30, no. 4, pp. 1855-1865, Apr. 2015.

[20] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, "A Dual Voltage Control Strategy for Single-Phase PWM Converters with Power Decoupling Function," *IEEE. Trans. Power Electron.,* DOI 10.1109/TPEL.2014.2385032

[21] Y. Tang, and F. Blaabjerg, "A Component-Minimized Single-Phase Active Power Decoupling Circuit With Reduced Current Stress to Semiconductor Switches," *IEEE. Trans. Power Electron.,* vol. 30, no.6, pp. 2905-2910, June 2015.

[22] Film Capacitors "Metallized Polypropylene Film Capacitors (MKP)", http://www.epcos.com/epcos-en/529464/products/product-catalog/film-capacitors/metallized-polypropylene-capacitors--mkp-mfp- [Online: accessed 13-JAN-2015].

[23] Film Capacitors – AC Capacitors, http://www.epcos.com/inf/20/25/ds/B32356.pdf [Online: accessed 19-JAN-2015].

[24] MKP1847 AC Filtering, http://www.vishay.com/docs/28172/mkp1847ac.pdf [Online: accessed 19-JAN-2015].

[25] MKP1848C DC-Link, http://www.vishay.com/docs/26015/mkp1848cdclink.pdf [Online: accessed 19-JAN-2015].

[26] Film Capacitors – Power Electronic Capacitors. http://en.tdk.eu/inf/20/50/ds/B2562_.pdf [Online: accessed 19-JAN-2015].

Zian Qin (S'13) received the B.Eng. degree in Automation from Beihang University, Beijing, China, in 2009, M.Eng. degree in Control Science and Engineering from Beijing Institute of Technology, Beijing, China, in 2012, and Ph.D. degree from Aalborg University, Aalborg, Denmark, in 2015. From October 2015, he has been working as a Postdoctoral Research Fellow in Aalborg University. In 2014, he was a Visiting Scientist with the Institute for Power Generation and Storage Systems (PGS), Aachen University, Aachen, Germany, where he focused on the wind power generation. His interest is power converter design.

Yi Tang (S'10-M'14) received the B.Eng. degree in electrical engineering from Wuhan University, Wuhan, China, in 2007 and the M.Sc. and Ph.D. degrees from the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2008 and 2011, respectively.

From 2011 to 2013, he was a Senior Application Engineer with Infineon Technologies Asia Pacific, Singapore. From 2013 to 2015, he was a Postdoctoral Research Fellow with Aalborg University, Aalborg, Denmark. Since March 2015, he has been with Nanyang Technological University, Singapore as an Assistant Professor.

Dr. Tang received the Infineon Top Inventor Award in 2012.

Poh Chiang Loh received his B.Eng (Hons) and M.Eng from the National University of Singapore in 1998 and 2000 respectively, and his Ph.D from Monash University, Australia, in 2002, all in electrical engineering. His interests are in power converters and their grid applications.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he was a Ph.D. Student with Aalborg University, Aalborg, Denmark. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives.

He has received 15 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014 and the Villum Kann Rasmussen Research Award 2014. He was an Editor-in-Chief of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011.